

N-channel 75 V, 20 mΩ typ., 32 A STripFET™ F3 Power MOSFET in a PowerFLAT™ 3.3x3.3 package

Datasheet - production data

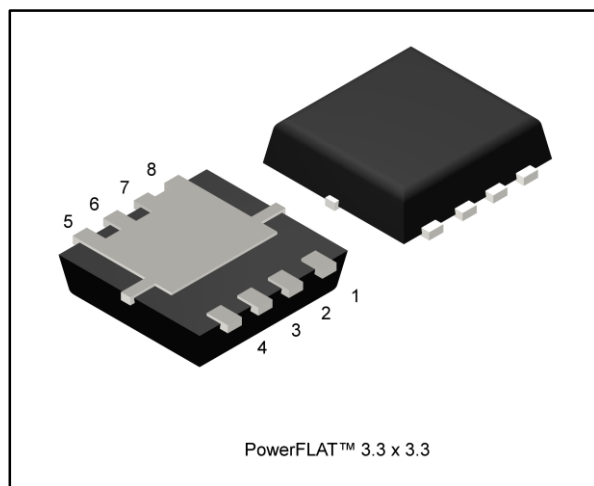
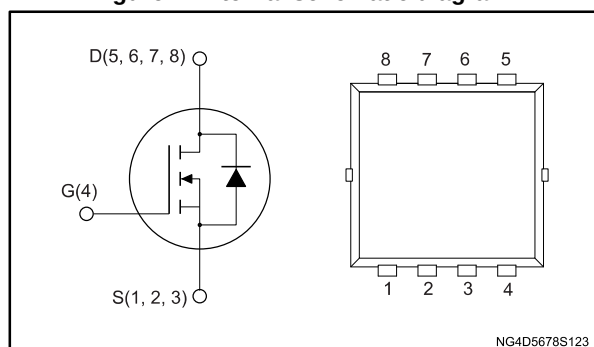


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STL35N75LF3	75 V	25 mΩ	32 A	50 W

- Low gate charge
- Low threshold voltage device

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STripFET™ F3 technology. It is designed to minimize on-resistance and gate charge to provide superior switching performance.

Table 1: Device summary

Order code	Marking	Package	Packing
STL35N75LF3	35N75	PowerFLAT™ 3.3x3.3	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	75	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$	32	A
	Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$	20	
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	128	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	8	A
	Drain current (continuous) at $T_{pcb} = 100\text{ }^{\circ}\text{C}$	5	
$P_{TOT}^{(1)}$	Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$	50	W
$P_{TOT}^{(3)}$	Total dissipation at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	2.9	W
$E_{AS}^{(4)}$	Single pulse avalanche energy	230	mJ
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

Notes:

⁽¹⁾The value is rated according to $R_{thj-case}$.

⁽²⁾ Pulse width is limited by safe operating area.

⁽³⁾The value is rated according to $R_{thj-pcb}$.

⁽⁴⁾Starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = 6\text{ A}$, $V_{DD} = 50\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	2.5	$^{\circ}\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max.	42.8	

Notes:

⁽¹⁾When mounted on a 1 inch², 2 oz Cu, FR-4 board, $t < 10\text{ s}$.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	75			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 75\text{ V}$			1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 75\text{ V}$, $T_{\text{case}} = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			10	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 20\text{ V}$			± 100	nA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	1		2.4	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 4\text{ A}$		20	25	m Ω
		$V_{\text{GS}} = 4.5\text{ V}$, $I_{\text{D}} = 4\text{ A}$		25	30	m Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ISS}	Input capacitance	$V_{\text{DS}} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	800	-	pF
C_{OSS}	Output capacitance		-	110	-	
C_{RSS}	Reverse transfer capacitance		-	15	-	
Q_{g}	Total gate charge	$V_{\text{DD}} = 37.5\text{ V}$, $I_{\text{D}} = 8\text{ A}$, $V_{\text{GS}} = 4.5\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	7.5	-	nC
Q_{gs}	Gate-source charge		-	3.2	-	
Q_{gd}	Gate-drain charge		-	3.0	-	

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 37.5\text{ V}$, $I_{\text{D}} = 4\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	6.8	-	ns
t_{r}	Rise time		-	3	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	22.8	-	
t_{f}	Fall time		-	2.2	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0 \text{ V}$, $I_{SD} = 8 \text{ A}$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 8 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$	-	26		ns
Q_{rr}	Reverse recovery charge		-	24		nC
I_{RRM}	Reverse recovery current		-	1.8		A

Notes:

⁽¹⁾ Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

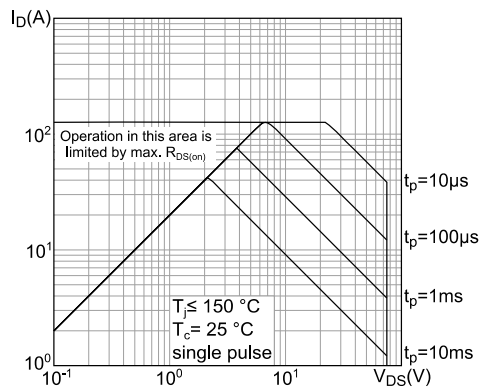


Figure 3: Thermal impedance

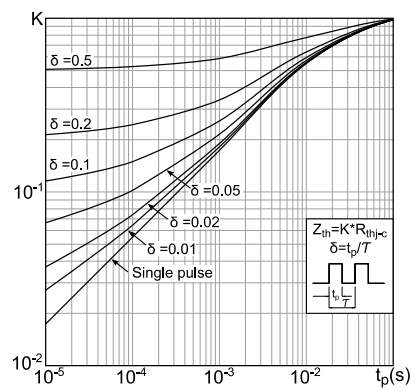


Figure 4: Output characteristics

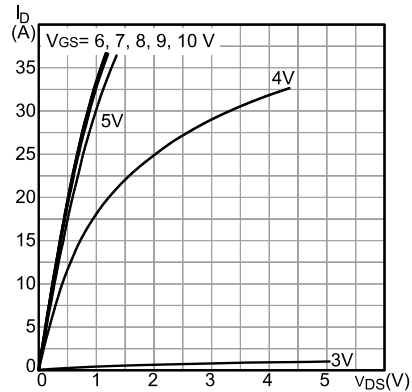


Figure 5: Transfer characteristics

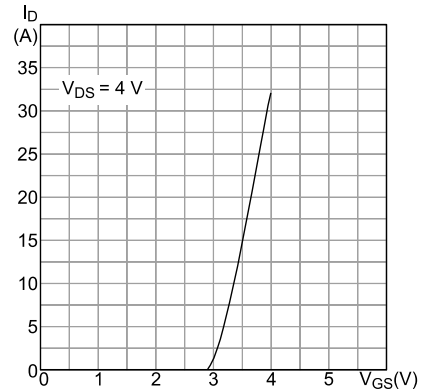


Figure 6: Normalized gate threshold voltage vs. temperature

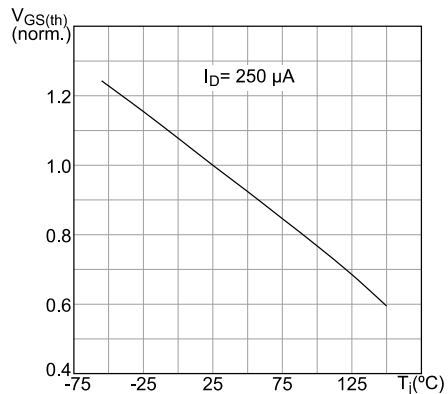


Figure 7: Normalized V(BR)DSS vs. temperature

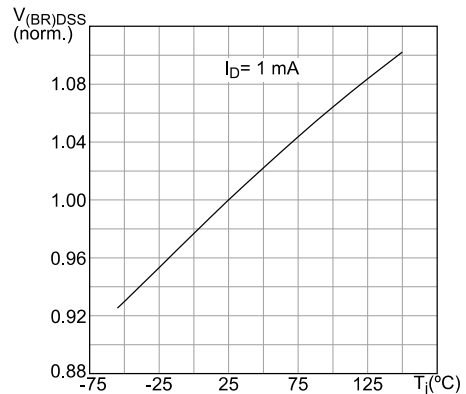


Figure 8: Static drain-source on-resistance

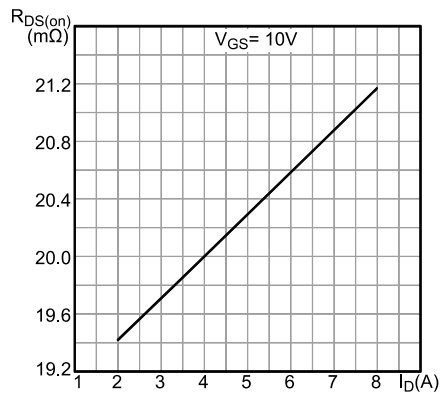


Figure 9: Normalized on-resistance vs. temperature

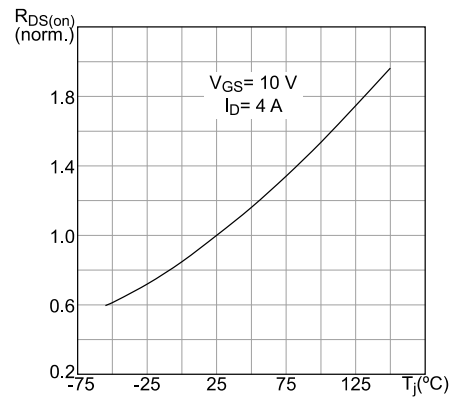


Figure 10: Gate charge vs. gate-source voltage

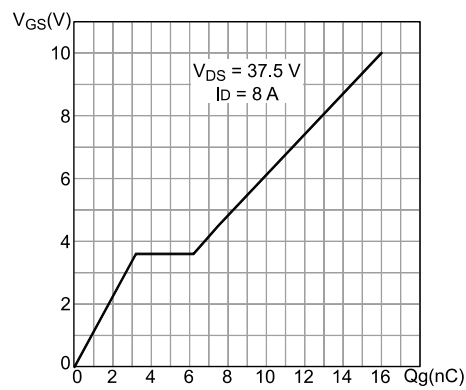


Figure 11: Capacitance variations

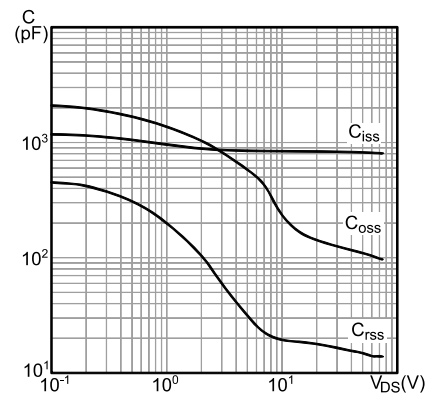
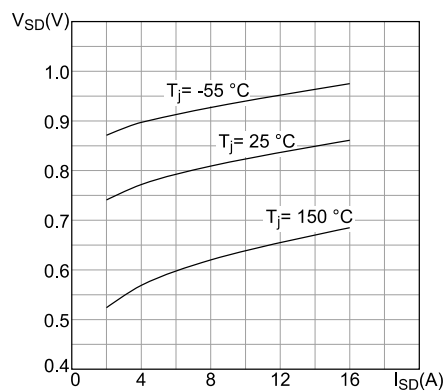
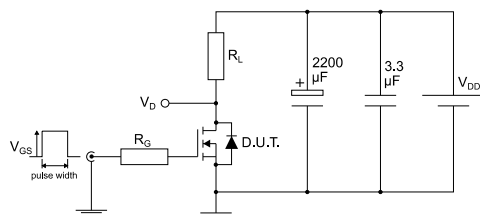


Figure 12: Source-drain diode forward characteristics



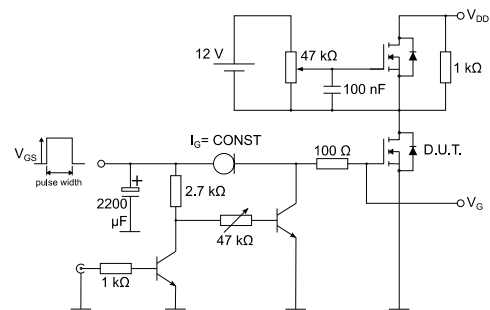
3 Test circuits

Figure 13: Test circuit for resistive load switching times



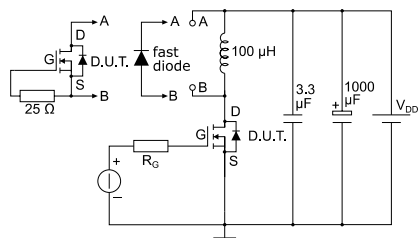
AM01468v1

Figure 14: Test circuit for gate charge behavior



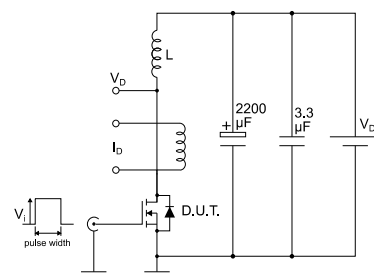
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Figure 15: Test circuit for inductive load switching and diode recovery times



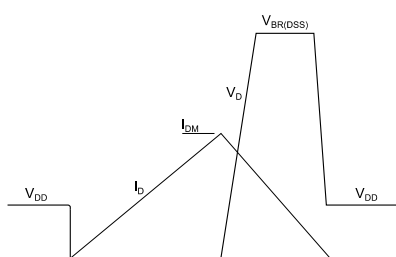
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Figure 16: Unclamped inductive load test circuit



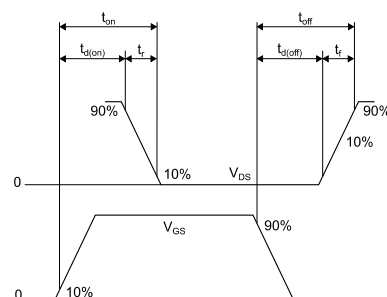
AM01471v1

Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 3.3x3.3 package information

Figure 19: PowerFLAT™ 3.3x3.3 package outline

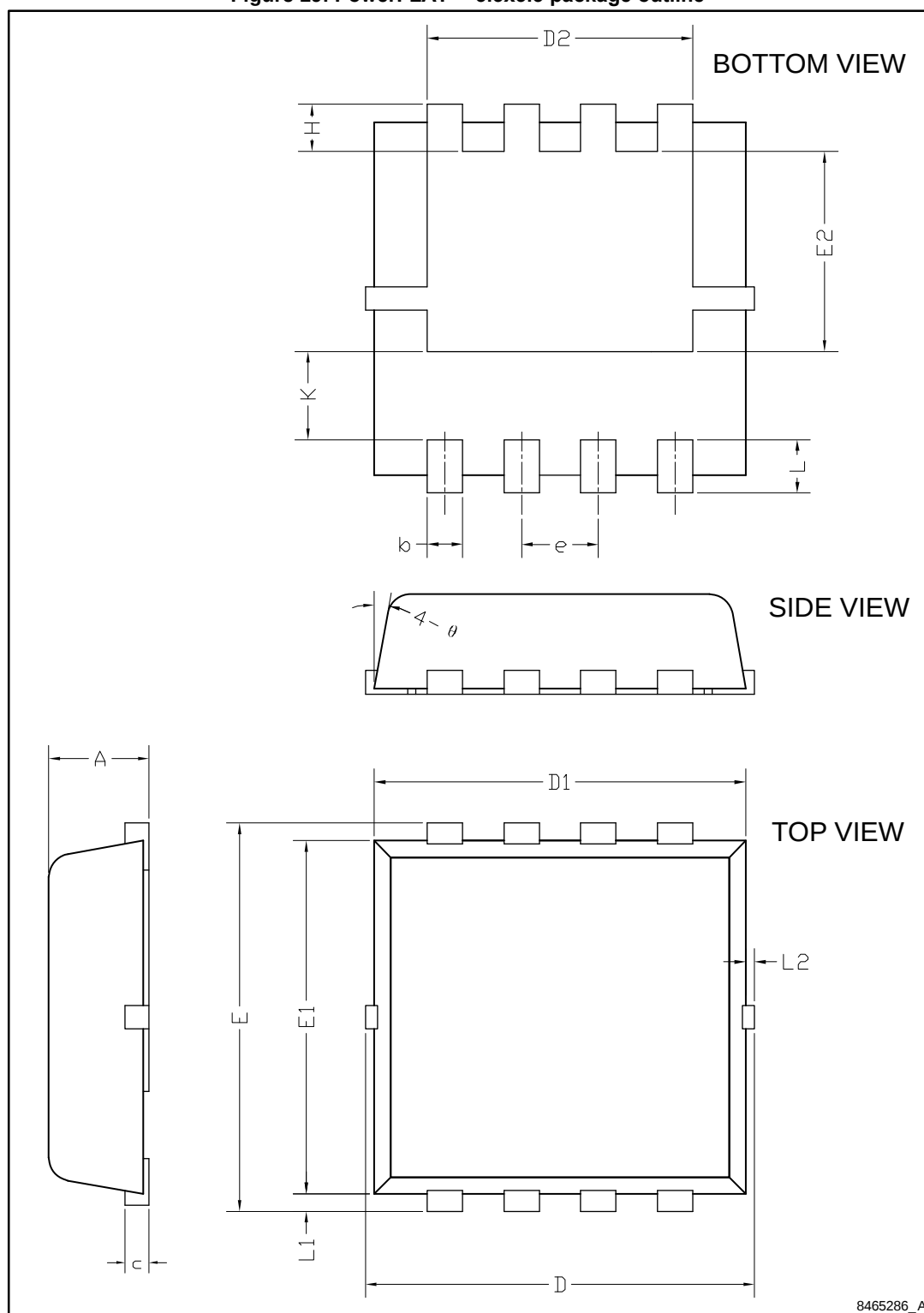
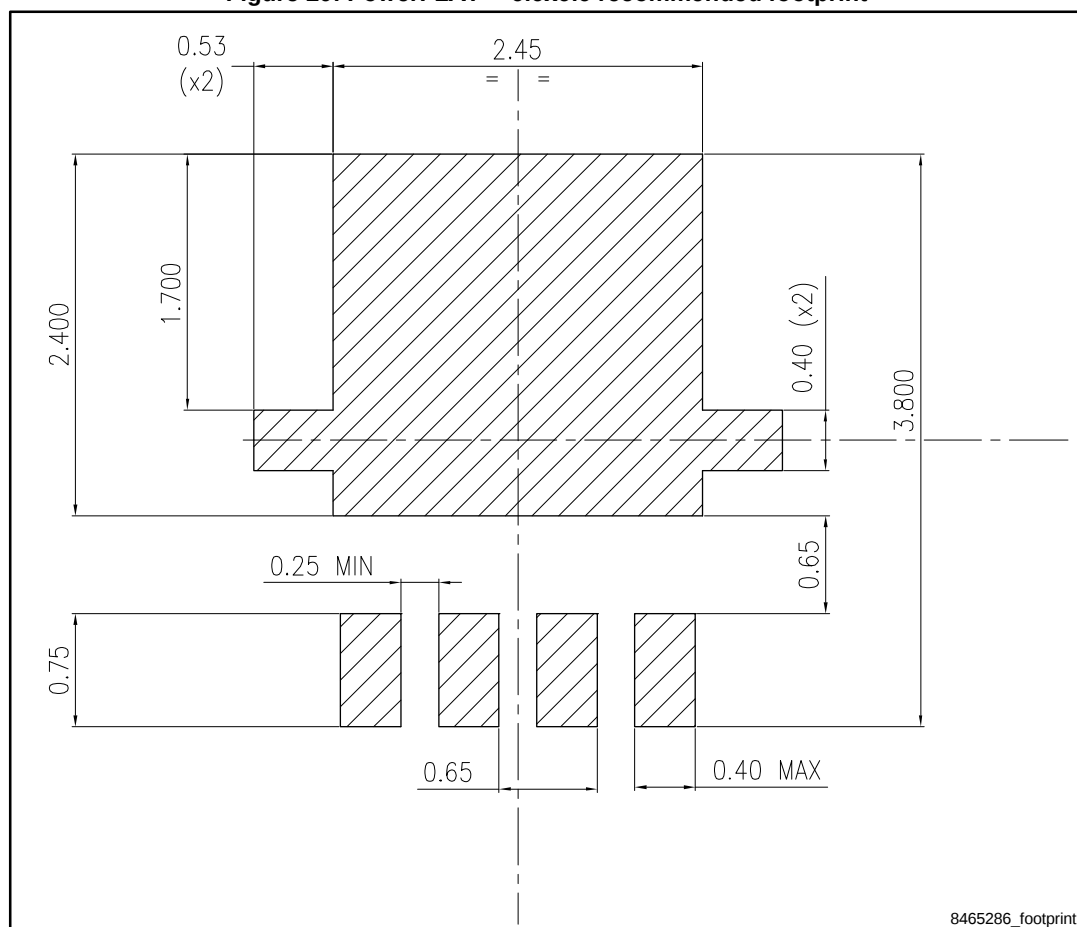


Table 8: PowerFLAT™ 3.3x3.3 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2			0.15
θ	8°	10°	12°

Figure 20: PowerFLAT™ 3.3x3.3 recommended footprint



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
16-Jul-2014	1	First release.
12-Nov-2014	2	Document status promoted from preliminary to production data. Added <i>Section 2.1: Electrical characteristics (curves)</i> . Minor text changes.
27-Jun-2016	3	Updated title and package silhouette in cover page. Updated <i>Section 1: "Electrical ratings"</i> . Updated <i>Section 2: "Electrical characteristics"</i> . Updated <i>Section 2.1: "Electrical characteristics (curves)"</i> . Minor text edits.
08-Aug-2016	4	Updated <i>Section 2: "Electrical characteristics"</i> .

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