

MC74VHC257

Quad 2-Channel Multiplexer with 3-State Outputs

The MC74VHC257 is an advanced high speed CMOS quad 2-channel multiplexer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

It consists of four 2-input digital multiplexers with common select (S) and enable ($\overline{OE}$) inputs. When ($\overline{OE}$) is held High, selection of data is inhibited and all the outputs go Low.

The select decoding determines whether the A or B inputs get routed to the corresponding Y outputs.

The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

- High Speed: $t_{PD} = 4.1$ ns (Typ) at $V_{CC} = 5.0$ V
- Low Power Dissipation: $I_{CC} = 4.0$ μ A (Max) at $T_A = 25^\circ\text{C}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.8$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: FETs = 100; Equivalent Gates = 25
- These Devices are Pb-Free and are RoHS Compliant

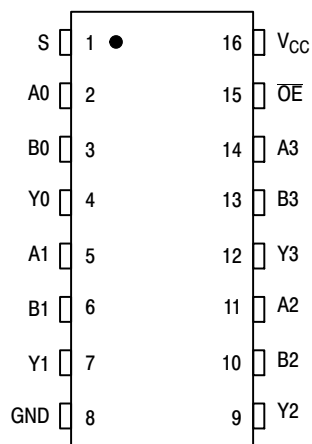


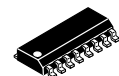
Figure 1. Pin Assignment



ON Semiconductor™

<http://onsemi.com>

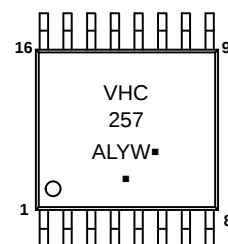
MARKING DIAGRAMS



SO-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ■ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
MC74VHC257DG	SO-16	48 Units/Rail
MC74VHC257DR2G	SO-16	2500 Units/Reel
MC74VHC257DTG	TSSOP-16	96 Units/Rail
MC74VHC257DTR2G	TSSOP-16	2500 Units/Reel

MC74VHC257

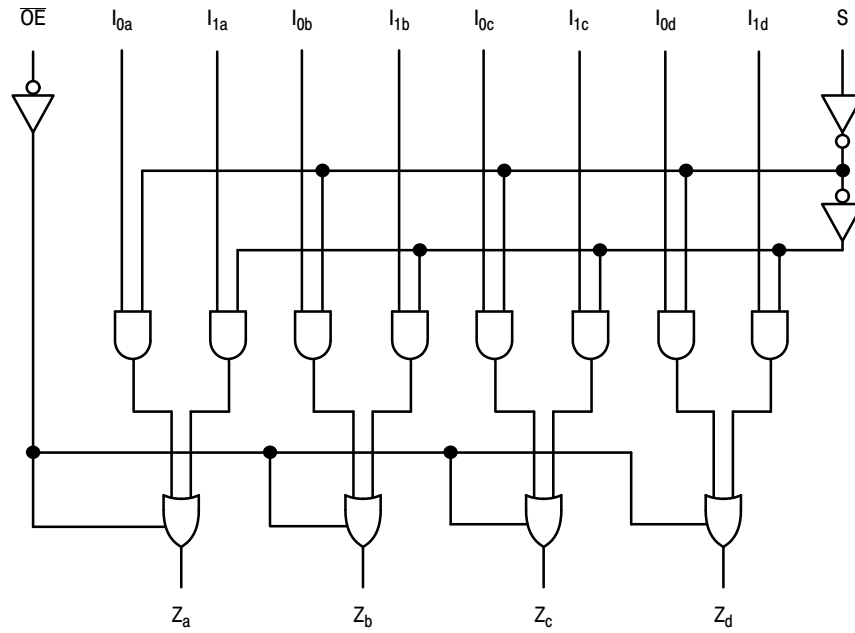


Figure 2. Expanded Logic Diagram

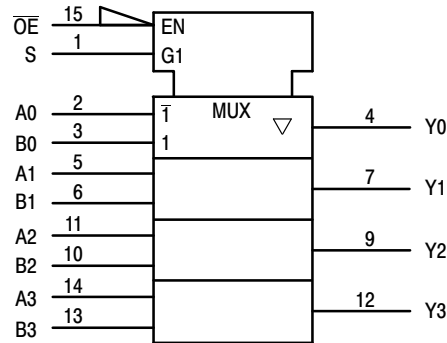


Figure 3. IEC Logic Symbol

FUNCTION TABLE

Inputs		Outputs Y0 – Y3
$\overline{OE}$	S	
H	X	Z
L	L	A0 – A3
L	H	B0 – B3

A0 – A3, B0 – B3 = the levels of the respective Data-Word Inputs.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

MC74VHC257

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Positive DC Supply Voltage	−0.5 to +7.0	V
V _{IN}	Digital Input Voltage	−0.5 to +7.0	V
V _{OUT}	DC Output Voltage	−0.5 to V _{CC} +0.5	V
I _{IK}	Input Diode Current	−20	mA
I _{OK}	Output Diode Current	± 20	mA
I _{OUT}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 75	mA
P _D	Power Dissipation in Still Air SOIC Package TSSOP	200 180	mW
T _{STG}	Storage Temperature Range	−65 to +150	°C
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	>2000 >200 >2000	V
I _{LATCHUP}	Latchup Performance Above V _{CC} and Below GND at 125°C (Note 4)	± 300	mA
θ _{JA}	Thermal Resistance, Junction-to-Ambient SOIC Package TSSOP	143 164	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1 Tested to EIA/JESD22-A114-A
- 2 Tested to EIA/JESD22-A115-A
- 3 Tested to JESD22-C101-A
- 4 Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	5.5	V
V _{IN}	DC Input Voltage	0	5.5	V
V _{OUT}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature Range, all Package Types	-55	125	°C
t _r , t _f	Input Rise or Fall Time	V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

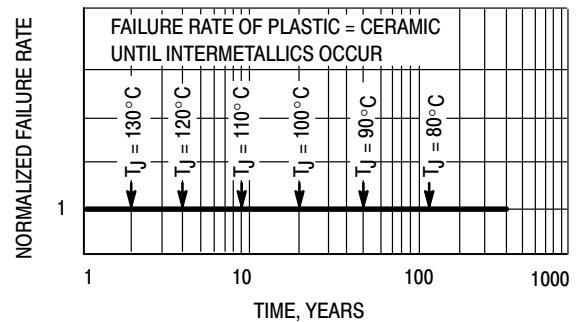


Figure 4. Failure Rate vs. Time Junction Temperature

MC74VHC257

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 to 5.5	1.5 V _{CC} × 0.7			1.5 V _{CC} × 0.7	1.5 V _{CC} × 0.7	1.5 V _{CC} × 0.7		V
V _{IL}	Maximum Low-Level Input Voltage		2.0 3.0 to 5.5			0.5 V _{CC} × 0.3		0.5 V _{CC} × 0.3		0.5 V _{CC} × 0.3	V
V _{OH}	Maximum High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA	3.0 4.5	2.58 3.94			2.48 3.8		2.34 3.66		
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = 4 mA I _{OH} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I _{OZ}	Maximum 3-State Leakage Current	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5			±0.25		±2.5		±2.5	μA
I _{CC}	Maximum Quiescent Supply Current (per package)	V _{IN} = V _{CC} or GND	5.5			4.0		40.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay A or B to Y	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF		5.8 8.3	9.3 12.8	1.0 1.0	11.0 14.5	1.0 1.0	11.0 14.5	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		3.6 5.1	5.9 7.9	1.0 1.0	7.0 9.0	1.0 1.0	7.0 9.0	
t _{PLH} , t _{PHL}	Maximum Propagation Delay S to Y	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF		7.0 9.5	11.0 14.5	1.0 1.0	13.0 16.5	1.0 1.0	13.0 16.5	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		4.0 5.5	6.8 8.8	1.0 1.0	8.0 10.0	1.0 1.0	8.0 10.0	
t _{PZL} , t _{PZH}	Maximum Output Enable Time OE to Y	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF R _L = 1 kΩ C _L = 50 pF		6.7 9.2	10.5 14.0	1.0 1.0	12.5 16.0	1.0 1.0	12.5 16.0	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF R _L = 1 kΩ C _L = 50 pF		3.6 5.1	6.8 8.8	1.0 1.0	8.0 10.0	1.0 1.0	8.0 10.0	
t _{PLZ} , t _{PHZ}	Maximum Output Disable Time OE to Y	V _{CC} = 3.3 ± 0.3 V C _L = 50 pF R _L = 1 kΩ		12.0	15.0	1.0	16.0	1.0	17.5	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 50 pF R _L = 1 kΩ		5.7	13.0	1.0	14.0	1.0	15.0	
C _{IN}	Maximum Input Capacitance			4	10		10		10	pF

C _{PD}	Power Dissipation Capacitance (Note 5)	Typical @ 25°C, V _{CC} = 5.0V	pF
		20	

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

MC74VHC257

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.3	-0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

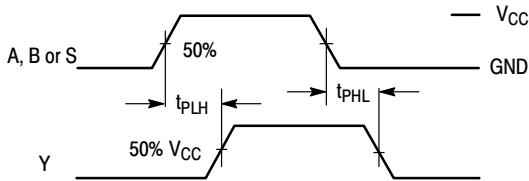


Figure 5. Switching Waveform

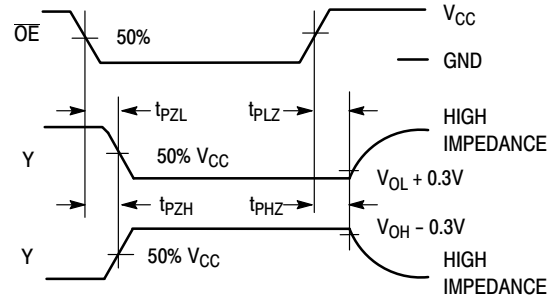
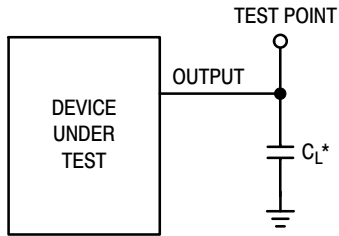
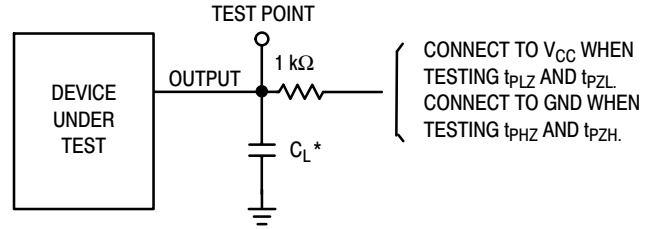


Figure 6. Switching Waveform



*Includes all probe and jig capacitance

Figure 7. Test Circuit



*Includes all probe and jig capacitance

Figure 8. Test Circuit

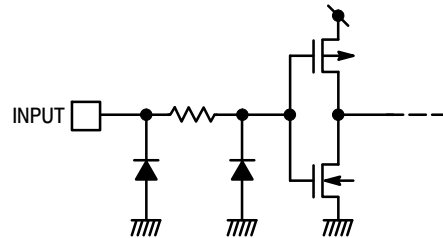
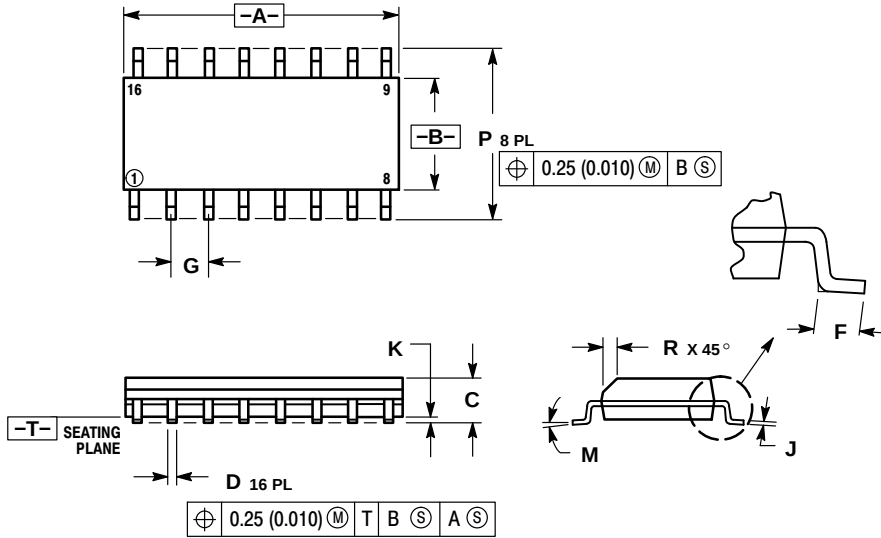


Figure 9. Input Equivalent Circuit

MC74VHC257

PACKAGE DIMENSIONS

SOIC-16
CASE 751B-05
ISSUE K

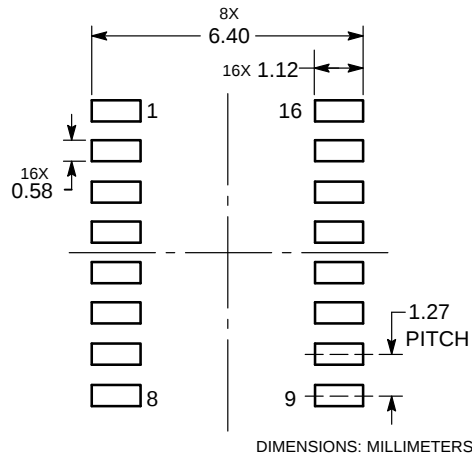


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

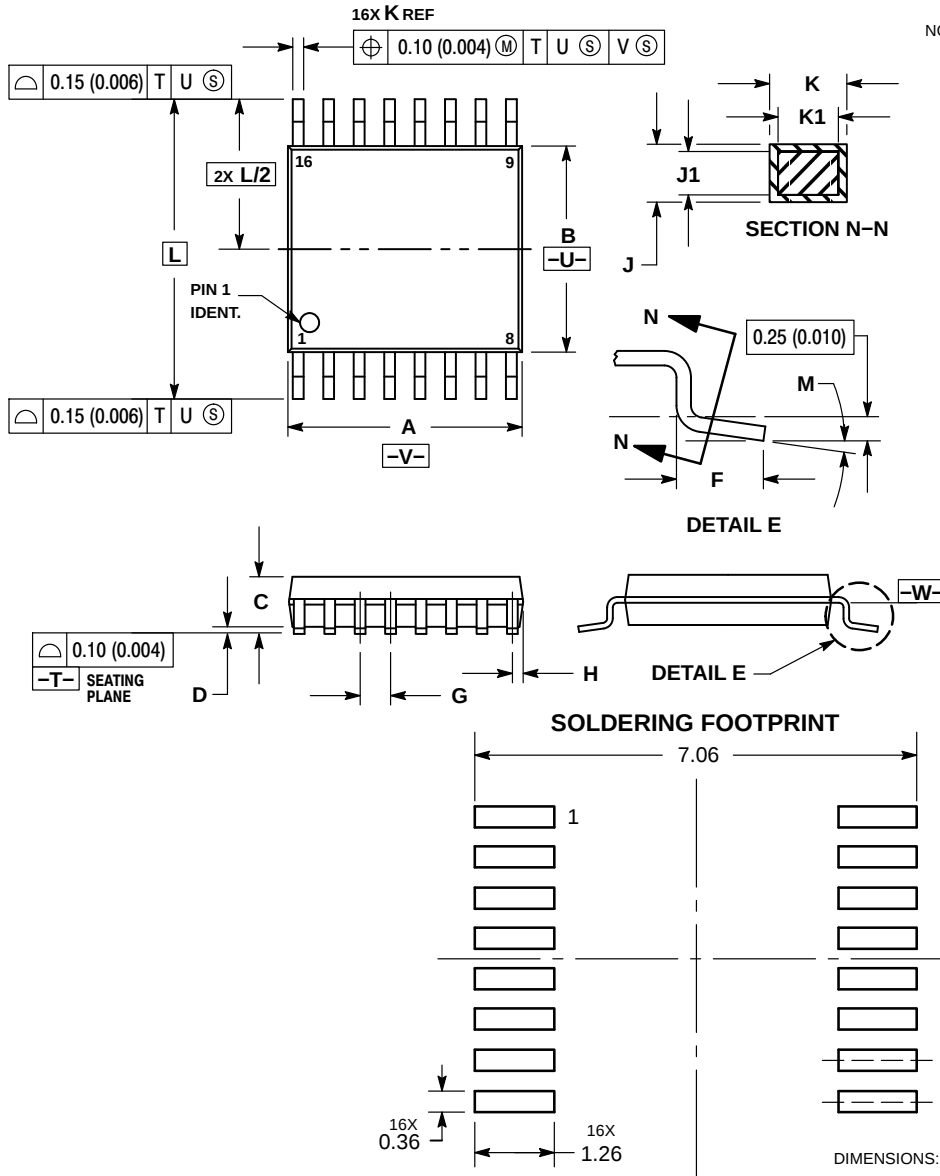
SOLDERING FOOTPRINT



MC74VHC257

PACKAGE DIMENSIONS

TSSOP-16
CASE 948F
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC	—	0.026 BSC	—
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC	0.252 BSC	—	—
M	0°	8°	0°	8°

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marketing.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

MC74VHC257/D