

# **TMS570LS31x Hercules Development Kit (HDK)**

## **User's Guide**



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## Read This First

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### About This Manual

This document describes the board level operations of the TMS570LS31 Hercules™ Development Kit (HDK). The HDK is based on the Texas Instruments TMS570LS3137 Microcontroller. The TMS570LS31 HDK is a table top card that allows engineers and software developers to evaluate certain characteristics of the TMS570LS3137 microcontroller to determine if the microcontroller meets the designer's application requirements as well as begin early application development. Evaluators can create software to execute on board or expand the system in a variety of ways.

### Notational Conventions

This document uses the following conventions.

The TMS570LS31 HDK will sometimes be referred to as the HDK.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing:

- equations
- !rd = !strobe&rw

### Information About Cautions

This book may contain cautions.

***This is an example of a caution statement.***

A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

### Related Documentation From Texas Instruments

Information regarding this device can be found at the following Texas Instruments website:  
<http://www.ti.com/tms570>

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## Introduction

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This development kit provides a product-ready hardware and software platform for evaluating the functionality of the Texas Instruments TMS570LS31 microcontroller family. Schematics, list of materials, and PCB layout are available to ease hardware development and reduce time to market.

### 1.1 Scope of Document

This user's guide lists the contents of the development kit, points out the features of the major components, and provides the instructions necessary to verify your development kit is in working order. Any additional usage instructions or details fall outside the scope of this document. Additional resources will be listed at the end of this user's guide.

### 1.2 TMS570LS31 HERCULES Development Kit (HDK) Features

The HDK comes with a full complement of on board devices that suit a wide variety of application environments. Key features include:

- A Hercules TMS570LS3137 337-pin BGA microcontroller
- Integrated USB JTAG Emulator (XDS100v2)
- External JTAG Headers (ARM® 20 pin and TI Compact 20-pin CTI)
- 10/100 Mbps Ethernet interface
- Two CAN transceivers (SN65HVDA541Q1) and screw terminal blocks
- One ambient light sensor
- One ambient temperature sensor
- Microcontroller's serial communication interface (SCI) universal asynchronous receiver/transmitter (UART) accessible through a USB virtual COM port
- One 8MB SDRAM
- Eight user programmable white LEDs around the MCU silicon
- One user programmable pushbutton
- Three expansion connectors for hardware prototyping
- Reset pushbuttons (nPORRST and nRST)
- One SD card slot (SPI mode)
- Embedded trace macrocell (ETM) debug interface via MIPI connector
- Configurable pin mux options
- 5 V and 3.3 V analog-to-digital converter (ADC) option jumper
- Current measurement capability for 3.3 V IO, 1.2 V core, 1.2 V core, 1.2 V PLL, 3.3 V or 5 V ADC, and 3.3 V  $V_{CCP}$
- Accepts an external power supply between +5V and +12V

### 1.3 HDK Board Block Diagram

Figure 1-1 illustrates the HDK block diagram.

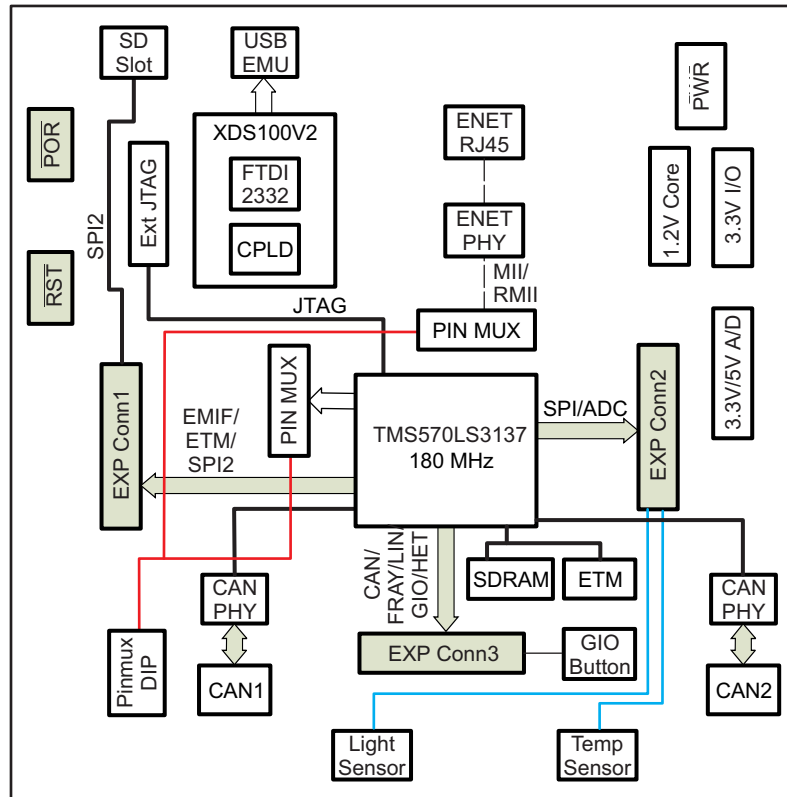


Figure 1-1. TMS570LS31 HDK Board Block Diagram

### 1.4 TMS570LS31 HDK Contents

The kit contains everything needed to develop and run applications for TMS570LS3137 microcontrollers including:

- Board:
  - TMS570LS31 Card
- Cables and Accessories
  - Type A to mini B USB cable for using on board XDS100V2 JTAG emulator
  - Ethernet cable
  - Flashlight for light sensor demo
- CCS DVD Containing:
  - Texas Instruments' Code Composer Studio™ Integrated Development Environments (IDE)
- Hercules DVD Containing:
  - Hercules Safety Demos
  - Hardware Abstraction Layer Code Generator (HALCoGen)
  - Training Videos
  - Device Documentation

Not included:

- 12-V power supply

Below are two options that electrically and mechanically will work with the HDK:

- [QAWA-24-12-US01](#)
  - 12-V output, 2-A max output current
  - Positive center
  - Barrel plug (2.1-mm x 5.5-mm)
  - Output Protection: Short Circuit, Overvoltage, Overcurrent
  - Safety approvals: CB, CE, UL, FCC, PSE, LPS, BSMI, RCM, and CCC
- [SMI24-12-V-P5](#)
  - 12-V output, 2-A max output current
  - Positive center
  - Barrel plug (2.1-mm x 5.5-mm)
  - Output Protection: Short Circuit, Overvoltage, Overcurrent
  - Safety approvals: UL/cUL, CCC, RCM, and PSE

## 1.5 HDK Specifications

- Board supply voltage: 5 V–12 V Vdc
- Board supply current: 130 mA typ (fully active, CPU at 180 MHz)
- Dimensions: 4.90" x 4.30" x 0.85" (LxWxH)

## 1.6 Basic Operation

The HDK is designed to work with TI's Code Composer Studio and other third party ARM IDEs. The IDE communicates with the board through the embedded emulator or an external JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Hercules-specific software. This process will install all of the necessary development tools, documentation and drivers.

## 1.7 Memory Map

The TMS570LS31 family of MCUs have a large byte addressable address space. [Table 1-1](#) shows the address space of a TMS570LS3137 microcontroller on the left with specific details of how each region is used by the HDK on the right. By default, the internal memory sits at the beginning of the address space.

The SDRAM is mapped into CS0 space on the EMIF. CS[4:2] are used for synchronous memory for example SRAM, NOR Flash, NAND Flash, and so forth.

To use EMIF, the MPU has to be enabled, and the CS regions have to be configured as "device mode" or "strongly ordered mode" through MPU.

**Table 1-1. TMS570LS31 Memory Map**

| Start Address | End Address | HDK            |
|---------------|-------------|----------------|
| 0x0000 0000   | 0x002F FFFF | Flash          |
| 0x0800 0000   | 0x0803 FFFF | RAM            |
| 0x0840 0000   | 0x0843 FFFF | RAM-ECC        |
| 0x6000 0000   | 0x63FF FFFF | CS2 Async RAM  |
| 0x6400 0000   | 0x67FF FFFF | CS3 Async RAM  |
| 0x6800 0000   | 0x7BFF FFFF | CS4 Async RAM  |
| 0x8000 0000   | 0x87FF FFFF | CS0 Sync SDRAM |

## 1.8 Power Supply

The HDK board operates from a single +12 V external power supply connected to the main power input (P1), a 2.5 mm, barrel-type plug. Internally, the +12 V input is converted into +1.2 V, +3.3 V and +5.0 V using Texas Instruments swift voltage regulators and PTH power module. The +1.2 V supply is used for the MCU core while the +3.3 V supply is used for the MCU's I/O buffers and other module on the board. The +5.0 V supply is used for ADC power (second option) and USB VBUS.

There are multiple power test points on the HDK board. The three main test point pairs provide a convenient mechanism to check the HDK's current for each supply. [Table 1-2](#) shows the voltages for each test point and what the supply is used for.

**Table 1-2. Power Test Points**

| Test Point Pair | Voltage                              | Voltage Use             |
|-----------------|--------------------------------------|-------------------------|
| TP14 and TP15   | 1.2 V                                | MCU core                |
| TP16 and TP17   | 3.3 V                                | MCU IO and logic        |
| TP18 and TP19   | 1.2 V                                | MCU PLL                 |
| TP20 and TP21   | 3.3 V                                | MCU Flash pump          |
| TP22 and TP23   | 3.3 V or 5.0 V<br>(J8 to enable 5 V) | MCU MibADC, and ADREFHI |



## Physical Description

This section describes the physical layout of the TMS570LS31 HDK board and its interfaces.

### 2.1 Board Layout

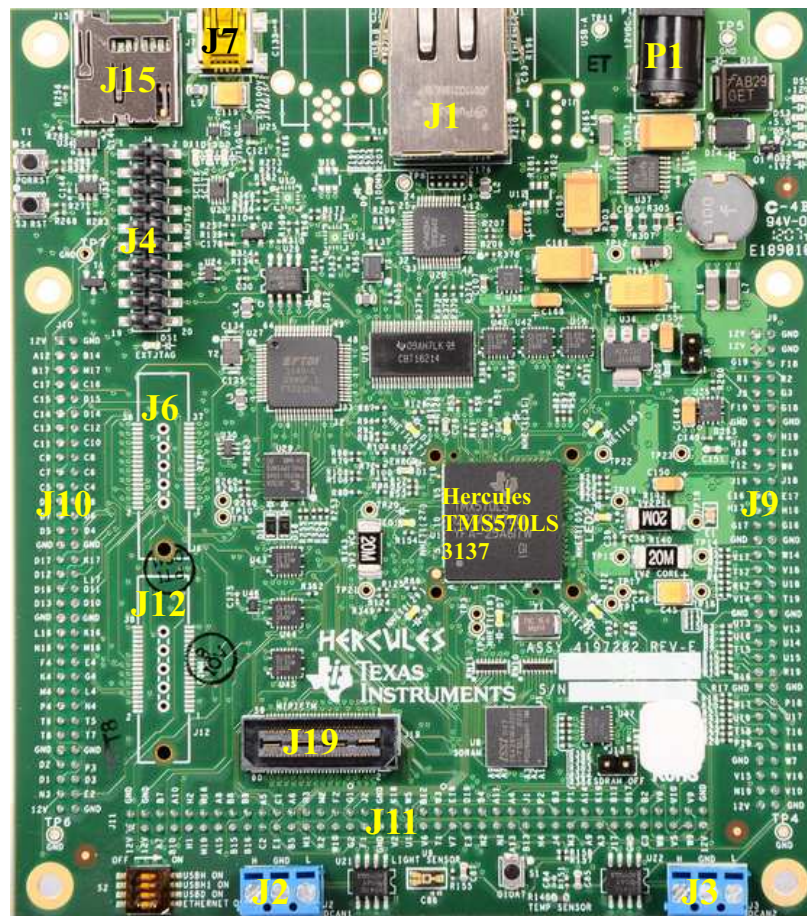
The TMS570LS31 HDK board is a 4.9 x 4.3 inch (125 x 109 mm) eight layer printed circuit board that is powered by an external +5 V to approximately +12 V only power supply. [Figure 2-1](#) shows the layout of the TMS570LS31 HDK board.



Figure 2-1. TMS570LS31 HDK Board, Interfaces Top Side

## 2.2 Connectors

The HDK board has 13 interfaces to various peripherals. These interfaces are described in the following sections.



**Figure 2-2. Connectors on TMS570LS31 HDK**

**Table 2-1. Connectors on HDK Board**

| Connector | Size               | Function                           |
|-----------|--------------------|------------------------------------|
| J1        | RJ45               | Ethernet                           |
| J2        | 3 terminal, 2.54mm | DCAN1                              |
| J3        | 3 terminal, 2.54mm | DCAN2                              |
| J4        | 10x2, 2.54mm       | ARM 20pin JTAG header              |
| J6        | 19x2, mictor       | RTP                                |
| J7        | 4pin, Mini-B USB   | XDS100V2 USB                       |
| J9        | 33x2, 2mm          | Exp P1, SPI1, SPI5, ADC            |
| J10       | 33x2, 2mm          | EXP P2, SPI2, EMIF, ECLK           |
| J11       | 40x2, 2mm          | EXP P3, SPI3, GIO, NHET, DCAN, LIN |
| J12       | 19x2, mictor       | DMM                                |
| J15       |                    | SD card                            |
| J19       | 30x2, MIPI         | ETM MIPI Header                    |
| P1        | 2.5mm              | +12 V In                           |

### 2.2.1 20-Pin ARM JTAG Header

In addition to on board XDS100V2 JTAG, one 20-pin ARM JTAG header is added for using external emulator. This is the standard interface used by JTAG emulators to interface to ARM microcontrollers. The pinout for the connector is shown in [Table 2-2](#).

**Table 2-2. 20-Pin ARM JTAG Header**

| Signal Name | Pin Number | Pin Number | Signal Name     |
|-------------|------------|------------|-----------------|
| Vref        | 1          | 2          | V <sub>CC</sub> |
| nTRST       | 3          | 4          | GND             |
| TDI         | 5          | 6          | GND             |
| TMS         | 7          | 8          | GND             |
| TCK         | 9          | 10         | GND             |
| RTCK        | 11         | 12         | GND             |
| TDO         | 13         | 14         | GND             |
| nRST        | 15         | 16         | GND             |
| NC          | 17         | 18         | GND             |
| NC          | 19         | 20         | GND             |

### 2.2.2 Ethernet Interface

The TMS570LS3137 integrates an MII/RMII Ethernet MAC on chip. This interface is routed to the on board PHY via CBT switches. The board uses a DP83640 PHY. The interface is isolated and brought out to a RJ-45 connector with integrated magnetics, J1. The pinmux control DIP S2 is used to control the CBT FET switch for RMII, MII or other functions.

The J1 connector is used to provide a 10/100 Mbps Ethernet interface. This is a standard RJ-45 connector. The cable end pinout for the J1 connector is shown in [Table 2-3](#).

**Table 2-3. J1, Ethernet Interface**

| Pin Number | Signal | Pin Number | Signal |
|------------|--------|------------|--------|
| 1          | D0+    | 2          | D0-    |
| 3          | D1-    | 4          | D2+    |
| 5          | D2-    | 6          | D1-    |
| 7          | D3+    | 8          | D3-    |

Two LEDs are embedded into the connector to report link status (green LED) and transmit and receive status of the PHY (yellow LED).

### 2.2.3 CAN Interface

The TMS570LS3137 has up to three DCAN interfaces that provide a high-speed serial interface. Two 3-pin screw terminal blocks, J2, J3, are used to interface to the DCAN bus. The pinouts for this connector are shown in [Figure 2-4](#). H means CAN High (CAN H), and L means CAN Low (CAN L).

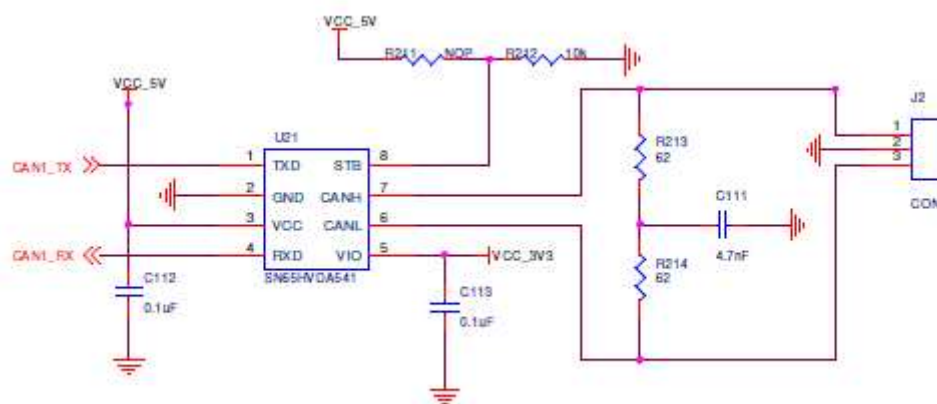


Figure 2-3. CAN Bus Termination

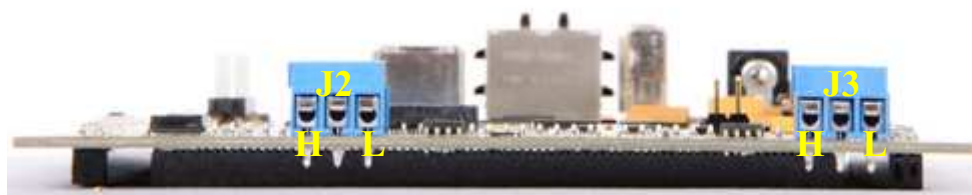


Figure 2-4. J2, J3 CAN Bus Interface (Screw Terminal)

## 2.2.4 J19, MIPI ETM Connector

Figure 2-5 and Table 2-4 show the 60 pin MIPI header.

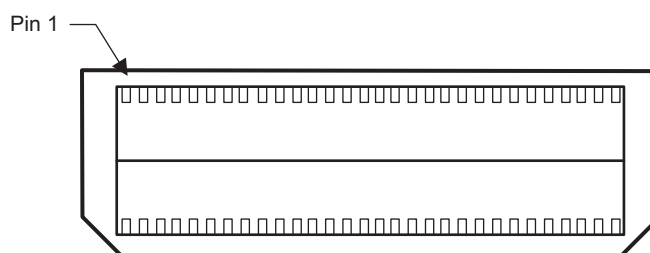


Figure 2-5. J19, 60 Pin MIPI ETM Header



**Table 2-4. J19, MIPI Connector Signal Mapping**

| MCU Signals     | Pin Number |  | Pin Number | MCU Signals  |
|-----------------|------------|--|------------|--------------|
| 3.3V            | 1          |  | 2          | TMS          |
| TCK             | 3          |  | 4          | TDO          |
| TDI             | 5          |  | 6          | System reset |
| RTCK            | 7          |  | 8          | nTRST        |
| NC              | 9          |  | 10         | NC           |
| NC              | 11         |  | 12         | 3.3 V        |
| ETMTACECLKOUT   | 13         |  | 14         | NC           |
| To GND thru 0 W | 15         |  | 16         | GND          |
| EMTTRACECTL     | 17         |  | 18         | ETMDATA[19]  |
| ETMDATA[0]      | 19         |  | 20         | ETMDATA[20]  |
| ETMDATA[1]      | 21         |  | 22         | ETMDATA[21]  |
| ETMDATA[2]      | 23         |  | 24         | ETMDATA[22]  |
| ETMDATA[3]      | 25         |  | 26         | ETMDATA[23]  |
| ETMDATA[4]      | 27         |  | 28         | ETMDATA[24]  |
| ETMDATA[5]      | 29         |  | 30         | ETMDATA[25]  |
| ETMDATA[6]      | 31         |  | 32         | ETMDATA[26]  |
| ETMDATA[7]      | 33         |  | 34         | ETMDATA[27]  |
| ETMDATA[8]      | 35         |  | 36         | ETMDATA[28]  |
| ETMDATA[9]      | 37         |  | 38         | ETMDATA[29]  |
| ETMDATA[10]     | 39         |  | 40         | ETMDATA[30]  |
| ETMDATA[11]     | 41         |  | 42         | ETMDATA[31]  |
| ETMDATA[12]     | 43         |  | 44         | NC           |
| ETMDATA[13]     | 45         |  | 46         | NC           |
| ETMDATA[14]     | 47         |  | 48         | NC           |
| ETMDATA[15]     | 49         |  | 50         | NC           |
| ETMDATA[16]     | 51         |  | 52         | NC           |
| ETMDATA[17]     | 53         |  | 54         | NC           |
| ETMDATA[18]     | 55         |  | 56         | NC           |
| GND             | 57         |  | 58         | GND          |
| NC              | 59         |  | 60         | NC           |

### 2.2.5 J7, XDS100V2 USB JTAG Interface

The USB connector J7 is used to connect to the host development system that is running the software development IDE, Code Composer Studio. The signals on this connector are shown in [Table 2-5](#).

**Table 2-5. J7, XDS100V2 USB JTAG Interface**

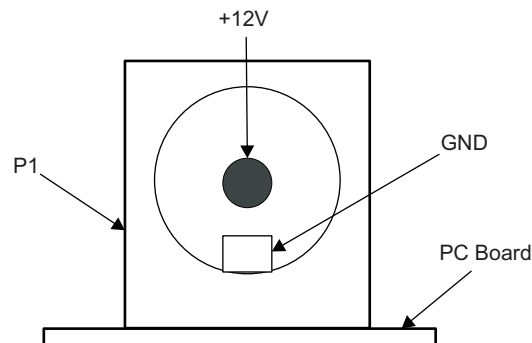
| Pin Number | Signal Name |
|------------|-------------|
| 1          | USBVDD      |
| 2          | D-          |
| 3          | D+          |
| 4          | NC          |
| 5          | USBVSS      |

Before the board is shipped, the XDS100V2 port1 is configured as JTAG, and port2 is configured as SCI. The CPLD on the board is also programmed to route the JTAG signals to the MCU.

There is a circuitry to detect the external JTAG emulator. If a device is plugged onto the header J4 and J19, the DS1 LED will be turned on, and XDS100V2 JTAG is disabled.

### 2.2.6 P1, +5 V to +12 V Input

Connector P1 is the input power connector. This connector brings in +5 V to +12 V to the HDK board. This is a 2.5 mm jack. [Figure 2-6](#) shows this connector as viewed from the card edge.



**Figure 2-6. +12 V Input Jack**

### 2.2.7 SCI Interface

The internal SCI on the TMS570LS3137 device is connected to the second port of the XDS100V2. The XDS100V2 USB driver makes the FT2232H second channel appear as a virtual COM port (VCP). This allows the user to communicate with the USB interface via a standard PC serial emulation port.

### 2.2.8 Daughter Card Interface

The HDK provides expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their EVM platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for all major interfaces including asynchronous memory, peripherals, and A/D expansion.

There are three daughter card interfaces: J9, J10, J11. These connectors are described in [Table 2-6](#).

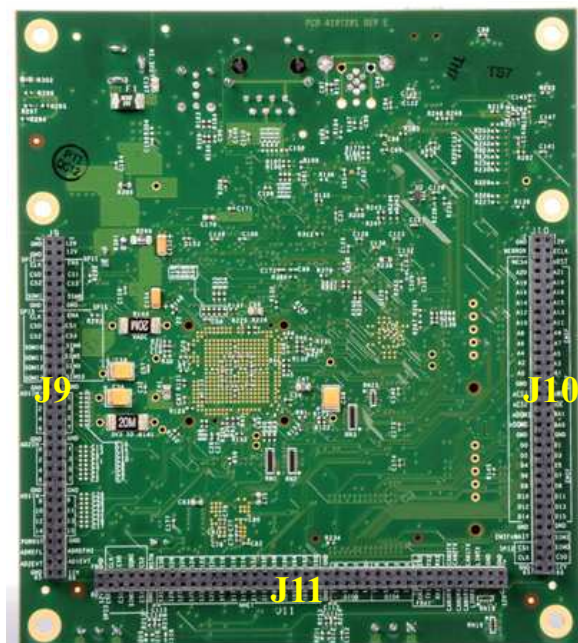


Figure 2-7. J9, J10, and J11 on HDK

Table 2-6. Expansion Connector P1 (J9, Left, BottomView)

| Signal Name    | Pin Number | Number | Pin Number | Signal Name        |
|----------------|------------|--------|------------|--------------------|
| EXP_12V        |            | 1      | 2          | GND                |
| EXP_12V        |            | 3      | 4          | GND                |
| MibSPI1ENA     | G19        | 5      | 6          | F18 MibSPI1CLK     |
| MibSPI1CS[1]   | F3         | 7      | 8          | R2 MibSPI1CS[0]    |
| MibSPI1CS[3]   | J3         | 9      | 10         | G3 MibSPI1CS[2]    |
| MibSPI1SIMO    | F19        | 11     | 12         | G18 MibSPI1SOMI    |
| GND            |            | 13     | 14         | GND                |
| MibSPI5ENA     | H18        | 15     | 16         | H19 MibSPI5CLK     |
| MibSPI5CS[1]   | B6         | 17     | 18         | E19 MibSPI5CS[0]   |
| MibSPI5CS[3]   | T12        | 19     | 20         | W6 MibSPI5CS[2]    |
| MibSPI5SIMO[0] | J19        | 21     | 22         | MibSPI5SOMI[0]     |
| MibSPI5SIMO[1] | E16        | 23     | 24         | E17 MibSPI5SOMI[1] |
| MibSPI5SIMO[2] | H17        | 25     | 26         | H16 MibSPI5SOMI[2] |
| MibSPI5SIMO[3] | G17        | 27     | 28         | G16 MibSPI5SOMI[3] |
| GND            |            | 29     | 30         | GND                |
| AD1IN[1]       | V17        | 31     | 32         | W14 AD1IN[0]       |
| AD1IN[3]       | T17        | 33     | 34         | V18 AD1IN[2]       |
| AD1IN[5]       | R17        | 35     | 36         | U18 AD1IN[4]       |
| AD1IN[7]       | V14        | 37     | 38         | T19 AD1IN[6]       |
| GND            |            | 39     | 40         | GND                |
| AD2IN[1]       | U13        | 41     | 42         | V13 AD2IN[0]       |
| AD2IN[3]       | U16        | 43     | 44         | U14 AD2IN[2]       |
| AD2IN[5]       | T15        | 45     | 46         | U15 AD2IN[4]       |
| AD2IN[7]       | R16        | 47     | 48         | R19 AD2IN[6]       |
| AGND           |            | 49     | 50         | GND                |

**Table 2-6. Expansion Connector P1 (J9, Left, BottomView) (continued)**

| Signal Name | Pin Number | Number |    | Pin Number | Signal Name |
|-------------|------------|--------|----|------------|-------------|
| AD1IN[9]    | W17        | 51     | 52 | P18        | AD1IN[8]    |
| AD1IN[11]   | U19        | 53     | 54 | U17        | AD1IN[10]   |
| AD1IN[13]   | T18        | 55     | 56 | T16        | AD1IN[12]   |
| AD1IN[15]   | P19        | 57     | 58 | R18        | AD1IN[14]   |
| GND         |            | 59     | 60 |            | POR_RSTn    |
| ADREFHI     | V15        | 61     | 62 | V16        | ADREFLO     |
| AD1EVT      | N19        | 63     | 64 | V10        | AD2EVT      |
| EXP_12V     |            | 65     | 66 |            | GND         |

**Table 2-7. Expansion Connector P2 (J10, Right, BottomView)**

| Signal Name   | Pin Number | Number | Pin Number | Signal Name |               |
|---------------|------------|--------|------------|-------------|---------------|
| EXP_12V       |            | 1      | 2          | GND         |               |
| ECLK          | A12        | 3      | 4          | B14         | ERRORn        |
| RST           |            | 5      | 6          | M17         | EMIF_CS[4]    |
| NC            | C17        | 7      | 8          | C16         | NC            |
| NC            | C15        | 9      | 10         | D15         | NC            |
| NC            | C14        | 11     | 12         | D14         | NC            |
| NC            | C13        | 13     | 14         | C12         | NC            |
| NC            | C11        | 15     | 16         | C10         | EMIF_ADDR[12] |
| EMIF_ADDR[11] | C9         | 17     | 18         | C8          | EMIF_ADDR[10] |
| EMIF_ADDR[9]  | C7         | 19     | 20         | C6          | EMIF_ADDR[8]  |
| EMIF_ADDR[7]  | C5         | 21     | 22         | C4          | EMIF_ADDR[6]  |
| EMIF_ADDR[5]  | D9         | 23     | 24         | D8          | EMIF_ADDR[4]  |
| EMIF_ADDR[3]  | D7         | 25     | 26         | D6          | EMIF_ADDR[2]  |
| EMIF_ADDR[1]  | D5         | 27     | 28         | D4          | EMIF_ADDR[0]  |
| GND           |            | 29     | 30         |             | GND           |
| EMIF_Wen      | D17        | 31     | 32         | K17         | EMIF_CS[3]    |
| EMIF_Oen      | D12        | 33     | 34         | L17         | EMIF_CS[2]    |
| EMIF_BA[1]    | D16        | 35     | 36         | D11         | EMIF_DQMn[1]  |
| EMIF_BA[0]    | D13        | 37     | 38         | D10         | EMIF_DQMn[0]  |
| GND           |            | 39     | 40         |             | GND           |
| EMIFDATA[1]   | L16        | 41     | 42         | K16         | EMIFDATA[0]   |
| EMIFDATA[3]   | N16        | 43     | 44         | M16         | EMIFDATA[2]   |
| EMIFDATA[5]   | F4         | 45     | 46         | E4          | EMIFDATA[4]   |
| EMIFDATA[7]   | K4         | 47     | 48         | G4          | EMIFDATA[6]   |
| EMIFDATA[9]   | M4         | 49     | 50         | L4          | EMIFDATA[8]   |
| EMIFDATA[11]  | P4         | 51     | 52         | N4          | EMIFDATA[10]  |
| EMIFDATA[13]  | T6         | 53     | 54         | T5          | EMIFDATA[12]  |
| EMIFDATA[15]  | T8         | 55     | 56         | T7          | EMIFDATA[14]  |
| GND           |            | 57     | 58         |             | GND           |
| SPI2_SOMI     | D2         | 59     | 60         | P3          | EMIF_nWAIT    |
| SPI2_SIMO     | D1         | 61     | 62         | D3          | SPI2_CS1      |
| SPI2_CS0      | N3         | 63     | 64         | E2          | SPI2_CLK      |
| EXP_12V       |            | 65     | 66         |             | GND           |



**Table 2-8. Expansion Connector P3 (J11, Bottom One, TopView)**

| Signal Name  | Pin Number | Number | Pin Number | Signal Name |              |
|--------------|------------|--------|------------|-------------|--------------|
| EXP_12V      |            | 1      | 2          | GND         |              |
| EXP_12V      |            | 3      | 4          | GND         |              |
| LINRX        | A7         | 5      | 6          | B7          | LINTX        |
| CAN1RX       | B10        | 7      | 8          | A10         | CAN1TX       |
| CAN2RX       | H1         | 9      | 10         | H2          | CAN2TX       |
| CAN3RX       | M19        | 11     | 12         | M18         | CAN3TX       |
| FRAYRX1      | A15        | 13     | 14         | A8          | FRAYRX2      |
| FRAYTX1      | B15        | 15     | 16         | B8          | FRAYTX2      |
| FRAYTXEN1    | B16        | 17     | 18         | B9          | FRAYTXEN2    |
| GIOA[1]      | C2         | 19     | 20         | A5          | GIOA[0]      |
| GIOA[3]      | E1         | 21     | 22         | C1          | GIOA[2]      |
| GIOA[5]      | B5         | 23     | 24         | A6          | GIOA[4]      |
| GIOA[7]      | M1         | 25     | 26         | H3          | GIOA[6]      |
| GIOB[1]      | K2         | 27     | 28         | M2          | GIOB[0]      |
| GIOB[3]      | W10        | 29     | 30         | F2          | GIOB[2]      |
| GIOB[5]      | G2         | 31     | 32         | G1          | GIOB[4]      |
| GIOB[7]      | F1         | 33     | 34         | J2          | GIOB[6]      |
| GND          |            | 35     | 36         |             | GND          |
| NHET1[1]     | V2         | 37     | 38         | K18         | NHET1[0]     |
| NHET1[3]     | U1         | 39     | 40         | W5          | NHET1[2]     |
| NHET1[5]     | V6         | 41     | 42         | B12         | NHET1[4]     |
| NHET1[7]     | T1         | 43     | 44         | W3          | NHET1[6]     |
| NHET1[9]     | V7         | 45     | 46         | E18         | NHET1[8]     |
| NHET1[11]    | E3         | 47     | 48         | D19         | NHET1[10]    |
| NHET1[13]    | N2         | 49     | 50         | B4          | NHET1[12]    |
| NHET1[15]    | N1         | 51     | 52         | A11         | NHET1[14]    |
| NHET1[17]    | A13        | 53     | 54         | A4          | NHET1[16]    |
| NHET1[19]    | B13        | 55     | 56         | J1          | NHET1[18]    |
| NHET1[21]    | H4         | 57     | 58         | P2          | NHET1[20]    |
| NHET1[23]    | J4         | 59     | 60         | B3          | NHET1[22]    |
| NHET1[25]    | M3         | 61     | 62         | P1          | NHET1[24]    |
| NHET1[27]    | A9         | 63     | 64         | A14         | NHET1[26]    |
| NHET1[29]    | A3         | 65     | 66         | K19         | NHET1[28]    |
| NHET1[31]    | J17        | 67     | 68         | B11         | NHET1[30]    |
| GND          |            | 69     | 70         |             | GND          |
| MibSPI3CS[3] | C3         | 71     | 72         | B2          | MibSPI3CS[2] |
| MibSPI3SIMO  | W8         | 73     | 74         | V8          | MibSPI3SOMI  |
| MibSPI3CS[1] | V5         | 75     | 76         | V10         | MibSPI3CS[0] |
| MibSPI3ENA   | W9         | 77     | 78         | V9          | MibSPI3CLK   |
| EXP_12V      |            | 79     | 80         |             | GND          |

## 2.3 LEDs

The TMS570LS31 HDK board has 19 LEDs. Eight of these LEDs (shown in [Table 2-9](#)) are under user control. Those LEDs are controlled and programmed by NHET signals.

LEDs DS2, DS3, DS4, and DS5 indicate the presence of the power (+1.2 V, +5 V, 3.3 V, and 12 V) s on the board. The LED functions are summarized in [Table 2-9](#) and [Table 2-10](#).

**Table 2-9. Demo LEDs**

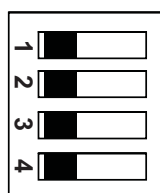
| LED Number | Location     | Signals   | Color |
|------------|--------------|-----------|-------|
| D3         | Left Top     | NHET1[17] | White |
| D4         | Top          | NHET1[31] | White |
| D5         | Right Top    | NHET1[0]  | White |
| D6         | Right Bottom | NHET1[25] | White |
| D7         | Bottom       | NHET1[18] | White |
| D8         | Left bottom  | NHET1[29] | White |
| LED1       | Left         | NHET1[27] | White |
| LED2       | Right        | NHET1[05] | White |

**Table 2-10. Other LEDs as Indicator**

| Number | LED             | Color |
|--------|-----------------|-------|
| D1     | nERROR          | Red   |
| D10    | XDS100V2 SCI RX | Blue  |
| D11    | XDS100V2 SCI TX | Blue  |
| D12    | XDS100V2 PWRENn | Blue  |
| D2     | JTAG TDI        | Blue  |
| D9     | Ethernet Speed  | Blue  |
| DS1    | ARM JTAG Plugin | Blue  |
| DS2    | VCC_1V2         | Blue  |
| DS3    | VCC_5V          | Blue  |
| DS4    | VCC_3V3         | Blue  |
| DS5    | VCC_12V         | Blue  |

## 2.4 S2 DIP Switch

There is one 4-position DIP switches located on the left-bottom corner at reference designator S2. By default, all of the switches are set to the “OFF” position and should remain in that position when completing the steps in this user's guide.


**Figure 2-8. DIP Switch Settings**

The S2 DIP switch is reserved for user application general purpose. [Table 2-11](#) describes the function of each channel on S2.

**Table 2-11. S2 DIP Switch Functions**

| Switch              | OFF Position        | ON Position        |
|---------------------|---------------------|--------------------|
| S2:1 <sup>(1)</sup> | USB Host0 Disabled  | USB Host0 Enabled  |
| S2:2 <sup>(2)</sup> | USB Host1 Disabled  | USB Host1 Enabled  |
| S2:3 <sup>(2)</sup> | USB Device Disabled | USB Device Enabled |
| S2:4 <sup>(3)</sup> | Ethernet Disabled   | Ethernet Enabled   |

<sup>(1)</sup> S2:1 indicates slide 1 on the S2 DIP switch, S2:2 indicates slide 2 on the S2 DIP switch, and so on.

<sup>(2)</sup> S2:2 and S2:3 cannot be enabled at the same time since those two ports have pinmux.

<sup>(3)</sup> To use Ethernet, S2:4 should be enabled and all other have to be disabled.

## 2.5 Jumpers

The HDK board has two jumpers that are used to enable and disable the on-board SDRAM and select 5 V or 3.3 V ADC.

**Table 2-12. Jumpers**

| Jumper Number | OFF      | ON        |
|---------------|----------|-----------|
| J8            | 5 V ADC  | 3.3 V ADC |
| J13           | SDRAM on | SDRAM Off |

## 2.6 S4, Power On Reset Switch

TMS570LS31 MCU has two resets: warm reset (nRST) and power-on reset (nPORRST). Switch S4 is a momentary switch that asserts power on reset to the TMS570LS3137 device. The nPORRST condition is intended to reset all logic on the device including the test and emulation circuitry.

## 2.7 S3, System Reset Switch

Switch S3 is used to assert a warm reset the TMS570LS3137 device. Warm reset does not reset any test or emulation logic. The reset signal from window watchdog will also assert a warm reset to the MCU. The warm reset can be invoked by pushing nRST button, or by RESET signals from XDS100 CPLD, ARM JTAG SREST.

## *Operation Notices*

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### **A.1 Operation Notices**

The user assumes all responsibility and liability for proper and safe handling of the boards. It is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

- For additional information regarding the embedded emulation, see the XDS100 USB wiki on the TI web site at the following URL: <http://tiexpressdsp.com/index.php?title=XDS100>
- Code Composer Studio support is available via a forum at: <http://community.ti.com/forums/138.aspx>
- Hercules MCU support is available via a forum at: <http://www.ti.com/hercules-support>



## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from B Revision (September 2013) to C Revision           | Page |
|------------------------------------------------------------------|------|
| • Updated TMS570LS31 HDK Contents power supply information. .... | 6    |

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3. **Regulatory Notices:**
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    - 3.1.1 *Notice applicable to EVMs not FCC-Approved:*

**FCC NOTICE:** This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.
    - 3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

### CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

### FCC Interference Statement for Class A EVM devices

*NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

## FCC Interference Statement for Class B EVM devices

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

## 3.2 Canada

### 3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

#### Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

#### Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

#### Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

#### Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.



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8.1 *General Limitations.* IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS, REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMNITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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