User's Guide
SLVU677–August 2012

TPS54494 Dual Channel SWIFT™ Evaluation Module

This user's guide contains information for the TPS54494EVM-057 evaluation module as well as for the TPS54494. Included are the performance specifications, schematic, and the bill of materials of the TPS54494EVM-057.

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SWIFT, Eco-mode, D-CAP2 are trademarks of Texas Instruments.

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1 Introduction

The TPS54494 is a dual, adaptive on-time, D-CAP2™-mode, synchronous buck converter requiring a low, external component count. The D-CAP2 control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. The switching frequency is internally set at a nominal of 700 kHz. The high-side and low-side switching MOSFETs are incorporated inside the TPS54494 package along with the gate drive circuitry. The low, drain-to-source on-resistance of the MOSFETs allows the TPS54494 to achieve high efficiencies and helps keep the junction temperature low at high-output currents. The TPS54494 also features auto-skip Eco-mode™ operation for improved light-load efficiency. The TPS54494 dual DC/DC synchronous converter is designed to provide up to 4 A output on CH1 and 2 A output on CH2 from an input voltage source of 4.5 V to 18 V. The output voltage range is from 0.76 V to 7 V. Rated input voltage and output current range for the evaluation module are given in Table 1.

The TPS54494EVM evaluation module is a dual, synchronous buck converter providing 3.3 V at 4 A on CH1 and 1.5 V at 2 A on CH2. This user's guide describes the TPS54494 EVM performance.

NOTE: Throughout the document, x means 1 or 2, for example, VFBx means VFB1 or VFB2.

Table 1. Input Voltage, Output Voltage and Output Current Summary

TPS54494EVM	Input Voltage Range	Output Voltage	Output Current Range
CH1	V_{IN1} = 6 V to 18 V	3.3 V	0 A to 4 A
CH2	V_{IN2} = 5 V to 18 V	1.5 V	0 A to 2 A

2 Performance Specification Summary

A summary of the TPS54494 EVM performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{INx} = 12 V and an output voltage of 3.3 V and 1.5 V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2. TPS54494 EVM Performance Specifications Summary

Specifications		Test Conditions	Min	Typ	Max	Unit
Input voltage range (V_{INx})				(1)12	18	V
Output voltages	V_{OUT1}			3.3		V
	V_{OUT2}			1.5		
Operating frequency		V_{IN1}, V_{IN2} = 12 V, I_{OUT1} = 2 A, I_{OUT2} = 1 A		700		kHz
Output current range	CH1		0		4	A
	CH2		0		2	
Line regulation, V_{OUT1}		I_{OUT1} = 2 A, I_{OUT2} = 0 A, V_{IN1}, V_{IN2}= 6 V to 18 V		+0.25 , -0.52		%
Line regulation, V_{OUT2}		I_{OUT2} = 1 A, I_{OUT1} = 0 A, V_{IN1}, V_{IN2}= 5 V to 18 V		+0.2, -0.4		%
Load regulation, V_{OUT1}		V_{IN1}, V_{IN2} = 12 V, I_{OUT1} = 0 A to 4 A		+0.65, -0.1		%
Load regulation, V_{OUT2}		V_{IN1}, V_{IN2} = 12 V, I_{OUT2} = 0 A to 2 A		+0.6, -0.05		%
Over current limit, V_{OUT1}		V_{IN1} = 12 V, L_1 = 2.2 µH	4.5	5.7	7.0	A
Over current limit, V_{OUT2}		V_{IN2} = 12 V, L_1 = 1.5 µH	2.8	3.9	5.0	A
Output ripple voltage, V_{OUT1}		V_{IN1} = 12 V, I_{OUTx} = 4 A		15		mV_{PP}
Output ripple voltage, V_{OUT2}		V_{IN2} = 12 V, I_{OUTx} = 2 A		25		mV_{PP}
Maximum efficiency, V_{OUT1}		V_{IN1} = 5 V, I_{OUTx}= 0.7 A		94.9%		
Maximum efficiency, V_{OUT2}		V_{IN2} = 5 V, I_{OUTx}= 0.7 A		90.1%		

(1) See Table 1

3 Modifications

This evaluation module is designed to provide access to the features of the TPS54494. Some modifications can be made to this module.

3.1 Output Voltage Setpoint

To change the output voltages of the EVM, it is necessary to change the value of the top resistor of the feedback divider, R1 or R3. Please refer to the top assembly in Figure 20 to locate the resistors close to the output connectors. Changing the value of R1 or R3 can change the output voltage above 0.765 V. The value of R1 or R3 for a specific output voltage can be calculated using Equation 1.

For output voltage from 0.76 V to 7 V:

$$V_{OUT1} = 0.765\ V \times \left(1 + \frac{R1}{R2}\right);\ V_{OUT2} = 0.765\ V \times \left(1 + \frac{R3}{R4}\right) \quad (1)$$

Table 3 lists the R1 or R3 values for some common output voltages. For output voltages of 1.8 V or above, a feedforward capacitor (C21 or C20) may be required to improve the phase margin. Pads for this component (C21 or C20) are provided on the printed-circuit board. Note that the resistor values given in Table 3 are standard values and not the exact values calculated using Equation 1.

Table 3. Output Voltages

Output Voltage (V)	R1, R3 (kΩ)	R2, R4 (kΩ)	C21, C20 (pF)	L1, L2 (µH)	C14, C15, C18 Total Capacitance, C16, C17, C19 Total Capacitance (µF)
1	6.81	22.1		1.5 - 2.2	22 - 68
1.05	8.25	22.1		1.5 - 2.2	22 - 68
1.2	12.7	22.1		1.5 - 2.2	22 - 68
1.5	21.5	22.1		1.5 - 2.2	22 - 68
1.8	30.1	22.1	5 - 22	2.2 - 3.3	22 - 68
2.5	49.9	22.1	5 - 22	2.2 - 3.3	22 - 68
3.3	73.2	22.1	5 - 22	2.2 - 3.3	22 - 68
5	124	22.1	5 - 22	4.7	22 - 68
6.5	165	22.1	5 - 22	4.7	22 - 68

3.2 Output Filter and Closed-Loop Response

The TPS54494 relies on the output filter characteristics to ensure stability of the control loop. The recommended output filter components for common output voltages are given in Table 3. It may be possible for other output filter component values to provide acceptable closed-loop characteristics. R11 and R12 are provided for convenience in breaking the control loop and measuring the closed-loop response.

4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54494EVM. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, input voltage ripple, start-up, and switching frequency.

4.1 Input/Output Connections

The TPS54494EVM is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 4 A must be connected to J1 through a pair of 20 AWG wires. The loads must be connected to J3 and/or J2 through a pair of 20 AWG wires. The maximum load current capability is 2 times 2 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the input voltage (V_{IN}) with TP7 providing a convenient ground reference. TP4 and TP3 are used to monitor the output voltages with TP5 and TP6 as the ground references.

Table 4. Connection and Test Points

Reference Designator	Function
J1	V_{IN} (see Table 1 for V_{IN} range)
J2	V_{OUT2}, 1.5 V at 2 A maximum
J3	V_{OUT1}, 3.3 V at 4 A maximum
J4	EN1 control. Connect EN1 to off to disable converter 1; connect EN1 to on to enable converter 1.
J5	EN2 control. Connect EN2 to off to disable converter 2; connect EN2 to on to enable converter 2.
JP1	Jumper to give the possibility to use another input voltage for converter 2.
TP1	V_{IN} test point at V_{IN} connector
TP2	V_{IN2} test point after JP1.
TP3	Output voltage test point for converter 2.
TP4	Output voltage test point for converter 1.
TP5, TP6, TP7	Ground test points at input and output connectors.
TP8	EN2 test point.
TP9	EN1 test point.
TP10	Switch node test point of converter 1.
TP11	Switch node test point of converter 2.
TP12	VREG5 test point.
TP13	PG1 test point.
TP14	PG2 test point.
TP15	Analog ground test point.

4.2 Start-Up Procedure

1. Ensure that the jumper at J4 and/or J5 (Enable control) are set from ENx to off.
2. Apply appropriate V_{IN} voltage to VIN and PGND terminals at J1.
3. Move the jumper at J4 and/or J5 (Enable control) to cover ENx and on. The EVM enables the according output voltage.

4.3 Efficiency

4.3.1 Efficiency of Converter 1

Figure 1 shows the efficiency for the converter 1 on the TPS54494EVM at an ambient temperature of 25°C.

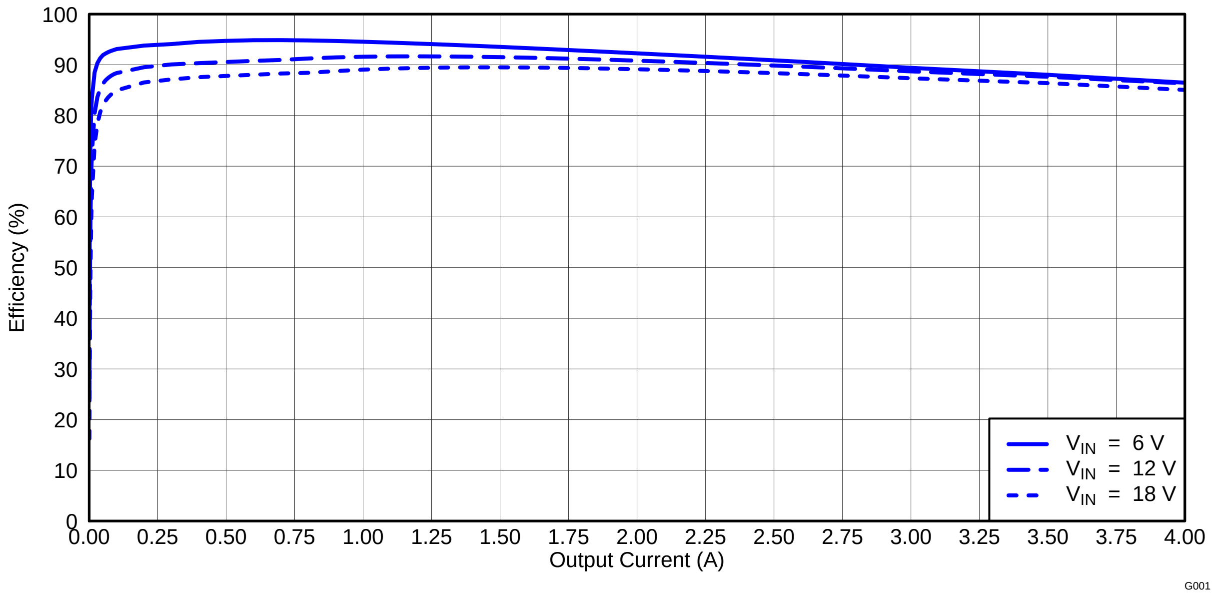


Figure 1. TPS54494EVM Converter 1 Efficiency

Figure 2 shows the light load efficiency for converter 1 on the TPS54494EVM at an ambient temperature of 25°C.

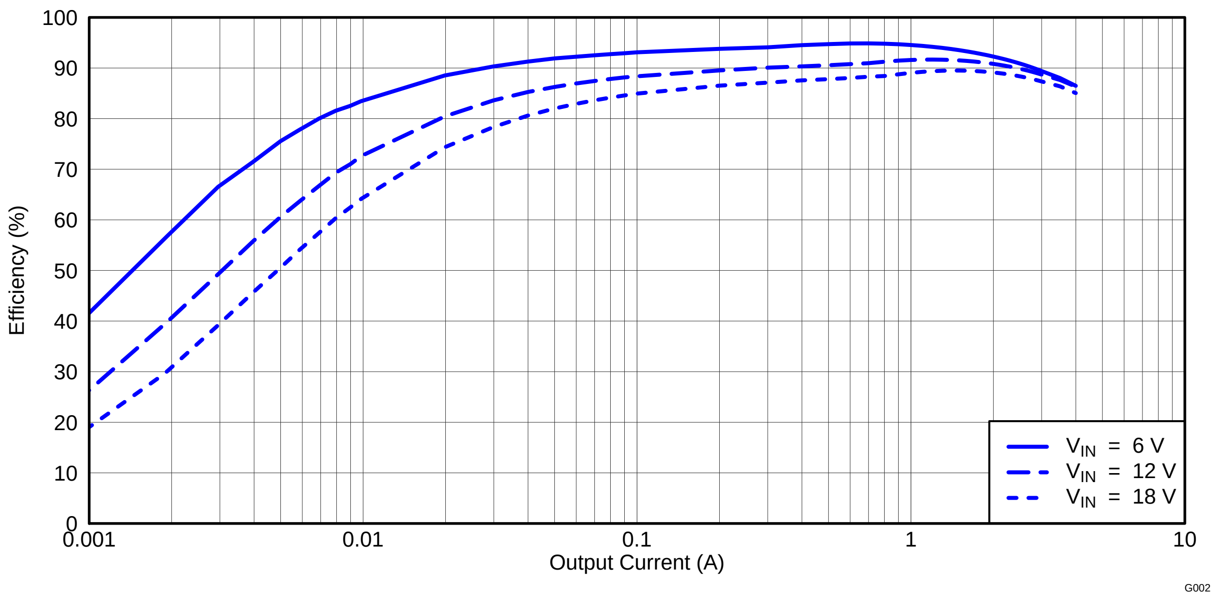


Figure 2. TPS54494EVM Converter 1 Light Load Efficiency

4.3.2 Efficiency of Converter 2

Figure 3 shows the efficiency for the converter 2 on the TPS54494EVM at an ambient temperature of 25°C.

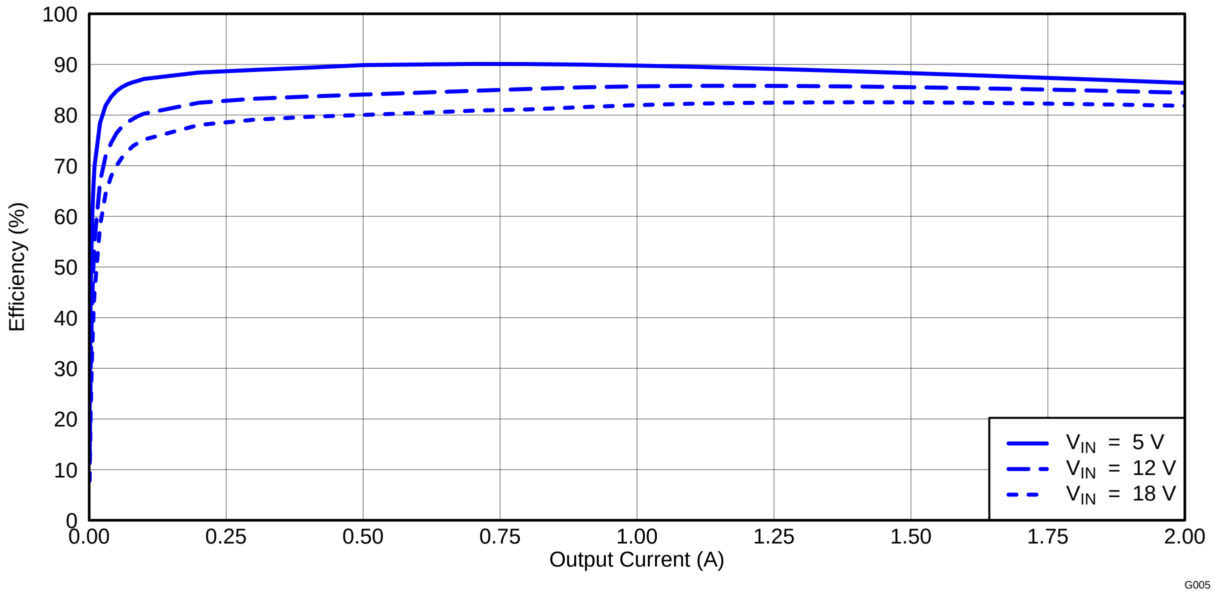


Figure 3. TPS54494EVM Converter 2 Efficiency

Figure 4 shows the light load efficiency for the converter 2 on the TPS54494EVM at an ambient temperature of 25°C.

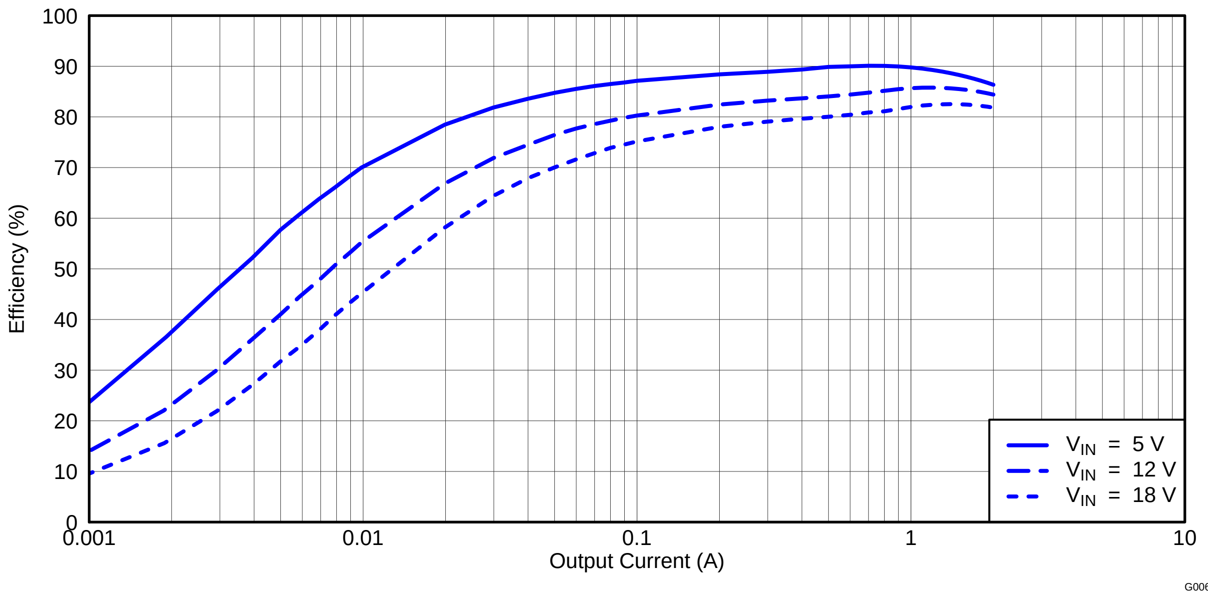


Figure 4. TPS54494EVM Converter 2 Light Load Efficiency

4.4 Load Regulation

4.4.1 Load Regulation of Converter 1

The load regulation for the converter 1 on the TPS54494EVM is shown in Figure 5. On the EVM, the load regulation of converter 1 is independent on the load of converter 2.

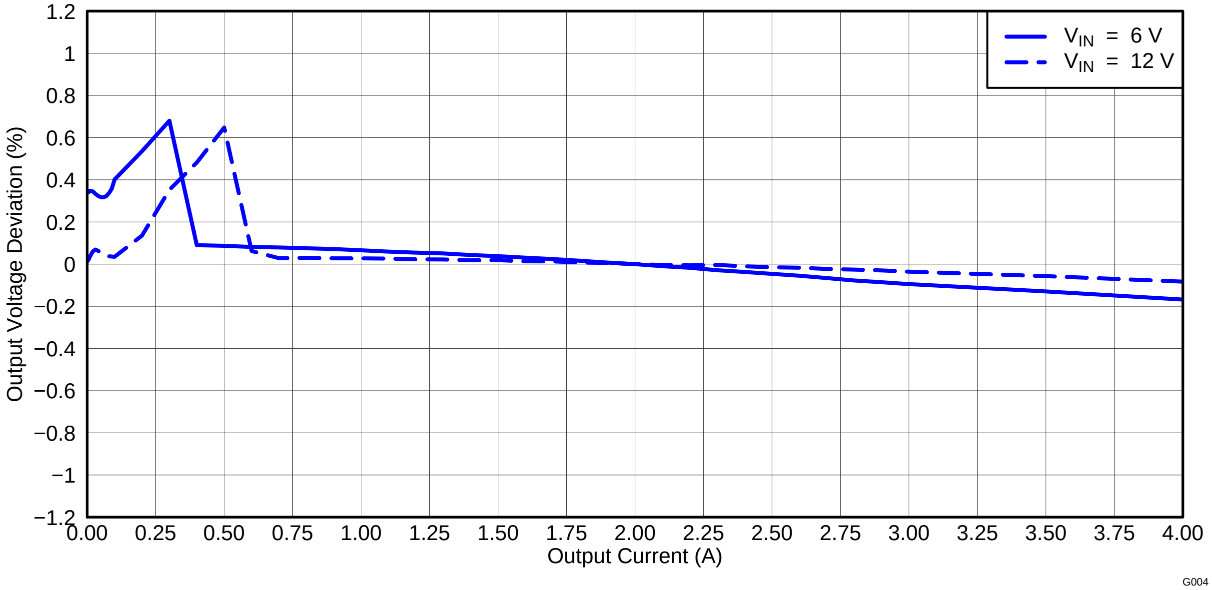


Figure 5. TPS54494EVM Converter 1 Load Regulation

4.4.2 Load Regulation of Converter 2

The load regulation for the converter 2 on the TPS54494EVM is shown in Figure 6. For 5V input voltage, the converter 2 shows on the EVM some dependency on the load of converter 1.

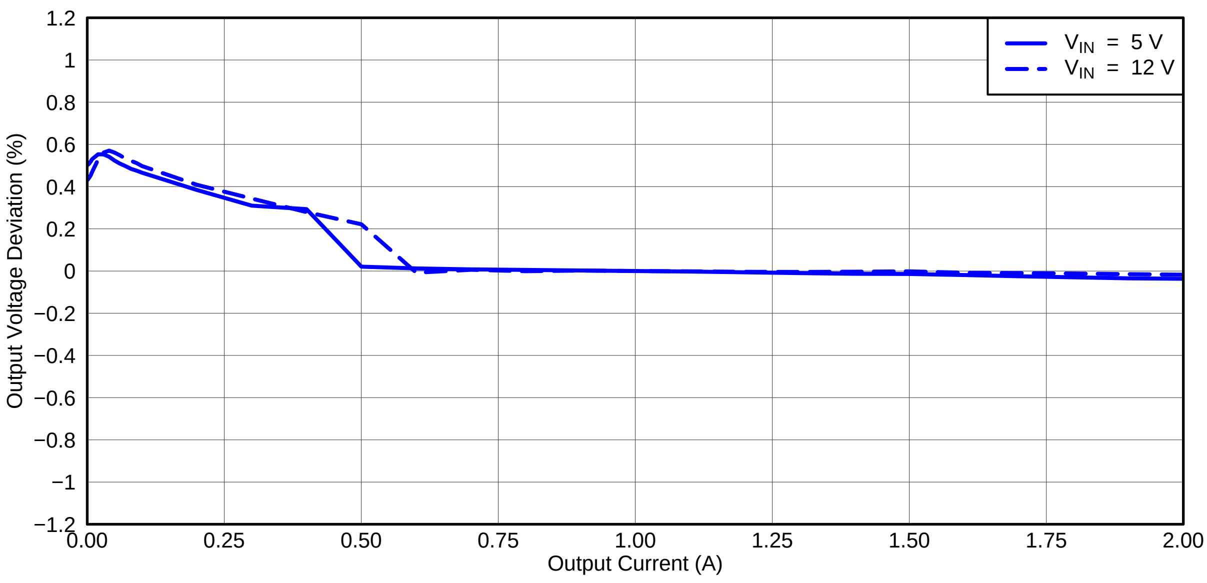


Figure 6. TPS54494EVM Converter 2 Load Regulation

4.5 Line Regulation

4.5.1 Line Regulation Converter 1

The line regulation of converter 1 on the TPS54494EVM is shown in Figure 7.

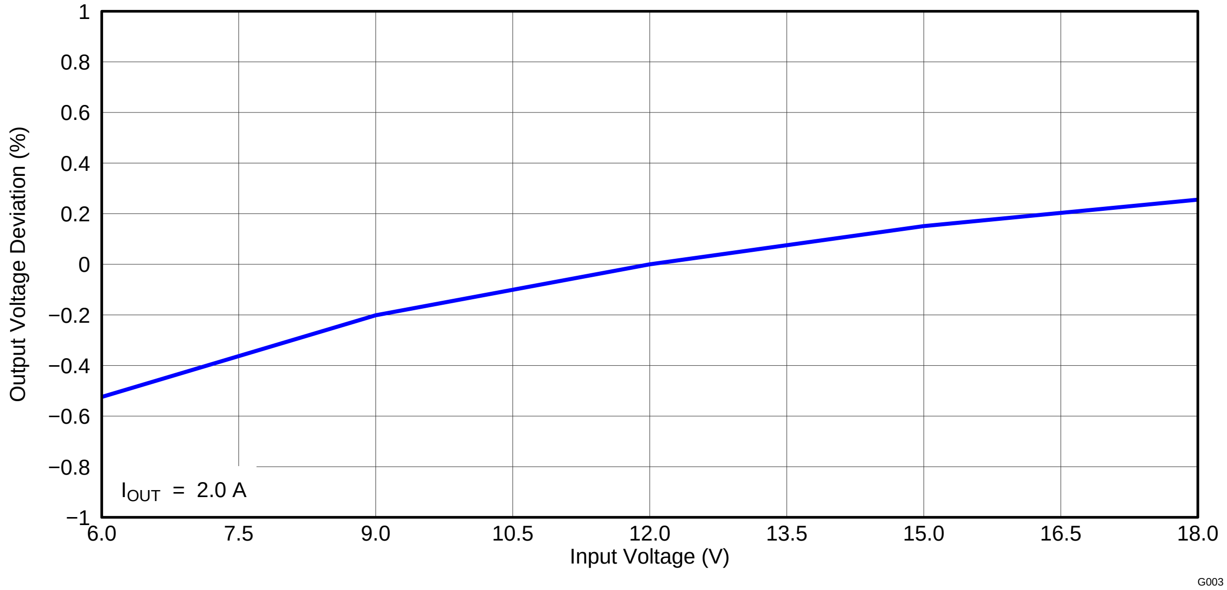


Figure 7. TPS54494EVM Converter 1 Line Regulation

4.5.2 Line Regulation Converter 2

The line regulation of converter 2 on the TPS54494EVM is shown in Figure 8.

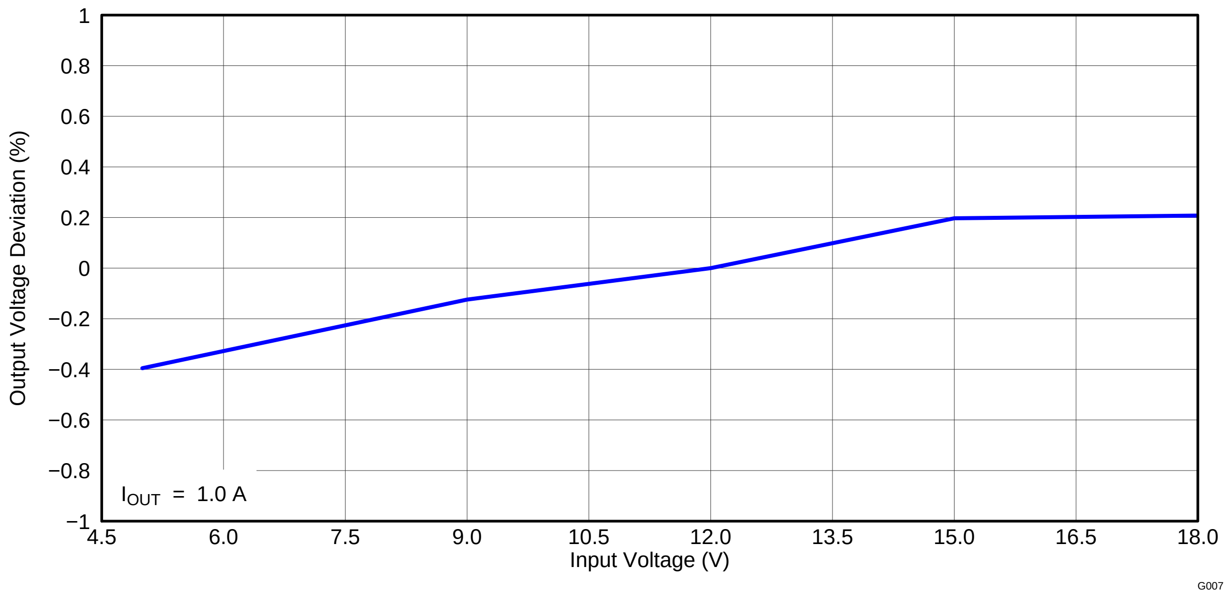


Figure 8. TPS54494EVM Converter 2 Line Regulation

4.6 Load Transient Response

4.6.1 Load Transient Response Converter 1

The response of converter 1 on the TPS54494EVM to a load transient is shown in Figure 9.

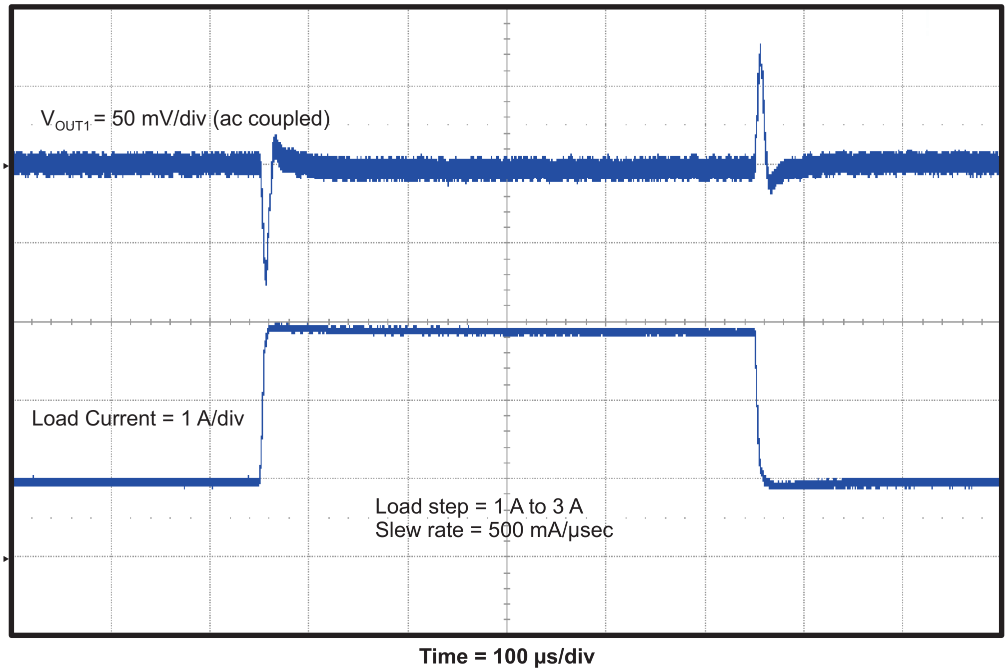


Figure 9. TPS54494EVM Converter 1 Load Transient Response

4.6.2 Load Transient Response Converter 2

The response of converter 2 on the TPS54494EVM to a load transient is shown in Figure 10.

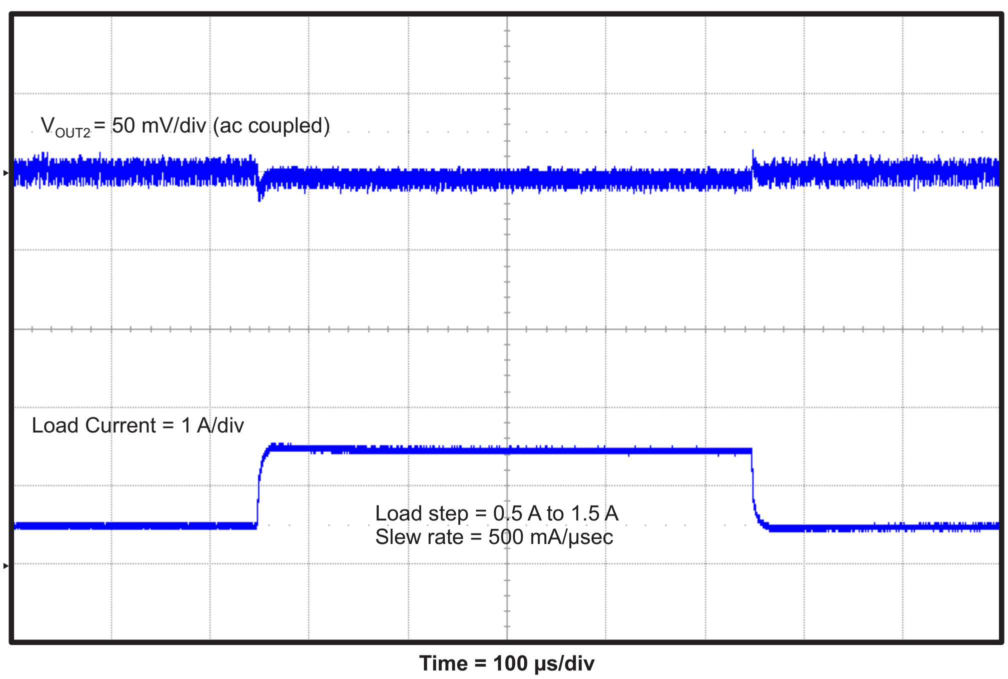


Figure 10. TPS54494EVM Converter 2 Load Transient Response

4.7 Output Voltage Ripple

4.7.1 Output Voltage Ripple Converter 1

The output voltage ripple of converter 1 on the TPS54494EVM is shown in Figure 11. The output current is the rated full load of 4 A.

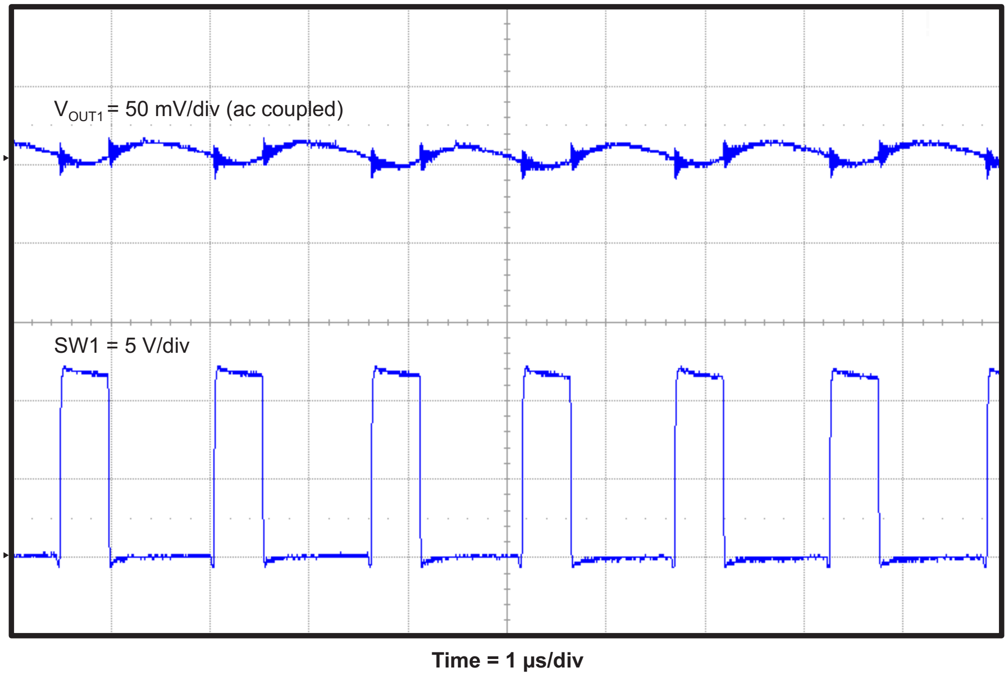


Figure 11. TPS54494EVM Converter 1 Output Voltage Ripple

The output voltage ripple of converter 1 on the TPS54494EVM during Eco-mode™ operation at no load is shown in Figure 12.

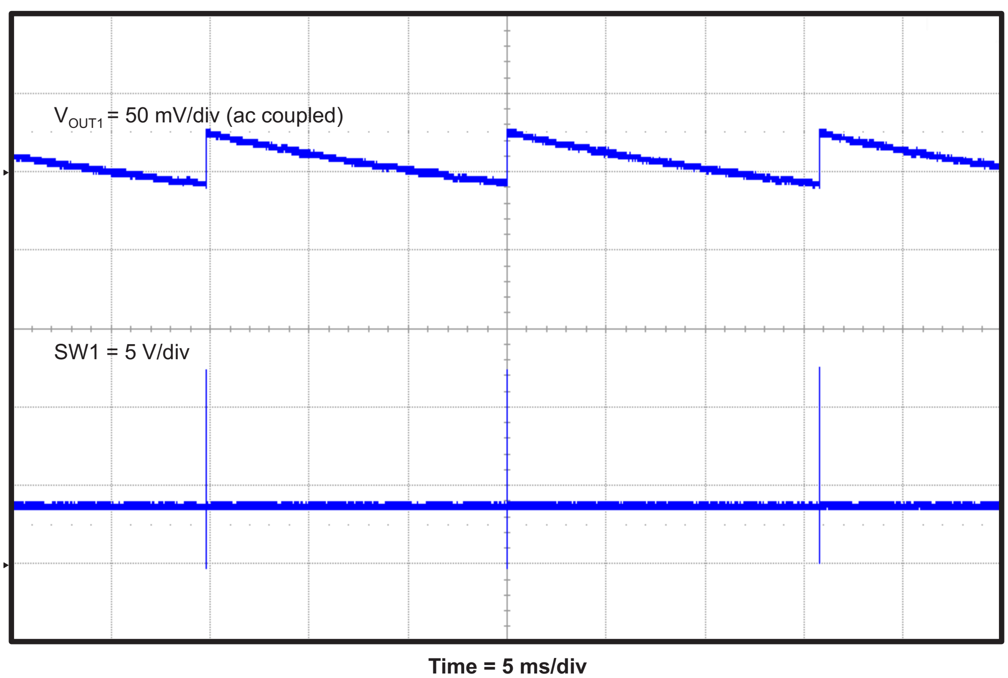
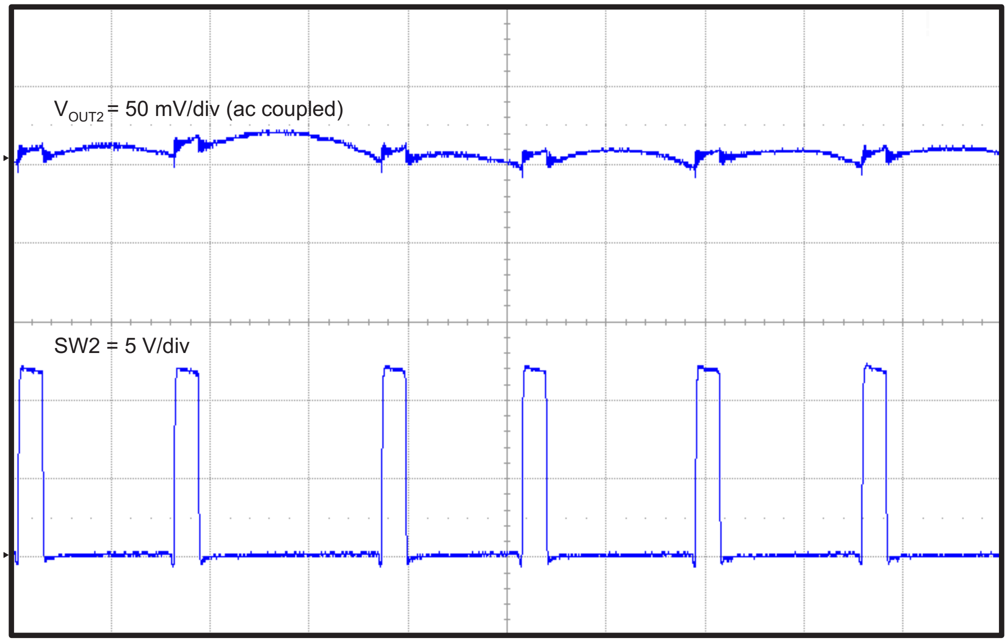


Figure 12. TPS54494EVM Converter 1 Eco-mode™ Output Voltage Ripple at No Load

4.7.2 Output Voltage Ripple Converter 2

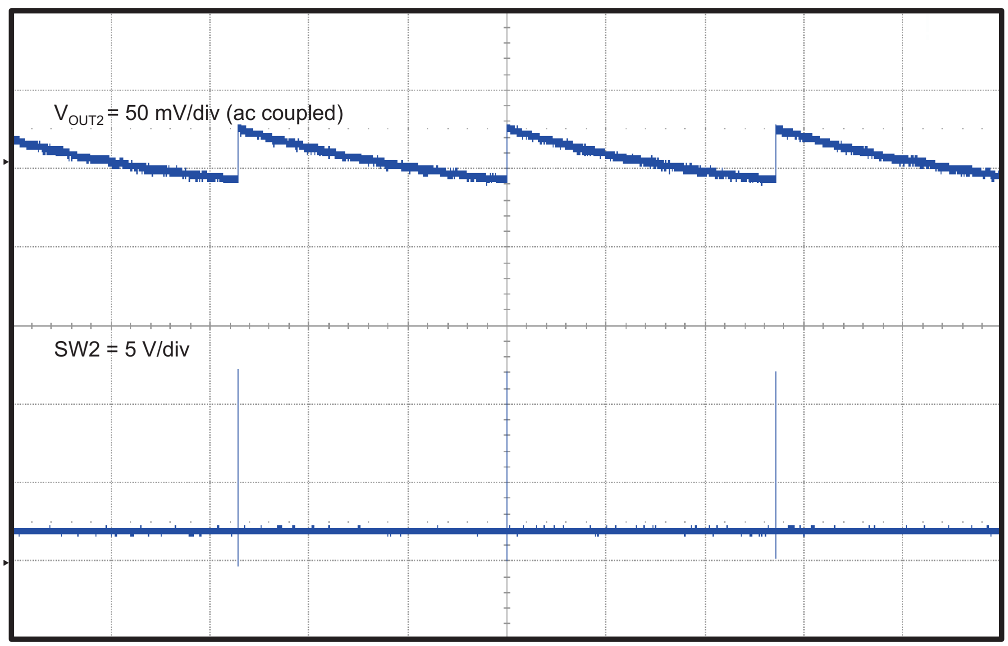
The output voltage ripple of converter 2 on the TPS54494EVM is shown in Figure 13. The output current is the rated full load of 2 A.



Time = 1 µs/div

Figure 13. TPS54494EVM Converter 2 Output Voltage Ripple

The output voltage ripple of converter 2 on the TPS54494EVM during Eco-mode™ operation at no load is shown in Figure 14.



Time = 10 ms/div

Figure 14. TPS54494EVM Converter 2 Eco-mode™ Output Voltage Ripple at No Load

4.8 Input Voltage Ripple

The TPS54494EVM input voltage ripple is shown in Figure 15. The output currents are the rated full load currents of 4 A CH1 and 2 A CH2.

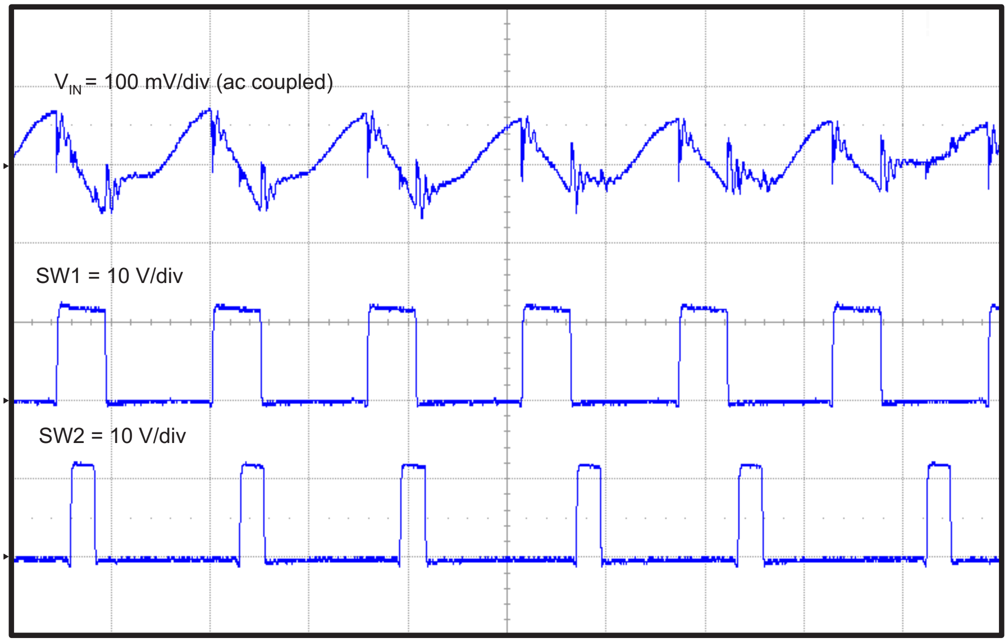


Figure 15. TPS54494EVM Input Voltage Ripple

4.9 Start-Up

4.9.1 Converter 1 Start-Up

The TPS54494EVM start-up waveform of converter 1 relative to V_{IN} is shown in Figure 16.

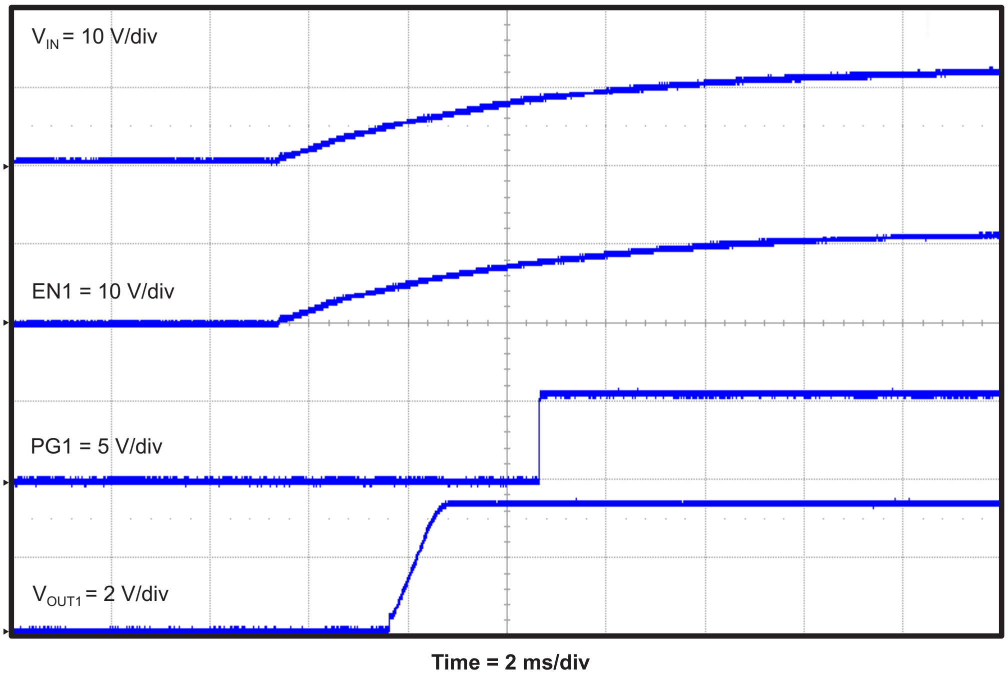


Figure 16. TPS54494EVM Converter 1 Start-Up Relative to V_{IN}

The TPS54494EVM start-up waveform of converter 1 relative to EN1 is shown in Figure 17.

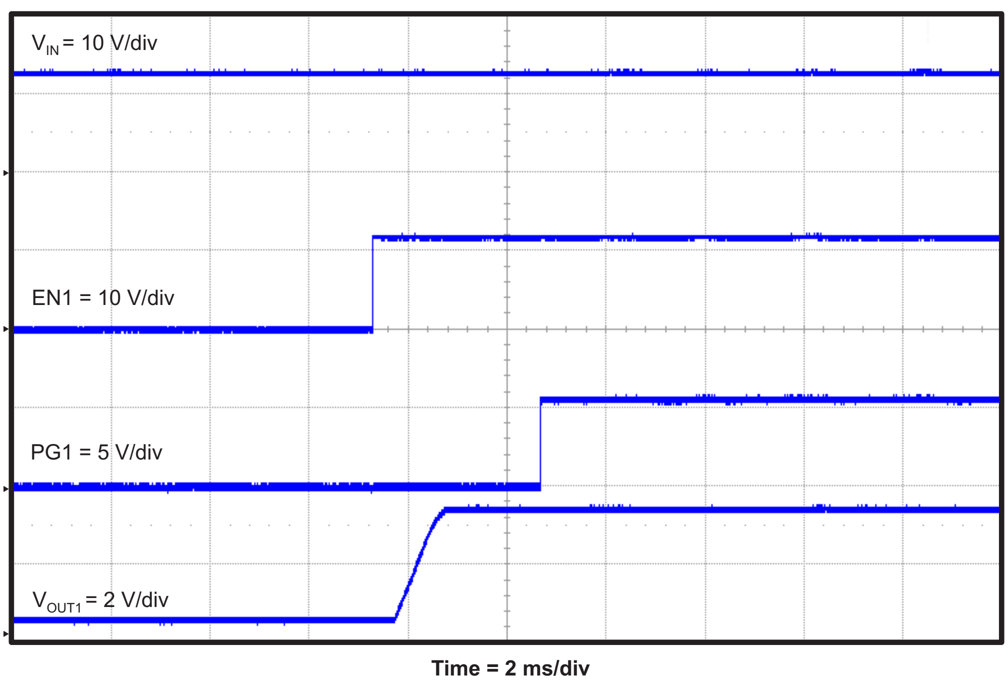


Figure 17. TPS54494EVM Start-Up Relative to EN1

4.9.2 Converter 2 Start-Up

The TPS54494EVM start-up waveform of converter 2 relative to V_{IN} is shown in Figure 18.

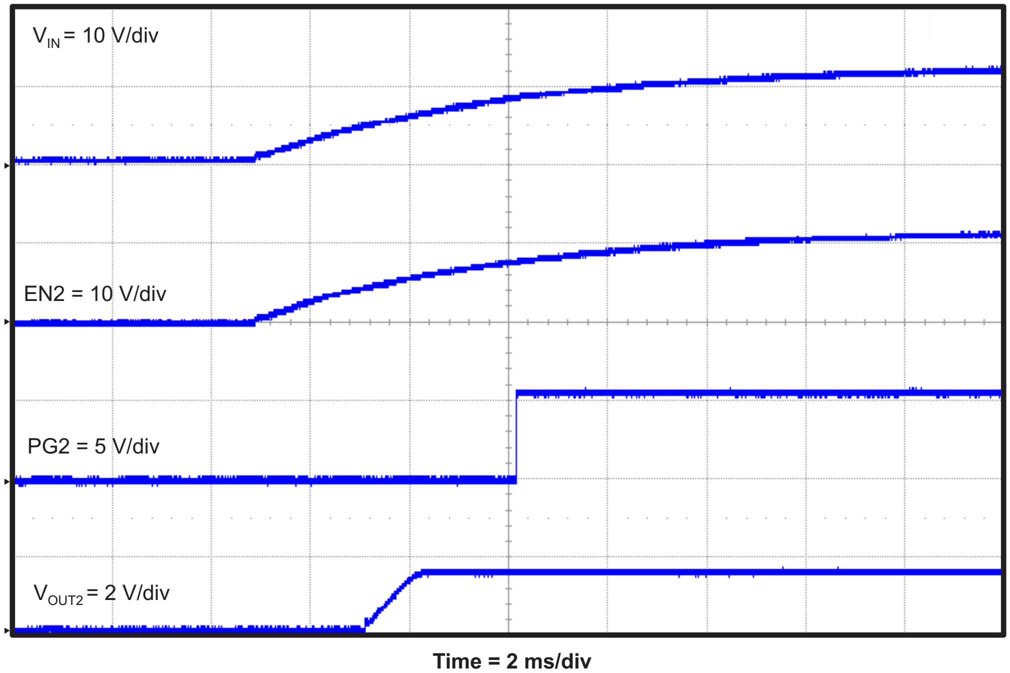


Figure 18. TPS54494EVM Converter 2 Start-Up Relative to V_{IN}

The TPS54494EVM start-up waveform of converter 2 relative to EN2 is shown in Figure 19.

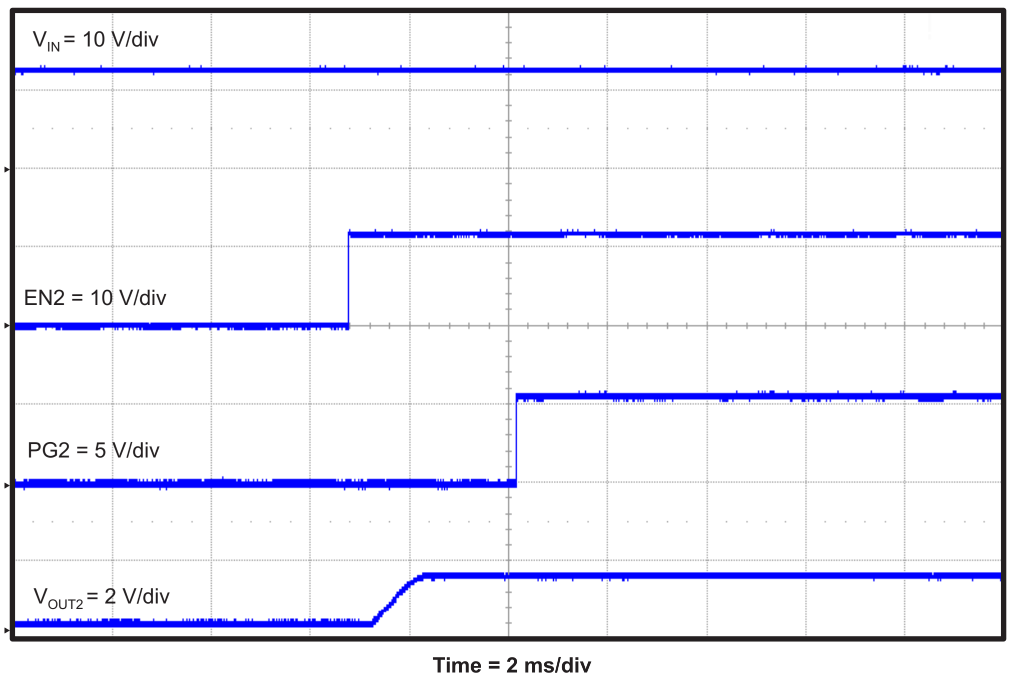


Figure 19. TPS54494EVM Start-Up Relative to EN2

5 Board Layout

This section provides a description of the TPS54494EVM, board layout, and layer illustrations.

5.1 Layout

The board layout for the TPS54494EVM is shown in Figure 20 through Figure 25. The top layer contains the main power traces for VIN and VOUTx. Also on the top layer are connections for the pins of the TPS54494 and a large area filled with ground. Many of the signal traces also are located on the top side. The input decoupling capacitors are located as close to the IC as possible. The input and output connectors, test points, and all of the assembled components are located on the top side. An analog ground (GND) area is provided on the top side. Analog ground (GND) and power ground (PGND) are connected at a single point on the top layer near the IC. The other layers are primarily power ground but the bottom layer has some traces to connect the test points for SSx and ENx.

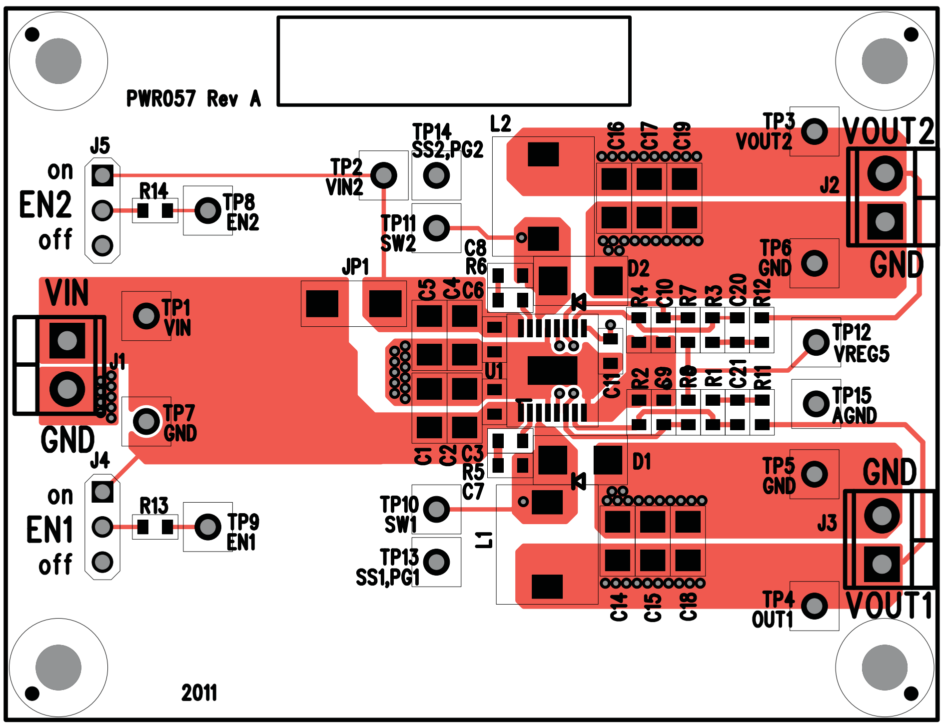


Figure 20. Top Assembly

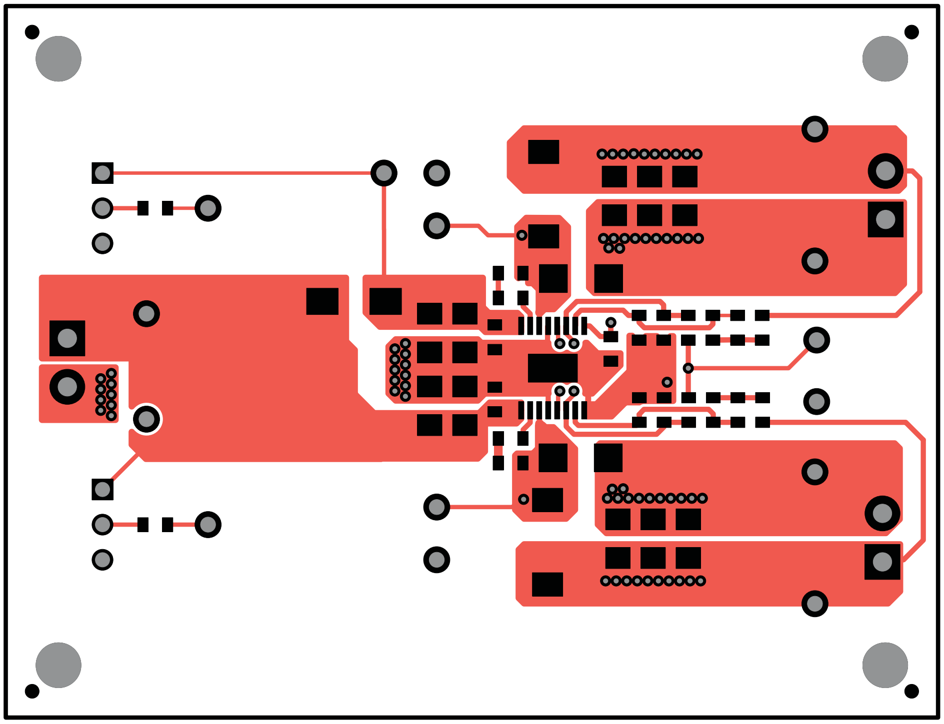


Figure 21. Top Layer

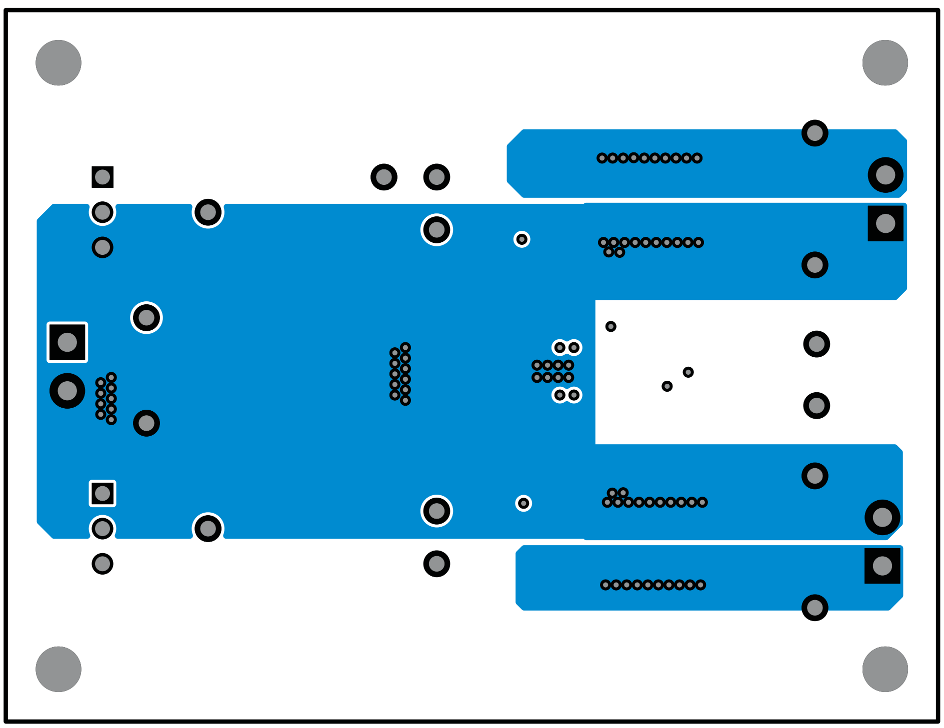


Figure 22. Internal 1 Layer

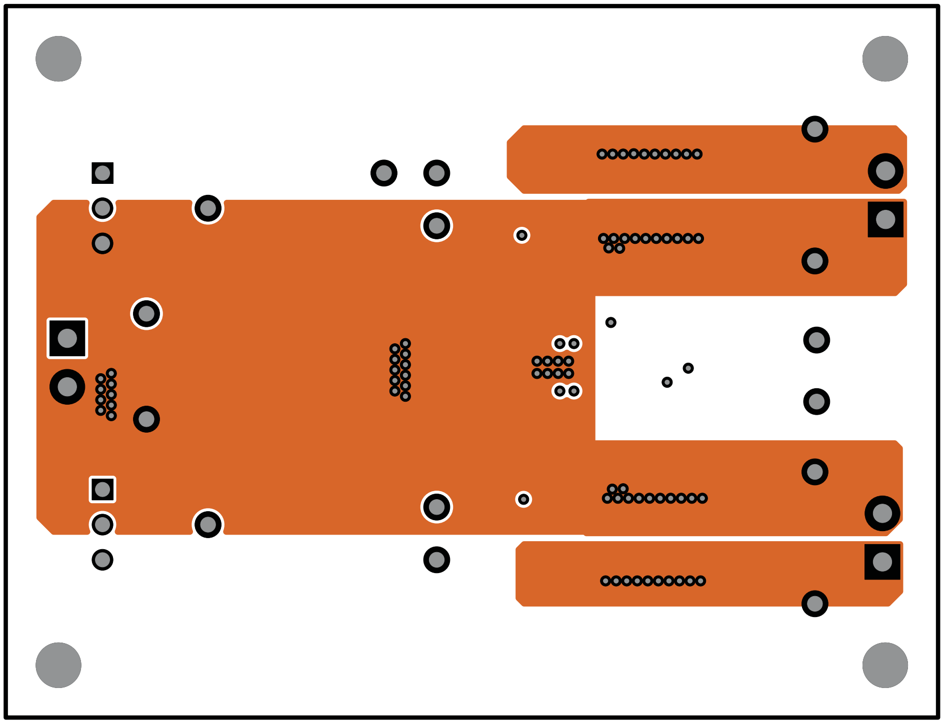


Figure 23. Internal 2 Layer

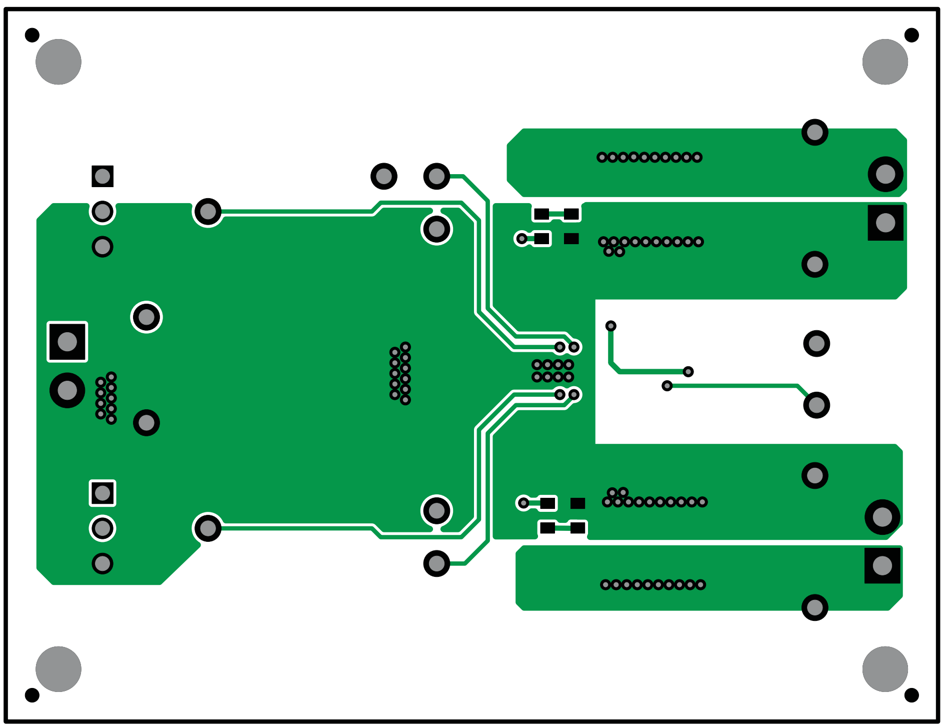


Figure 24. Bottom Layer

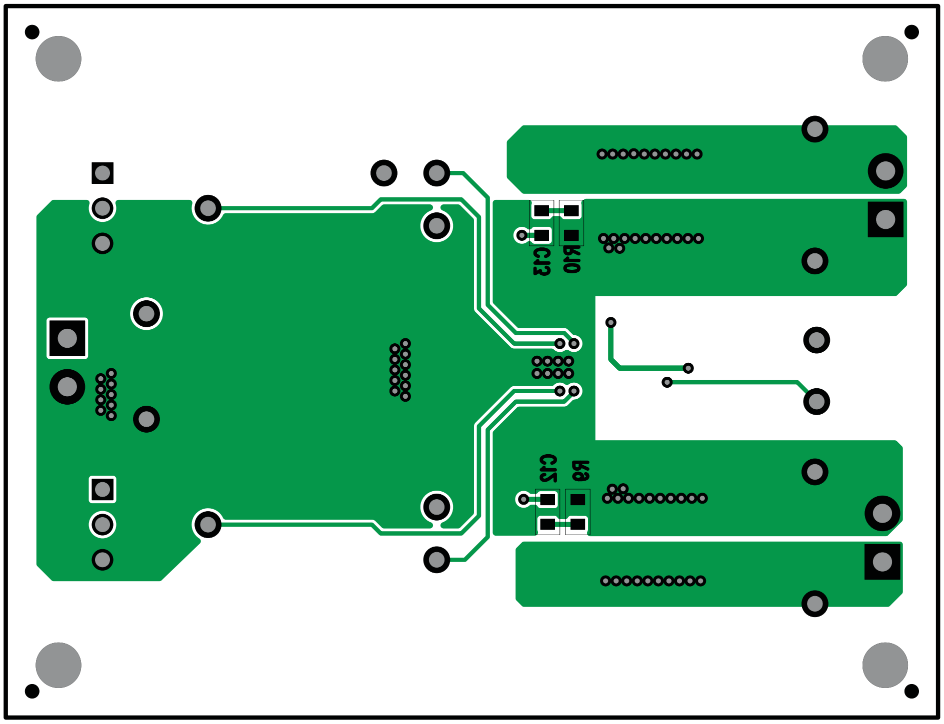


Figure 25. Bottom Assembly

6 Schematic, Bill of Materials, and Reference

6.1 Schematic

Figure 26 is the schematic for the TPS54494EVM.

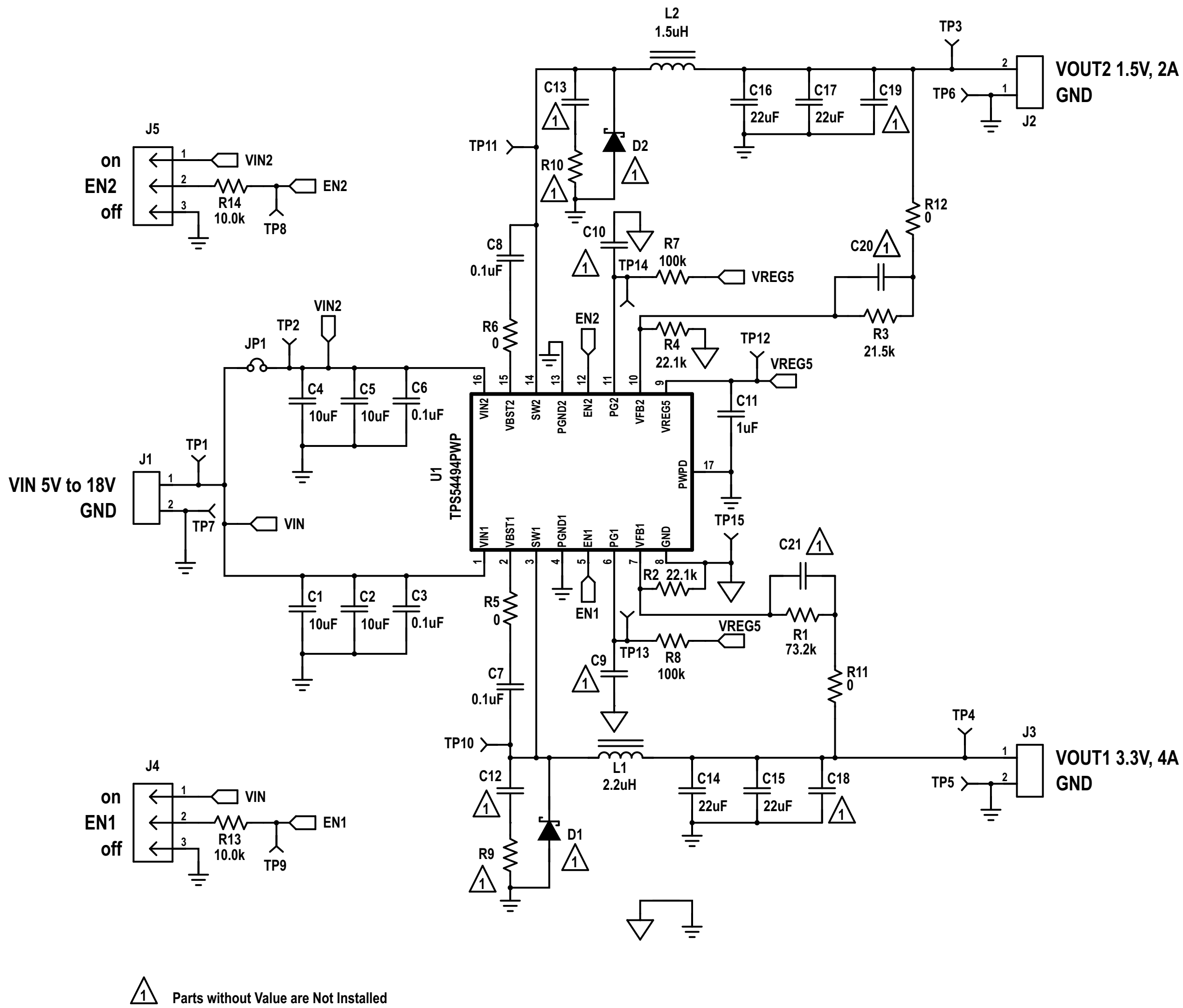


Figure 26. TPS54494EVM Schematic Diagram

6.2 Bill of Materials

Table 5. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	Manufacturer
1	C11	1 µF	Capacitor, ceramic, 16 V, X7R, 10%	0603	GRM188R71C105KA12	Murata
4	C1-2 C4-5	10 µF	Capacitor, ceramic, 25 V, X7R, 10%	1206	GRM31CR71E106KA12	Murata
0	C12-13	open	Capacitor, ceramic, 50 V, X7R, 10%	0603	GRM188R71H104KA93	Murata
4	C14-17	22 µF	Capacitor, ceramic, 6.3 V, X7R, 10%	1206	GRM31CR70J226KE19	Murata
0	C18-19	open	Capacitor, ceramic, 6.3 V, X7R, 10%	1206		
0	C20-21	open	Capacitor, ceramic, 50 V, X7R, 10%	0603	Std	Std
4	C3 C6-8	0.1 µF	Capacitor, ceramic, 50 V, X7R, 10%	00603	GRM188R71H104KA93	Murata
0	C9-10	open	Capacitor, ceramic, 50 V, X7R, 10%	0603	Std	Std
0	D1-2	open	Diode, Schottky	SMA	STD	STD
1	L1	2.2 µH	Inductor, power line, magnetic shielded, ±30%, 4.3A	6.9 × 7.2 mm	SPM6530-2R2M	TDK
1	L2	1.5 µH	Inductor, power line, magnetic shielded, ±30%, 4.1A	6.9 × 7.2 mm	SPM6530-1R5M	TDK
1	R1	73.2 kΩ	Resistor, chip, 1/16W, 1%	0603	STD	STD
2	R11-12	0 Ω	Resistor, chip, 1/16W, 5%	0603	STD	STD
2	R13-14	10.0 kΩ	Resistor, chip, 1/16W, 1%	0603	STD	STD
2	R2 R4	22.1 kΩ	Resistor, chip, 1/16W, 1%	0603	STD	STD
1	R3	21.5 kΩ	Resistor, chip, 1/16W, 1%	0603	STD	STD
2	R5-6	0 Ω	Resistor, chip, 1/16W, 1%	0603	STD	STD
2	R7-8	100 kΩ	Resistor, chip, 1/16W, 1%	0603	STD	STD
0	R9-10	open	Resistor, chip, 1/16W, 1%	0603	STD	STD
1	U1	TPS54494PWP	IC, 4A/2A, dual output fully synchronous buck converter with integrated FET	TSSOP	TPS54494PWP	TI

C14-C19 must be replaced with capacitors which have a higher voltage rating when the output voltage is set above 4V.

6.3 Reference

1. *TPS54494, 3-A Dual Channel Synchronous Step-Down Switcher With Integrated FETs* data sheet (SLVSBH1)

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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【ご使用にあたっての注】

本開発キットは技術基準適合証明を受けておりません。

本製品のご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。

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EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM’s electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI’s recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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