4 ppm/°C, 100 µA SOT23-6 SERIES VOLTAGE REFERENCES

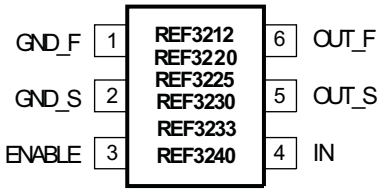
Check for Samples: REF3212-EP, REF3220-EP, REF3225-EP, REF3230-EP, REF3233-EP, REF3240-EP

FEATURES

- **Excellent Specified Drift Performance:**
  - **7ppm/°C (Max) at 0°C to 125°C**
  - **20ppm/°C (Max) at –40°C to 125°C**
  - **40ppm/°C (Max) at –55°C to 125°C**
- **Microsize Package: SOT23-6**
- **High Output Current: ±10 mA**
- **High Accuracy: 0.01%**
- **Low Quiescent Current: 100 µA**
- **Low Dropout: 5 mV**

APPLICATIONS

- **Portable Equipment**
- **Data Acquisition Systems**
- **Medical Equipment**
- **Test Equipment**

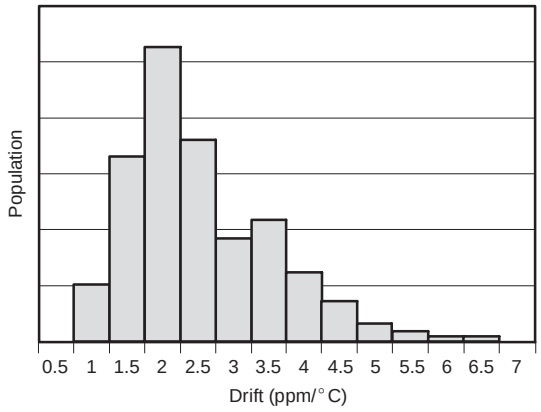


SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

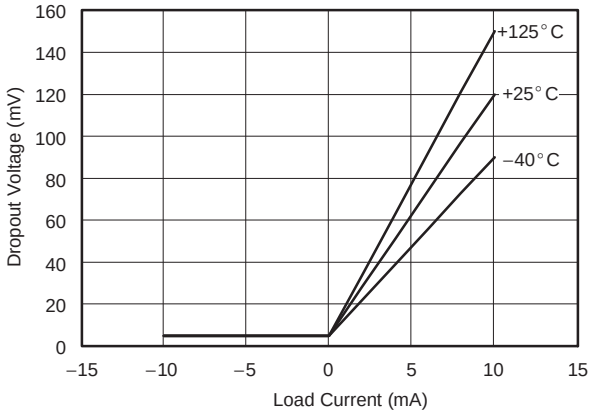
- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Additional temperature ranges are available - contact factory

TEMPERATURE DRIFT
(0°C to +125°C)



DROPOUT VOLTAGE
vs LOAD CURRENT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION

The REF32xx is a very low drift, micropower, low-dropout, precision voltage reference family available in the tiny SOT23-6 package.

The small size and low power consumption (120 µA max) of the REF32xx make it ideal for portable and battery-powered applications. This reference is stable with most capacitive loads.

The REF32xx can be operated from a supply as low as 5 mV above the output voltage, under no load conditions. All models are specified for the wide temperature range of –55°C to 125°C.

AVAILABLE OUTPUT VOLTAGES

PRODUCT	VOLTAGE
REF3212	1.25 V
REF3220	2.048 V
REF3225	2.5 V
REF3230	3 V
REF3233	3.3 V
REF3240	4.096 V

Table 1. PACKAGE/ORDERING INFORMATION(1)

PRODUCT	OUTPUT VOLTAGE	PACKAGE-LEAD	PACKAGE DESIGNATOR(2)	PACKAGE MARKING
REF3212AMDBVREP	1.25 V	SOT23-6	DBV	R3AM
REF3220AMDBVREP	2.048 V	SOT23-6	DBV	R3BM
REF3225AMDBVREP	2.5 V	SOT23-6	DBV	R3CM
REF3230AMDBVREP	3 V	SOT23-6	DBV	R3DM
REF3233AMDBVREP	3.3 V	SOT23-6	DBV	R3EM
REF3240AMDBVREP	4.096 V	SOT23-6	DBV	R3FM

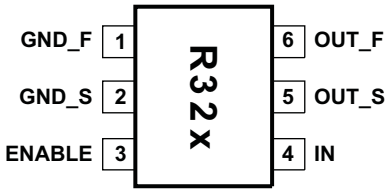
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Figure 1. PIN CONFIGURATION

SOT23-6
(TOP VIEW)



A. The location of pin 1 on the REF32xx is determined by orienting the package marking as shown.

PIN DESCRIPTIONS

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
ENABLE	3	Digital input	This pin enables and disables the device
GND_F	1	Analog output	Ground connection of the device
GND_S	2	Analog input	Ground sense at the load
IN	4	Analog input	Positive supply voltage
OUT_F	6	Analog output	Output of Reference Voltage
OUT_S	5	Analog input	Sense connection at the load

Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Input voltage			7.5	V
Output short-circuit		Continuous		
Operating temperature range		–55	125	°C
Storage temperature range		–65	150(2)	°C
Junction temperature			150	°C
ESD rating	Human-Body Model		4	kV
	Charged-Device Model		1	
	Machine Model		400	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

Electrical Characteristics

Boldface limits apply over the listed temperature range.
T_A = 25°C, I_{LOAD} = 0 mA, and V_{IN} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
REF3212 (1.25 V)							
V_{OUT}	Output voltage			1.2475	1.25	1.2525	V
	Initial accuracy			–0.2	0.01	0.2	%
Noise	Output voltage noise		f = 0.1 Hz to 10 Hz		17		μV_{PP}
	Voltage noise		f = 10 Hz to 10 kHz		24		μV_{RMS}
REF3220 (2.048 V)							
V_{OUT}		Output voltage		2.044	2.048	2.052	V
		Initial accuracy		–0.2	0.01	0.2	%
Noise		Output voltage noise	f = 0.1 Hz to 10 Hz		27		μV_{PP}
		Voltage noise	f = 10 Hz to 10 kHz		39		μV_{RMS}
REF3225 (2.5 V)							
V_{OUT}	Output voltage			2.495	2.5	2.505	V
	Initial accuracy			–0.2	0.01	0.2	%
Noise	Output voltage noise		f = 0.1 Hz to 10 Hz		33		μV_{PP}
	Voltage noise		f = 10 Hz to 10 kHz		48		μV_{RMS}
REF3230 (3 V)							
V_{OUT}	Output voltage			2.994	3	3.006	V
	Initial accuracy			–0.2	0.01	0.2	%
Noise	Output voltage noise		f = 0.1 Hz to 10 Hz		39		μV_{PP}
	Voltage noise		f = 10 Hz to 10 kHz		57		μV_{RMS}
REF3233 (3.3 V)							
V_{OUT}	Output voltage			3.293	3.3	3.307	V
	Initial accuracy			–0.2	0.01	0.2	%
Noise	Output voltage noise		f = 0.1 Hz to 10 Hz		43		μV_{PP}
	Voltage noise		f = 10 Hz to 10 kHz		63		μV_{RMS}
REF3240 (4.096 V)							
V_{OUT}	Output voltage			4.088	4.096	4.104	V
	Initial accuracy			–0.2	0.01	0.2	%
Noise	Output voltage noise		f = 0.1 Hz to 10 Hz		53		μV_{PP}
	Voltage noise		f = 10 Hz to 10 kHz		78		μV_{RMS}
REF3212/REF3220/REF3225/REF3230/REF3233/REF3240							
dV_{OUT}/dT	Output voltage temperature drift		T_A = 25°C		4	7	ppm/°C
			–55°C ≤ T_A ≤ 125°C		10.5	40	
	Long-term stability		0 tp 1000 h		55		ppm
	Line regulation		V_{OUT} + 0.05 (1) ≤ V_{IN} ≤ 5.5 V	–65	15	65	ppm/V
dV_{OUT}/dI_{LOAD}	Load regulation (2)	Sourcing	0 mA < I_{LOAD} < 10 mA, V_{IN} = V_{OUT} + 250 mV (1)	–40	3	40	µV/mA
		Sinking	–10 mA < I_{LOAD} < 0 mA, V_{IN} = V_{OUT} + 100 mV (1)	–60	20	60	
dT	Thermal hysteresis (3)	First cycle			100		ppm
		Additional cycles			25		
$V_{IN} – V_{OUT}$	Dropout voltage (1)		25°C ≤ T_A ≤ +125°C		5	50	mV

(1) The minimum supply voltage for the REF3212 is 1.8 V.
(2) Load regulation is using force and sense lines; see the *Load Regulation* section for more information.
(3) Thermal hysteresis procedure is explained in more detail in the *Applications Information* section.

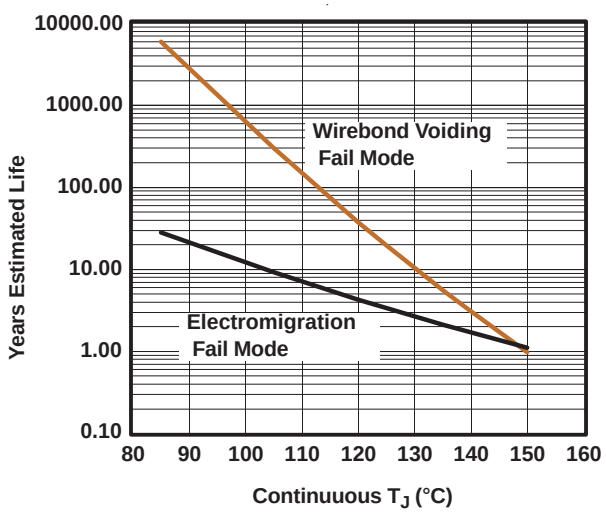
Electrical Characteristics (continued)

Boldface limits apply over the listed temperature range.
T_A = 25°C, I_{LOAD} = 0 mA, and V_{IN} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LOAD}	Output current		$V_{IN} = V_{OUT}$ + 250 mV(1)	–10		10	mA
I_{SC}	Short-circuit current	Sourcing			50		mA
		Sinking			40		
	Turn-on settling time		0.1% at V_{IN} = 5 V with C_L = 0		60		µs
V_L	Enable/shutdown(4)		Reference in shutdown mode	0		0.7	V
V_H			Reference is active	1.5		V_{IN}	
V_{IN}	Power supply Voltage		I_L = 0	V_{OUT} + 0.05(1)		5.5	V
I_Q	Power supply Current		I_L = 0, ENABLE > 1.5 V		100	120	µA
I_S	Overtemperature shutdown		–55°C ≤ T_A ≤ 125°C		**115**	**135**	µA
			ENABLE < 0.7 V		0.1	1	µA
	Temperature range	Specified		–55		125	°C
		Operating		–55		125	
		Storage		–65		150	
θ_{JA}	Thermal resistance, SOT23-6				200		°C/W

(4) If the rise time of the input voltage is less than or equal to 2ms, the ENABLE and IN pins can be tied together. For rise times greater than 2ms, see the *Supply Voltage* section.

Figure 2. Operating Life Derating Chart



A. See Datasheet for Absolute Maximum and Minimum Recommended Operating Conditions.

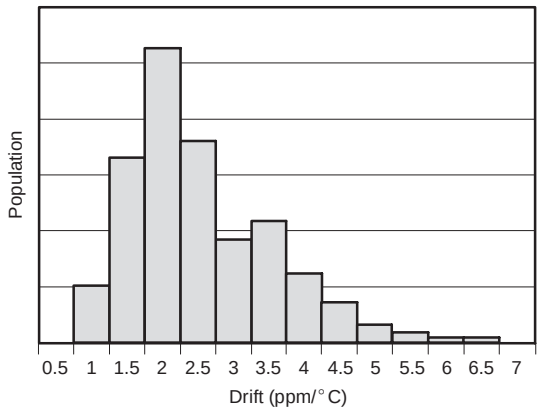
B. Silicon Operating Life Design Goal is 10 years at 105°C Junction Temperature (does not include package interconnect life).

C. Enhanced Plastic Product Disclaimer Applies.

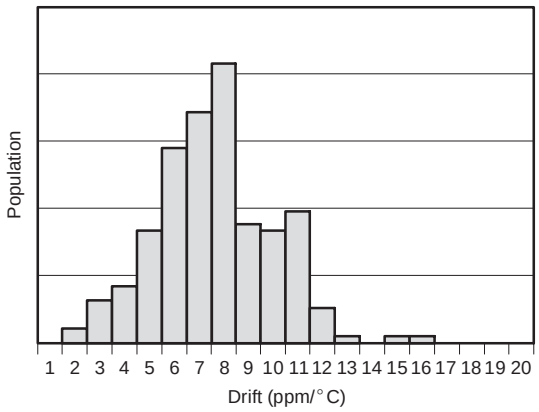
TYPICAL CHARACTERISTICS

T_A = 25°C, I_{LOAD} = 0 mA, V_{IN} = 5 V power supply, REF3225 is used for typical characteristics (unless otherwise noted)

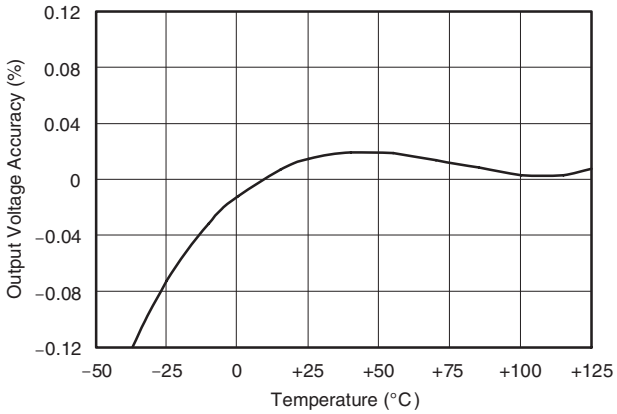
TEMPERATURE DRIFT
(0°C to +125°C)



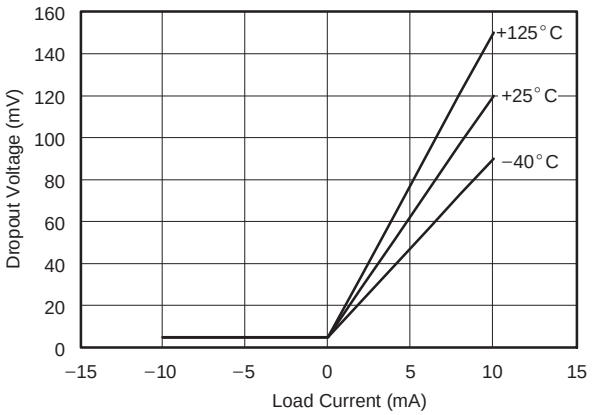
TEMPERATURE DRIFT
(−40°C to +125°C)



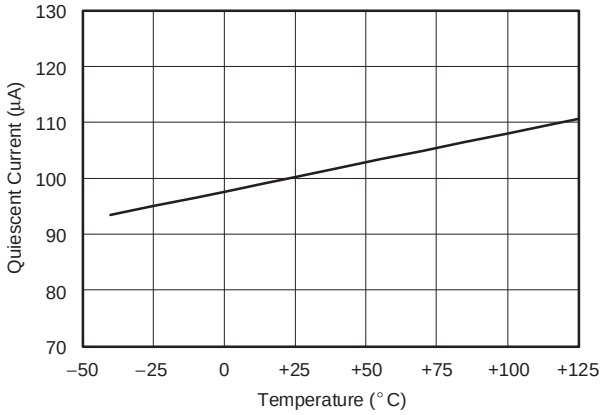
OUTPUT VOLTAGE ACCURACY
vs TEMPERATURE



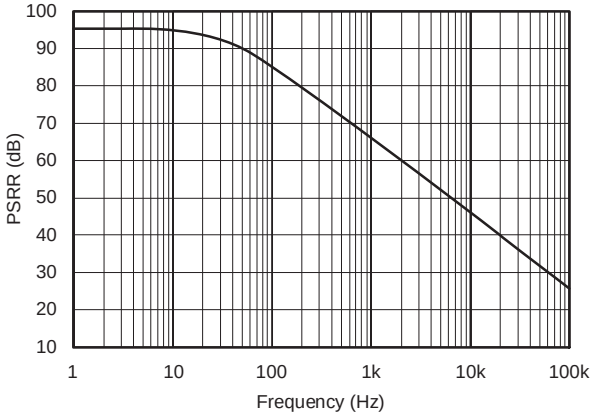
DROPOUT VOLTAGE
vs LOAD CURRENT



QUIESCENT CURRENT
vs TEMPERATURE



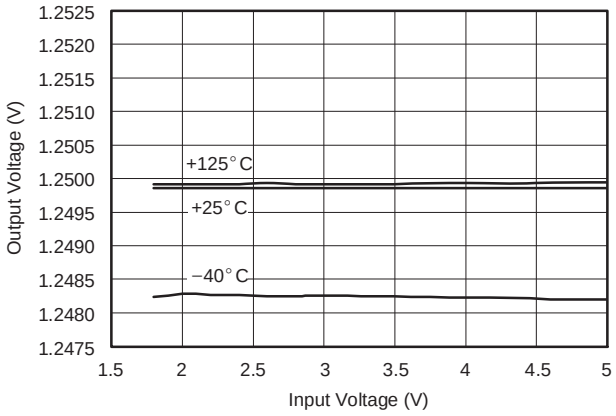
POWER−SUPPLY REJECTION RATIO
vs FREQUENCY



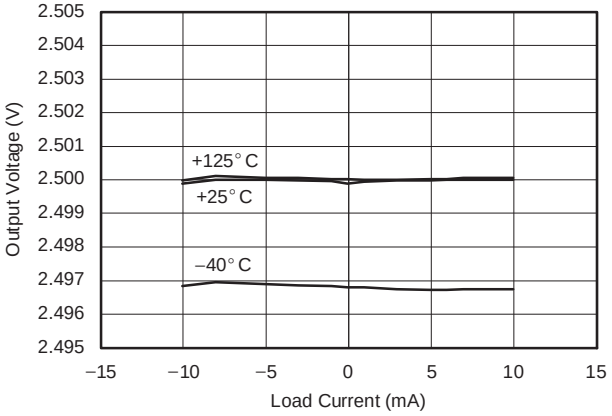
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, I_{LOAD} = 0 mA, V_{IN} = 5 V power supply, REF3225 is used for typical characteristics (unless otherwise noted)

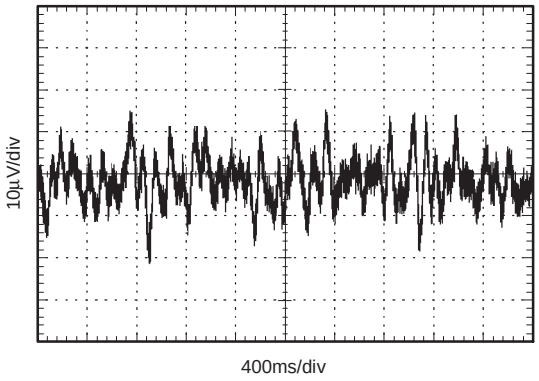
OUTPUT VOLTAGE vs INPUT VOLTAGE
(REF3212)



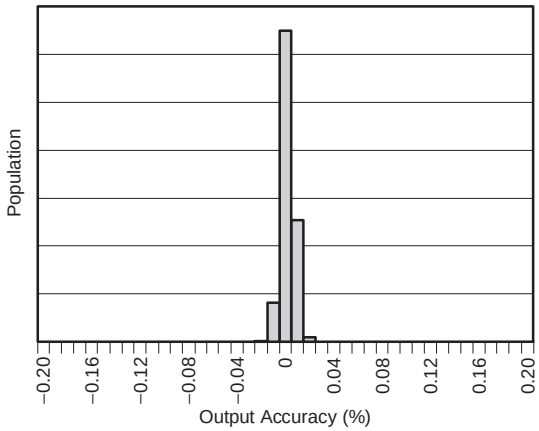
OUTPUT VOLTAGE
vs LOAD CURRENT



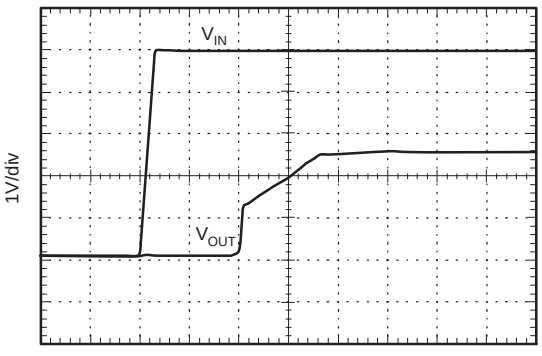
0.1Hz TO 10Hz
NOISE



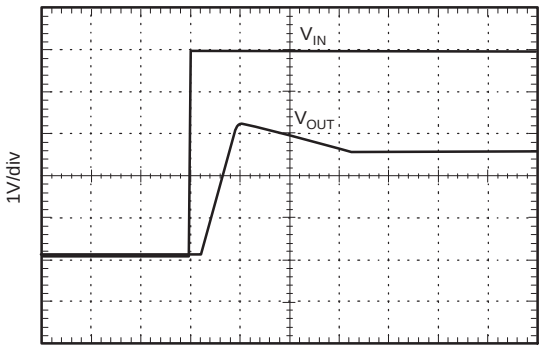
OUTPUT VOLTAGE
INITIAL ACCURACY



STEP RESPONSE
C_L = 0pF, 5V STARTUP



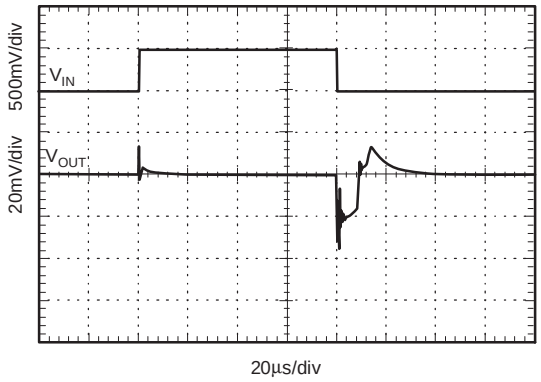
STEP RESPONSE
C_L = 1µF



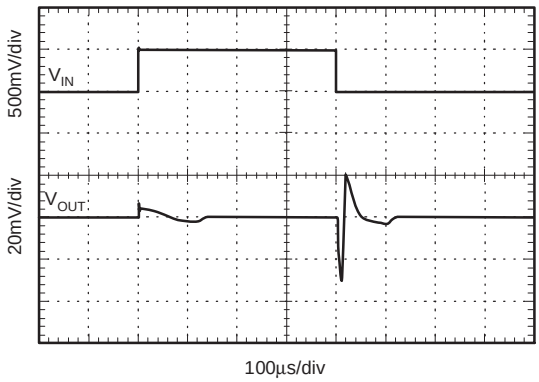
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, I_{LOAD} = 0 mA, V_{IN} = 5 V power supply, REF3225 is used for typical characteristics (unless otherwise noted)

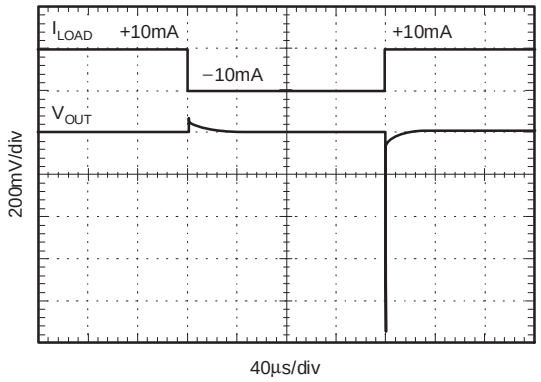
LINE TRANSIENT
C_L = 0pF



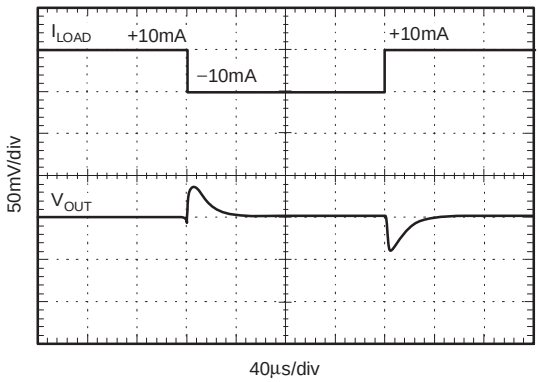
LINE TRANSIENT
C_L = 10µF



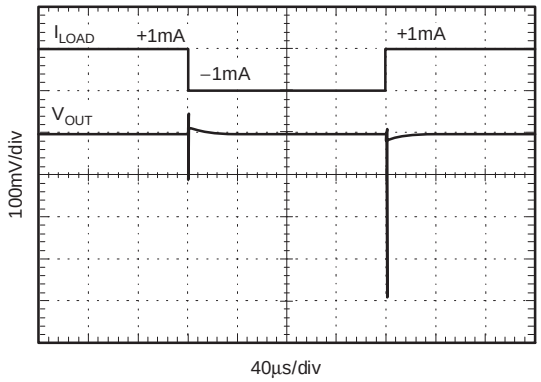
LOAD TRANSIENT
C_L = 0pF, ±10mA OUTPUT PULSE



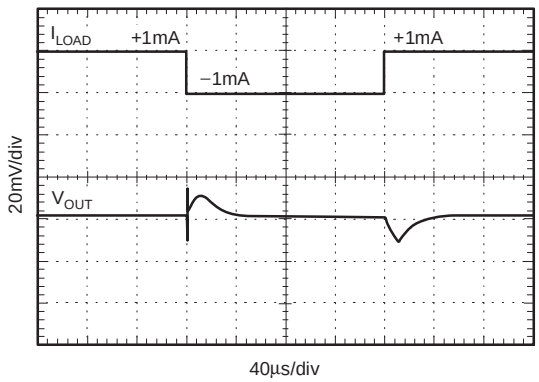
LOAD TRANSIENT
C_L = 1µF, ±10mA OUTPUT PULSE



LOAD TRANSIENT
C_L = 0pF, ±1mA OUTPUT PULSE

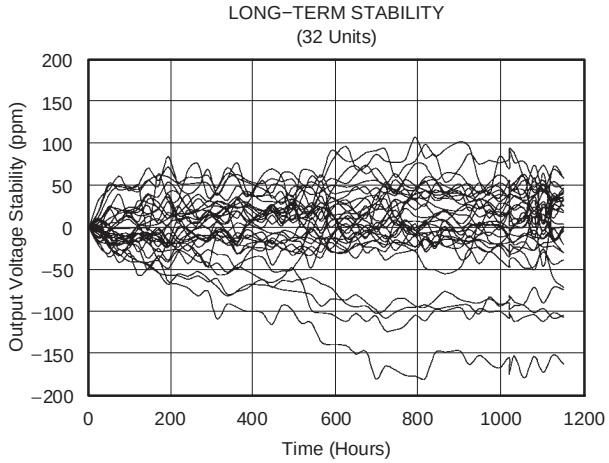


LOAD TRANSIENT
C_L = 1µF, ±1mA OUTPUT PULSE



TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, I_{LOAD} = 0 mA, V_{IN} = 5 V power supply, REF3225 is used for typical characteristics (unless otherwise noted)



THEORY OF OPERATION

The REF32xx is a family of CMOS, precision bandgap voltage references. Figure 3 shows the basic bandgap topology. Transistors Q_1 and Q_2 are biased so that the current density of Q_1 is greater than that of Q_2. The difference of the two base-emitter voltages ($Vbe_1 - Vbe_2$) has a positive temperature coefficient and is forced across resistor R_1. This voltage is amplified and added to the base-emitter voltage of Q_2, which has a negative temperature coefficient. The resulting output voltage is virtually independent of temperature.

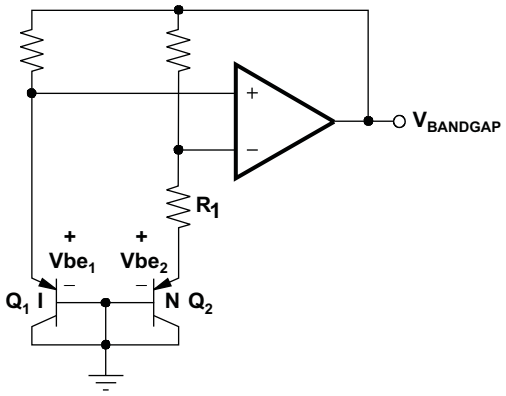


Figure 3. Simplified Schematic of Bandgap Reference

APPLICATION INFORMATION

The REF32xx does not require a load capacitor and is stable with most capacitive loads, see Load Capacitance Guidelines. Figure 4 shows typical connections required for operation of the REF32xx. A supply bypass capacitor of 0.47 µF is recommended.

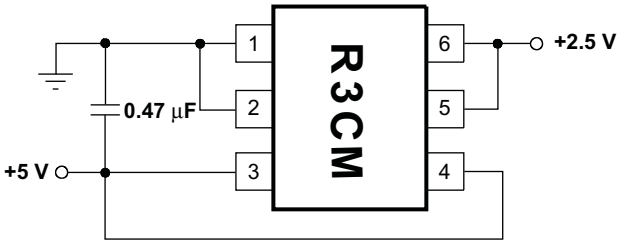


Figure 4. Typical Operating Connections for the REF3225

Supply Voltage

The REF32xx family of references features an extremely low dropout voltage. With the exception of the REF3212, which has a minimum supply requirement of 1.8 V, these references can be operated with a supply of only 5 mV above the output voltage in an unloaded condition. For loaded conditions, a typical dropout voltage versus load is shown in the Typical Characteristic curves.

The REF32xx also features a low quiescent current of 100 µA, with a maximum quiescent current over temperature of just 135 µA. The quiescent current typically changes less than 2 µA over the entire supply range, as shown in Figure 5.

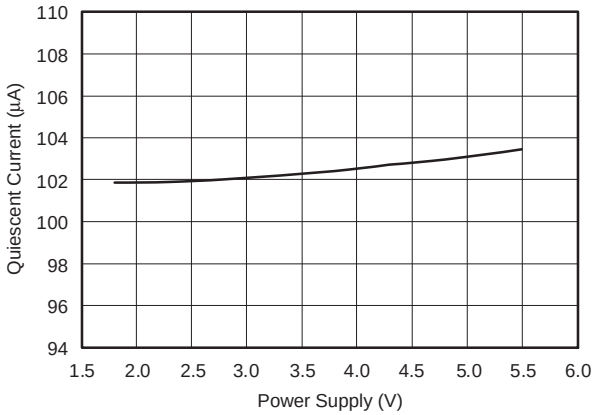


Figure 5. Supply Current vs Supply Voltage

Supply voltages below the specified levels can cause the REF32xx to momentarily draw currents greater than the typical quiescent current. This momentary current draw can be prevented by using a power supply with a fast rising edge and low output impedance.

For optimal startup when the IN pin and ENABLE pin are tied together, keep the input voltage rise time less than or equal to 2ms. For rise times greater than 2ms, the ENABLE pin must be kept below 0.7V until the voltage at the IN pin has reached the minimum operating voltage. One way to control the voltage at the ENABLE pin is with an additional RC filter, such as that shown in Figure 6. The RC filter must hold the voltage at the ENABLE pin below the threshold voltage until the voltage at the input pin has reached the minimum operating voltage.

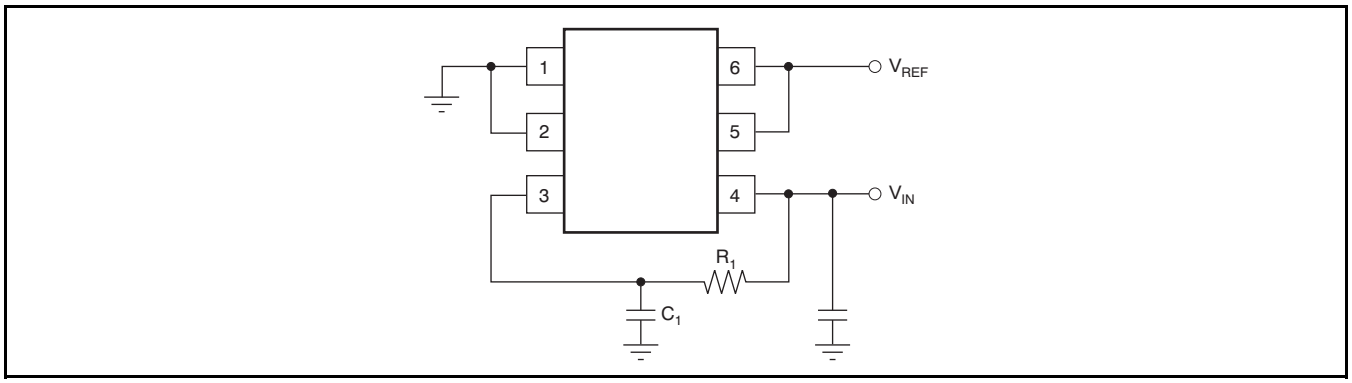


Figure 6. Application Circuit to Control the REF32xx ENABLE Pin

The RC filter in Figure 6 can be used as a starting point for the REF3240. The values for R_1 and C_1 have been calculated so that the voltage at the ENABLE pin reaches 0.7V after the input voltage has reached 4.15V; Table 2 lists these values. For output voltage options other than 4.096V, the RC filter can be made faster.

Table 2. Recommended R_1 and C_1 Values for the REF3240

RISE TIME	R_1 VALUE	C_1 VALUE
2ms	150kΩ	100nF
5ms	150kΩ	220nF
10ms	330kΩ	220nF
20ms	390kΩ	330nF
50ms	680kΩ	470nF
100ms	680kΩ	1000nF

In this document, rise time is defined as the time until an exponential input signal reaches 90% of its final voltage. For example, the 2ms value shown in Table 2 is valid for an end value of 5V.

If the input voltage has a different shape or the end value is not 5V, then the time until the minimum dropout voltage has been reached should be used to decide if the IN and ENABLE pins can be tied together. Table 3 lists these times.

Table 3. Minimum Dropout Voltage Times

DEVICE	TIME
REF3212	0.4ms
REF3220	0.5ms
REF3225	0.7ms
REF3230	0.9ms
REF3233	1.0ms
REF3240	1.6ms

Note that because the leakage current of the EN pin is in the range of a few nA, it can be disregarded in most applications.

Shutdown

The REF32xx can be placed in a low-power mode by pulling the ENABLE/SHUTDOWN pin low. When in shutdown mode the output of the REF32xx becomes a resistive load to ground. The value of the load depends on the model, and ranges from approximately 100 kΩ to 400 kΩ.

The ENABLE pin must always be driven to a valid voltage level (V_L or V_H) as shown in the Electrical Characteristics section of this datasheet. To maintain the low quiescent current (100 µA typ), the ENABLE pin was designed without an internal pull-up resistor. In applications where the shutdown feature will not be used, connecting the ENABLE pin high (to the IN pin) will ensure enabled operation of the device.

Thermal Hysteresis

Thermal hysteresis for the REF32xx is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. It can be expressed as:

$$V_{HYST} = \left(\frac{|V_{PRE} - V_{POST}|}{V_{NOM}} \right) \times 10^6 (ppm) \quad (1)$$

Where:

V_{HYST} = Thermal hysteresis (in units of ppm)

V_{NOM} = The specified output voltage

V_{PRE} = Output voltage measured at 25°C pretemperature cycling

V_{POST} = Output voltage measured after the device has been cycled through the specified temperature range of –40°C to 125°C and returned to 25°C

Temperature Drift

The REF32xx is designed to exhibit minimal drift error, which is defined as the change in output voltage over varying temperature. The drift is calculated using the box method, as described by the following equation:

$$\text{Drift} = \left(\frac{V_{OUTMAX} - V_{OUTMIN}}{V_{OUT} \times \text{Temp Range}} \right) \times 10^6 (ppm) \quad (2)$$

The REF32xx features a typical drift coefficient of 4 ppm/°C from 0°C to 125°C — the primary temperature range for many applications. For the extended temperature range of –55°C to 125°C, the REF32xx family drift increases to a typical value of 10.5 ppm/°C.

Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise can be seen in the Typical Characteristic curve, *0.1-Hz to 10-Hz Voltage Noise*. The noise voltage of the REF32xx increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade ac performance.

Long-Term Stability

Long-term stability refers to the change of the output voltage of a reference over a period of months or years. This effect lessens as time progresses, as is shown by the long-term stability Typical Characteristic curves. The typical drift value for the REF32xx is 55 ppm from 0 to 1000 hours. This parameter is characterized by measuring 30 units at regular intervals for a period of 1000 hours.

Load Regulation

Load regulation is defined as the change in output voltage as a result of changes in load current. The load regulation of the REF32xx is measured using force and sense contacts, as shown in Figure 7. The force and sense lines can be used to effectively eliminate the impact of contact and trace resistance, resulting in accurate voltage at the load. By connecting the force and sense lines at the load, the REF32xx compensates for the contact and trace resistances because it measures and adjusts the voltage actually delivered at the load.

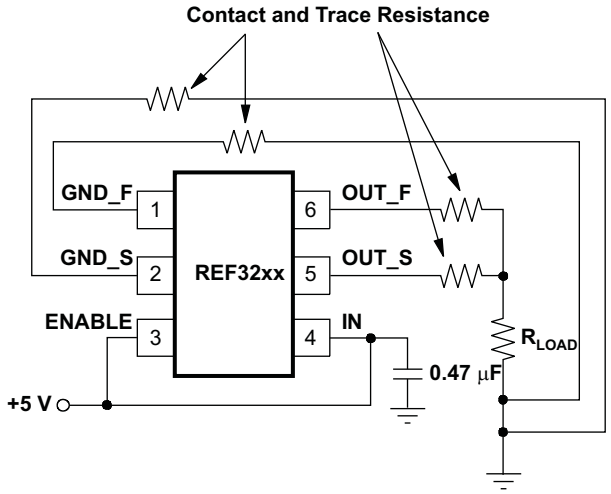


Figure 7. Accurate Load Regulation of REF32xx

The GND_S pin is connected to the internal ground of the device through ESD protection diodes. Because of that connection, the maximum differential voltage between the GND_S and GND_F pins must be kept below 200mV to prevent these dioes from unintentionally turning on.

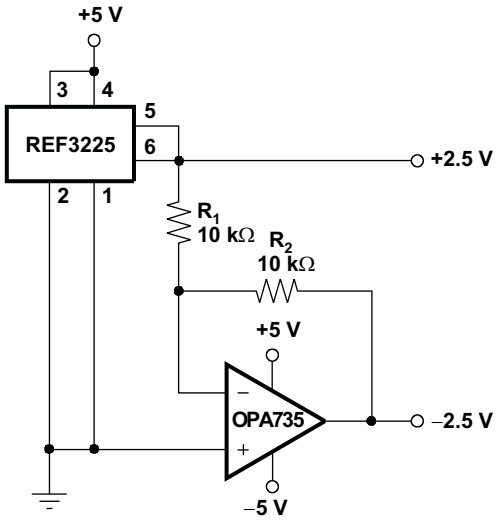
Load Capacitance Guidelines

The REF32xx series is designed to be stable with most capacitive loads. Common load capacitance values range between 1 µF and 47 µF. To minimize noise and provide specified performance, all models will benefit from an ESR value above 1 Ω with capacitive loads higher than 10 µF. However, the REF3212 must have an ESR value above 1Ω with capacitive loads higher than 10 µF to avoid oscillation.

APPLICATION CIRCUITS

Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the REF32xx and OPA735 can be used to provide a dual-supply reference from a 5-V supply. Figure 8 shows the REF3225 used to provide a 2.5-V supply reference voltage. The low drift performance of the REF32xx complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Care must be taken to match the temperature coefficients of R_1 and R_2.



Note: Bypass capacitor is not shown.

Figure 8. REF3225 Combined With OPA735 to Create Positive and Negative Reference Voltages

Data Acquisition

Data acquisition systems often require stable voltage references to maintain accuracy. The REF32xx family features stability and a wide range of voltages suitable for most microcontrollers and data converters. Figure 9, Figure 10, and Figure 11 show basic data acquisition systems.

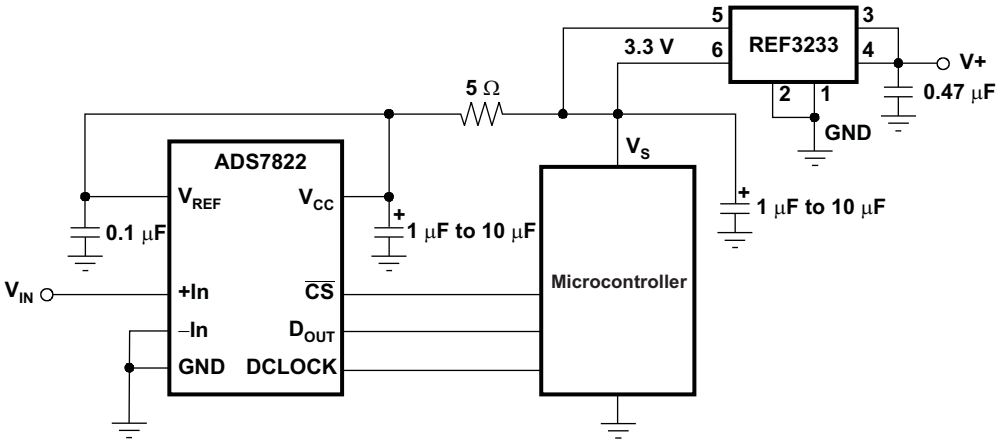


Figure 9. Basic Data Acquisition System 1

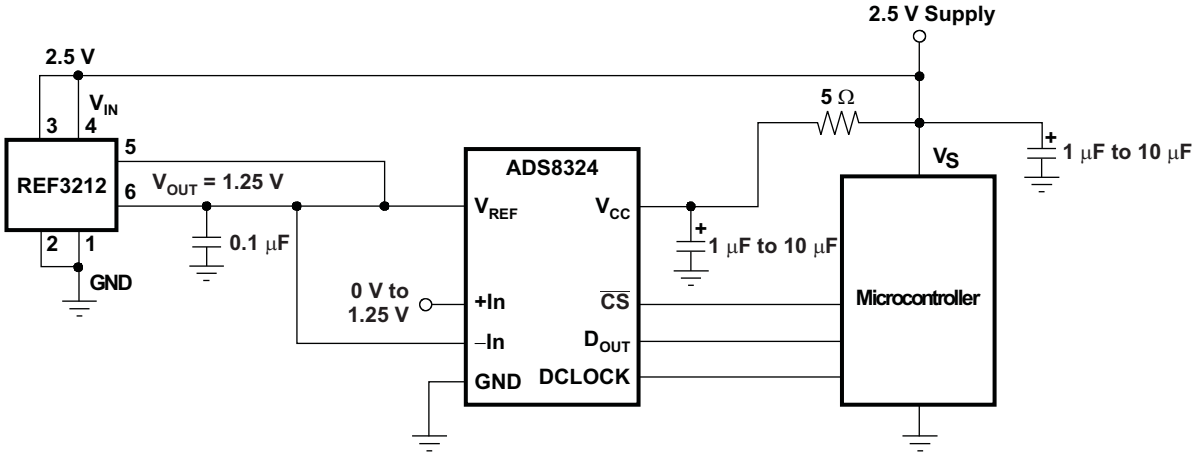


Figure 10. Basic Data Acquisition System 2

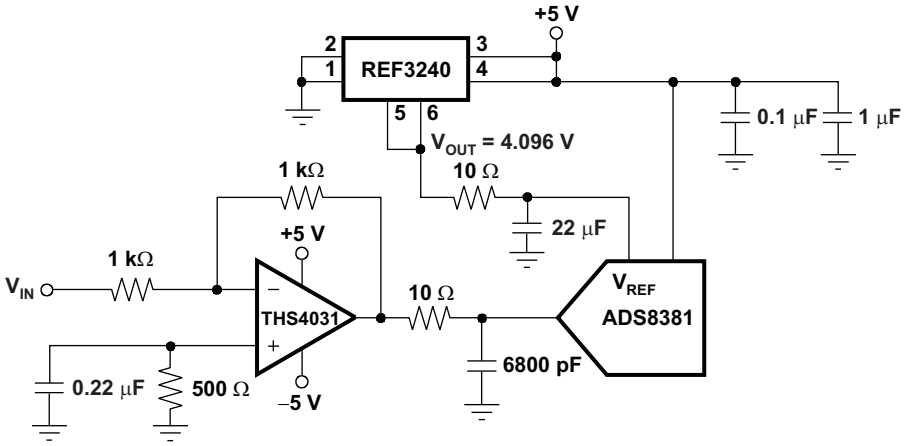


Figure 11. REF3240 Provides an Accurate Reference for Driving the ADS8381

Changes from Revision A (April 2007) to Revision B **Page**

- Added Pin Descriptions table 3
- Added note to Enable/Shutdown parameter 5
- Changed the minimum voltage for Enable/Shutdown with reference active from 0.75 x V_{IN} to 1.5 5
- Changed current test condition from 0.75 x V_{IN} to 1.5 V 5
- Added text, two tables and one figure to Supply Voltage section 11
- Changed pin 3 in Figure 7 from SHDN to ENABLE (typo) 14
- Added paragraph to Load Regulation section 14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF3212AMDBVREP	NRND	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	R3AM	
REF3220AMDBVREP	NRND	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	R3BM	
REF3225AMDBVREP	NRND	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	R3CM	
REF3230AMDBVREP	NRND	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	R3DM	
REF3240AMDBVREP	NRND	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	R3FM	
V62/07602-01XE	NRND	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	R3AM	
V62/07602-02XE	NRND	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	R3CM	
V62/07602-03XE	NRND	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	R3DM	
V62/07602-04XE	NRND	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	R3FM	
V62/07602-05XE	NRND	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	R3BM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF REF3212-EP, REF3220-EP, REF3225-EP, REF3230-EP, REF3240-EP :

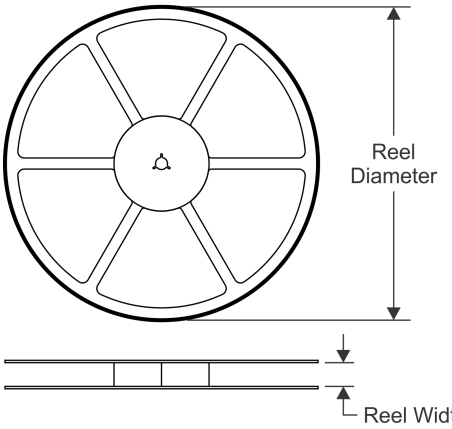
- Catalog: REF3212, REF3220, REF3225, REF3230, REF3240

NOTE: Qualified Version Definitions:

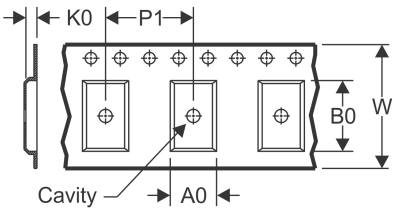
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

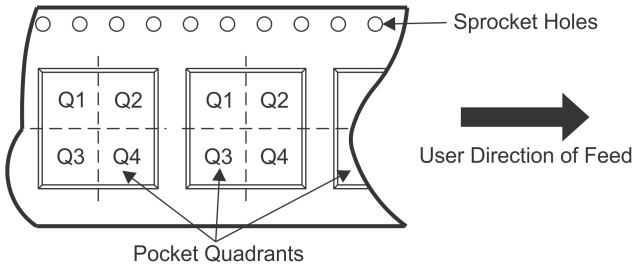


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

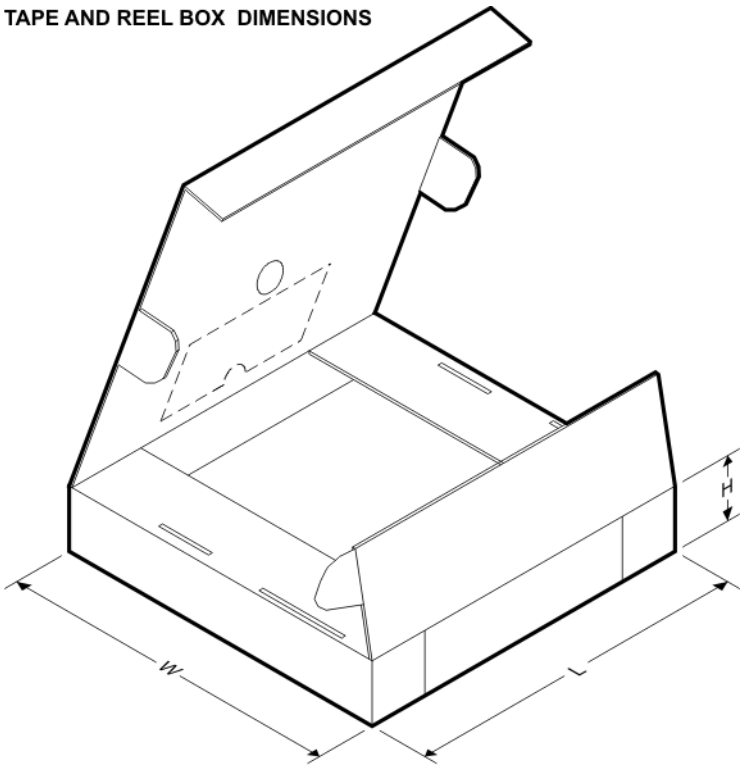
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF3212AMDBVREP	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REF3220AMDBVREP	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REF3225AMDBVREP	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REF3230AMDBVREP	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

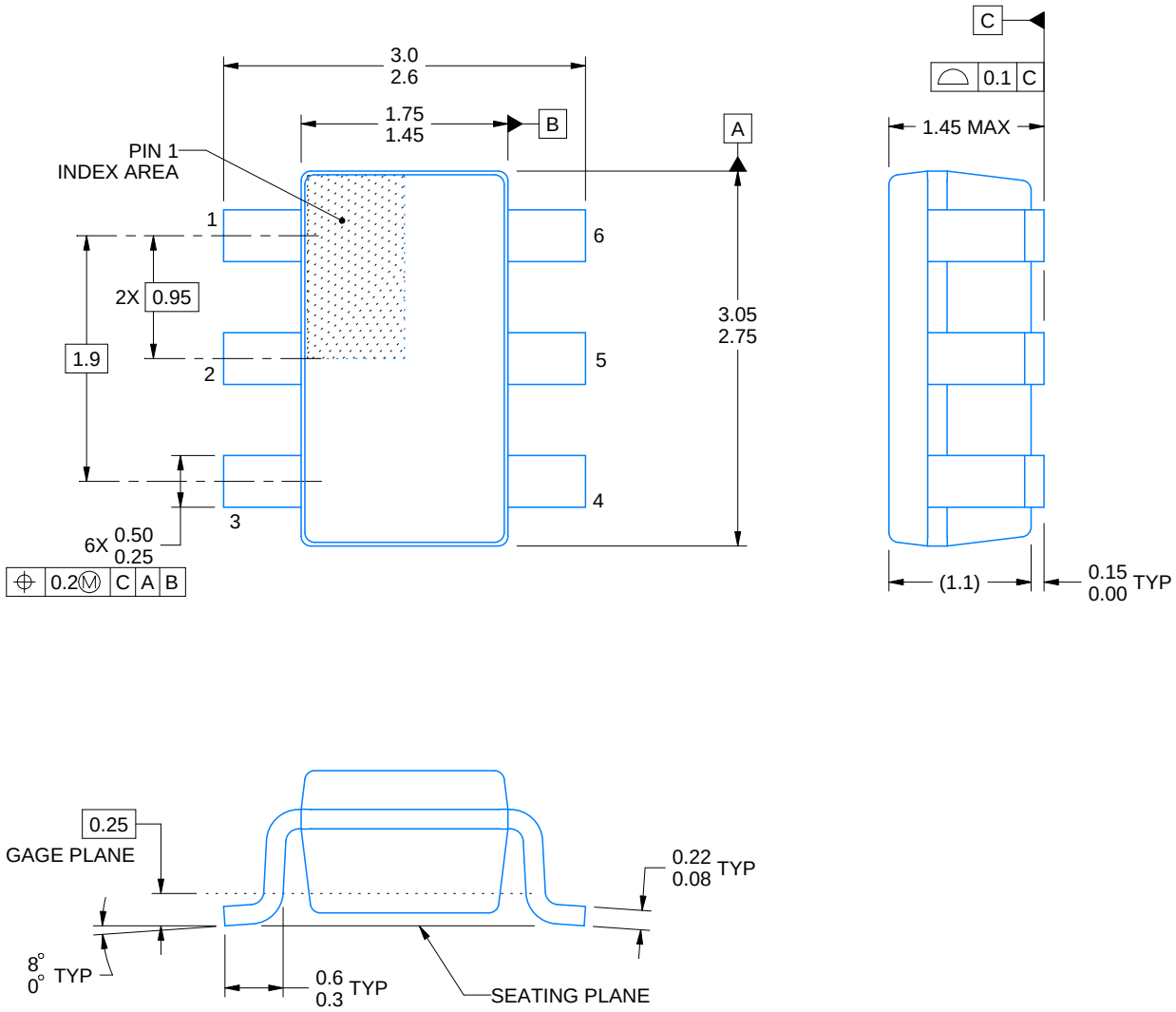
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF3212AMDBVREP	SOT-23	DBV	6	3000	445.0	220.0	345.0
REF3220AMDBVREP	SOT-23	DBV	6	3000	445.0	220.0	345.0
REF3225AMDBVREP	SOT-23	DBV	6	3000	445.0	220.0	345.0
REF3230AMDBVREP	SOT-23	DBV	6	3000	445.0	220.0	345.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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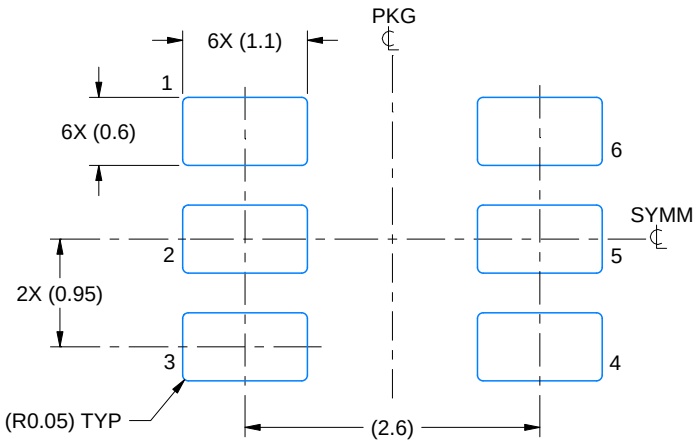
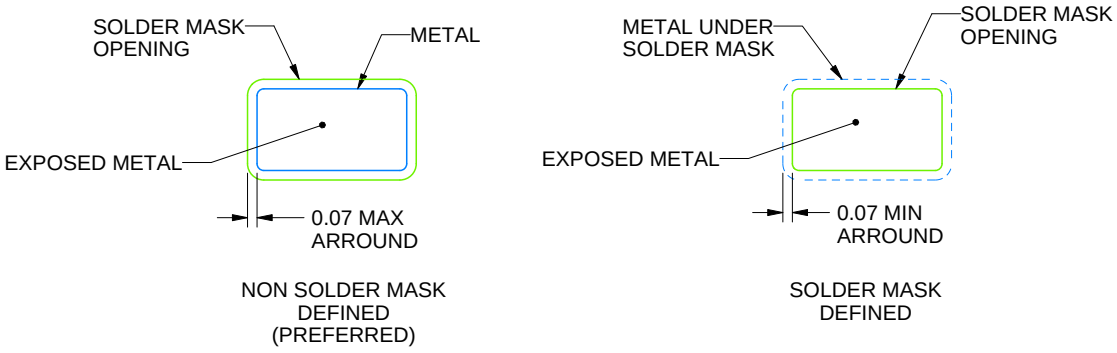
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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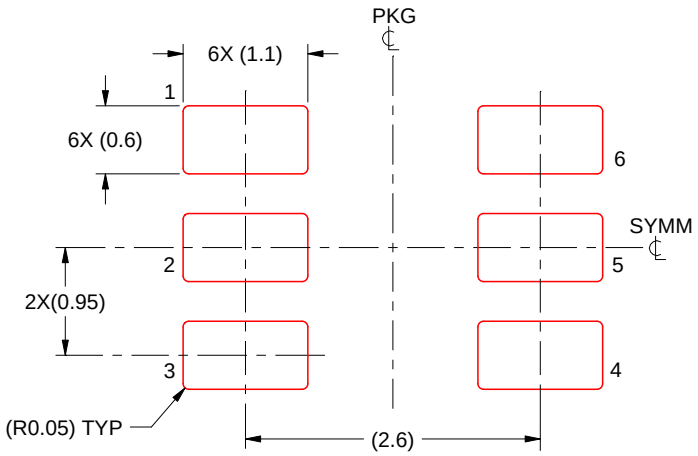
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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