Smart Battery Charger

FEATURES

- **Single Chip Smart Battery Charger Controller**
- **100% Compliant (Rev 1.0) SMBus Support Allows for Operation with or without Host**
- **SMBus Accelerator Improves SMBus Timing**
- Hardware Interrupt and SMBAlert Response Eliminate Interrupt Polling
- High Efficiency Synchronous Buck Charger
- 0.5V Dropout Voltage; Maximum Duty Cycle > 99.5%
- **AC Adapter Current Limit Maximizes Charge Rate***
- **1% Voltage Accuracy; 5% Current Accuracy**
- Up to 8A Charging Current Capability
- Dual 10-Bit DACs for Charger Voltage and Current Programming
- User-Selectable Overvoltage and Overcurrent Limits
- High Noise Immunity Thermistor Sensor
- Small 36-Lead Narrow (0.209") SSOP Package

APPLICATIONS

- Portable Computers
- Portable Instruments
- Docking Stations

*US Patent Number 5,723,970

DESCRIPTION

The LTC®1759 Smart Battery Charger is a single chip charging solution that dramatically simplifies construction of an SBS compliant system. The LTC1759 implements a Level 2 charger function whereby the charger can be programmed by the battery or by the host. A thermistor on the battery being charged is monitored for temperature, connectivity and battery type information. The SMBus interface remains alive when the AC power adapter is removed and responds to all SMBus activity directed to it, including thermistor status (via the ChargerStatus command). The charger also provides an interrupt to the host whenever a status change is detected (e.g., battery removal, AC adapter connection).

Charging current and voltage are restricted to chemistry specific limits for improved system safety and reliability. Limits are programmable by two external resistors. Additionally, the maximum average current from the AC adapter is programmable to avoid overloading the adapter when simultaneously supplying load current and charging current. When supplying system load current, charging current is automatically reduced to prevent adapter overload.

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TYPICAL APPLICATION

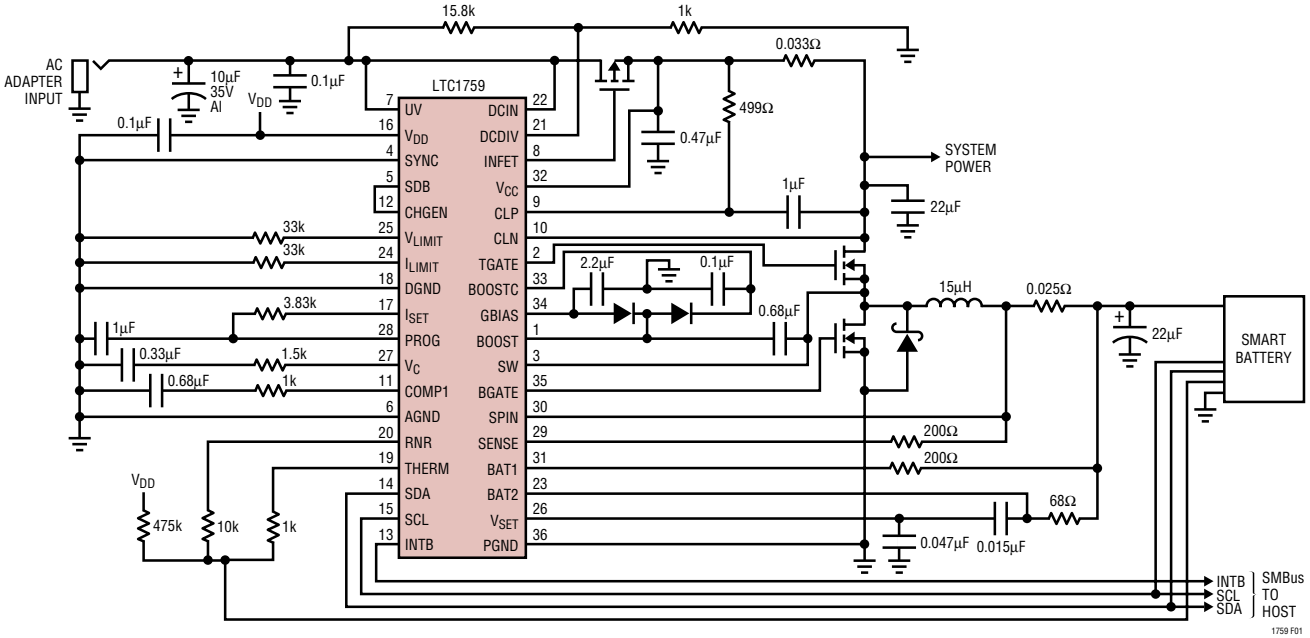


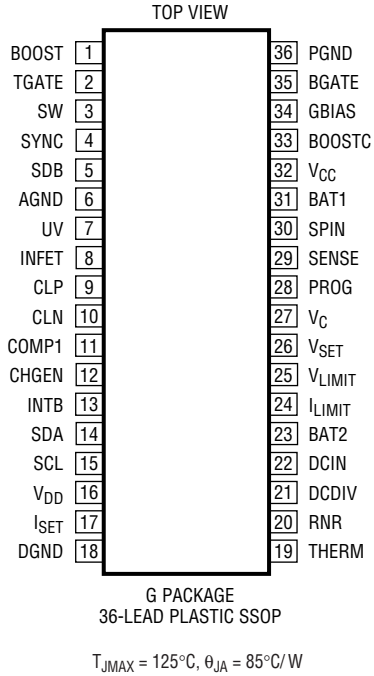
Figure 1. 4A SMBus Smart Battery Charger

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Voltage at V_{CC}, UV, BAT1, CLP,CLN, SPIN, SENSE with respect to AGND .....–0.3V to 27V
Voltage at DCIN, BAT2 with Respect to DGND .....–0.3V to 27V
Voltage at INTB, SDA, SCL, DCDIV with Respect to DGND ..... –0.3V to 7V
BOOST, BOOSTC Voltage with Respect to V_{CC} 10V
Voltage at V_{DD} with Respect to DGND ..... –0.3V to 7V
SW Voltage with Respect to AGND ..... –2V to V_{CC}
GBIAS, SYNC ..... –0.3V to 10V
V_C, PROG, V_{SET} Voltage with Respect to AGND .....–0.3V to 7V
TGATE, BGATE Current Continuous .....±200mA
TGATE, BGATE Output Energy (per Cycle) 2µJ
PGND, DGND with Respect to AGND .....±0.3V
Current into Any Pin .....±100mA
Operating Ambient Temperature Range..... 0°C to 70°C
Operating Junction Temperature Range ..... –40°C to 125°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
36-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 85°C/W

ORDER PART NUMBER
LTC1759CG

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range (T_J = 0°C to 100°C), otherwise specifications are T_A = 25°C. V_{CC} = DCIN = 18V, $V_{BAT1, 2}$ = 12.6V, V_{DD} = 3.3V unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply and Reference						
DCIN, V_{CC} Operating Voltage		●	11		24	V
V_{CC} Operating Current	$V_{CC} \le 24V$	●		12	20	mA
DCIN Operating Current	V_{DCIN} = 24V	●		85	150	µA
UV Lockout Threshold	Voltage on UV Pin Rising	●	6.3	6.7	7.25	V
UV Pin Input Current	$0V \le V_{UV} \le 8V$	●	–1		5	µA
Battery Discharge Current	$V_{UV} \le 0.4V$, All Connected Pins			40	80	µA
V_{DD} Operating Voltage		●	3.0		5.5	V
V_{DD} Operating Current	Charging, V_{DD} = 5.5V, Shorted Thermistor Not Charging, V_{DD} = 5.5V			1.35 80	2 150	mA µA
V_{DD} Undervoltage Lockout		●	1.6	2.2	2.9	V
Switching Regulator						
Charging Voltage Accuracy (Notes 3, 5)	$2.465V \le V_{BAT2} \le V_{MAX}$	●	–1		1	%
Charging Current Accuracy (Note 3)	R_{SET} Tolerance = 1%		–5		5	%

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range (T_J = 0°C to 100°C), otherwise specifications are T_A = 25°C. V_{CC} = DCIN = 18V, $V_{BAT1, 2}$ = 12.6V, V_{DD} = 3.3V unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BOOST Pin Current	$V_{BOOST} = V_{SW} + 8V$, $0V \le V_{SW} \le 20V$					
	TGATE High			2	3	mA
	TGATE Low			2	3	mA
V_{BOOST} Threshold to Turn T_{GATE} Off (Note 6)	Measured at ($V_{BOOST} - V_{SW}$)					
	Low to High	●	6.8	7.3	7.6	V
	Hysteresis			0.25		V
BOOSTC Pin Current	$V_{BOOSTC} = V_{CC} + 8V$			1		mA
Sense Amplifier CA1 Gain and Input Offset Voltage	$11V \le V_{CC} \le 24V$, $0V \le V_{BAT} \le 20V$					
(With $R_{S2} = R_{S3} = 200\Omega$)	R_{SET} = 4.93k	●	92	100	108	mV
(Measured Across R_{S1}) (Note 4)	R_{SET} = 49.3k		7	10	13	mV
CA1 Bias Current (SENSE, BAT1)	V_{SDB} = High	●		–50	–120	µA
	V_{SDB} = Low (Shutdown)				–10	µA
CA1 Input Common Mode Range		●	–0.25		V_{CC} – 0.3	V
SPIN Input Current	V_{SDB} = High, V_{SPIN} = 12.6V	●			2	mA
	V_{SDB} = Low				10	µA
CL1 Turn-On Threshold	0.5mA Output Current		87	92	97	mV
CL1 Transconductance	Output Current from 50µA to 500µA		0.5	1	3	mho
CLP Input Current	0.5mA Output Current			1	3	µA
CLN Input Current	0.5mA Output Current			0.8	2	mA
CA2 Transconductance	V_C = 1V, I_{VC} = ±1µA		150	200	300	µmho
V_A Transconductance (Note 5)	Ouput Current from 50µA to 500µA		0.21	0.6	1	mho
Gate Drivers						
V_{GBIAS}	$V_{CC} \ge 11V$, $I_{GBIAS} \le 15mA$, V_{SDB} = High	●	8.4	9.1	9.6	V
V_{TGATE} High ($V_{TGAGE} - V_{SW}$)	$I_{TGATE} \le 20mA$	●	5.6	6.6		V
V_{BGATE} High	$I_{BGATE} \le 20mA$	●	6.2	7.2		V
V_{TGATE} Low ($V_{TGATE} - V_{SW}$)	$I_{TGATE} \le 50mA$	●			0.8	V
V_{BGATE} Low	$I_{BGATE} \le 50mA$	●			0.8	V
INFET "ON" Clamping Voltage ($V_{CC} - V_{INFET}$)		●	6.5	7.8	9	V
INFET "ON" Drive Current	$V_{INFET} = V_{CC} - 6V$	●	8	20		mA
INFET "OFF" Clamping Voltage	V_{CC} Not Connected, $I_{INFET} < -2\mu A$				1.4	V
INFET "OFF" Drive Current	V_{CC} = 12.4V, ($V_{CC} - V_{INFET}$) ≥ 2V			–2.5		mA
V_{TGATE}, V_{BGATE} at Shutdown	V_{SDB} = Low, $I_{TGATE} = I_{BGATE}$ = 10µA	●			1	V
Trip Points						
DCDIV Threshold	V_{DCDIV} Rising from 0.8V to 1.2V	●	0.9	1.0	1.1	V
DCDIV Hysteresis				25		mV
DCDIV Input Bias Current	V_{DCDIV} = 1V	●			100	nA
Power-Fail Indicator ($V_{BAT2} \ge V_{DCIN}$) (Note 7)	AC_PRESENT = 1, V_{DCIN} = 6V	●	0.84	0.89	0.97	V/V
Power-Fail Indicator Hysteresis ($V_{BAT2} \ge V_{DCIN}$)	AC_PRESENT = 1, V_{DCIN} = 6V			0.02		V/V
SYNC Pin Threshold			0.9	1.4	2.0	V
SYNC Pin Input Current	V_{SYNC} = 0V				–500	µA
	V_{SYNC} = 2V				–30	µA

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Thermistor Decoder (Note 11)						
Combined Input Leakage on RNR and THERM					200	nA
Thermistor Trip (COLD/OR)	R_{WEAK} = 475k ±1%	●	80	100	120	kΩ
Thermistor Trip (IDEAL/COLD)	R_{NR} = 10k ±1%	●	26.4	30	33.6	kΩ
Thermistor Trip (HOT/IDEAL)	R_{NR} = 10k ±1%	●	2.64	3	3.36	kΩ
Thermistor Trip (UR/HOT)	R_{UR} = 1k ±1%	●	440	500	560	Ω
DACs						
Charging Current Resolution	Guaranteed Monotonic Above I_{MAX}/16		10			bits
Charging Current Granularity	R_{ILIMIT} = 0 R_{ILIMIT} = 10k ±1% R_{ILIMIT} = 33k ±1% R_{ILIMIT} = Open (or Short to V_{DD})			1 2 4 8		mA mA mA mA
Wake-Up Charging Current ($I_{WAKE-UP}$) (Note 8)				80		mA
Charging Current Limit (I_{MAX})	R_{ILIMIT} = 0 R_{ILIMIT} = 10k ±1% R_{ILIMIT} = 33k ±1% R_{ILIMIT} = Open (or Short to V_{DD})			1023 2046 4092 8184		mA mA mA mA
I_{SET} $R_{DS(ON)}$				25		Ω
I_{SET} I_{OFF}	V_{ISET} = 2.7V	●			1	µA
Charging Voltage Resolution	Guaranteed Monotonic (2.5V ≤ V_{BAT} ≤ 21V)		10			bits
Charging Voltage Granularity	R_{VLIMIT} = 0 R_{VLIMIT} = 10k ±1% R_{VLIMIT} = 33k ±1% R_{VLIMIT} = 100k ±1% R_{VLIMIT} = Open (or Short to V_{DD})			16 16 32 32 32		mV mV mV mV mV
Charging Voltage Limit	R_{VLIMIT} = 0 R_{VLIMIT} = 10k ±1% R_{VLIMIT} = 33k ±1% R_{VLIMIT} = 100k ±1% R_{VLIMIT} = Open (or Short to V_{DD}) (Note 2)	● ● ● ● 	8.33 12.50 16.67 20.82 	8.432 12.64 16.864 21.056 32.736	8.485 12.72 16.97 21.18 	V V V V V
Logic Levels (Note 12)						
SCL/SDA Input Low Voltage (V_{IL})		●			0.6	V
SCL/SDA Input High Voltage (V_{IH})		●	1.4			V
SDA Output Low Voltage (V_{OL})	I_{PULLUP} = 350µA	●			0.4	V
SCL/SDA Input Current (I_{IL})	V_{SDA}, V_{SCL} = V_{IL}	●			1	µA
SCL/SDA Input Current (I_{IH})	V_{SDA}, V_{SCL} = V_{IH}	●			1	µA
INTB Output Low Voltage (V_{OL})	I_{PULLUP} = 500µA	●			0.4	V
INTB Output Pull-Up Current	V_{INTB} = V_{OL}	●	3.5	10	17.5	µA
CHGEN Output Low Voltage (V_{OL})	I_{OL} = 200µA	●			0.4	V
CHGEN Output High Voltage (V_{OH})	I_{OH} = –200µA	●	V_{DD} – 0.4			V
SDB Shutdown Threshold		●	1		2	V
SDB Pin Current	0V ≤ V_{SDB} ≤ 3V				8	µA
Power-On Reset Duration	V_{DD} Ramp from 0V to > 3V in < 5µs			100		µs

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Charger Timing						
V_{TGATE}, V_{BGATE} Rise/Fall Time	1nF Load			25		ns
TGATE, BGATE Peak Drive Current	10nF Load			1		A
Regulator Switching Frequency		●	170	200	230	kHz
Synchronization Frequency		●	240		280	kHz
Maximum Duty Cycle in Start-Up Mode (Note 9)		●	85	90		%
$t_{TIMEOUT}$ for Wake-Up Charging a Cold or Underrange Battery		●	140	175	210	sec
SMBus Timing (refer to System Management Bus Specification, Revision 1.0, section 2.1 for timing diagrams) (Note 12)						
SCL Serial Clock High Period (t_{HIGH})	I_{PULLUP} = 350µA, C_{LOAD} = 150pF	●	4			µs
SCL Serial Clock Low Period (t_{LOW})	I_{PULLUP} = 350µA, C_{LOAD} = 150pF	●	4.7			µs
SDA/SCL Rise Time (t_r)	C_{LOAD} = 150pF	●			1000	ns
SDA/SCL Fall Time (t_f)		●	30		300	ns
SMBus Accelerator Boosted Pull-Up Current	V_{DD} = 3V	●	1	2.5		mA
Start Condition Setup Time ($t_{SU:STA}$)		●	4.7			µs
Start Condition Hold Time ($t_{HD:STA}$)		●	4.0			µs
SDA to SCL Rising-Edge Setup Time ($t_{SU:DAT}$)		●	250			ns
SDA to SCL Falling-Edge Hold Time, Slave Clocking in Data ($t_{HD:DAT}$)		●	300			ns
$t_{TIMEOUT}$ Between Receiving Valid ChargingCurrent() and ChargingVoltage() Commands (Note 10)		●	140	175	210	sec

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: This limit is greater than the absolute maximum for the charger. Therefore, there is no effective limitation on voltage when this option is selected. If the charger is requested to charge with a higher voltage than the nominal limit, the VOLTAGE_OR bit will be set.

Note 3: Total system accuracy from SMBus request to output voltage or output current.

Note 4: Test Circuit #1.

Note 5: Voltage accuracy is calculated using measured reference voltage, obtained from V_{SET} pin using Test Circuit #2, and VDAC resistor divider ratio.

Note 6: When supply and battery voltage differential is low, high oscillator duty cycle is required. The LTC1759 has a unique design to achieve duty cycle greater than 99% by skipping cycles. Only when V_{BOOST} drops below the comparator threshold, will TGATE be turned off. See Applications Information section.

Note 7: Power failure bit is set when the battery voltage is above 89% of the power adapter voltage (V_{DCIN}).

Note 8: The charger provides wake-up current when a battery is inserted into the connector, prior to the battery requesting charging current and voltage. See Smart Battery Charger Specification (Revision 1.0), section 6.1.3 and 6.1.8.

Note 9: In system start-up, C6 (boost capacitor) has no charge stored in it. The LTC1759 will keep TGATE off, and turn BGATE on for 0.2µs, thus charging C6. A comparator senses V_{BOOST} and switches to the normal PWM mode when V_{BOOST} is above its threshold.

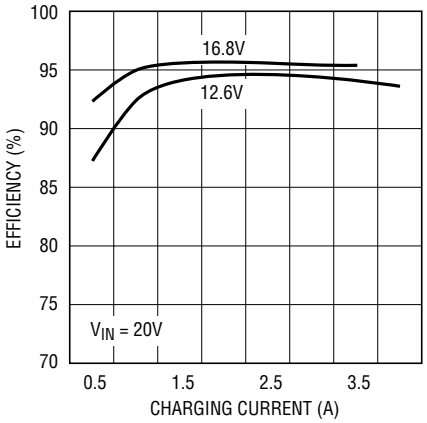
Note 10: Refer to Smart Battery Charge Specification (Revision 1.0), section 6.1.2.

Note 11: Maximum total external capacitance on RNR and THERM pins is 75pF.

Note 12: SMBus operation guaranteed by design from –40°C to 85°C.

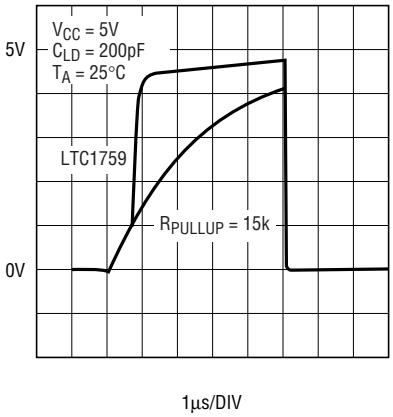
TYPICAL PERFORMANCE CHARACTERISTICS

Charger Efficiency



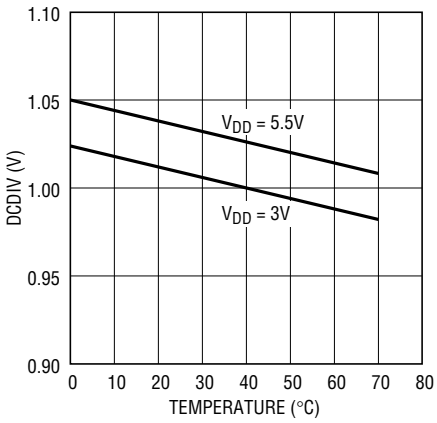
1759 G09

SMBus Accelerator Operation



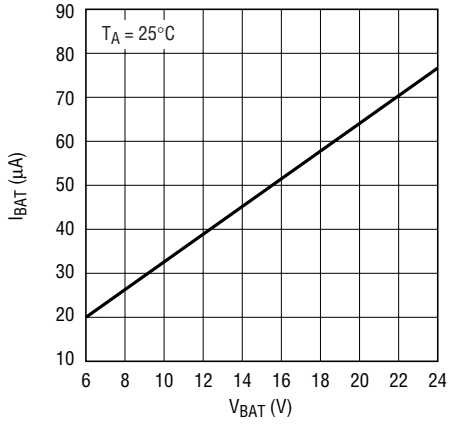
1759 G02

DCDIV Trip Point vs Temperature



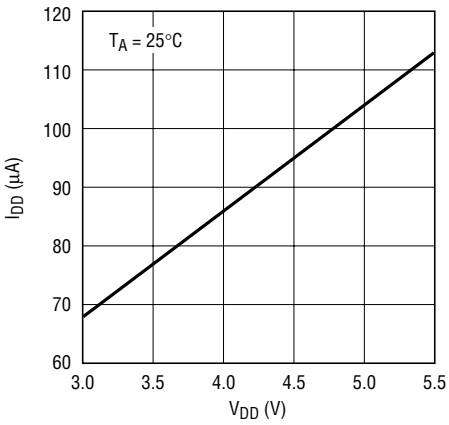
1759 G03

Current from Battery vs Battery Voltage (Does Not Include V_{DD} Current)



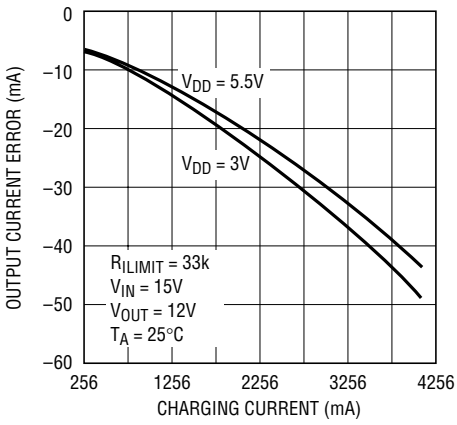
1759 G04

I_{DD} vs V_{DD} (Not Charging)



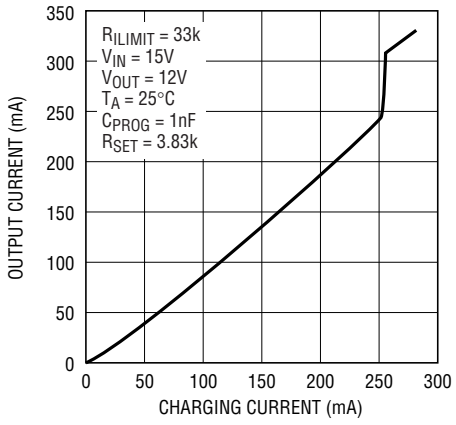
1759 G05

Programmed Current Accuracy



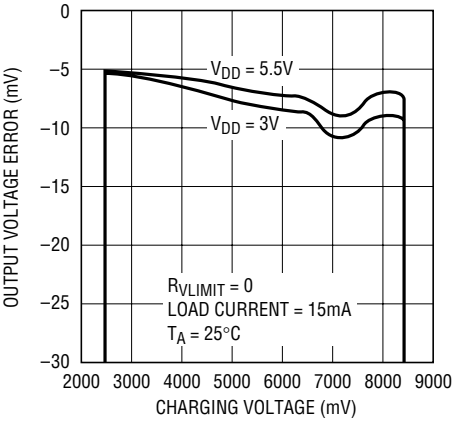
1759 G06

Low Current Mode



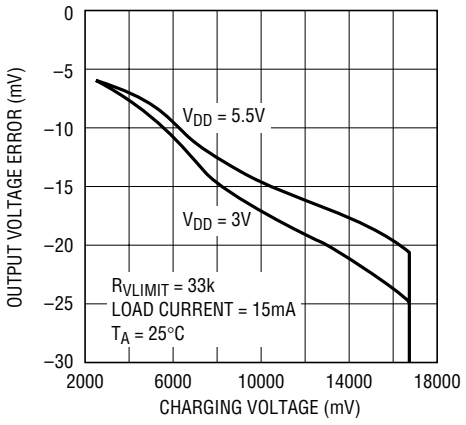
1759 G01

Charging Voltage Error



1759 G07

Charging Voltage Error



1759 G08

PIN FUNCTIONS

Input Power-Related Pins

UV (Pin 7): Charger Section Undervoltage Lockout Pin. The rising threshold is 6.7V with a hysteresis of 0.5V. Switching stops in undervoltage lockout. Connect this input to the input voltage source with no resistor divider. UV must be pulled below 0.7V when there is no input voltage source (5k resistor from adapter output to ground is required) to obtain the lowest quiescent battery current.

INFET (Pin 8): Gate Drive to Input P-channel FET. For very low dropout applications, use an external P-channel FET to connect the adapter output and V_{CC}. INFET is clamped to 7.8V below V_{CC}.

CLP (Pin 9): Positive Input to the Input Current Limit Amplifier CL1. When used to limit supply current, a filter (R3 and C1 of Figure 10) is needed to filter out the switching noise. The threshold is set at 92mV.

CLN (Pin 10): Negative Input to the Input Current Limit Amplifier CL1. It should be connected to V_{CC} (to the V_{CC} bypass capacitor C2 for less noise).

COMP1 (Pin 11): Compensation Node for the Input Current Limit Amplifier CL1. At input adapter current limit, this node rises to 1V. By forcing COMP1 low with an external transistor, amplifier CL1 will be defeated (no adapter current limit). COMP1 can source 200µA. Ground (to AGND) this pin if the adapter current limiting function is not used.

Battery Charging-Related Pins

BOOST (Pin 1): This pin is used to bootstrap and supply power for the topside power switch gate drive and control circuity. In normal operation, V_{BOOST} is powered from an internally generated 8.6V regulator V_{GBIAS}, $V_{BOOST} \approx V_{CC}$ + 9.1V when TGATE is high. Do not force an external voltage on BOOST pin.

TGATE (Pin 2): This pin provides gate drive to the topside power FET. When TGATE is driven on, the gate voltage will be approximately equal to V_{SW} + 6.6V. A series resistor of 5Ω to 10Ω should be used from this pin to the gate of the topside FET.

SW (Pin 3): This pin is the reference point for the floating topside gate drive circuitry. It is the common connection for the top and bottom side switches and the output inductor. This pin switches between ground and V_{CC} with very high dv/dt rates. Care needs to be taken in the PC layout to keep this node from coupling to other sensitive nodes. A 1A Schottky clamping diode should be placed very close to the chip from the ground pin to this pin to prevent the chip substrate diode from turning on. See Applications Information for more details.

SYNC (Pin 4): External Clock Synchronization Input. Pulse width range: 10% to 90%.

SDB (Shutdown Bar) (Pin 5): Active Low Digital Input. The charger is disabled when asserted. This pin is connected to the CHGEN pin to enable charger control through the SMBus interface.

CHGEN (Pin 12): Digital Output to Enable Charger Function. Connect CHGEN to SDB.

I_{SET} (Pin 17): Open-Drain CMOS Switch to DGND. An external resistor, R_{SET}, is connected from I_{SET} to the current programming input, the PROG pin of the battery charger section, which sets the range of the charging current.

I_{LIMIT} (Pin 24): An external resistor is connected between this pin and DGND. The value of the external resistor programs the range and resolution of the programmed charger current. See Electrical Characteristics table for more information.

V_{LIMIT} (Pin 25): An external resistor is connected between this pin and DGND. The value of the external resistor programs the range and resolution of the V_{SET} divider. See Electrical Characteristics table for more information.

V_{SET} (Pin 26): This is the tap point of the programmable resistor divider, which provides battery voltage feedback to the charger.

PIN FUNCTIONS

V_C (Pin 27): This is the control signal of the inner loop of the current mode PWM. Switching starts at 0.9V. Higher V_C corresponds to higher charging current in normal operation. A capacitor of at least 0.33µF to AGND filters out noise and controls the rate of soft start.

PROG (Pin 28): This pin is for programming the charging current and for system loop compensation. During normal operation, the pin voltage is approximately 2.465V.

SENSE (Pin 29): Current Amplifier CA1 Input. Sensing must be at the positive terminal of the battery.

SPIN (Pin 30): This pin is for the internal amplifier CA1 bias. It must be connected to R_{SENSE} as shown in Figure 1.

BAT1 (Pin 31): Current Amplifier CA1 Input.

BOOSTC (Pin 33): This pin is used to bootstrap and supply the current sense amplifier CA1 for very low dropout conditions. V_{CC} can be as low as only 0.4V above the battery voltage. A diode and a capacitor are needed to get the voltage from V_{BOOST}. If low dropout is not needed and V_{CC} is always 3V or greater than V_{BAT}, this pin can be left floating or tied to V_{CC}. Do not force this pin to a voltage lower than V_{CC}.

BGATE (Pin 35): Drives the gate of the bottom external N-channel FET of the charger buck converter.

Monitor/Fault Diagnostic Pins

DCDIV (Pin 21): Supply Divider Input. This is a high impedance comparator input with a 1V threshold (rising edge) and hysteresis.

DCIN (Pin 22): Input connected to the DC input source to monitor the DC input for power-fail condition.

BAT2 (Pin 23): Sensing Point for Voltage Control Loop. Connect this to the positive terminal of the battery.

Internal Power Supply Pins

AGND (Pin 6): DC Accurate Ground for Analog Circuitry.

V_{DD} (Pin 16): Low Voltage Power Supply Input. Bypass this pin with 0.1µF.

DGND (Pin 18): Ground for Digital Circuitry and DACs. Should be connected to AGND at the negative terminal of the charger output filter capacitor.

V_{CC} (Pin 32): Power Input for Battery Charger Section. Bypass this pin with 0.47µF.

GBIAS (Pin 34): 8.6V Regulator Output for Bootstrapping V_{BOOST} and V_{BOOSTC}. A bypass capacitor of at least 2µF is needed. Switching will stop if V_{BOOST} drops below 7.1V.

PGND (Pin 36): High Current Ground Return for Charger Gate Drivers.

SBS Interface Pins

INTB (Interrupt Bar) (Pin 13): Active Low Interrupt Output to Host. Signals host that there has been a change of status in the charger registers and that the host should read the LTC1759 status registers to determine if any action on its part is required. This signal can be connected to the optional SMBALERT# line of the SMBus. Open drain with weak current source pull-up to V_{DD} (with Schottky to allow it to be pulled to 5V externally, see Figure 2).

SDA (Pin 14): SMBus Data Signal from Main (Host-controlled) SMBus.

SCL (Pin 15): SMBus Clock Signal from Main (Host-Controlled) SMBus. External pull-up resistor is required.

THERM (Pin 19): Thermistor Force/Sense Pin to Smart Battery. See Electrical Characteristics table for more detail. Maximum allowed combined capacitance on THERM and RNR is 75pF.

RNR (Pin 20): Thermistor Force/Sense Pin to Smart Battery. See Electrical Characteristics table for more detail. Maximum allowed combined capacitance on THERM and RNR is 75pF.

BLOCK DIAGRAM

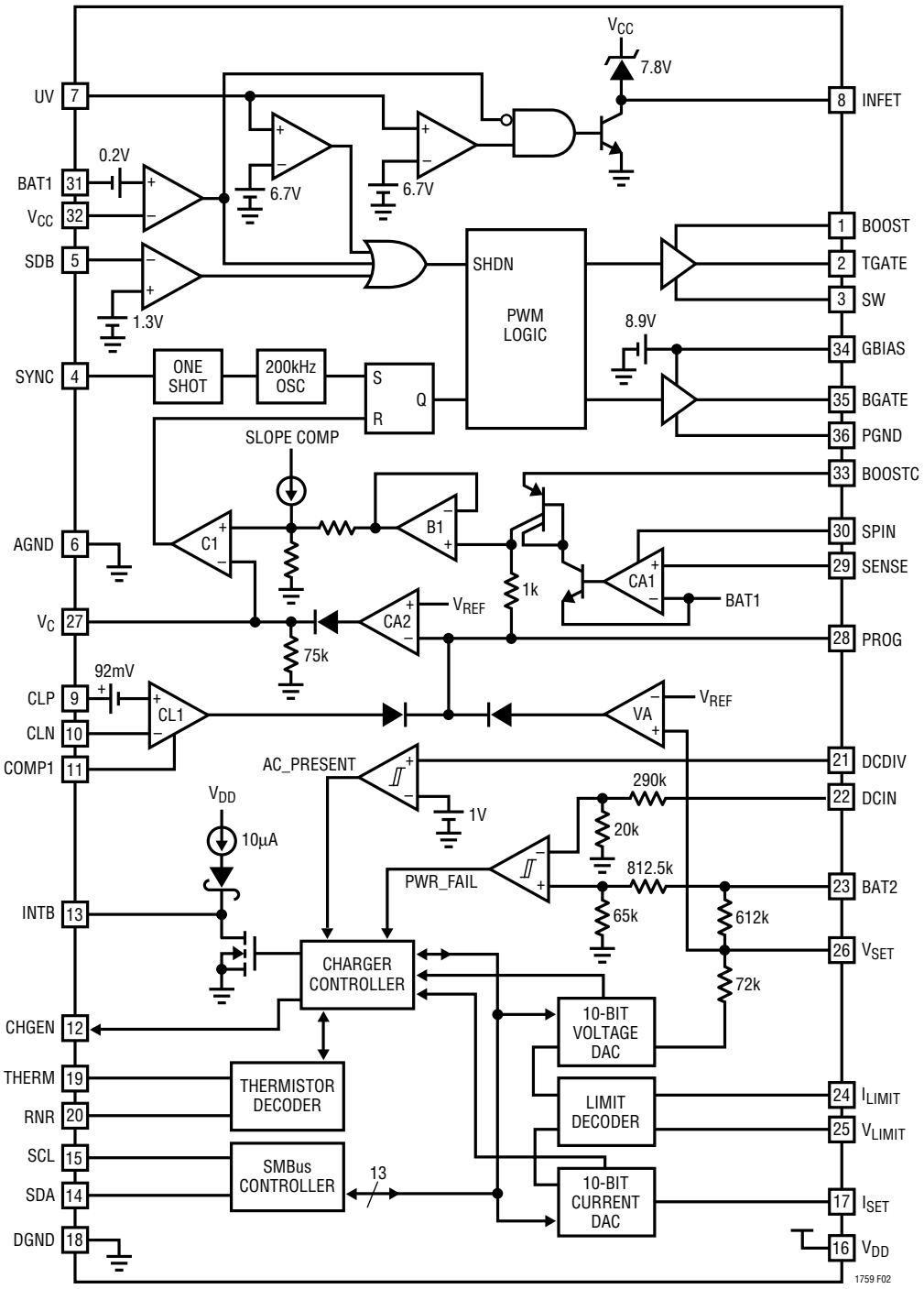
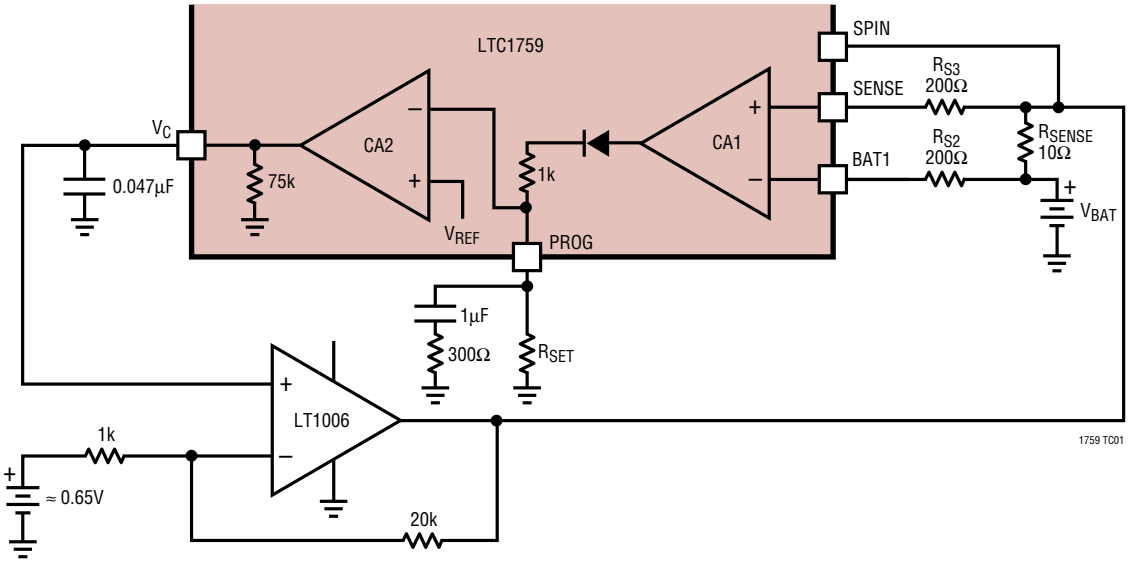


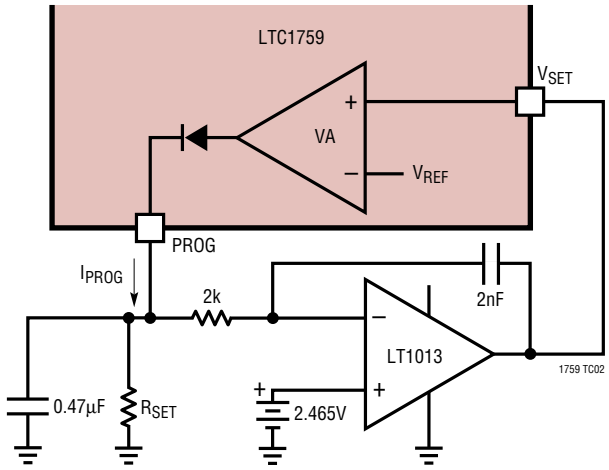
Figure 2

TEST CIRCUITS

Test Circuit 1



Test Circuit 2



OPERATION

Overview (Refer to Block Diagram and Figure 10)

The LTC1759 is composed of a battery charger section, a charger controller, two 10-bit DACs to control charger parameters, a thermistor decoder, limit decoder and an SMBus controller block. If no battery is present, the thermistor decoder indicates a THERM_OR condition and charging is disabled by the charger controller (CHGEN = Low). Charging will also be disabled if AC_PRESENT is low, or the battery thermistor is decoded as THERM_HOT. If a battery is inserted or AC power is connected, the battery will be charged with an 80mA "wake-up" current. The wake-up current is discontinued after three minutes if the thermistor is decoded as THERM_UR or THERM_COLD, and the battery or host doesn't transmit charging commands.

The SMBus controller block receives ChargingCurrent() and ChargingVoltage() commands via the SMBus. If ChargingCurrent() and ChargingVoltage() command pairs are received within a three-minute interval, the values are stored in the current and voltage DACs and the charger controller asserts the CHGEN line if the decoded thermistor value will allow charging to commence. ChargingCurrent () and ChargingVoltage() values are compared against limits programmed by the limit decoder block; if the commands exceed the programmed limits these limits are substituted and overrange flags are set.

The charger controller will assert INTB whenever a status change is detected. The host may query the charger, via the SMBus, to obtain ChargerStatus() information. INTB will be deasserted upon a successful read of ChargerStatus() or a successful Alert Response Address (ARA) request.

Battery Charger Section

The LTC1759 is synchronous current mode PWM step-down (Buck) switcher. The battery DC charging current is programmed with a current DAC via the SMBus interface. Amplifier CA1 converts the charging current through R_{SENSE} to a much lower current I_{PROG} ($I_{PROG} = I_{BAT} \bullet R_{SENSE}/R_{S2}$) fed into the PROG pin. Amplifier CA2 compares the output of CA1 with the programmed current and drives the PWM loop to force them to be equal. High DC accuracy is achieved with averaging capacitor C_{PROG}. Note that I_{PROG} has both AC and DC components. I_{PROG} generates a ramp signal that is fed to the PWM control comparator C1 through buffer B1 and level shift resistors forming the current mode inner loop. The BOOST pin supplies the top power switch gate drive. The LTC1759 generates a 8.9V V_{GBIAS} for bootstrapping V_{BOOST} and V_{BOOSTC} as well as to drive the bottom power FET. The BOOSTC pin supplies the current amplifier CA1 with a voltage higher than V_{CC} for low dropout applications. Amplifier VA reduces the charging current when the battery voltage reaches the set voltage programmed by the VDAC and the 2.465V reference voltage.

The amplifier CL1 monitors and limits the input current, normally from the AC adapter, to a preset level (92mV/R_{CL}). At input current limit, CL1 will supply the programming current I_{PROG} and thus reduce battery charging current.

The INFET pin drives an external input P-channel FET for low dropout applications.

SMBus Interface

All communications over the SMBus are interpreted by the SMBus controller block. The SMBus controller is an SMBus slave device. All internal LTC1759 registers may be updated and accessed through the SMBus controller, and charger controller as required. The SMBus protocol is a derivative of the I^2C^{TM} bus (Reference *"I^2C-Bus and How to Use It, V1.0"* by Philips and *"System Management Bus Specification"* by the Smart Battery System Organization*, for a complete description of the bus protocol requirements.)

All data is clocked into the shift register on the rising edge of SCL. All data is clocked out of the shift register on the falling edge of SCL. Detection of an SMBus Stop condition, or power-on reset via the V_{DD} undervoltage lockout, will reset the controller to an initial state at any time.

The LTC1759 command set is interpreted by the SMBus controller and passed onto the charger controller block as control signals or updates to internal registers.

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*http://www. SBS-FORUM.org

OPERATION

Table 1: Supported Charger Functions

FUNCTION	SMBus ADDRESS (7-BIT)	COMMAND CODE (8-BIT hex)	ACCESS	DATA TYPE
ChargerSpecInfo()	b0001_001	h11	r	Register
ChargerMode()	b0001_001	h12	w	Register
ChargerStatus()	b0001_001	h13	r	Register
ChargingCurrent()	b0001_001	h14	w	Register
ChargingVoltage()	b0001_001	h15	w	Register
AlarmWarning()	b0001_001	h16	w	Control
LTCVersionFunction()	b0001_001	h3c	r	Register
OptionalMfgFunction3()	b0001_001	h3d	–	Not Supported
OptionalMfgFunction2()	b0001_001	h3e	–	Not Supported
OptionalMfgFunction1()	b0001_001	h3f	–	Not Supported
Alert Response Address[1]	b0001_100	N/A	Read Byte	Interrupt Address

[1]Read-byte format. 89h is returned as the interrupt address of the LTC1759. Rev 1.0 SMBus Compliant.

Table 2: SMBus Word Bit Definitions for All Allowed LTC1759 Functions

FUNCTION	FIELD	WORD BIT MAPPING	POWER-ON RESET VALUE (BINARY)	ALLOWED VALUES
ChargerSpecInfo	CHARGER_SPEC	3:0	0001	• The CHARGER_SPEC Reports the Version of the Smart Battery Charger Specification the Charger Supports • 0001 – Version 1.0 • All Other Codes Reserved • Always Returns 0001 • Read Only. Write Will NACK
	SELECTOR_SUPPORT	4	0	• 0 – Charger Does Not Support the Optional Smart Battery Selector Commands • 1 – Charger Supports the Optional Smart Battery Selector Commands • Always Returns 0 • Read Only. Write Will NACK
	Reserved	15:5	0	• These Bits Are Reserved and Must Return Zero • Read Only. Write Will NACK
ChargerMode()	INHIBIT_CHARGE	0	0	• 0 – Enable Charging (Power-On Default) • 1 – Inhibit Charging • Write Only. Read Will NACK • Cleared to Power-On Reset Value When: 1) POR_RESET = 1 2) AC_PRESENT = 0 3) BATTERY_PRESENT = 0
	ENABLE_POLLING	1	0	• 0 – Disable Polling (Power-On Default for Smart Battery Controlled Chargers) • 1 – Enable Polling (Power-On Default for Host Controlled Chargers). • Ignored by LTC1759 • Write Only. Read Will NACK
	POR_RESET	2	0	• 0 – Mode Unchanged (Default) • 1 – Set Charger to Power-On Defaults • This Reset Only Affects the Charger_Controller Block • Write Only. Read Will NACK

OPERATION

FUNCTION	FIELD	WORD BIT MAPPING	POWER-ON RESET VALUE (BINARY)	ALLOWED VALUES
	RESET_TO_ZERO	3	0	• 0 – Charging Value Unchanged • 1 – Set Charging Values to Zero **NOTE:** This function is implemented by forcing the charger to CHARGING_NONE_STATE and not allowing charge to resume until a valid ChargingCurrent() and ChargingVoltage() Pair Is received. • Write Only. Read Will NACK
	Reserved	15:4	0	• Not Implemented. Writes to These Bits Are Ignored. • Write Only. Read Will NACK
ChargerStatus()	CHARGE_INHIBITED	0	0	This Is the ChargerMode() INHIBIT_CHARGE Bit • 0 – Charger Is Enabled • 1 – Charger Is Inhibited • Read Only. Write Will NACK
	MASTER_MODE	1	0	• 0 – Charger Is in Slave Mode (Polling Disabled) • 1 – Charger Is in Master Mode (Polling Enabled) • Always Returns 0 • Read Only. Write Will NACK
	VOLTAGE_NOTREG	2	0	• 0 – Charger's Output Voltage Is in Regulation • 1 – Requested ChargingCurrent() Is Not Being Met • Not Supported; Always Returns 0 • Read Only. Write Will NACK
	CURRENT_NOTREG	3	0	• 0 – Charger's Output Current Is in Regulation • 1 – Requested ChargingCurrent() Is Not Being Met • Not Supported; Always Returns 0 • Read Only. Write Will NACK
	LEVEL_3:LEVEL_2	5:4	01	• 00 – Reserved • 01 – Charger Is a Smart Battery Controlled • 10 – Reserved • 11 – Charger Is a Host Controlled • Always Returns 01 • Read Only. Write Will NACK
	CURRENT_OR	6	0	• 0 – ChargingCurrent() Value Is Valid • 1 – ChargingCurrent() Value Is Invalid • This Value Is Valid Only When Charging with CHARGE_INHIBITED = 0 or 1 • Read Only. Write Will NACK
	VOLTAGE_OR	7	0	• 0 – ChargingVoltage() Value Is Valid • 1 – ChargingVoltage() Value Is Invalid • This Value Is Valid Only When Charging with CHARGE_INHIBITED = 0 or 1 • Read Only. Write Will NACK
	THERM_OR	8	Value	• 0 – Thermistor Indicates Not Overrange • 1 – Thermistor Indicates Overrange • Read Only. Write Will NACK
	THERM_COLD	9	Value	• 0 – Thermistor Indicates Not Cold • 1 – Thermistor Indicates Cold • Read Only. Write Will NACK
	THERM_HOT	10	Value	• 0 – Thermistor Indicates Not Hot • 1 – Thermistor Indicates Hot • Read Only. Write Will NACK

OPERATION

FUNCTION	FIELD	WORD BIT MAPPING	POWER-ON RESET VALUE (BINARY)	ALLOWED VALUES
	THERM_UR	11	Value	• 0 – Thermistor Indicates Not Underrange • 1 – Thermistor Indicates Underrange • Read Only. Write Will NACK
	ALARM_INHIBITED	12	0	• 0 – Charger Not Alarm Inhibited • 1 – Charger Alarm Inhibited. This Bit Is Set but Never Cleared by AlarmWarning() • Read Only. Write Will NACK • Cleared to Power-On Reset Value When: 1) POR_RESET = 1 2) BATTERY_PRESENT = 0 3) AC_PRESENT = 0 4) A Valid ChargingVoltage(), ChargingCurrent() Pair Is Received
	POWER_FAIL	13	Value	• 0 – $V_{BAT}/V_{DCIN} < 0.9$ • 1 – $V_{BAT}/V_{DCIN} > 0.9$ • Read Only. Write Will NACK
	BATTERY_PRESENT	14	Value	• 0 – Battery Is Not Present • 1 – Battery Is Present • Read Only. Write Will NACK
	AC_PRESENT	15	Value	• 0 – Charge Power Is Not Available • 1 – Charge Power Is Available • Read Only. Write Will NACK
ChargingCurrent()	CHARGING_CURRENT [15:0]	15:0	0	• Unsigned Integer Representing Charger Current in mA • Three Possible Responses – Supply the Current Requested – Supply Its Programmatic Maximum Current If the Request Is Greater Than Its Programmatic Value and Less Than hffff – Supply Its Maximum Safe Current If the Request Is hffff [Supply Current Required to Meet ChargingVoltage()]. • Write Only. Read Will NACK
ChargingVoltage()	CHARGING_VOLTAGE [15:0]	15:0	0	• Unsigned Integer Representing Charger Voltage in mV • Three Possible Responses – Supply the Voltage Requested – Supply Its Programmatic Maximum Voltage If the Request Is Greater Than Its Programmatic Value and Less Than hffff – Supply Its Maximum Voltage If the Request Is hffff [Supply Voltage Required to Meet ChargingCurrent()]. • Write Only. Read Will NACK
AlarmWarning()	OVER_CHARGED_ ALARM	15	0	• 1 – Terminate Charging Immediately • Write Only. Read Will NACK • Writing a 0 to This Bit Will Be Ignored
	TERMINATE_CHARGE_ ALARM	14	0	• 1 – Terminate Charging Immediately • Write Only. Read Will NACK • Writing a 0 to This Bit Will Be Ignored.
	RESERVED_ALARM1	13	0	• 1 – Terminate Charging Immediately • Write Only. Read Will NACK • Writing a 0 to This Bit Will Be Ignored.
	OVER_TEMP_ALARM	12	0	• 1 – Terminate Charging Immediately • Write Only. Read Will NACK • Writing a 0 to This Bit Will Be Ignored.

OPERATION

FUNCTION	FIELD	WORD BIT MAPPING	POWER-ON RESET VALUE (BINARY)	ALLOWED VALUES
	TERMINATE_ DISCHARGE_ALARM	11	0	• This Bit May Be Used to Signal That the Charger May Be Restarted After a Battery Conditioning Cycle Has Been Completed • Write Only. Read Will NACK • Writing a 0 to This Bit Will Be Ignored • Not Supported by LTC1759
	Reserved	10	–	• Not Supported by LTC1759 • Write Only. Read Will NACK
	REMAINING_ CAPACITY_ALARM	9	–	• Intended for Host • Not Supported by LTC1759 • Write Only. Read Will NACK
	REMAINING_TIME_ ALARM	8	–	• Intended for Host • Not Supported by LTC1759 • Write Only. Read Will NACK
	INITIALIZED	7	–	• Intended for Host • Not Supported by LTC1759 • Write Only. Read Will NACK
	DISCHARGING	6	–	• Intended for Host • Not Supported by LTC1759 • Write Only. Read Will NACK
	FULLY_CHARGED	5	–	• Intended for Host • Not Supported by LTC1759 • Write Only. Read Will NACK
	FULLY_DISHARGED	4	–	• Intended for Host • Not Supported by LTC1759 • Write Only. Read Will NACK
	ERROR	3:0	–	• Intended for Host • All Bits Set High Prior to AlarmWarning() Transmission • Not Supported by LTC1759 • Write Only. Read Will NACK
LTCVersionFunction ()	LTC_VERSION	15:0	0101hex	• Returns LTC Version Number • Read Only • Always Returns 0101hex

SMBus Accelerator Pull-Ups

Both SCL and SDA have SMBus accelerator circuits which reduce the rise time on systems with significant capacitance on the two SMBus signals. The dynamic pull-up circuitry detects a rising edge on SDA or SCL and applies 2mA to 5mA pull-up to V_{DD} for approximately 1µs (external pull-up resistors are still required to supply DC current). This action allows the bus to meet SMBus rise time requirements with as much as 150pF on each SMBus signal. The improved rise time will benefit all of the devices which use the SMBus, especially those devices that use the I^2C logic levels. Note that the dynamic pull-up circuits only pull to V_{DD}, so some SMBus devices that are not compliant to the SMBus specifications may still have rise time compliance problems if the SMBus pull-up resistors are terminated with voltages higher than V_{DD}.

OPERATION

The Charger Controller Block

The LTC1759 charger operations are handled by the charger controller block. This block is capable of charging the selected battery autonomously or under host control. The charger controller can request communications with the system management host (SMHost) by asserting INTB = 0; this will cause the SMHost, if present, to poll the LTC1759.

The charger controller receives SMBus slave commands from the SMBus controller block.

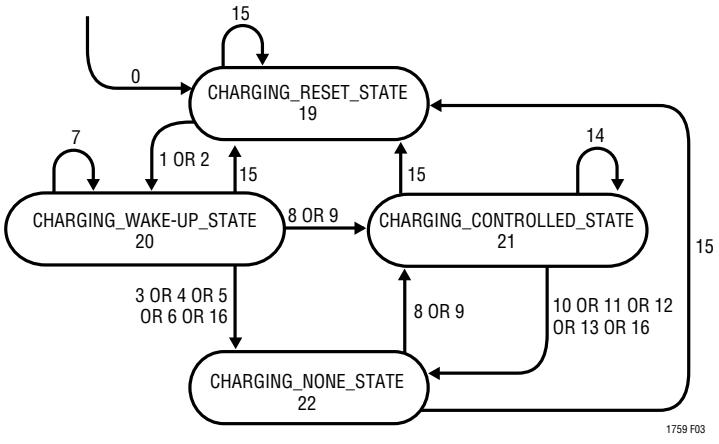
The charge controller allows the LTC1759 to meet the following Smart Battery-controlled (Level 2) charger requirements:

1. Implements the Smart Battery's critical warning messages over the SMBus.
2. Operates as an SMBus slave device that responds to ChargingVoltage() and ChargingCurrent() commands and adjusts the charger output characteristics accordingly.

The charger controller allows the LTC1759 to meet the following host-controlled (Level 3) Smart Battery charger requirements.

1. In a host-controlled system the host is able to operate as an SMBus master device.
2. The host may determine the appropriate charging algorithm by querying the battery or providing an alternative special charging algorithm.
3. The host may control charging by disabling the Smart Battery's ability to transmit ChargingCurrent() and ChargingVoltage() request functions and broadcasting the charging commands to the LTC1759 over the SMBus.
4. The LTC1759 will still respond to Smart Battery critical warning messages without host intervention.

The charger controller block uses the state machine of Figure 3. The functional features for state transitions and general control are detailed in Table 3.



NOTE: NUMBERS REFER TO CONDITIONS AND STATE DESCRIPTION IN TABLE 3

Figure 3. Charger Controller State Machine

OPERATION

Table 3. Charger_Controller Functional Features

#	CONDITION	ACTION
0	POWER_ON_RESET = 1	CHARGING_RESET_STATE =1 (Asynchronously Reset the Charger_Controller State Machine During Power-On Reset)
1	CHARGING_RESET_STATE = 1 AND the Battery Is Present AND AC_PRESENT = 1 AND INHIBIT_CHARGE = 0 AND Thermistor Is Ideal	CHARGING _WAKE-UP_STATE = 1 The Charger_Controller Will "Wake Up" Charge the Battery at $I_{WAKE-UP}$ Indefinitely
2	CHARGING_RESET_STATE = 1 AND the Battery Is Present AND AC_PRESENT =1 AND INHIBIT_CHARGE = 0 AND THERM_UR = 1 OR THERM_COLD = 1	CHARGING_WAKE-UP_STATE = 1 The Charger_Controller Will "Wake Up" Charge the Battery at $I_{WAKE-UP}$ Until Condition 3 Is Met
3	CHARGING_WAKE-UP_STATE = 1 AND the Time-Out Period Exceeds $t_{TIMEOUT}$ AND THERM_UR = 1 OR THERM_COLD = 1	CHARGING_NONE_STATE = 1 The Charger_Controller Stops Charging the Battery. It Cannot "Wake Up" Charge Again Until Condition 15 Is Met. It Can Supply "Controlled Charge" to the Battery If Conditions 8 or 9 Are Met
4	CHARGING_WAKE-UP_STATE = 1 AND an AlarmWarning() Message Is Received with Any Bit in the Upper Nibble Set	CHARGING_NONE_STATE =1 The Charger_Controller Stops Charging the Battery. It Cannot "Wake Up" Charge Again Until Condition 15 Is Met. It Can Supply "Controlled Charge" to the Battery If Conditions 8 or 9 Are Met
5	CHARGING_WAKE-UP_STATE = 1 (from Condition 1 above) AND THERM_HOT Changes from 0 to 1 AND THERM_UR = 0	CHARGING_NONE_STATE = 1 The Charger_Controller Stops Charging the Battery. It Cannot "Wake Up" Charge Again Until Condition 15 Is Met. It Can Supply "Controlled Charge" to the Battery If Conditions 8 or 9 Are Met
6	CHARGING_WAKE-UP_STATE = 1 (from Condition 2 above) AND THERM_UR Changes from 1 to 0 AND THERM_HOT = 1	CHARGING_NONE_STATE = 1 The Charger_Controller Stops Charging the Battery. It Cannot "Wake Up" Charge Again Until Condition 15 Is Met. It Can Supply "Controlled Charge" to the Battery If Conditions 8 or 9 Are Met
7	CHARGING_WAKE-UP-STATE = 1 AND INHIBIT_CHARGE Is Set to 1	CHARGING_WAKE-UP_STATE =1 The Charger_Controller Stops Charging the Selected Battery. The Timer Continues to Run. The Charger Can Resume "Wake-Up" Charging If INHIBIT_CHARGE = 0
8	(CHARGING_WAKE-UP_STATE = 1 OR CHARGING_NONE_STATE = 1) AND (Both ChargingCurrent() AND ChargingVoltage() Commands Are Received within $t_{TIMEOUT}$) AND INHIBIT_CHARGE = 0 AND THERM_HOT = 0	CHARGING_CONTROLLED_STATE = 1 The Charger_Controller Will Supply "Controlled Charge" to the Battery as Specified in the Current and Voltage Commands
9	(CHARGING_WAKE-UP_STATE = 1 OR CHARGING_NONE_STATE = 1) AND (Both ChargingCurrent() AND ChargingVoltage() Commands Are Received within $t_{TIMEOUT}$) AND INHIBIT_CHARGE = 0 AND THERM_UR = 1	CHARGING_CONTROLLED_STATE = 1 The Charger_Controller Will Supply "Controlled Charge" to the Battery as Specified in the Current and Voltage Commands
10	CHARGING_CONTROLLED_STATE = 1 AND No New ChargingCurrent() and ChargingVoltage() Commands Are Received for a Time-Out Period of $t_{TIMEOUT}$	CHARGING_NONE_STATE = 1 The Charger_Controller Stops Charging the Battery. It Cannot "Wake Up" Charge Again Until Condition 15 Is Met. It Can Supply "Controlled Charge" to the Battery If Conditions 8 or 9 Are Met
11	CHARGING_CONTROLLED_STATE = 1 The Charger_Controller Is Supplying "Controlled Charge" to the Battery AND (an AlarmWarning() Message Is Received with Any Bit in the Upper Nibble Set)	CHARGING_NONE_STATE = 1 The Charger_Controller Stops Charging the Battery. It Cannot "Wake Up" Charge Again Until Condition 15 Is Met. It Can Supply "Controlled Charge" to the Battery If Conditions 8 or 9 Are Met

OPERATION

#	CONDITION	ACTION
12	CHARGING_CONTROLLED_STATE = 1 AND THERM_HOT Changes from 0 to 1 AND THERM_UR = 0	CHARGING_NONE_STATE = 1 The Charger_Controller Stops Charging the Battery. It Cannot "Wake Up" Charge Again Until Condition 15 Is Met. It Can Supply "Controlled Charge" to the Battery If Conditions 8 or 9 Are Met
13	CHARGING_CONTROLLED_STATE = 1 AND THERM_UR Changes from 1 to 0 AND THERM_HOT = 1	CHARGING_NONE_STATE = 1 The Charger_Controller Stops Charging the Battery. It Cannot "Wake Up" Charge Again Until Condition 15 Is Met. It Can Supply "Controlled Charge" to the Battery If Conditions 8 or 9 Are Met
14	CHARGING_CONTROLLED_STATE = 1 AND INHIBIT_CHARGE Is Set to 1	CHARGING_CONTROLLED_STATE = 1 INHIBIT_CHARGE Asynchronously Inhibits Charging Without Affecting the Charger_Controller State Machine. This Means the Charger Stops Charging the Battery but Continues to Accept New ChargingCurrent() and ChargingVoltage() Commands, Continues to Monitor the Battery Thermistor Input and Continues to Track the Communication Time-Out. It Will Resume Charging the Battery If INHIBIT_CHARGE Is Cleared to 0, Possibly at Different Current and Voltage If New Commands Have Been Sent in the Interim
15	ANY STATE The Charger_Controller Is in Any State AND (the Battery Is Removed OR AC_PRESENT = 0 OR a 1 Is Written to POR_RESET) **NOTE:** Condition 15 Takes Precedence Over Any Other Condition.	CHARGING_RESET_STATE= 1 The Charger_Controller Is Set to Its Power-On Default State
16	(CHARGING_CONTROLLED_STATE = 1) OR CHARGING_WAKE-UP_STATE = 1) AND A 1 Is Written to RESET_TO_ZERO	CHARGING_NONE_STATE = 1 The Charger_Controller Stops Charging the Battery. It Cannot "Wake Up" Charge Again Until Condition 15 Is Met. It Can Supply "Controlled Charge" to the Battery If Conditions 8 or 9 Are Met. The Valid Charge Command Timer Is Cleared When RESET_TO_ZERO = 1. This Prevents Charging from Continuing Until After a Valid ChargeCurrent() and ChargeVoltage() Pair Is Received
18	ANY STATE AND AC_PRESENT Transitions 0 to 1 or 1 to 0 OR BATTERY_PRESENT Transitions 0 to 1 or 1 to 0	Alert SMHost of Change by Setting INTB = 0
19	CHARGING_RESET_STATE = 1	CHGEN = 0 The Charger Is Not Charging
20	CHARGING _WAKE-UP_STATE = 1	CHGEN = ~INHIBIT_CHARGE The Charger Will Provide a Wake-Up Current When CHGEN = 1
21	CHARGING_CONTROLLED_STATE = 1	CHGEN = ~INHIBIT_CHARGE The Charger Will Provide Specified Charging Voltage and Current When CHGEN = 1 A Zero Value for ChargingVoltage() Is Handled by Forcing CHGEN = 0
22	CHARGING_NONE_STATE = 1	CHGEN = 0 The Charger Is Not Charging

OPERATION

The Thermistor Decoder Block

This block measures the resistance of the battery's thermistor and features high noise immunity at critical trip points. The low power standby mode supports all SMB charger reporting requirements when AC is not present. The thermistor decoder is shown in Figure 4.

Thermistor sensing is accomplished by a state machine that reconfigures the switches of Figure 4 using RNR_SELB and RUR_SELB. The three allowable modes are as follows:

1. **Overrange Detection.** The RUR_SELB and RNR_SELB switches are off and the external R_{WEAK} resistor forms a voltage divider with R_{THERM}. The resulting voltage is monitored at THERM, compared to an internal reference and sampled at the output of the OR comparator. This detection mode is always active allowing low power operation when AC power is not available.
2. **Cold/Ideal/Hot Range Detection.** The RNR_SELB switch is on and the RUR_SELB switch is off. The external R_{NR} and R_{WEAK} resistors form a voltage divider with R_{THERM}. The resulting voltage is monitored at THERM, compared to an internal reference and sampled at the output of the cold and hot comparators. This detection mode is only activated if OR tested low.
3. **Underrange Detection.** The RNR_SELB switch is off and the RUR_SELB switch is on. The external R_{UR} and R_{WEAK} resistors form a voltage divider with R_{THERM}. The resulting voltage is monitored at RNR, compared to an internal reference and sampled at the output of the UR comparators. This detection mode is only activated if HOT tested high.

NOTE: The underrange detection scheme is a very important feature of the LTC1759. The R_{UR}/R_{THERM} divider trip point of 0.333 • V_{DD} (1V) is well above the 0.047 • V_{DD} (140mV) threshold of a system using a 10k pull-up. A system using a 10k pull-up would not be able to resolve the important underrange to hot transition point with a modest 100mV of ground offset between battery and thermistor detection circuitry. Such offsets are anticipated when charging at normal current levels.

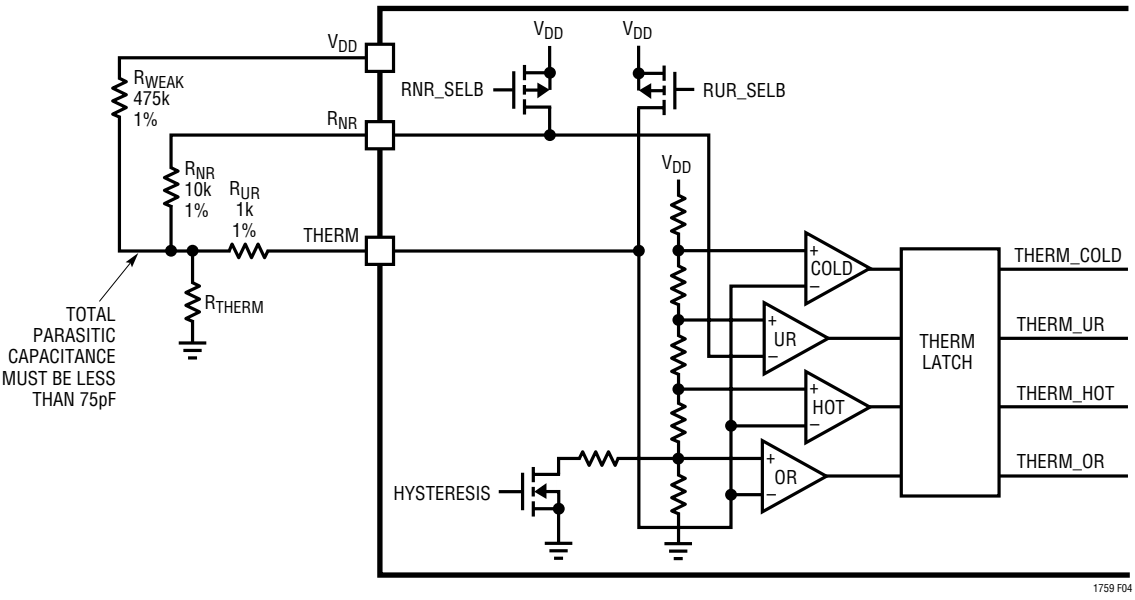


Figure 4. Thermistor Decoder Block

OPERATION

When AC power is not available the thermistor block supports the following low power operating features:

1. Only the low power THERM_OR detection circuitry is kept alive to support battery present interrupts.
2. The ChargeStatus() read function forces the thermistor block to update thermistor status at the beginning of the read. The low power mode is immediately reentered upon completion of the read.

The thermistor impedance is interpreted according to Table 4.

Table 4. Thermistor State Ranges

THERMISTOR RESISTANCE	CHARGE STATUS BITS	DESCRIPTION
0Ω to 500Ω	THERM_UR, THERM_HOT BATTERY_PRESENT	Underrange
500Ω to 3kΩ	THERM_HOT BATTERY_PRESENT	Hot
3kΩ to 30kΩ	(NONE) BATTERY_PRESENT	Ideal
30kΩ to 100kΩ	THERM_COLD BATTERY_PRESENT	Cold
Above 100kΩ	THERM_OR THERM_COLD	Overrange

The required values for R_{WEAK}, R_{UR} and R_{NR} are shown in Table 5.

Table 5. Thermistor External Resistor Values

EXTERNAL RESISTOR	VALUE (Ω)
R_{WEAK}	475k ±1%
R_{UR}	1k ±1%
R_{NR}	10k ±1%

Note: The maximum allowed total external capacitance on THERM and RNR is 75pF, due to settling time requirements.

The I_{LIMIT} Decoder Block

The value of an external resistor connected from this pin to GND determines one of four current limits that are used to limit the maximum charging current value. These limits provide a measure of safety with a hardware restriction on charging current which cannot be overridden by software.

Table 6. I_{LIMIT} Trip Points and Ranges

EXTERNAL RESISTOR (R_{ILIMIT})	I_{LIMIT} VOLTAGE	NOMINAL CHARGING CURRENT RANGE	GRANULARITY
0	$V_{ILIMIT} < 0.09V_{DD}$	0 < I < 1023mA	1mA
10k ±1%	$0.17V_{VDD} < V_{ILIMIT} < 0.34V_{VDD}$	0 < I < 2046mA	2mA
33k ±1%	$0.42V_{VDD} < V_{ILIMIT} < 0.59V$	0 < I < 4092mA	4mA
Open (>250k, or Short to V_{DD})	$0.66V_{VDD} < V_{ILIMIT}$	0 < I < 8184mA	8mA

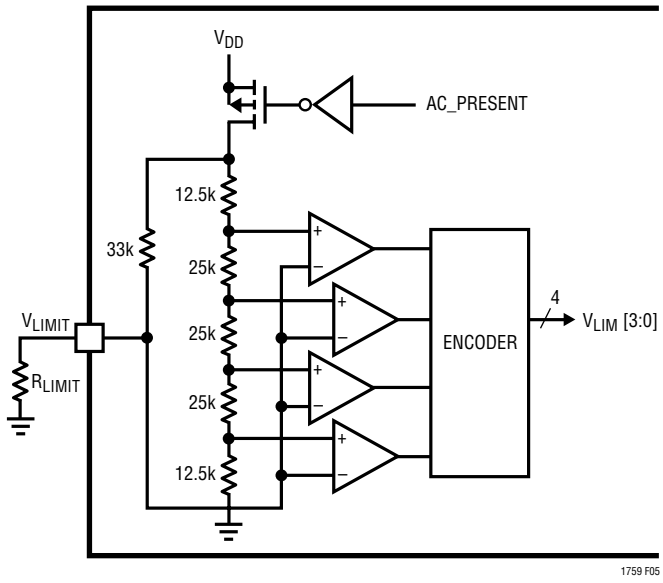


Figure 5. Simplified V_{LIMIT} Circuit Concept (I_{LIMIT} Is Similar)

The V_{LIMIT} Decoder Block

The value of an external resistor connected from this pin to GND determines one of five voltage limits that are applied to the charger output value. These limits provide a measure of safety with a hardware restriction on charging voltage which cannot be overridden by software.

OPERATION

Table 7. V_{LIMIT} Trip Points and Ranges

EXTERNAL RESISTOR (R_{VLIMIT})	V_{LIMIT} VOLTAGE	NOMINAL CHARGING VOLTAGE (V_{OUT}) RANGE	GRANULARITY
0	$V_{VLIMIT} < 0.09V_{VCCP}$	2465mV < V_{OUT} < 8432mV	16mV
10k ±1%	$0.17V_{VDD} < V_{VLIMIT} < 0.34V_{VDD}$	2465mV < V_{OUT} < 12640mV	16mV
33k ±1%	$0.42V_{VCCP} < V_{VLIMIT} < 0.59V_{VDD}$	2465mV < V_{OUT} < 16864mV	32mV
100k ±1%	$0.66V_{VDD} < V_{VLIMIT} < 0.84V_{VDD}$	2465mV < V_{OUT} < 21056mV	32mV
Open or Tied to V_{DD}	$0.91V_{VDD} < V_{VLIMIT}$	2465mV < V_{OUT} < 32768mV	32mV

The Voltage DAC Block

Note that the charge output voltage is offset by V_{REF}. Therefore, the value of V_{REF} is subtracted from the SMBus ChargingVoltage() value in order for the output voltage to be programmed properly (without offset). If the ChargingVoltage() value is below the nominal reference voltage of the charger, nominally 2.465V, the charger output voltage is programmed to zero. In addition, if the ChargingVoltage() value is above the limit set by the V_{LIMIT} pin, then the charger output voltage is set to the value determined by the V_{LIMIT} resistor and the VOLTAGE_OR bit is set. These limits are demonstrated in Figure 6.

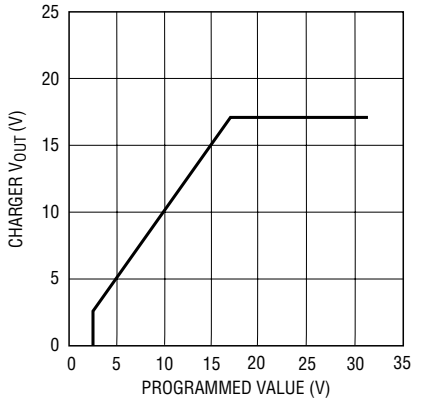


Figure 6. Transfer Function of Charger

The Current DAC Block

The current DAC is a delta-sigma modulator which controls the effective value of an external resistor, R_{SET}, used to set the current limit of the charger. Figure 7 is a simplified diagram of the DAC operation. The delta-sigma modulator and switch convert the ChargingCurrent() value, received via the SMBus, to a variable resistance equal to:

$$1.25R_{SET}/ChargingCurrent()/I_{LIMIT[x]})$$

Therefore, programmed current is equal to:

$$0.8V_{REF}/R_{SET}\ (ChargingCurrent()/I_{LIMIT}[x]),$$
$$\text{for } ChargingCurrent() < I_{LIMIT[x]}.$$

When a value less than 1/16th of the maximum current allowed by I_{LIMIT} is applied to the current DAC input, the current DAC enters a different mode of operation. The current DAC output is pulse width modulated with a high

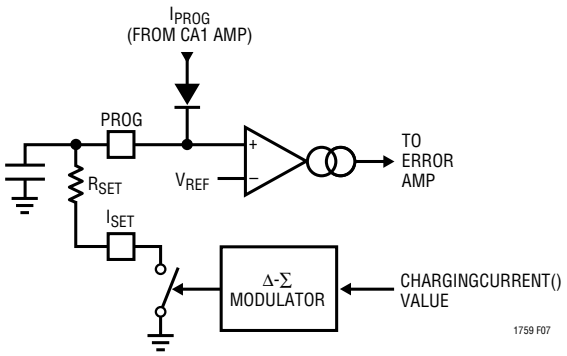


Figure 7. Current DAC Operation

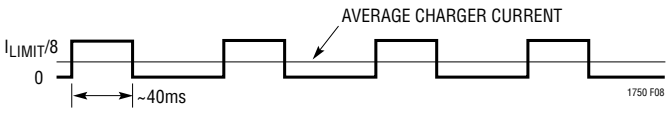


Figure 8. Charging Current Waveform in Low Current Mode

frequency clock having a duty cycle value of 1/8. Therefore, the maximum output current provided by the charger is $I_{MAX}/8$. The delta-sigma output gates this low duty cycle signal on and off. The delta-sigma shift registers are then clocked at a slower rate, about 45ms/bit, so that the charger has time to settle to the $I_{MAX}/8$ value. The resulting average charging current is equal to that requested by the ChargingCurrent() value.

OPERATION

When wake-up is asserted to the current DAC block, the delta-sigma is then fixed at a value equal to 80mA, independent of the I_{LIMIT} setting.

Note:

The external resistor connected to the I_{SET} pin must be multiplied by 0.8 to compensate for the 80% maximum duty cycle of the sigma-delta modulator. Note also that the 80% duty cycle converts the rise/fall time mismatches to a small gain error, rather than a nonlinearity. The parasitic capacitance at the I_{SET} pin should be minimized to keep these errors small.

The Battery Monitor Block (PWR_FAIL)

Two internal resistor dividers compare the BAT2 terminal to the DCIN terminal. When BAT2 is above 89% of the voltage at DCIN the PWR_FAIL bit is set to 1. A small amount of proportional hysteresis, ~2%, is used for noise immunity. The PWR_FAIL bit is set low if AC_PRESENT is low.

APPLICATIONS INFORMATION

Adapter Limiting

An important feature of the LTC1759 is the ability to automatically adjust charging current to a level which avoids overloading the wall adapter. This allows the product to operate at the same time that batteries are being charged without complex load management algorithms. Additionally, batteries will automatically be charged at the maximum possible rate of which the adapter is capable.

This feature is created by sensing total adapter output current and adjusting charging current downward if a preset adapter current limit is exceeded. True analog control is used, with closed loop feedback ensuring that adapter load current remains within limits. Amplifier CL1 in Figure 9 senses the voltage across R_{S4}, connected between the CLP and CLN pins. When this voltage exceeds 92mV, the amplifier will override programmed charging current to limit adapter current to $92mV/R_{S4}$. A lowpass filter formed by 500Ω and 1µF is required to eliminate switching noise. If the current limit is not used, both CLP and CLN pins should be connected to V_{CC}.

Setting Input Current Limit

To set the input current limit, you need to know the minimum wall adapter current rating. Subtract 5% for the input current limit tolerance and use that current to determine the resistor value.

$R_{S4} = 92mV/I_{LIMIT}$

I_{LIMIT} =

Adapter Min Current – (Adapter Min Current • 5%)

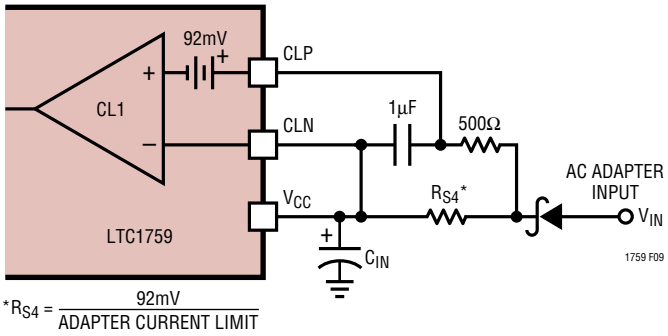


Figure 9. Adapter Current Limiting

Table 7. Common R_{S4} Resistor Values

ADAPTER RATING (A)	R_{S4} VALUE* (Ω) 1%	R_{S4} POWER DISSIPATION (W)	R_{S4} POWER RATING (W)
1.5	0.06	0.135	0.25
1.8	0.05	0.162	0.25
2	0.045	0.18	0.25
2.3	0.039	0.206	0.25
2.5	0.036	0.225	0.5
2.7	0.033	0.241	0.5
3	0.03	0.27	0.5

* Values shown above are rounded to nearest standard value.

As is often the case, the wall adapter will usually have at least a +10% current limit margin and many times one can simply set the adapter current limit value to the actual adapter rating (see Table 7).

APPLICATIONS INFORMATION

Charge Termination Issues

Batteries with constant current charging and voltage-based charger termination might experience problems with reductions of charger current caused by adapter limiting. It is recommended that input limiting feature be defeated in such cases. Consult the battery manufacturer for information on how your battery terminates charging.

Setting Output Current Limit (Refer to Figure 10)

The LTC1759 current DAC and the PWM analog circuitry must coordinate the setting of the charger current. Failure to do so will result in incorrect charge currents.

Table 8. Recommended Resistor Values

I_{MAX} (A)	R_{SENSE} (Ω) 1%	R_{SENSE} (W)	$R_{S1} = R_{S2}$ (Ω) 1%	R_{SET} (Ω) 1%	R_{ILIMIT} (Ω) 1%
1.023	0.100	0.25	200	3.83k	0
2.046	0.05	0.25	200	3.83k	10k
4.092	0.025	0.5	200	3.83k	33k
8.184	0.012	1	200	4.02k	Open

Warning

DO NOT CHANGE THE VALUE OF R_{ILIMIT} DURING OPERATION. The value must remain fixed and track the R_{SENSE} and R_{SET} values at all times. Changing the current setting can result in currents that greatly exceed the requested value and potentially damage the battery or overload the wall adapter if no input current limiting is provided.

Example Calculations

Setting up the output current to the desired value involves calculating these values:

1. R_{SENSE}: This resistor is the current sense resistor on the charger output.
2. R_{SET}: This resistor sets the current DAC output programming current scale.
3. R_{ILIMIT}: This resistor programs the full-scale value of the current DAC (I_{MAX}).

The value of R_{SENSE} and R_{SET} are directly related to each other based on the values chosen for R_{S1} and R_{S2}. To prevent current sense op amp input bias errors, the value of R_{S1} and R_{S2} are kept the same, about 200Ω. R_{SET} is used to scale the PROG pin current relative to the R_{SENSE} voltage drop to set the maximum current value.

The following example is for a 4A design.

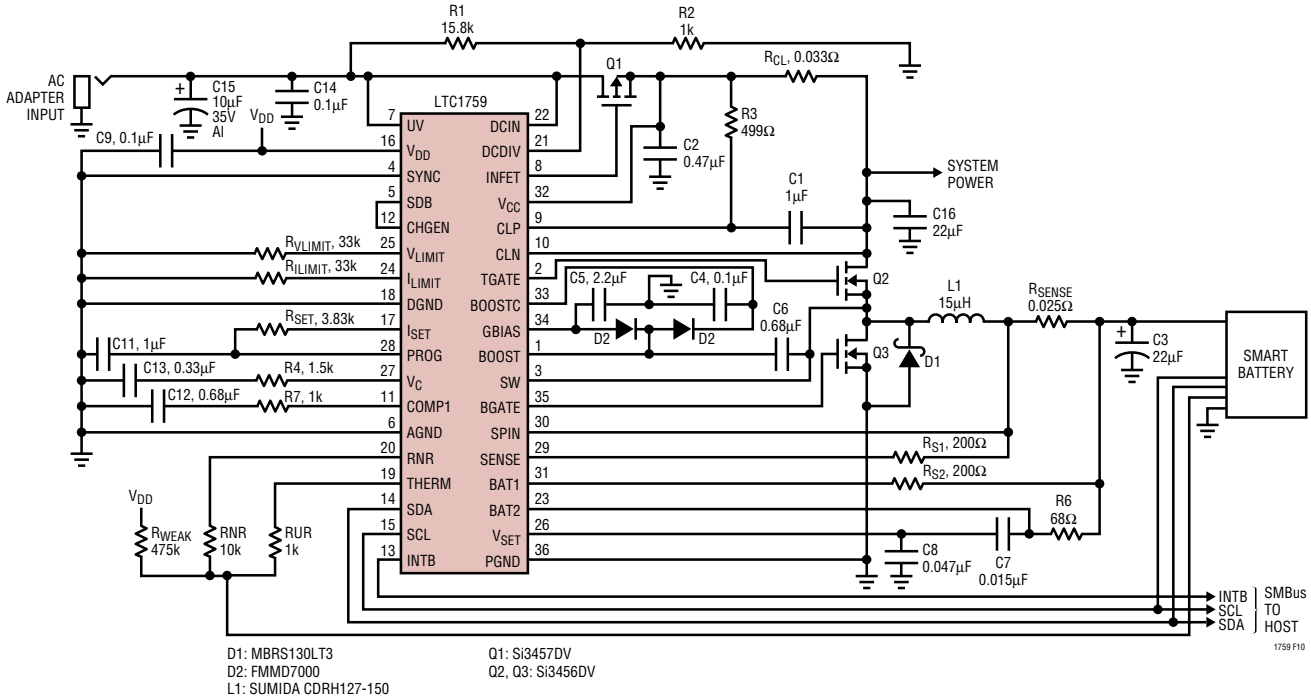


Figure 10. 4A SMBus Smart Battery Charger

APPLICATIONS INFORMATION

Step 1: Determine R_{SENSE}. Using your chosen I_{MAX} for your maximum charge current, calculate the sense resistor value and round to the nearest standard value. Any rounding error is made up by the R_{SET} resistor calculation. The value of the V_{SENSE} voltage is user-definable. A good trade-off between minimize power dissipation in the current sense resistor and maintaining good current scale accuracy is to use V_{SENSE} = 100mV for full-scale current.

$R_{SENSE} = V_{SENSE}/I_{MAX}$
$R_{SENSE} = 0.1V/4.092A = 0.024\Omega$
Use $R_{SENSE} = 0.025\Omega$

Step 2: Determine the value of R_{SET}. V_{REF} is 2.465V. Round R_{SET} to the nearest standard value.

$R_{SET} = V_{REF}/(1.25 \bullet I_{MAX}) \bullet R_{S1}/R_{SENSE}$
$R_{SET} = 2.465/(1.25 \bullet 4.092) \bullet 200/0.025 = 3.855k$
Use $R_{SET} = 3.83k\Omega$

Step 3: Determine the value of R_{ILIMIT}. This is simply a lookup function based on your I_{MAX} value. See the Electrical Characteristics table for allowable R_{ILIMIT} values. Refer to Table 8 per recommended resistor values.

Inductor Selection

Higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition, the effect of inductor value on ripple current and low current operation must also be considered. The inductor ripple current ΔI_L decreases with higher frequency and increases with higher V_{IN}.

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{MAX})$. Remember the maximum ΔI_L occurs at the maximum input voltage. The inductor value also has an effect on low current operation. The transition to low current operation begins when the inductor current reaches zero while the bottom MOSFET is on. Lower inductor values (higher ΔI_L) will cause this to occur at higher load currents, which can cause a dip in efficiency in the upper range of low current operation. In practice 15µH is the lowest value recommended for use.

Calculating IC Power Dissipation

The power dissipation of the LTC1759 is dependent upon the gate charge of Q2 and Q3. The gate charge is determined from the manufacturer's data sheet and is dependent upon both the gate voltage swing and the drain voltage swing of the FET.

$$P_D = (V_{VCC} - V_{GBIAS})[f_{PWM}(Q_{G2} + Q_{G3})] + V_{VCC} \bullet I_{VCC}$$

Example: V_{VCC} = 18V, V_{GBIAS} = 9.1V, f_{PWM} = 230kHz, $Q_{G2} = Q_{G3}$ = 20nC, I_{VCC} = 20mA.

$P_D = (18V - 9.1V)(230kHz \bullet 40nC) + 18V \bullet 20mA = 441mW$

Soft Start and Undervoltage Lockout

The LTC1759 is soft started by the 0.33µF capacitor on the V_C pin. On start-up, V_C pin voltage will rise quickly to 0.5V, then ramp up at a rate set by the internal 45µA pull-up current and the external capacitor. Battery charging current starts ramping up when V_C voltage reaches 0.7V and full current is achieved with V_C at 1.1V. With a 0.33µF capacitor, time to reach full charge current is about 10ms and it is assumed that input voltage to the charger will reach full value in less than 10ms. The capacitor can be increased up to 1µF if longer input start-up times are needed.

In any switching regulator, conventional timer-based soft starting can be defeated if the input voltage rises much slower than the time out period. This happens because the switching regulators in the battery charger and the computer power supply are typically supplying a fixed amount of power to the load. If input voltage comes up slowly compared to the soft start time, the regulators will try to deliver full power to the load when the input voltage is still well below its final value. If the adapter is current limited, it cannot deliver full power at reduced output voltages and the possibility exists for a quasi "latch" state where the adapter output stays in a current limited state at reduced output voltage. For instance, if maximum charger plus computer load power is 30W, a 15V adapter might be current limited at 2.5A. If adapter voltage is less than (30W/2.5A = 12V) when full power is drawn, the adapter

APPLICATIONS INFORMATION

voltage will be pulled down by the constant 30W load until it reaches a lower stable state where the switching regulators can no longer supply full load. This situation can be prevented by utilizing the DCDIV resistor divider, set higher than the minimum adapter voltage where full power can be achieved.

Input and Output Capacitors

In the 4A Lithium Battery Charger (Figure 10), the input capacitor (C14) is assumed to absorb all input switching ripple current in the converter, so it must have adequate ripple current rating. Worst-case RMS ripple current will be equal to one half of output charging current. Actual capacitance value is not critical. Solid tantalum low ESR capacitors have high ripple current rating in a relatively small surface mount package, *but caution must be used when tantalum capacitors are used for input or output bypass*. High input surge currents can be created when the adapter is hot-plugged to the charger or when a battery is connected to the charger. Solid tantalum capacitors have a known failure mechanism when subjected to very high turn-on surge currents. Only Kemet T495 series of "Surge Robust" low ESR tantalums are rated for high surge conditions such as battery to ground.

The relatively high ESR of an aluminum electrolytic for C15, located at the AC adapter input terminal, is helpful in reducing ringing during the hot-plug event.

Highest possible voltage rating on the capacitor will minimize problems. Consult with the manufacturer before use. Alternatives include new high capacity ceramic (at least 20µF) from Tokin, United Chemi-Con/Marcon, et al. However, using ceramic capacitors in the output filter of the charger can lead to acoustic noise radiation that can be confused with instability. At low charge currents, the charger operates in discontinuous current mode at an audible frequency. Other alternative capacitors include OSCON capacitors from Sanyo.

The output capacitor (C3) is also assumed to absorb output switching current ripple. The general formula for capacitor current is:

$$I_{RMS} = \frac{0.29\ (V_{BAT})\left(1 - \frac{V_{BAT}}{V_{CC}}\right)}{(L1)(f)}$$

For example, V_{CC} = 19V, V_{BAT} = 12.6V, L1 = 10µH, and f = 200kHz, I_{RMS} = 0.6A.

EMI considerations usually make it desirable to minimize ripple current in the battery leads, and beads or inductors may be added to increase battery impedance at the 200kHz switching frequency. Switching ripple current splits between the battery and the output capacitor depending on the ESR of the output capacitor and the battery impedance. If the ESR of C3 is 0.2Ω and the battery impedance is raised to 4Ω with a bead or inductor, only 5% of the current ripple will flow in the battery.

Charger Crowbar Protection

If V_{IN} connector of Figure 1 charger can be instantaneously shorted (crowbarred) to ground, then a small P-channel FET M4 should be used to fast turn off the input P-channel FET M3 (see Figure 11), otherwise, high surge current might damage M3. M3 can also be replaced by a diode if dropout voltage and heat dissipation are not problems.

Note that LT1759 will operate even when V_{BAT} is grounded. If V_{BAT} of Figure 1 charger gets shorted to ground very quickly (crowbarred) from a high battery voltage, slow loop response may allow charge current to build up and damage the topside N-channel FET M1. A small diode D5 (see Figure 12) from SDB pin to V_{BAT} will shut down switching and protect the charger.

Note that M4 and/or D5 are needed only if the charger system can be potentially crowbarred.

Protecting SMBus Inputs

The SMBus inputs, SCL and SDA, are exposed to uncontrolled transient signals whenever a battery is connected to the system. If the battery contains a static charge, the SMBus inputs are subjected to ESD which can cause damage after repeated exposure. Also, if the battery's positive terminal makes contact to the connector before the negative terminal, the SMBus inputs can be forced

APPLICATIONS INFORMATION

below ground with the full battery potential, causing a potential for latch-up in any of the devices connected to the SMBus inputs. Therefore it is good design practice to protect the SMBus inputs as shown in Figure 13.

PCB Layout Considerations

The LTC1759 has two layout critical areas. The first is the I_{SET} pin and the second is the DC/DC converter switching circuity.

I_{SET} Pin Layout: The LTC1759 I_{SET} pin lead length is critical and should be kept to a minimum to reduce parasitic capacitance. Any parasitic capacitance on this node will cause errors in the programmed current values. Place R_{SET} resistor directly next to the I_{SET} pad. The trace from R_{SET} to the LTC1759 PROG pin pad is not critical.

DC/DC PCB Layout Hints: For maximum efficiency, the switch node rise and fall time is kept as short as possible. To prevent magnetic and electrical field radiation and high frequency resonant problems, proper layout of the components connected to the IC is essential, especially the power paths (primary and secondary).

1. Keep the highest frequency loop path as small and tight as possible. This includes the bypass capacitors, with the higher frequency capacitors being closer to the noise source than the lower frequency capacitors. The highest frequency power path loop has the highest layout priority. For best results, avoid using vias in this loop and keep the entire high frequency loop on a single external PCB layer. If you must, use multiple vias to keep the impedance down (see Figure 15).
2. Run long power traces in parallel. Best results are achieved if you run each trace on separate PCB layer one on top of the other for maximum capacitance coupling and common mode noise rejection.
3. If possible, use a ground plane under the switcher circuitry to minimize capacitive interplane noise coupling.
4. Keep signal or analog ground separate. Tie this analog ground back to the power supply at the output ground using a single point connection.
5. For best current programming accuracy provide a Kelvin connection from R_{SENSE} to R_{S1} and R_{S2}. See Figure 14 as an example.

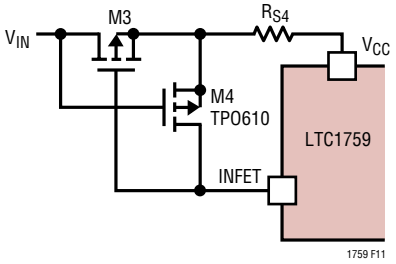


Figure 11. V_{IN} Crowbar Protection

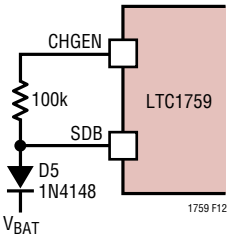


Figure 12. V_{BAT} Crowbar Protection

Interfacing with a Selector

The LTC1759 is designed to be used with a true analog multiplexer for the thermistor sensing path. Some selector ICs from various manufacturers may not implement this. Consult LTC applications department for more information.

Electronic Loads

The LTC1759 is designed to work with a real battery. Electronic loads will create instability within the LTC1759 preventing accurate programming currents and voltages. Consult LTC applications department for more information.

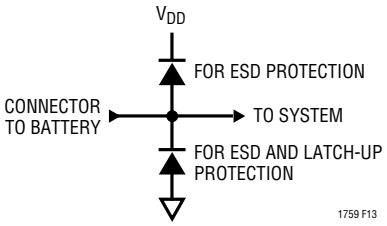


Figure 13

APPLICATIONS INFORMATION

Charging Indication

When a CHARGECURRENT() command with a value of zero is sent to the LTC1759, current stops flowing into the battery. However, the command does not cause the CHGEN pin to pull low. This prevents use of the CHGEN pin as a charge termination indication. Figure 16 shows a circuit that reliably indicates when the battery is receiving a charge current.

The circuit shown, except for the optional 555 timer IC, filters out the I_{SET} DAC 80kHz output into a smooth signal. Q1 and R5 partially isolate the capacitance of C1 from effecting the I_{SET} pin of the LTC1759. Q1 is configured as a crude voltage level detector looking for voltage going below approximately one volt on the emitter. The RC circuit consisting of R4 and C1 filters low pulses from the I_{SET} pin. Q2 buffers the RC filter circuit allowing a more logic level type interface. The circuit is powered from the logic output driver of the CHGEN pin of the LTC1759. The circuit does not need any capacitive supply bypassing to function and draws little current. When the CHGEN pin goes low, the current consumption of the circuit is eliminated. Note that some resistor values must change depending on the supply voltage connected to the V_{DD} pin of the LTC1759. An optional low power 555 timer can be added to to give a blinking LED charge indication.

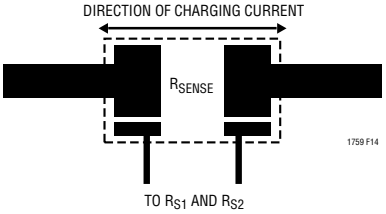


Figure 14. Kelvin Sensing of Charging Current

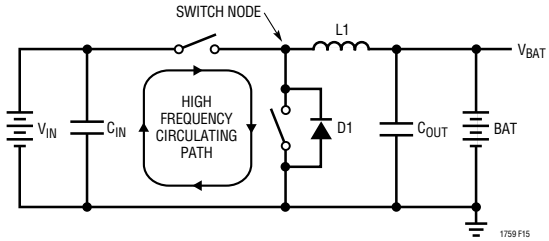


Figure 15. High Speed Switching Path

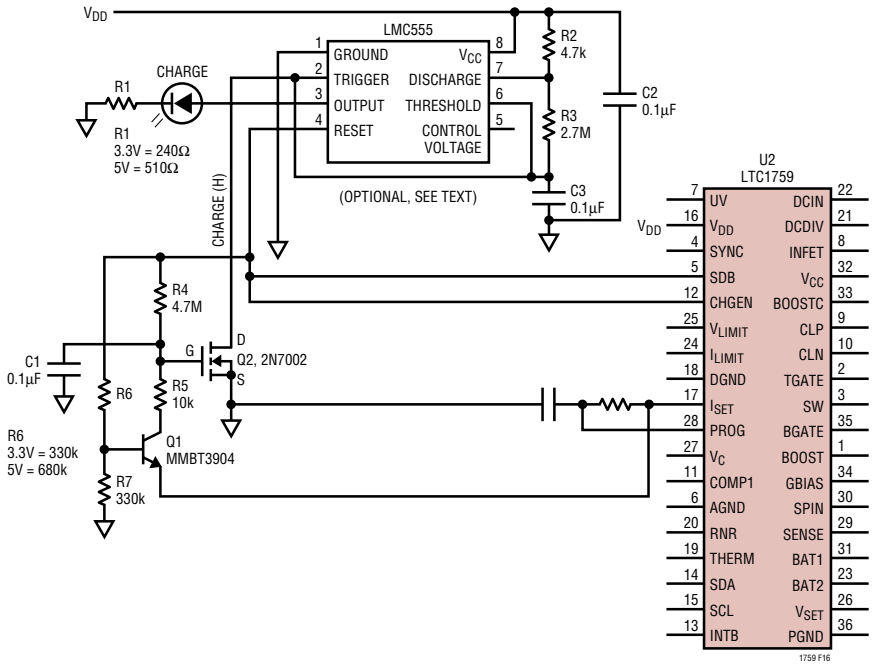
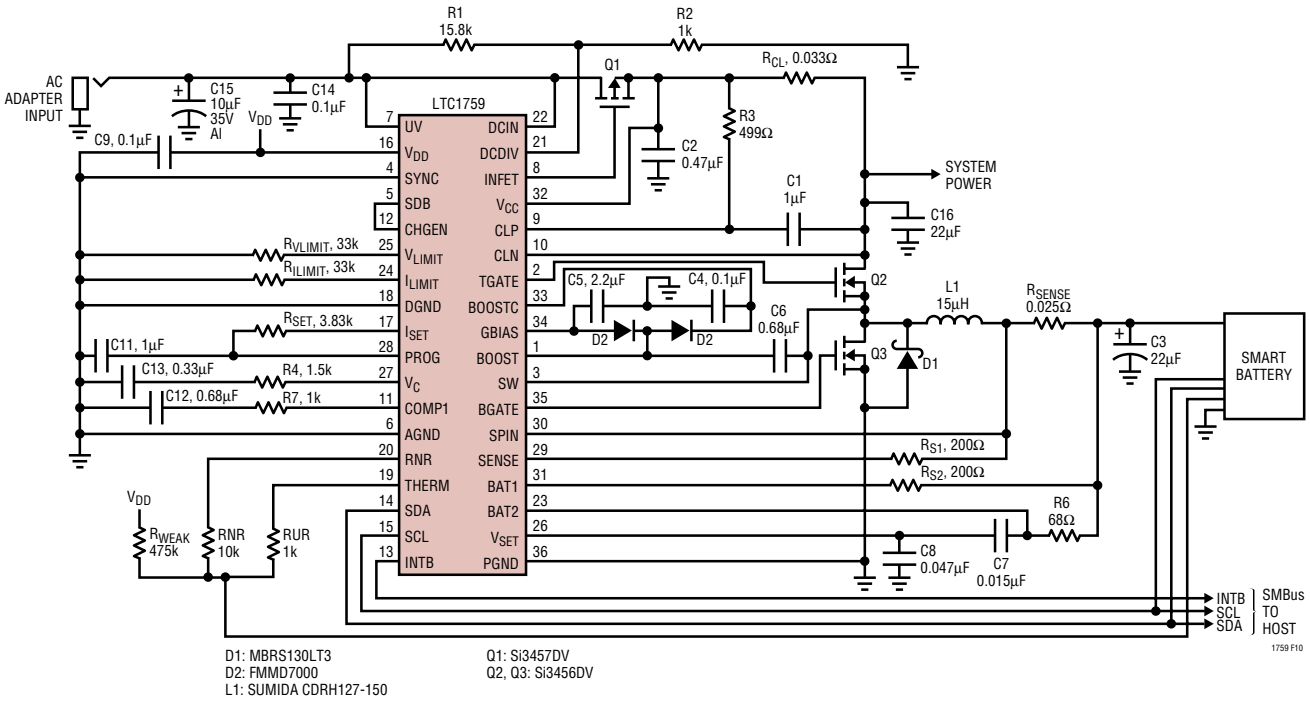


Figure 16. Battery Charge Indicator Circuit

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TYPICAL APPLICATION

4A SMBus Smart Battery Charger



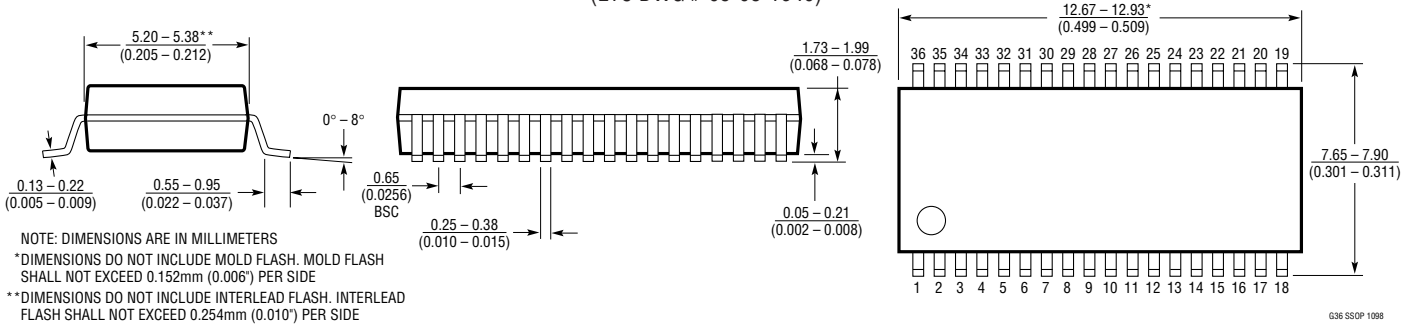
D1: MBRS130LT3
D2: FMMD7000
L1: SUMIDA CDRH127-150

Q1: Si3457DV
Q2, Q3: Si3456DV

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
36-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



NOTE: DIMENSIONS ARE IN MILLIMETERS

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (0.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1473	Dual PowerPath™ Switch Driver	Switches Between Two Voltages
LTC1479	PowerPath Controller for Dual Battery Systems	Switches Two Batteries, AC Adapter and Charger
LT1505	High Efficiency Constant-Current/Constant-Voltage Charger	Up to 97% Efficiency with Input Current Limiting
LT1511	Monolithic 3A Constant-Current/Constant-Voltage Charger	Input Current Limiting; No External MOSFETs
LTC1694	SMBus Accelerator in SOT-23 Package	Improves SMBus Data Integrity
LT1769	Monolithic 2A Constant-Current/Constant-Voltage Charger	Similar to LT1511 but 2A Rating, 28-Pin SSOP Package

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1759fs, sn1759 LTC/TP 0500 4K • PRINTED IN USA
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