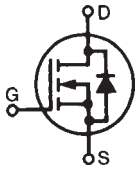
IXYS

PolarHT™ HiPerFET IXFN 140N20P
Power MOSFET

N-Channel Enhancement Mode
Fast Intrinsic Diode

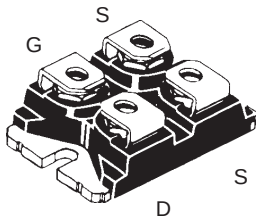


V_{DSS} = 200 V
I_{D25} = 115 A
$R_{DS(on)}$ ≤ 18 mΩ
t_{rr} ≤ 150 ns

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 175°C	200	V
V_{DGR}	T_J = 25°C to 175°C; R_{GS} = 1 MΩ	200	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	115	A
$I_{D(RMS)}$	External lead current limit	100	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	280	A
I_{AR}	T_C = 25°C	60	A
E_{AR}	T_C = 25°C	100	mJ
E_{AS}	T_C = 25°C	4	J
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100 A/μs, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$, R_G = 4 Ω	10	V/ns
P_D	T_C = 25°C	680	W
T_J		-55 ... +175	°C
T_{JM}		175	°C
T_{stg}		-55 ... +150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s	300	°C
V_{ISOL}	50/60 Hz, RMS, 1 minute	2500	V~
M_d	Terminal torque Mounting torque	1.13/10 1.13/10	Nm/lb.in. Nm/lb.in.
Weight		30	g

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0 V, I_D = 250 μA	200			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 4 mA	2.5		5.0	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0			±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0 V T_J = 150°C			25 250	μA μA
$R_{DS(on)}$	V_{GS} = 10 V, I_D = 70 A V_{GS} = 15 V, I_D = 140A Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %		14	18	mΩ mΩ

miniBLOC, SOT-227 B (IXFN)
E153432



G = Gate D = Drain
S = Source

Either source tab S can be used forsource current or Kelvin gate return.

Features

- International standard package
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect
- Fast intrinsic diode

Advantages

- Easy to mount
- Space savings
- High power density

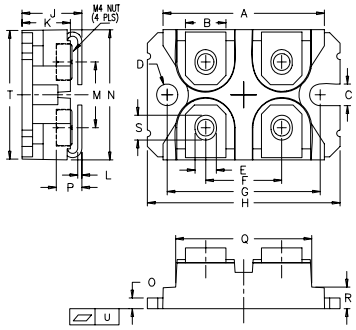
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Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) Min.	Typ.	Max.	
g_{fs}	V_{DS}= 10 V; I_D = 70 A	50	84		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		7500		pF
C_{oss}			1630		pF
C_{rss}			280		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 70 A R_G = 3.3 Ω (External)		30		ns
t_r			35		ns
$t_{d(off)}$			150		ns
t_f			90		ns
$Q_{g(on)}$	V_{GS}= 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 70 A		240		nC
Q_{gs}			50		nC
Q_{gd}			110		nC
R_{thJC}				0.22	K/W
R_{thCS}			0.05		K/W

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) Min.	Typ.	Max.	
I_S	V_{GS} = 0 V			140	A
I_{SM}	Repetitive			280	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %			1.5	V
t_{rr}	I_F = 25 A			200	ns
Q_{RM}	-di/dt = 100 A/µs		0.6		µC
I_{RM}	V_R = 100 V		6		A

SOT-227B miniBLOC



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.240	1.255	31.50	31.88
B	.307	.323	7.80	8.20
C	.161	.169	4.09	4.29
D	.161	.169	4.09	4.29
E	.161	.169	4.09	4.29
F	.587	.595	14.91	15.11
G	1.186	1.193	30.12	30.30
H	1.496	1.505	38.00	38.23
J	.460	.481	11.68	12.22
K	.351	.378	8.92	9.60
L	.030	.033	0.76	0.84
M	.496	.506	12.60	12.85
N	.990	1.001	25.15	25.42
O	.078	.084	1.98	2.13
P	.195	.235	4.95	5.97
Q	1.045	1.059	26.54	26.90
R	.155	.174	3.94	4.42
S	.186	.191	4.72	4.85
T	.968	.987	24.59	25.07
U	-.002	.004	-0.05	0.1

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or moreof the following U.S. patents: 4,835,592 4,850,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405B2 6,710,463 6,727,585 6,759,692 6,771,478 B2

Fig. 1. Output Characteristics @ 25ºC

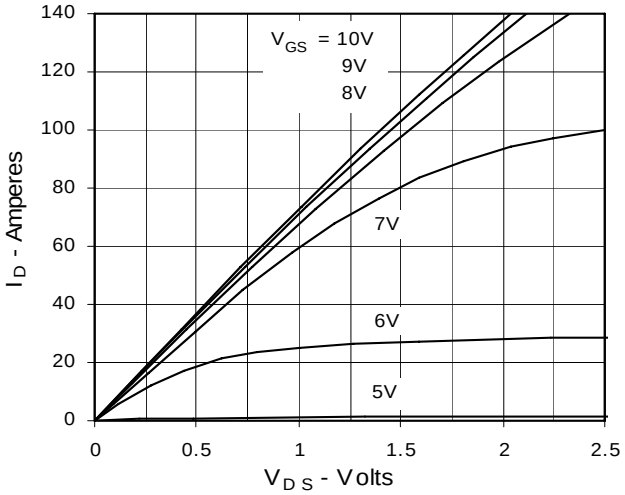


Fig. 2. Extended Output Characteristics @ 25ºC

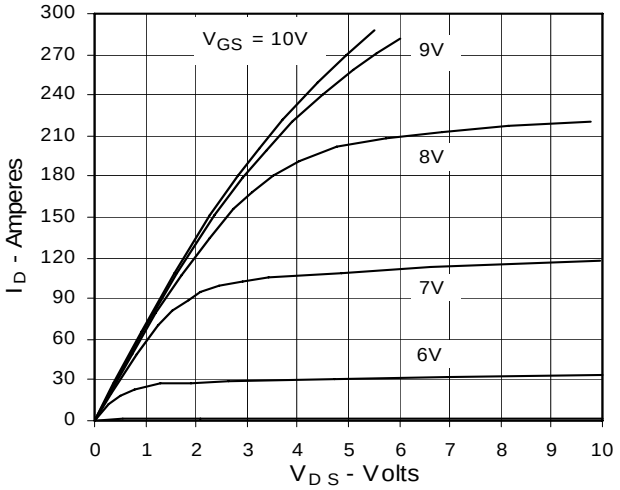


Fig. 3. Output Characteristics @ 150ºC

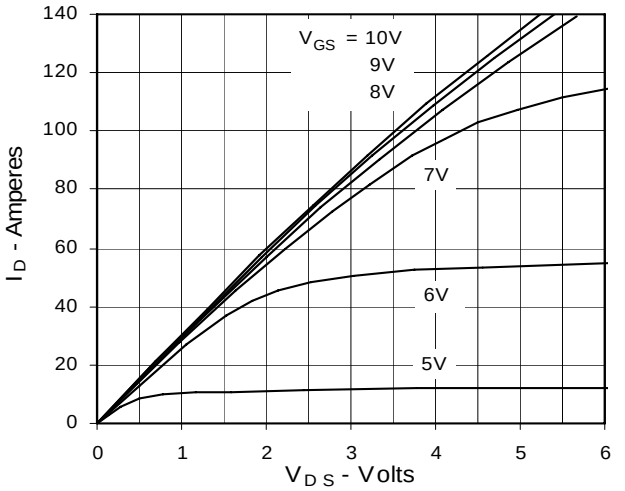


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 70A Value vs. Junction Temperature

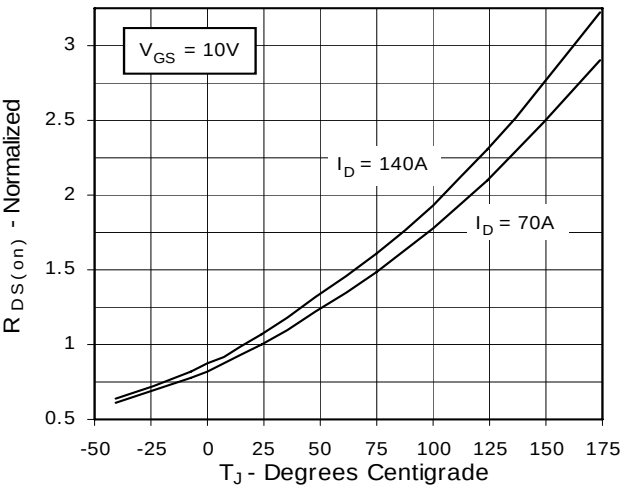


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 70A Value vs. Drain Current

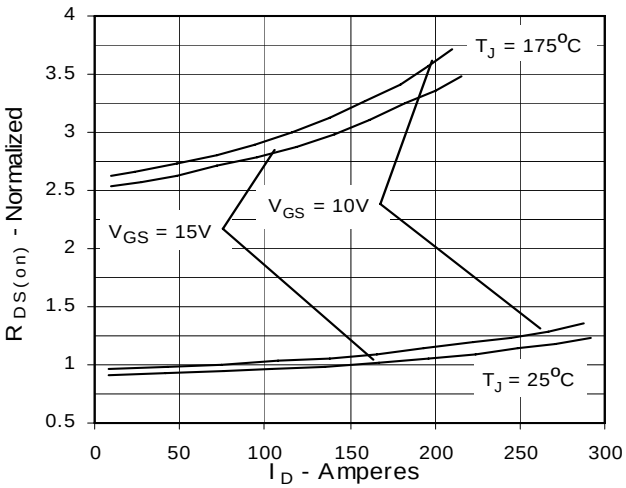
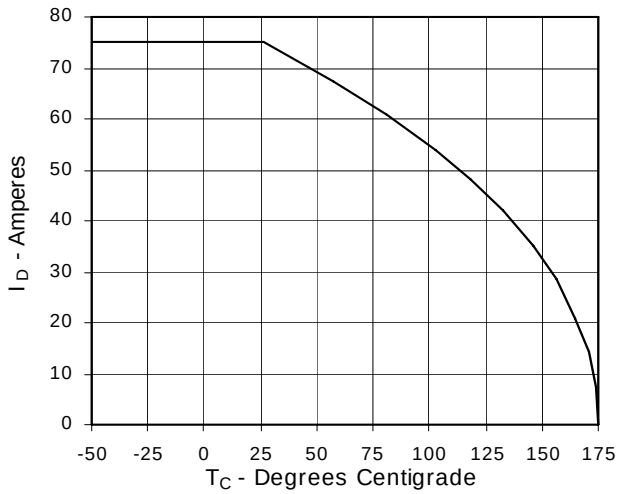


Fig. 6. Drain Current vs. Case Temperature



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Fig. 7. Input Admittance

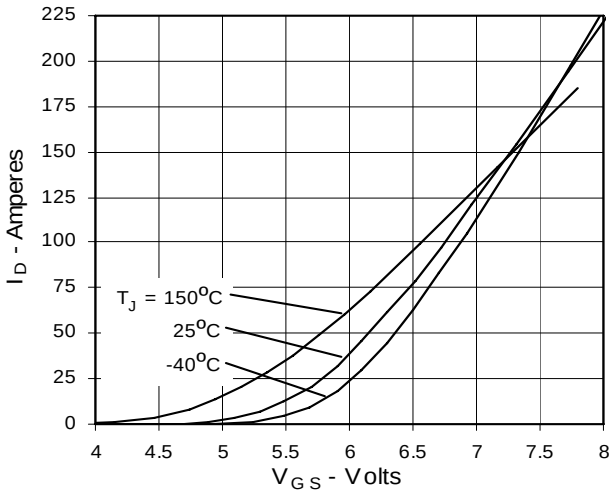


Fig. 8. Transconductance

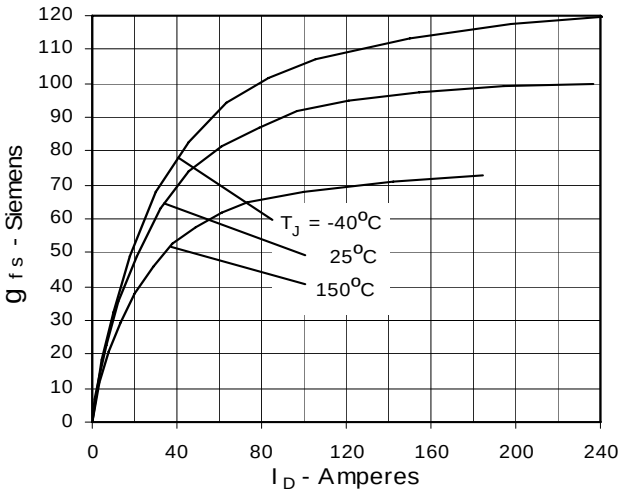


Fig. 9. Source Current vs. Source-To-Drain Voltage

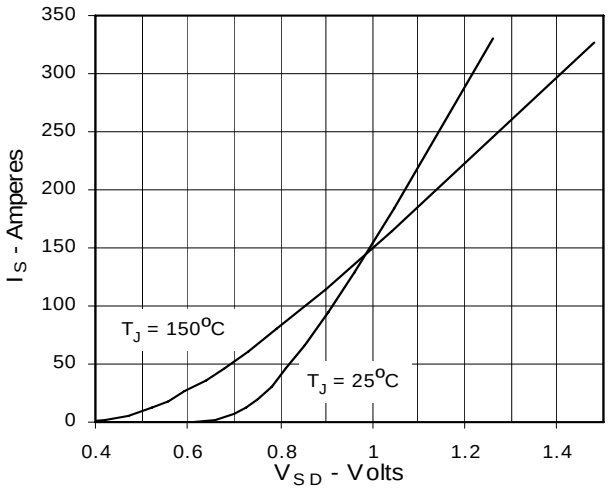


Fig. 10. Gate Charge

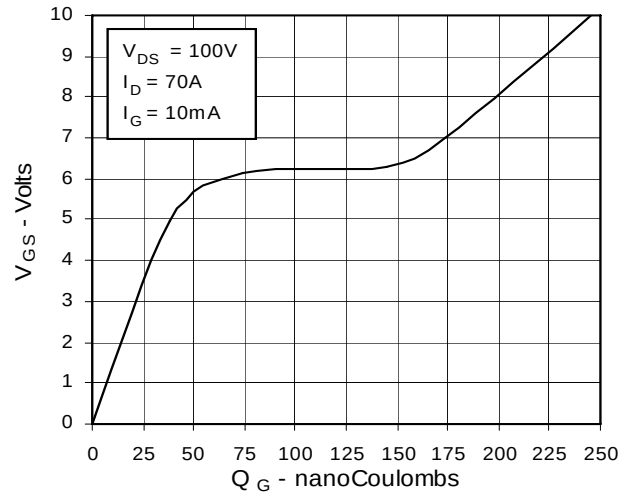


Fig. 11. Capacitance

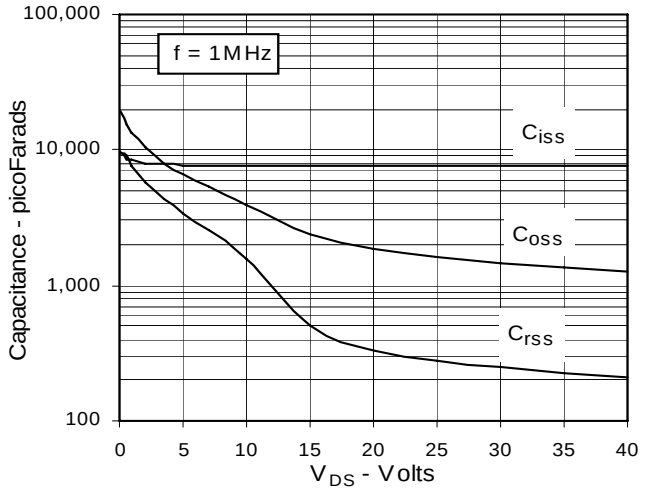
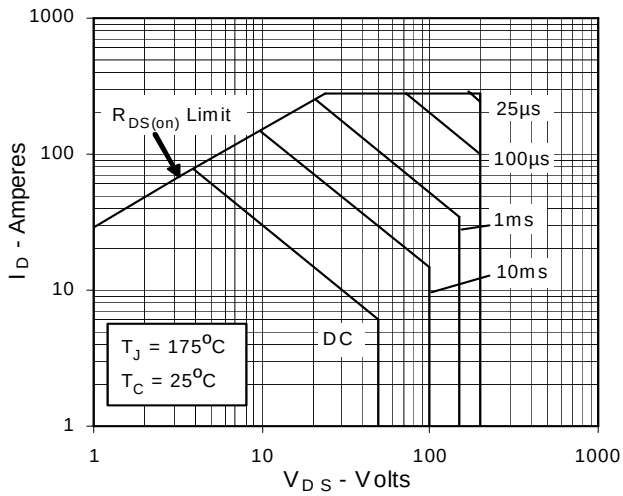
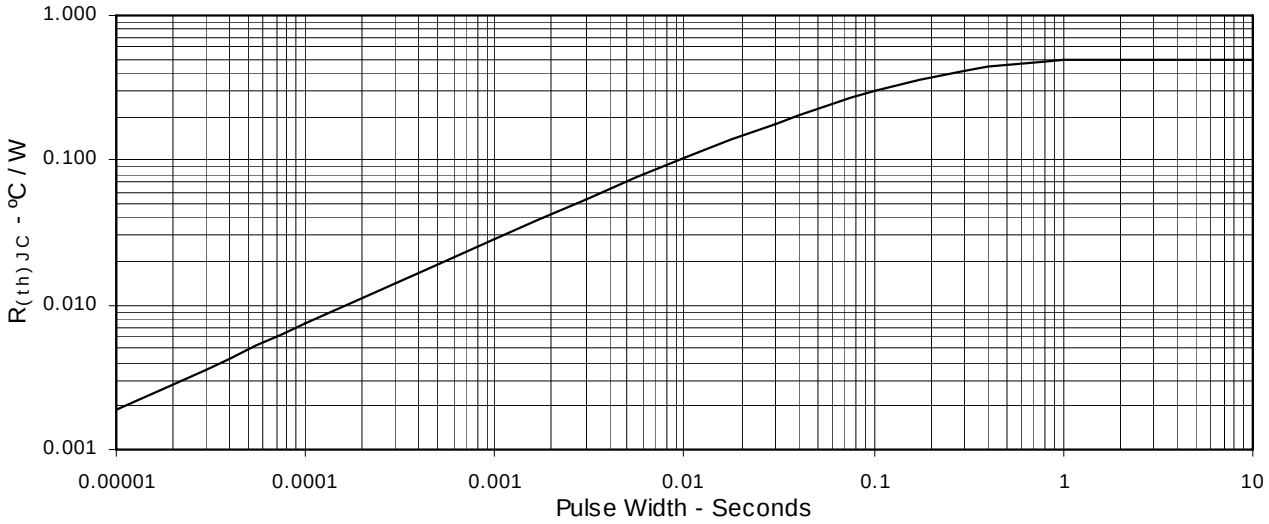


Fig. 12. Forward-Bias Safe Operating Area



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Fig. 13. Maximum Transient Thermal Resistance



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