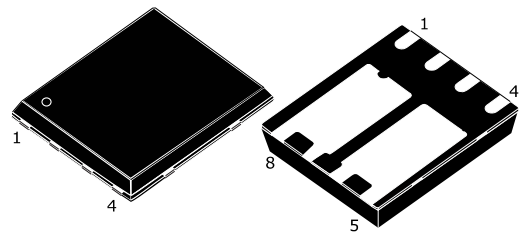
STL66DN3LLH5

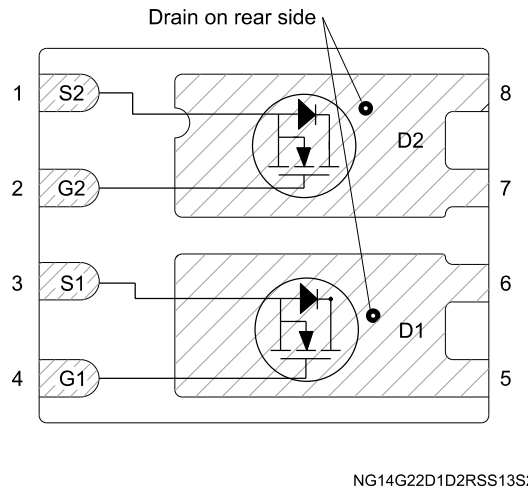
Automotive-grade dual N-channel 30 V, 5.9 mΩ typ., 20 A STripFET™ H5 Power MOSFET in a PowerFLAT™ 5x6 double island package

Datasheet - production data



PowerFLAT™ 5x6 double island

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL66DN3LLH5	30 V	6.5 mΩ	20 A	4.7 W

- Designed for automotive applications and AEC-Q101 qualified
- Logic level $V_{GS(th)}$
- 175 °C maximum junction temperature
- Wettable flanks package

Applications

- Switching applications

Description

This device is a dual N-channel Power MOSFET developed using STMicroelectronics' STripFET™ H5 technology. The device has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

Table 1: Device summary

Order code	Marking	Package	Packing
STL66DN3LLH5	66DN3LH5	PowerFLAT™ 5x6 double island	Tape and reel

This is information on a product in full production.

Contents

1 Electrical ratings 3
2 Electrical characteristics 4
2.1 Electrical characteristics (curves) 6
3 Test circuits 8
4 Package information 9
4.1 PowerFLAT™ 5x6 double island WF type C package information 9
4.2 PowerFLAT™ 5x6 WF packing information 12
5 Revision history 14

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	±22	V
I_D(1)	Drain current (continuous) at T_{case} = 25 °C	78.5	A
	Drain current (continuous) at T_{case} = 100 °C	55.5	
I_D(2)	Drain current (continuous) at T_{pcb} = 25 °C	20	A
	Drain current (continuous) at T_{pcb} = 100 °C	14.2	
I_{DM}(2)(3)	Drain current (pulsed)	80	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	72	W
P_{TOT}(1)	Total dissipation at T_{pcb} = 25 °C	4.7	
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Operating junction temperature		

Notes:

(1) This value is rated according to $R_{thj\text{-}c}$

(2) When mounted on a 1-inch² FR-4, 2 Oz copper board, t < 10 s.

(3) Pulse width is limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.08	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	32	

Notes:

(1) When mounted on a 1-inch² FR-4, 2 Oz copper board, t < 10 s.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AV}	Avalanche current, not repetitive	18.5	A
E_{AS}(1)	Single pulse avalanche energy	270	mJ

Notes:

(1) starting T_j = 25 °C, I_D = 38 A, V_{DD} = 24 V.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 30 V			1	µA
		V_{GS} = 0 V, V_{DS} = 30 V, T_C = 125 °C			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±22 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		3	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 10 A		5.9	6.5	mΩ
		V_{GS} = 4.5 V, I_D = 10 A		7.1	7.9	

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	1500	-	pF
C_{oss}	Output capacitance		-	230	-	
C_{rss}	Reverse transfer capacitance		-	23	-	
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 19 A, V_{GS} = 4.5 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	12	-	nC
Q_{gs}	Gate-source charge		-	5	-	
Q_{gd}	Gate-drain charge		-	4.4	-	

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V, I_D = 9.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*)	-	8.8	-	ns
t_r	Rise time		-	18	-	
$t_{d(off)}$	Turn-off delay time		-	26	-	
t_f	Fall time		-	4	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		20	A
I_{SDM}(1)	Source-drain current (pulsed)		-		80	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 19 A	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 19 A, di/dt = 100 A/µs, V_{DD} = 25 V, T_j = 150 °C (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	24		ns
Q_{rr}	Reverse recovery charge		-	12		nC
I_{RRM}	Reverse recovery current		-	1.8		A

Notes:

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

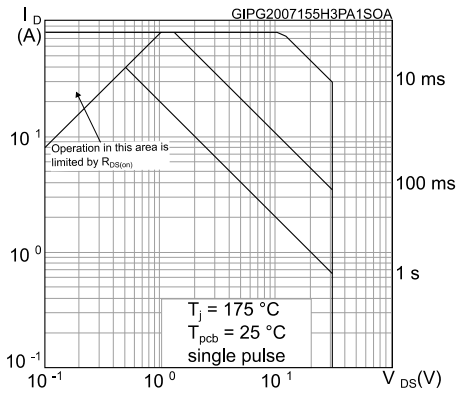


Figure 3: Thermal impedance

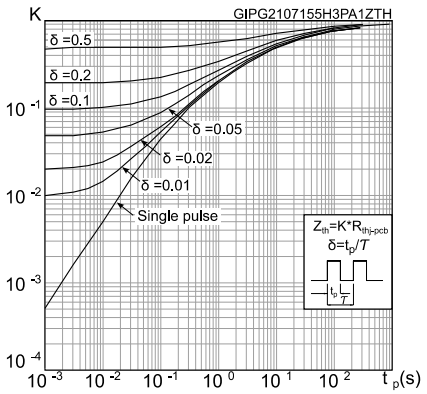


Figure 4: Output characteristics

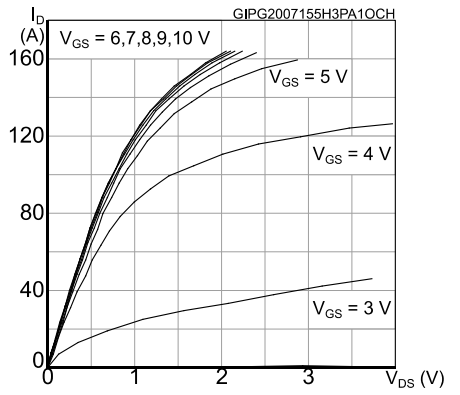


Figure 5: Transfer characteristics

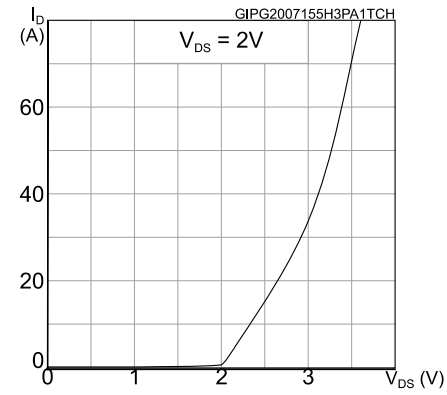


Figure 6: Gate charge vs gate-source voltage

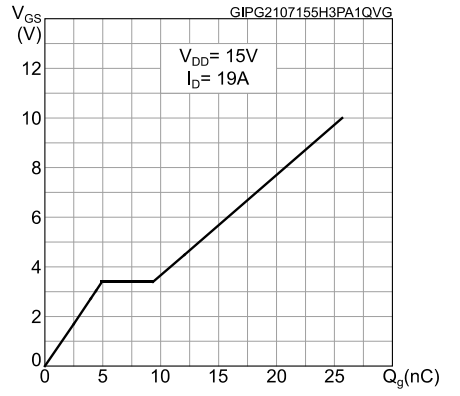


Figure 7: Static drain-source on-resistance

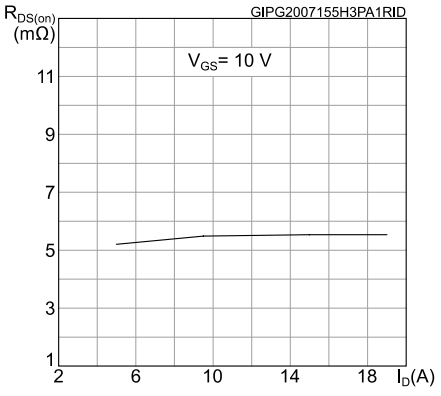


Figure 8: Capacitance variations

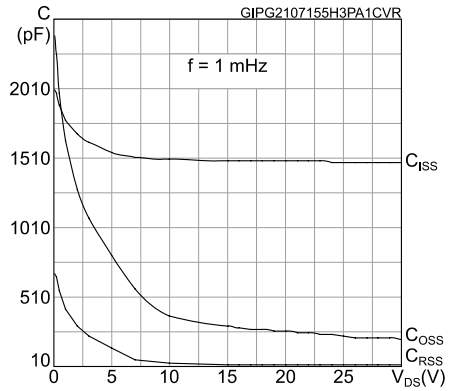


Figure 9: Normalized gate threshold voltage vs temperature

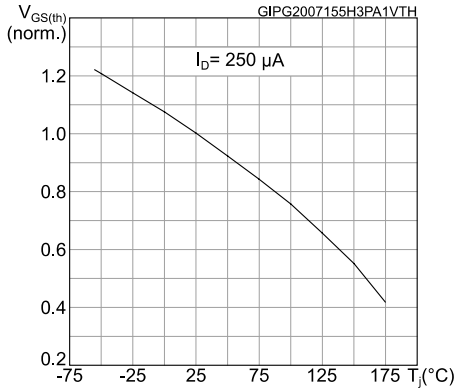


Figure 10: Normalized on-resistance vs temperature

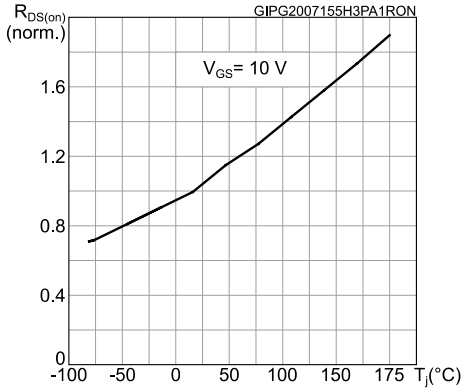


Figure 11: Normalized V(BR)DSS vs temperature

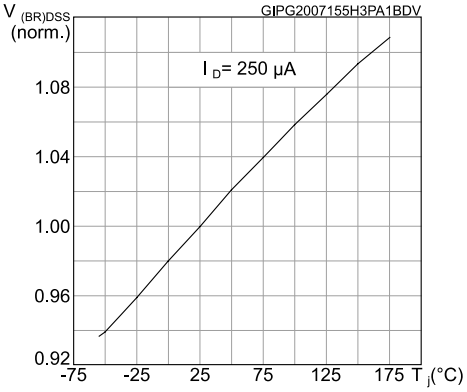
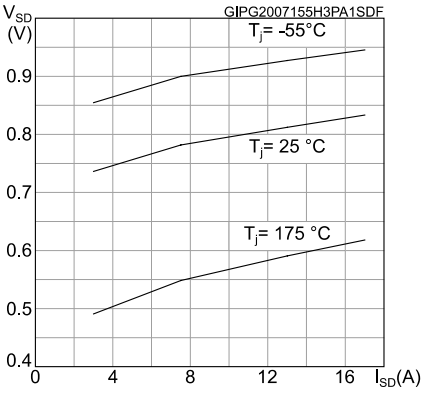


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

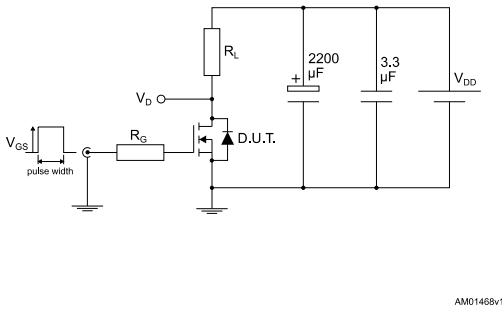


Figure 14: Test circuit for gate charge behavior

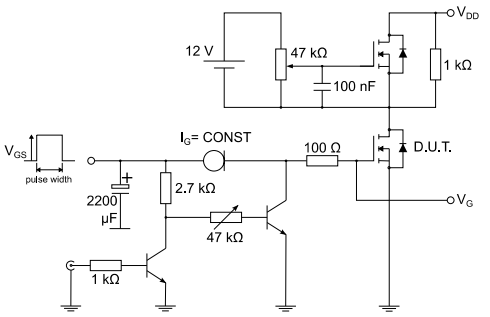


Figure 15: Test circuit for inductive load switching and diode recovery times

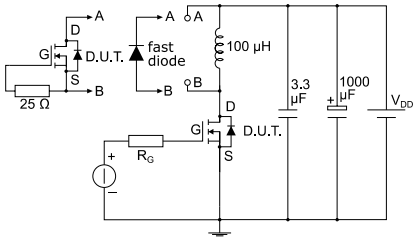


Figure 16: Unclamped inductive load test circuit

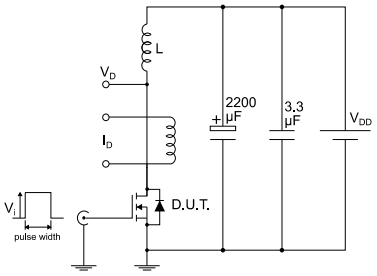


Figure 17: Unclamped inductive waveform

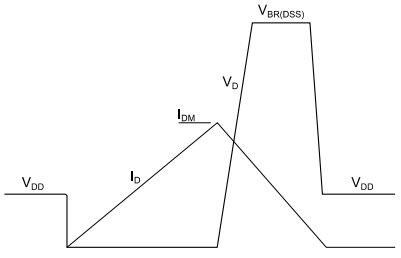
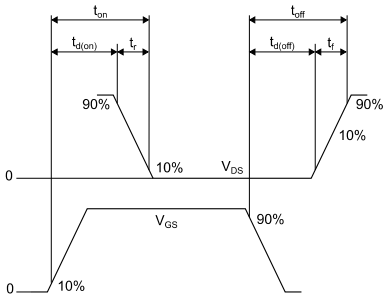


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 double island WF type C package information

Figure 19: PowerFLAT™ 5x6 double island WF type C package outline

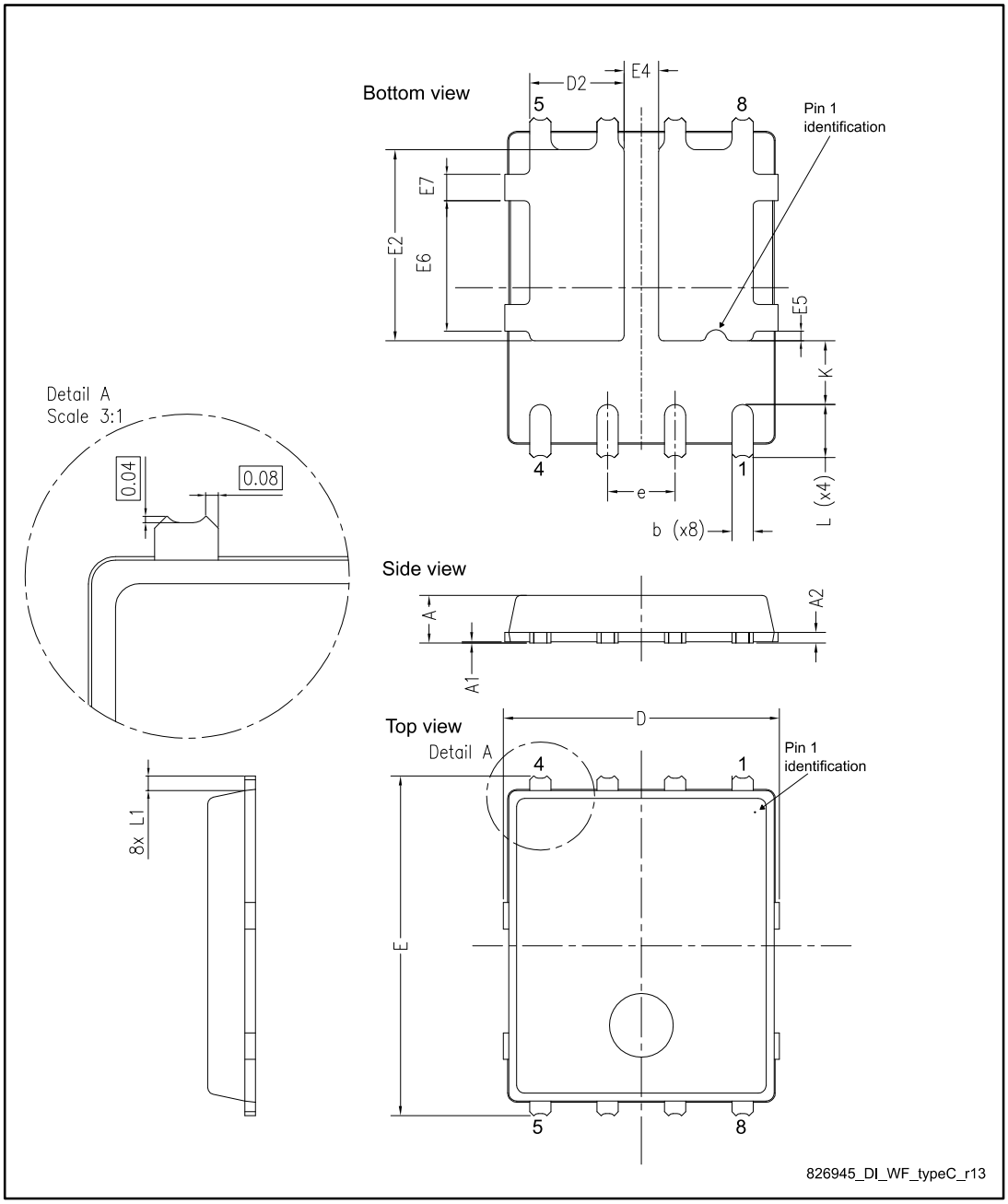
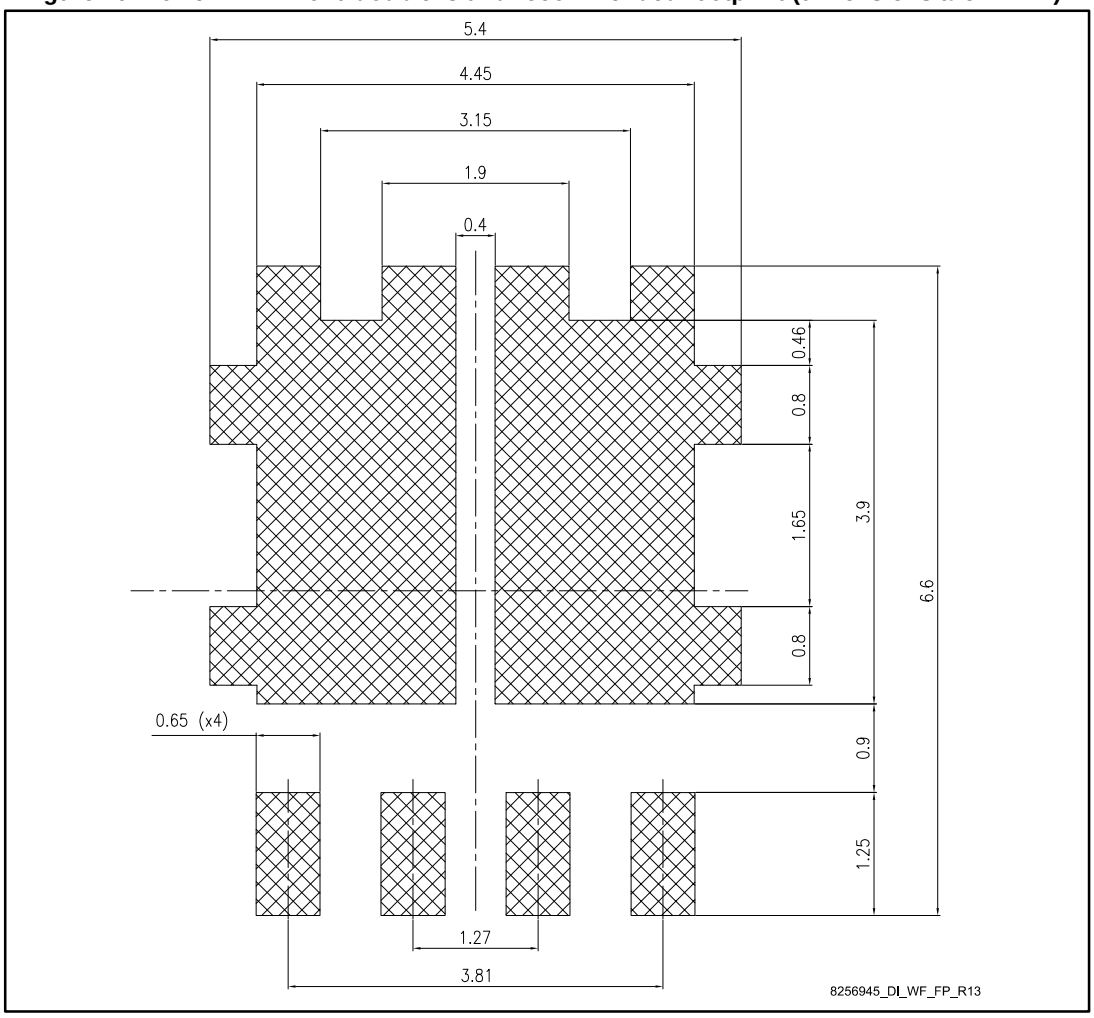


Table 9: PowerFLAT™ 5x6 double island WF type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
D2	1.68		1.88
E	6.20	6.40	6.60
E2	3.50		3.70
E4	0.55		0.75
E5	0.08		0.28
E6	2.35		2.55
E7	0.40		0.60
e		1.27	
L	0.90		1.10
L1		0.275	
K	1.05		1.35

Figure 20: PowerFLAT™ 5x6 double island recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 WF packing information

Figure 21: PowerFLAT™ 5x6 WF tape

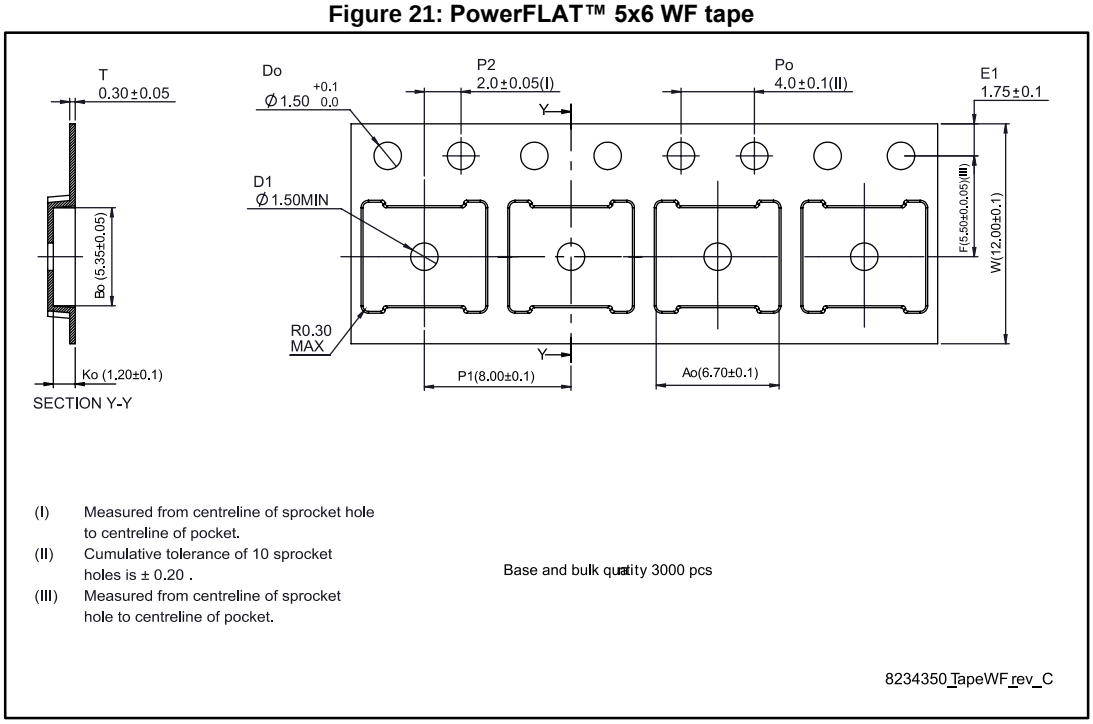


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

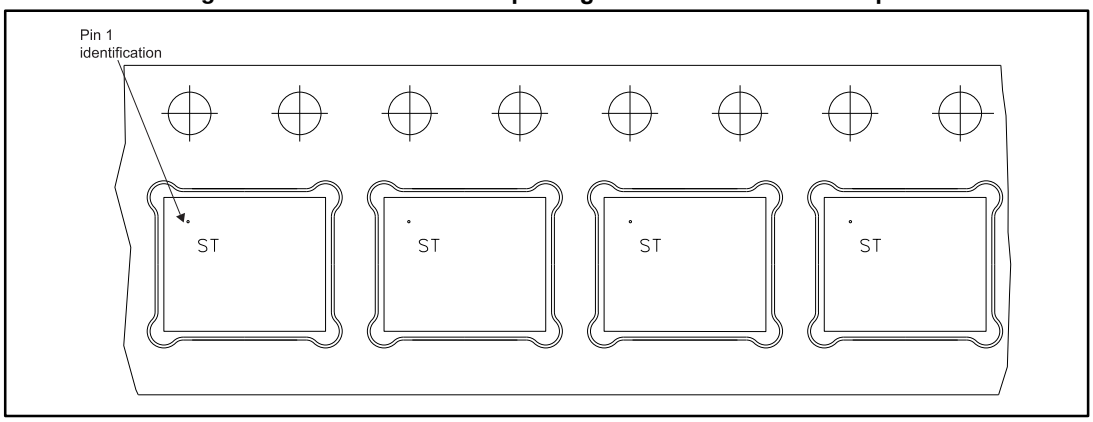
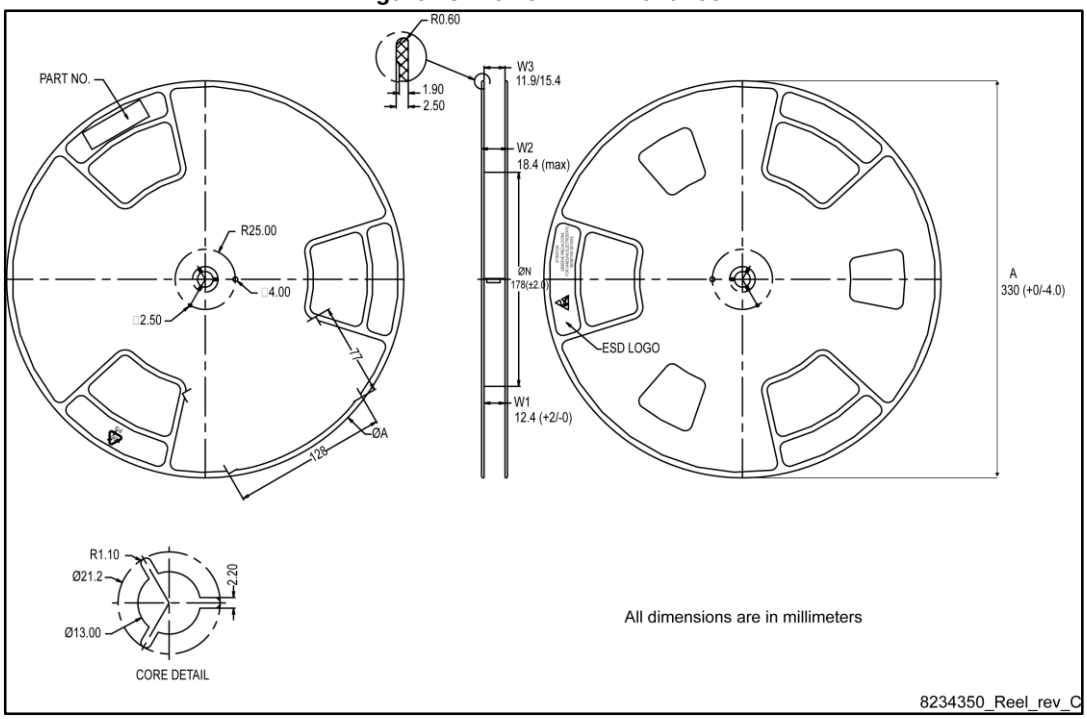


Figure 23: PowerFLAT™ 5x6 reel



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
12-Oct-2011	1	First release.
14-Mar-2012	2	Document status changed from preliminary data to production data. Inserted Section 5: Packaging mechanical data. Minor text changes.
28-Aug-2015	3	Text and formatting changes throughout document Updated device marking information. Updated device package information.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved