PIC18F87J10 Family Data Sheet Errata

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39663**D**), the following clarifications and corrections should be noted. Any silicon issues related to the PIC18F87J10 family will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

1. Module: Electrical Specifications (AC Characteristics)

Table 26-8: AC Characteristics: Internal RC Accuracy incorrectly specifies the frequency tolerance of the INTRC oscillator.

When clocked from the INTRC clock source, this clock source affects the following:

- Power-up Timer (PWRT)
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor (FSCM)
- Two Speed Start-up (IESO)
- Controller Speed

The INTRC clock source cannot be adjusted. The table is replaced as shown in Table 26-8.

TABLE 26-8: AC CHARACTERISTICS: INTERNAL RC ACCURACY PIC18F87J10 FAMILY (INDUSTRIAL)

Param No.	Characteristic	Min	Typ	Max	Units	Conditions
	INTRC Accuracy (31 kHz Nominal)	21.88	—	40.63	kHz	-40°C to +85°C, V_{DD} = 2.0-3.3V

2. Module: Table 26-1: Memory Programming Requirements

On page 355, Table 26-1 (Memory Programming Requirements) incorrectly specifies the self-timed page erase time. The table is corrected, as indicated by the bold text, for the following parameters:

- Parameter D133A – Parameter added with the symbol TIW. This is the write time for 64 bytes.
- Parameter D133B – Values corrected and symbol changed to TIE. This is the erase time for 1,024 bytes.
- The parameter, D132, which gives the minimum and maximum voltage levels of the Self-Timed Erase or Write for VDD and VDDCORE has been included.
- The parameter number for TWE is renamed as D140 and the condition column is updated.

The changed/appended values are indicated in bold text in the following table:

TABLE 26-1: MEMORY PROGRAMMING REQUIREMENTS

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	100	1K	—	E/W	-40°C to +85°C
D131	VPR	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D132	**VPEW**	**Voltage for Self-Timed Erase or Write**					
		VDD	**2.35**	—	**3.6**	V	**PIC18FXXJ10**
		VDDCORE	**2.25**	—	**2.7**	V	**PIC18LFXXJ10**
D133A	**TIW**	**Self-Timed Write Cycle Time**	**—**	**2.8**	**—**	**ms**	
D133B	**TIE**	Self-Timed Page Erased Cycle Time	**—**	**33.0**	**—**	**ms**	
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided, no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	
D140	**TWE**	**Writes per Erase Cycle**	**—**	**—**	**1**	**—**	**For each physical address**

† Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

3. Module: Flash Program Memory Erase Sequence

In **Section 6.4.1 "Flash Program Memory Erase Sequence",** Step 7:

The CPU will stall for duration of the erase for TIE (see parameter D133B).

4. Module: Flash Program Memory Write Sequence

In **Section 6.5.1 "Flash Program Memory Write Sequence",** Step 12:

The CPU will stall for duration of the write for TIW (see parameter D133A).

5. Module: Table 26-2: Comparator Specifications

On page 356, the maximum Input Offset Voltage (Param No. D300) is changed to ±25 mV.

The parameter numbers for TRESP and TMC2OV are changed to D303 and D304, respectively.

A new parameter, D305, for VIRV is added.

The note stating "* The parameters are characterized but not tested." is removed.

The modified values are indicated in bold text in the following table:

TABLE 26-2: COMPARATOR SPECIFICATIONS

Operating Conditions: 3.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	—	± 5.0	± **25**	mV	
D301	VICM	Input Common Mode Voltage	0	—	AVDD – 1.5	V	
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	
D303	TRESP	Response Time**(1)**	—	150	400	ns	
D304	TMC2OV	Comparator Mode Change to Output Valid	—	—	10	µs	
D305	**VIRV**	**Internal Reference Voltage**	**—**	**1.2**	**—**	**V**	**—**

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

6. Module: Table 26-4: Internal Voltage Regulator Specifications

On page 356, the comments column for CEFC is changed. The note, which states "* Parameters are characterized but not tested" is removed. The changed content is indicated in bold text in the following table:

TABLE 26-4: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
	VRGOUT	Regulator Output Voltage*	—	2.5	—	V	
	CEFC	External Filter Capacitor Value*	4.7	10	—	µF	**Capacitor must be low series resistance (<5 Ohms)**

7. Module: Section 26.1 “DC Characteristics: Supply Voltage PIC18F87J10 Family (Industrial)”

On page 345, a new parameter (D005) is added. The changed value is indicated in bold text in the following table.

26.1 DC Characteristics: Supply Voltage PIC18F87J10 Family (Industrial)

PIC18F87J10 Family (Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	VDDCORE 2.5	— —	3.6 3.6	V V	ENVREG = 0 ENVREG = 1
D001B	VDDCORE	**External Supply for Microcontroller Core**	2.0	—	2.75	V	ENVREG = 0
D002	VDR	**RAM Data Retention Voltage(1)**	1.5	—	—	V	
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	—	TBD	V	See **Section 4.3 “Power-on Reset (POR)”** for details.
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See **Section 4.3 “Power-on Reset (POR)”** for details.
D005	**VBOR**	**Brown-out Reset (BOR) Voltage**	**2.35**	**2.5**	**2.7**	**V**	

Legend: TBD = To Be Determined

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

8. Module: Section 26.3 “DC Characteristics: PIC18F87J10 Family (Industrial)

On page 353, the characteristics and conditions of the Input Leakage Current are updated for the Analog (D060) and included for the Digital (D060A) I/O ports. The changed values are indicated in bold text in the following table:

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial			
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**				
		All I/O ports:				
D030		with TTL buffer	VSS	0.15 VDD	V	VDD < 3.3V
D030A			—	0.8	V	3.3V ≤ VDD ≤ 3.6V
D031		with Schmitt Trigger buffer	VSS	0.2 VDD	V	
D032		$\overline{MCLR}$	VSS	0.2 VDD	V	
D033		OSC1	VSS	0.3 VDD	V	HS, HSPLL modes
D033A		OSC1	VSS	0.2 VDD	V	EC, ECPLL modes(1)
D034		T1CKI	VSS	0.3	V	
	VIH	**Input High Voltage**				
		I/O ports with non 5.5V tolerance:(4)				
D040		with TTL buffer	0.25 VDD + 0.8V	VDD	V	VDD < 3.3V
D040A			2.0	VDD	V	3.3V ≤ VDD ≤ 3.6V
D041		with Schmitt Trigger buffer	0.8 VDD	VDD	V	
		I/O ports with 5.5V tolerance:(4)				
Dxxx		with TTL buffer	0.25 VDD + 0.8V	5.5	V	VDD < 3.3V
DxxxA			2.0	5.5	V	3.3V ≤ VDD ≤ 3.6V
Dxxx		with Schmitt Trigger buffer	0.8 VDD	5.5	V	
D042		$\overline{MCLR}$	0.8 VDD	VDD	V	
D043		OSC1	0.7 VDD	VDD	V	HS, HSPLL modes
D043A		OSC1	0.8 VDD	VDD	V	EC, ECPLL modes
D044		T1CKI	1.6	VDD	V	
	IIL	**Input Leakage Current(2,3)**				
D060		**I/O ports with non 5.5V tolerance:(4)**	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
D060A		**I/O ports with 5.5V tolerance:(4)**	**—**	**±1**	**µA**	**VSS ≤ VPIN ≤ 5.5V, Pin at high-impedance**
D061		$\overline{MCLR}$	—	±1	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	±5	µA	VSS ≤ VPIN ≤ VDD

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC® device be driven with an external clock while in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: **Refer to Table 10-2 for the pins that have corresponding tolerance limits.**

9. Module: Section 18.3 “SPI Mode” and Section 18.4 “I²C™ Mode”

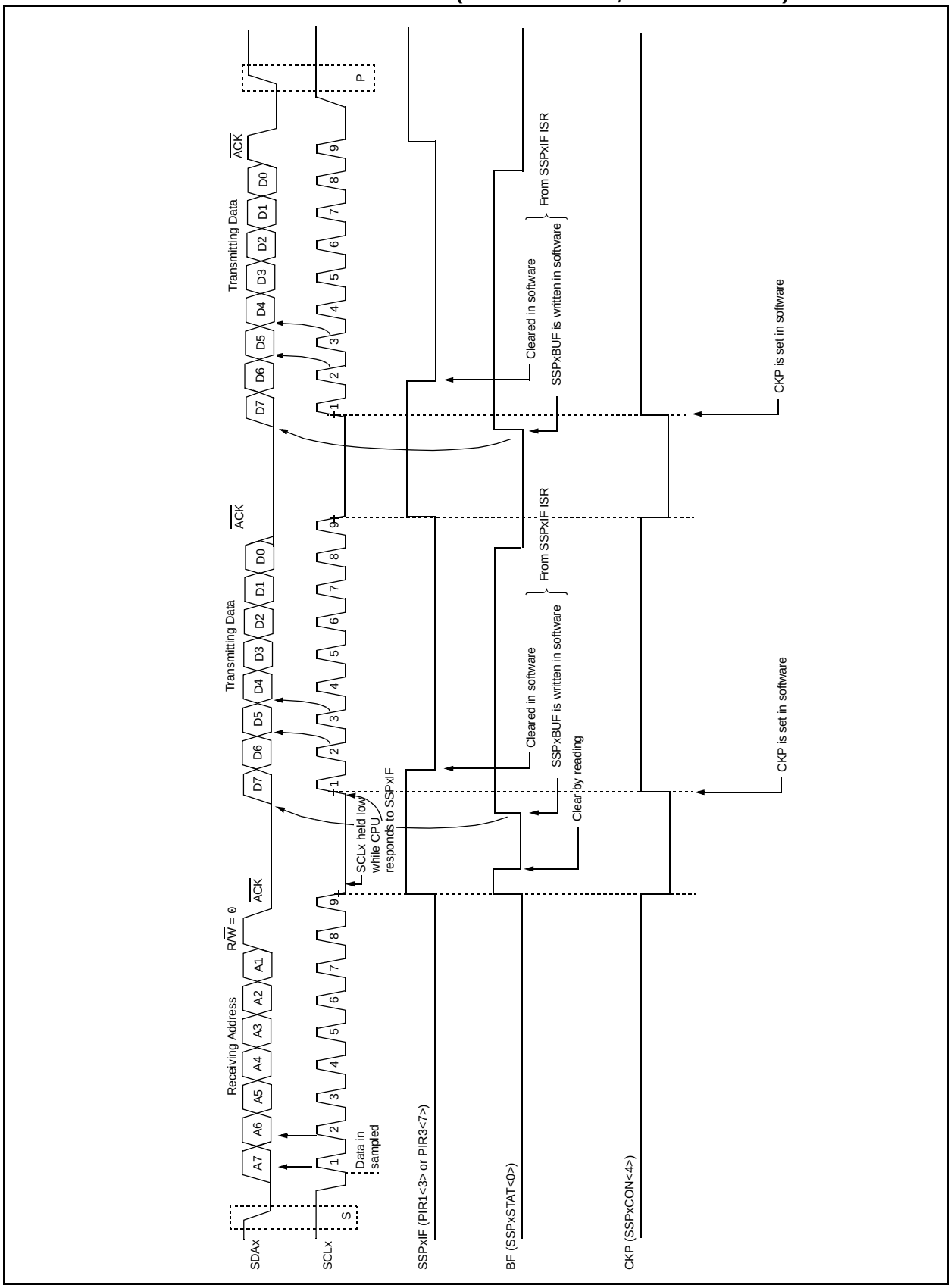
In **Section 18.3 “SPI Mode”** on page 189 and **Section 18.4 “I²C™ Mode”** on page 199, the following new note is included to describe the procedure to disable the MSSP module:

Note:	Disabling the MSSP module by clearing the SSPEN (SSPxCON1<5>) bit may not reset the module. It is recommended to clear the SSPxSTAT, SSPxCON1 and SSPxCON2 registers and select the mode prior to setting the SSPEN bit to enable the MSSP module.

10. Module: Figure 18-10: I²C™ Slave Mode Timing (Transmission, 7-Bit Address)

On page 209, the figure is replaced with the new timing diagram provided in Figure 18-10.

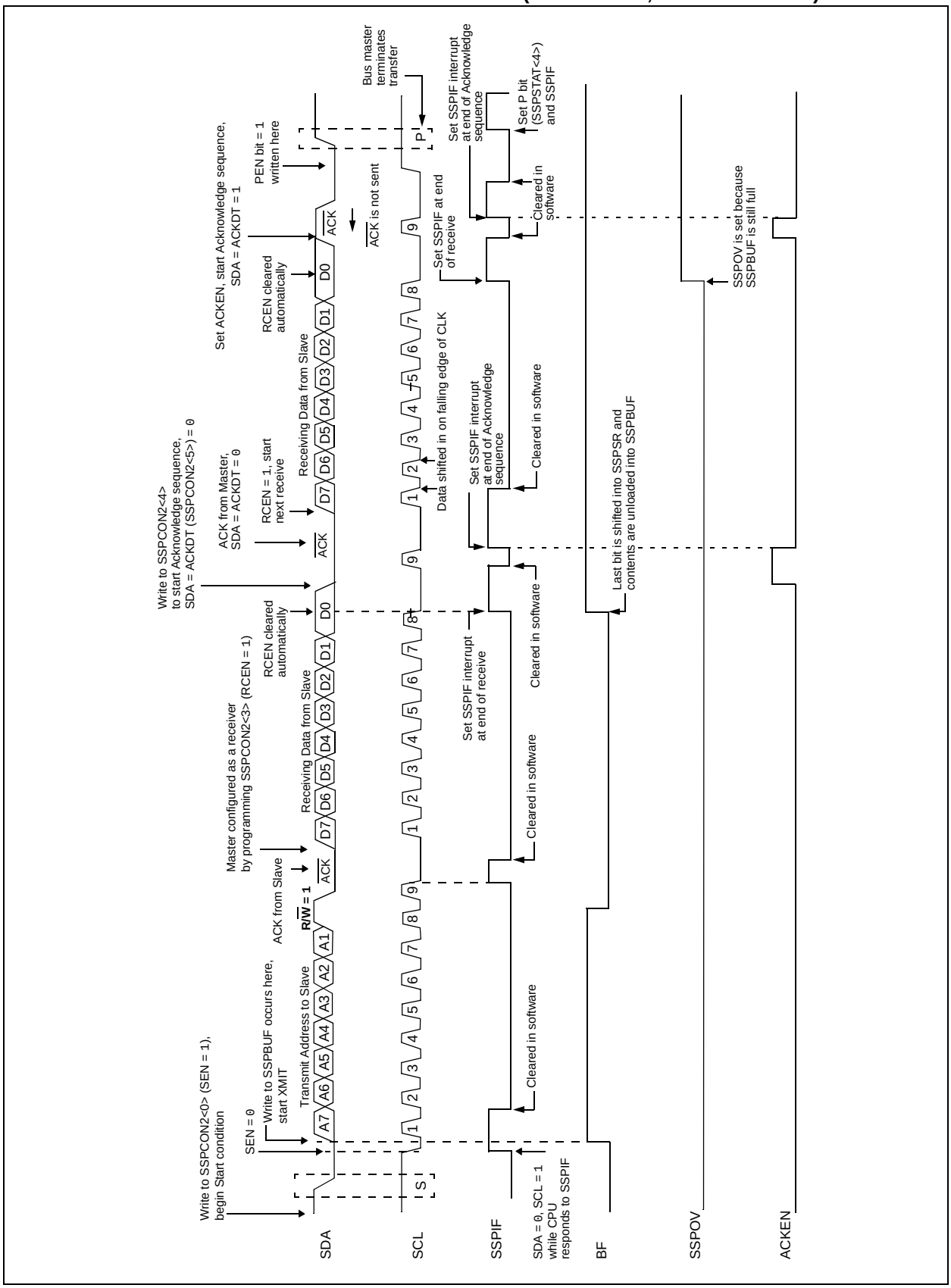
FIGURE 18-10: I²C™ SLAVE MODE TIMING (TRANSMISSION, 7-BIT ADDRESS)



11. Module: Figure 18-24: I²C™ Master Mode Waveform (Reception, 7-Bit Address)

On page 226, the condition (R/$\overline{W}$) when the Acknowledge signal (ACK) is received from the slave, after transmitting the address to the slave, is changed to '1'. The changed value is indicated in bold text in Figure 18-24.

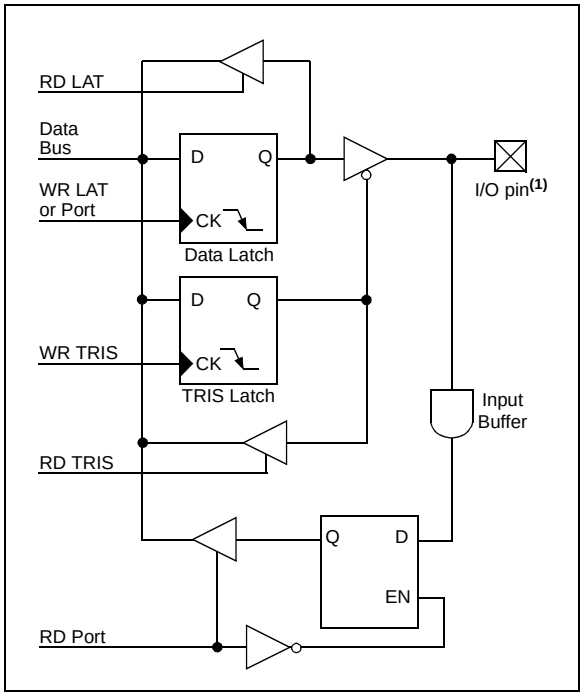
FIGURE 18-24: I²C™ MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)



12. Module: Figure 10-1: Generic I/O Port Operation

The note in Figure 10-1 on page 121 is removed.

FIGURE 10-1: GENERIC I/O PORT OPERATION



13. Module: Electrical Characteristics (DC Characteristics)

The second page of the two-page DC Characteristics table adds the content shown in bold text.

26.3 DC Characteristics: PIC18F87J10 Family (Industrial)

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial			
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VOL	**Output Low Voltage**				
D080		I/O ports (PORTB, PORTC)	—	0.4	V	**IOL = 8.5 mA, VDD 3.3V**
		I/O ports (PORTD, PORTE, PORTJ)	—	0.4	V	**IOL = 3.4 mA, VDD 3.3V**
		I/O ports (PORTA, PORTF, PORTG, PORTH)	—	0.4	V	**IOL = 3.4 mA, VDD 3.3V**
D083		OSC2/CLKO (EC, ECIO modes)	—	0.4	V	**IOL = 1.6 mA, VDD 3.3V**
	VOH	**Output High Voltage(3)**				
D090		I/O ports (PORTB, PORTC)	2.4	—	V	**IOL = -6 mA, VDD 3.3V**
		I/O ports (PORTD, PORTE, PORTJ)	2.4	—	V	**IOL = -2 mA, VDD 3.3V**
		I/O ports (PORTA, PORTF, PORTG, PORTH)	2.4	—	V	**IOL = -2 mA, VDD 3.3V**
D092		OSC2/CLKO (EC, ECIO modes)	2.4	—	V	**IOL = 1 mA, VDD 3.3V**
		Capacitive Loading Specs on Output Pins				
D100(4)	COSC2	OSC2 pin	—	15	pF	In HS mode when external clock is used to drive OSC1
D101	CIO	All I/O pins	—	50	pF	To meet the AC Timing Specifications
D102	CB	SCLx, SDAx	—	400	pF	I^2C™ Specification

Legend: TBD = To Be Determined

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PICmicro® device be driven with an external clock while in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

REVISION HISTORY

Rev A Document (3/2007)
Initial release of this document. Data Sheet Clarification issue 1 (Electrical Specifications – AC Characteristics).

Rev B Document (5/2008)
Added Data Sheet Clarification issue 2 (Electrical Specifications – Row Erase Time), 3 (Flash Program Memory Erase Sequence) and 4 (Flash Program Memory Write Sequence).

Rev C Document (10/2008)

Removed the previous Data Sheet Clarification issue 2 (Electrical Specifications – Row Erase Time). Added Data Sheet Clarification issues 2 (Table 26-1: Memory Programming Requirements), 5 (Table 26-2: Comparator Specifications), 6 (Table 26-4: Internal Voltage Regulator Specifications), 7 (Section 26.1 “DC Characteristics: Supply Voltage PIC18F87J10 Family – Industrial”), 8 (Section 26.3 “DC Characteristics: PIC18F87J10 Family – Industrial”), 9 (Section 18.3 “SPI Mode” and Section 18.4 “I^2C™ Mode”), 10 (Figure 18-10: I^2C™ Slave Mode Timing – Transmission, 7-Bit Address), 11 (Figure 18-24: I^2C™ Master Mode Waveform – Reception, 7-Bit Address) and 12 (Figure 10-1: Generic I/O Port Operation).

Rev D Document (11/2008)
Edits were made to Data Sheet Clarification issue 8 (Section 26.3 “DC Characteristics: PIC18F87J10 Family – Industrial”).

Rev E Document (February/2009)
Added Data Sheet Clarification 13 (**Section 26.3 “DC Characteristics”**).

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