0.4 GHz to 6 GHz, 35 W, GaN, Power Amplifier

Data Sheet **HMC8205BCHIPS**

FEATURES

High output power: 45.5 dBm typical at P_{IN} = 24 dBm
High power gain: 22 dB typical at P_{IN} = 24 dBm
High PAE: 40% typical at P_{IN} = 28 dBm
Die size: 4.8 mm × 3.4 mm × 0.1 mm

APPLICATIONS

Military jammers
Commercial and military radar
Power amplifier stage for wireless infrastructure
Test and measurement equipment

FUNCTIONAL BLOCK DIAGRAM

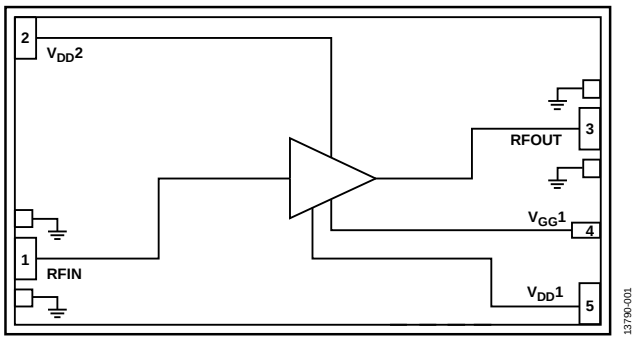


Figure 1.

GENERAL DESCRIPTION

The HMC8205BCHIPS is a gallium nitride (GaN), broadband power amplifier that delivers 45.5 dBm (35 W) with 40% power added efficiency (PAE) across an instantaneous bandwidth of 0.4 GHz to 6 GHz. No external matching is required to achieve full band operation. No external inductor is required to bias the amplifier. In addition, dc blocking capacitors for the RFIN and RFOUT pins are integrated into the HMC8205BCHIPS.

The HMC8205BCHIPS is ideal for pulsed or continuous wave (CW) applications, such as military jammers, wireless infrastructure, radar, and general-purpose amplification.

Rev. A **Document Feedback**
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REVISION HISTORY

4/2020—Rev. 0 to Rev. A
Updated Outline Dimensions ... 19

11/2018—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, supply voltage (V_{DD}) = 50 V, total supply current (I_{DQ}) = 1300 mA, and frequency range = 0.4 GHz to 0.8 GHz, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
FREQUENCY RANGE	0.4		0.8	GHz
GAIN				
Small Signal Gain		24		dB
Gain Flatness		±0.5		dB
RETURN LOSS				
Input		6		dB
Output		6.5		dB
POWER				
Output (P_{OUT})				
Input Power (P_{IN}) = 24 dBm		43		dBm
P_{IN} = 28 dBm		46		dBm
Gain				
P_{IN} = 24 dBm		19		dB
P_{IN} = 28 dBm		17		dB
POWER ADDED EFFICIENCY (PAE)				
P_{IN} = 24 dBm		35		%
P_{IN} = 28 dBm		40		%
TOTAL SUPPLY CURRENT (I_{DQ})		1300		mA
SUPPLY VOLTAGE (V_{DD})	28	50	55	V

T_A = 25°C, V_{DD} = 50 V, I_{DQ} = 1300 mA, and frequency range = 0.8 GHz to 4 GHz, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
FREQUENCY RANGE	0.8		4	GHz
GAIN				
Small Signal Gain	23	25		dB
Gain Flatness		±0.8		dB
RETURN LOSS				
Input		11		dB
Output		10		dB
POWER				
Output (P_{OUT})				
Input Power (P_{IN}) = 24 dBm	43	45.5		dBm
P_{IN} = 28 dBm		46.5		dBm
Gain				
P_{IN} = 24 dBm		22		dB
P_{IN} = 28 dBm		19		dB
POWER ADDED EFFICIENCY (PAE)				
P_{IN} = 24 dBm		35		%
P_{IN} = 28 dBm		40		%
TOTAL SUPPLY CURRENT (I_{DQ})		1300		mA
SUPPLY VOLTAGE (V_{DD})	28	50	55	V

T_A = 25°C, V_{DD} = 50 V, I_{DQ} = 1300 mA, and frequency range = 4 GHz to 6 GHz, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
FREQUENCY RANGE	4		6	GHz
GAIN				
Small Signal Gain	24.5	26.5		dB
Gain Flatness		±1.4		dB
RETURN LOSS				
Input		8		dB
Output		9		dB
POWER				
Output (P_{OUT})				
Input Power (P_{IN}) = 24 dBm	43.5	45.5		dBm
P_{IN} = 28 dBm		46		dBm
Gain				
P_{IN} = 24 dBm		19		dB
P_{IN} = 28 dBm		18.5		dB
POWER ADDED EFFICIENCY (PAE)				
P_{IN} = 24 dBm		32		%
P_{IN} = 28 dBm		32		%
TOTAL SUPPLY CURRENT (I_{DQ})		1300		mA
SUPPLY VOLTAGE (V_{DD})	28	50	55	V

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Drain Bias Voltage (V_{DD}x)	60 V dc
Gate Bias Voltage (V_{GG}1)	−8 V dc to 0 V dc
Radio Frequency Input Power (RFIN)	35 dBm
Continuous Power Dissipation (P_{DISS}), T = 85°C (Derate 826 mW/°C Above 85°C)	115.7 W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +85°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	Class 1A, Passed 375 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to mounting substrate design and operating environment. Careful attention to thermal design is required.

θ_{JC} is the junction to case thermal resistance, channel to bottom of die.

Table 5. Thermal Resistance

Package Type	θ_{JC}	Unit
C-5-7	1.21	°C/W

Table 6. Reliability Information

Parameter	Temperature (°C)
Junction Temperature to Maintain 1,000,000 Hour Mean Time to Failure (MTTF)	225
Nominal Junction Temperature (T = 85°C, V_{DD} = 50 V, I_{DQ} = 1300 mA)	163.7

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

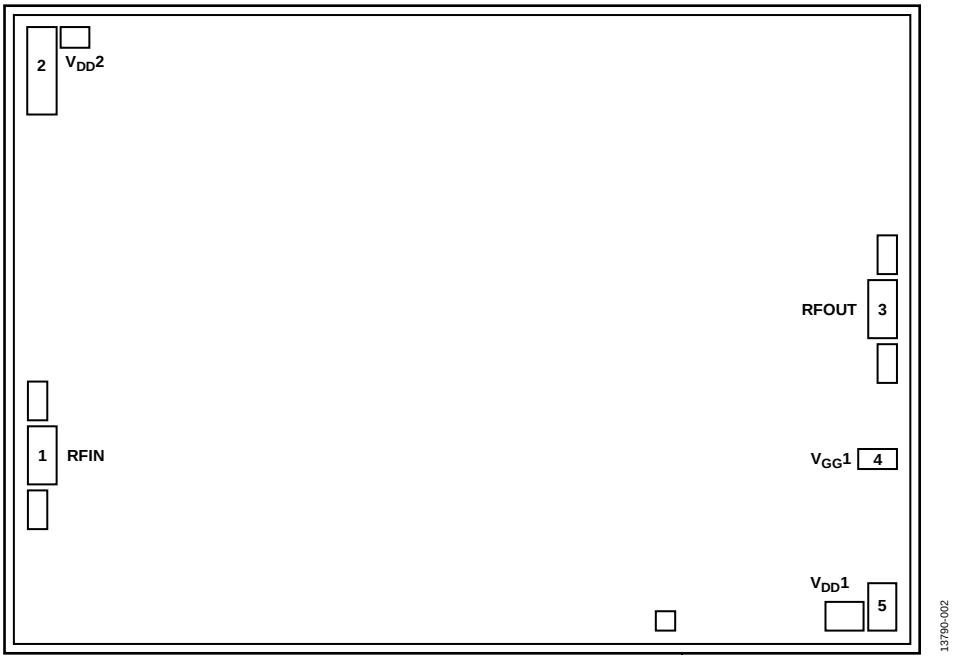


Figure 2. Pad Configuration

Table 7. Pad Function Descriptions

Pad No.	Mnemonic	Description
1	RFIN	RF Input (RFIN). This pin is ac-coupled and internally matched to 50 Ω. See Figure 4 for the RFIN interface schematic.
2	$V_{DD}2$	Drain Bias for Second Stage of Amplifier. See Figure 3 for the $V_{DD}2$ interface schematic.
3	RFOUT	RF Output (RFOUT). This pin is ac-coupled and internally matched to 50 Ω. See Figure 7 for the RFOUT interface schematic.
4	$V_{GG}1$	Gate Control for Second Stage of Amplifier. See Figure 6 for the $V_{GG}1$ interface schematic.
5	$V_{DD}1$	Drain Bias for First Stage of Amplifier. See Figure 5 for the $V_{DD}1$ interface schematic.
Die Bottom	GND	Ground. Die bottom must be connected to RF and dc ground. See Figure 8 interface schematic.

INTERFACE SCHEMATICS

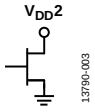


Figure 3. $V_{DD}2$ Interface

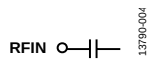


Figure 4. RFIN Interface

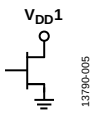


Figure 5. $V_{DD}1$ Interface

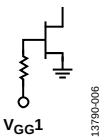


Figure 6. $V_{GG}1$ Interface



Figure 7. RFOUT Interface



Figure 8. GND Interface

TYPICAL PERFORMANCE CHARACTERISTICS

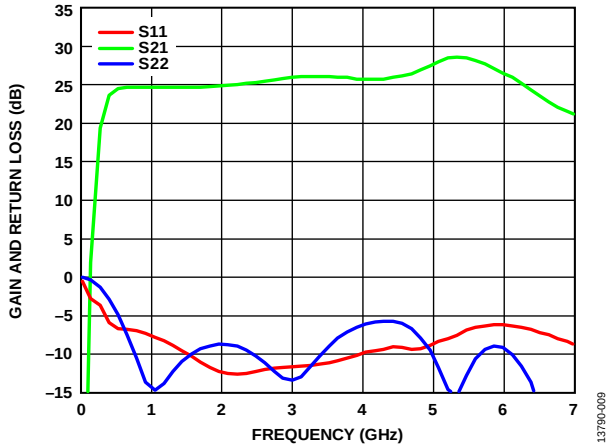


Figure 9. Gain and Return Loss vs. Frequency

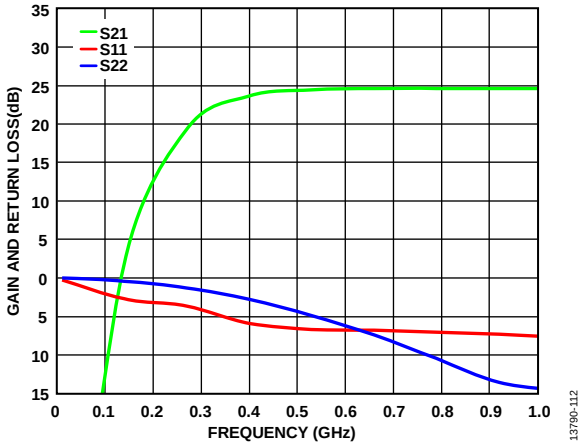


Figure 12. Gain and Return Loss vs. Frequency, 10 MHz to 1000 MHz

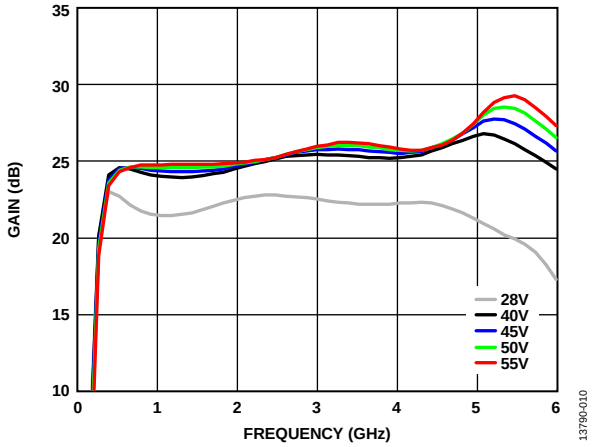


Figure 10. Gain vs. Frequency at Various Supply Voltages

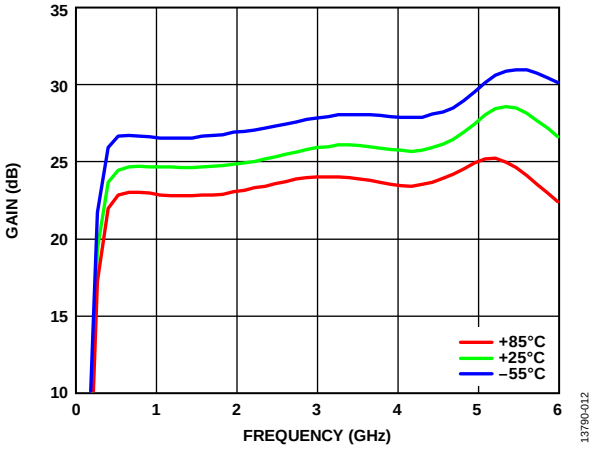


Figure 13. Gain vs. Frequency at Various Temperatures

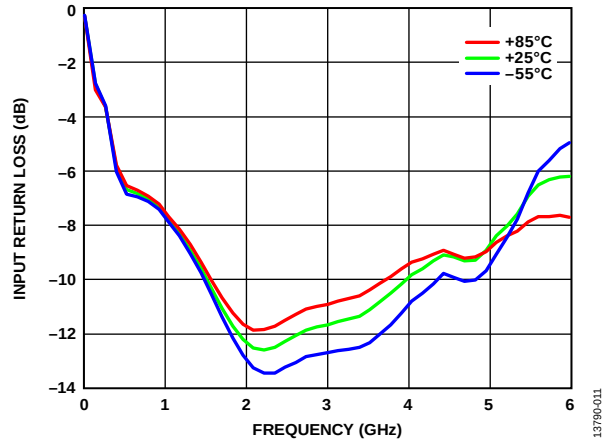


Figure 11. Input Return Loss vs. Frequency at Varoius Temperatures

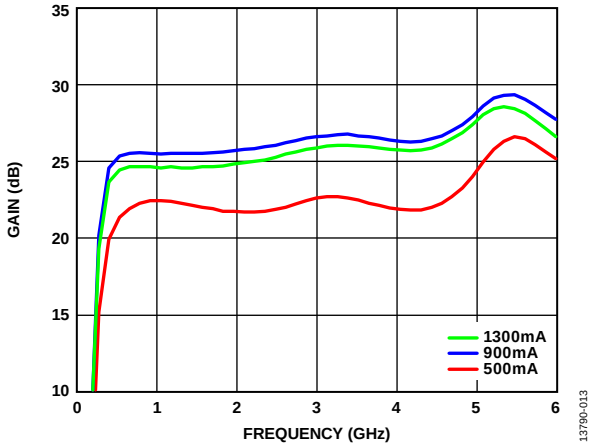


Figure 14. Gain vs. Frequency at Various Quiescent Supply Currents ($I_{DD}X$)

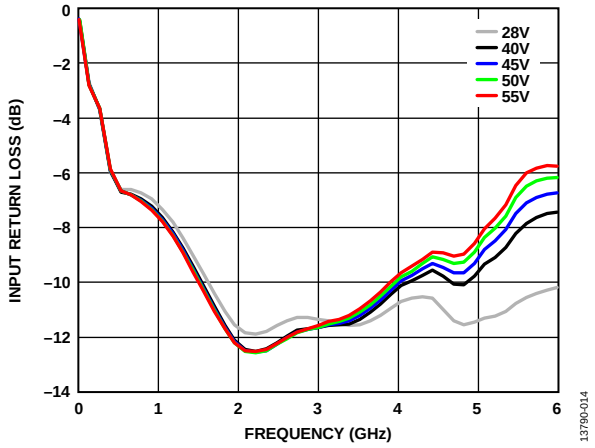


Figure 15. Input Return Loss vs. Frequency at Various Supply Voltages

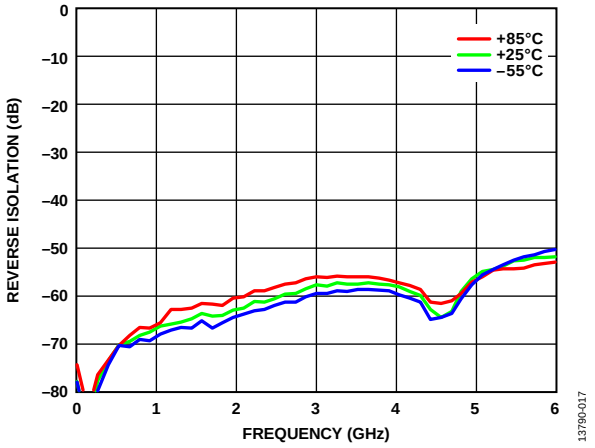


Figure 18. Reverse Isolation vs. Frequency at Various Temperatures

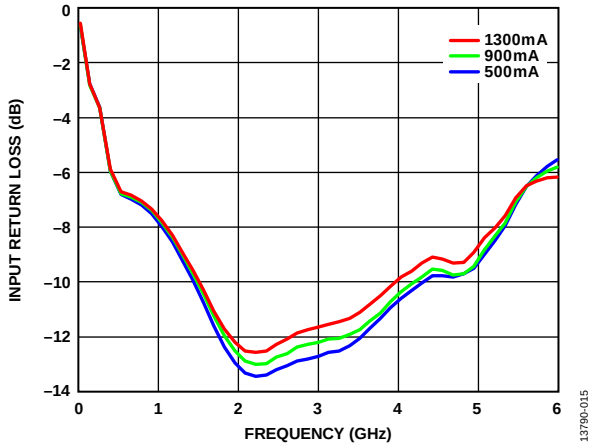


Figure 16. Input Return Loss vs. Frequency at Various Quiescent Supply Currents ($I_{DD}X$)

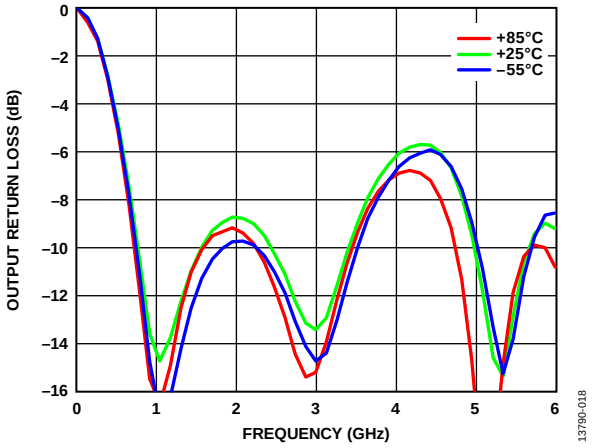


Figure 19. Output Return Loss vs. Frequency at Various Temperatures

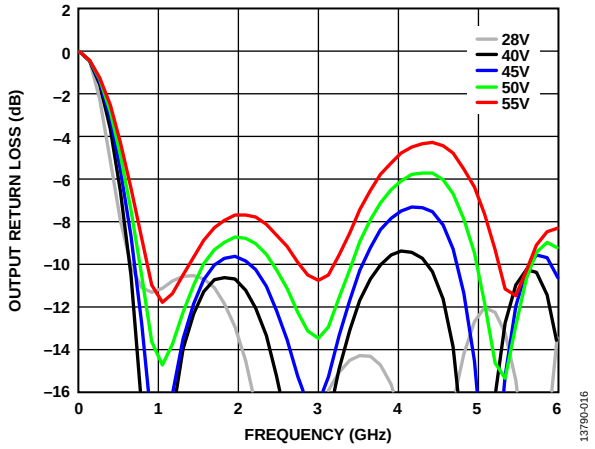


Figure 17. Output Return Loss vs. Frequency at Various Supply Voltages

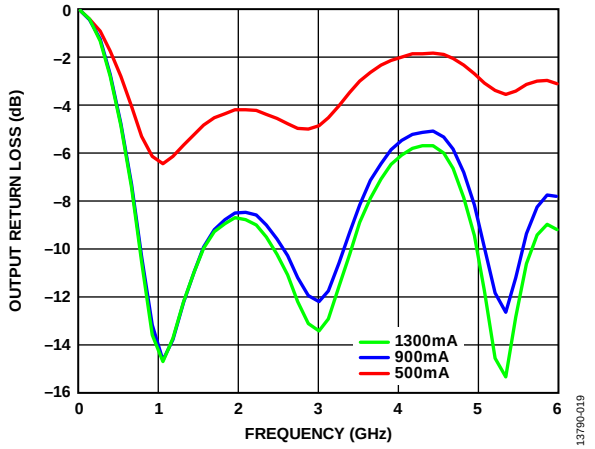


Figure 20. Output Return Loss vs. Frequency at Various Quiescent Supply Currents ($I_{DD}1 + I_{DD}2$)

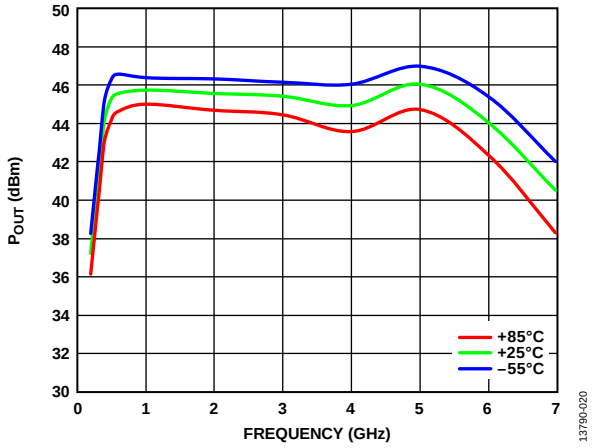


Figure 21. P_{OUT} vs. Frequency at Various Temperatures, P_{IN} = 24 dBm

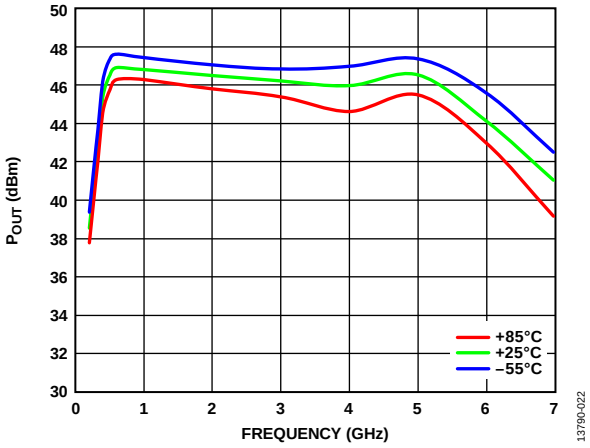


Figure 24. P_{OUT} vs. Frequency at Various Temperatures, P_{IN} = 28 dBm

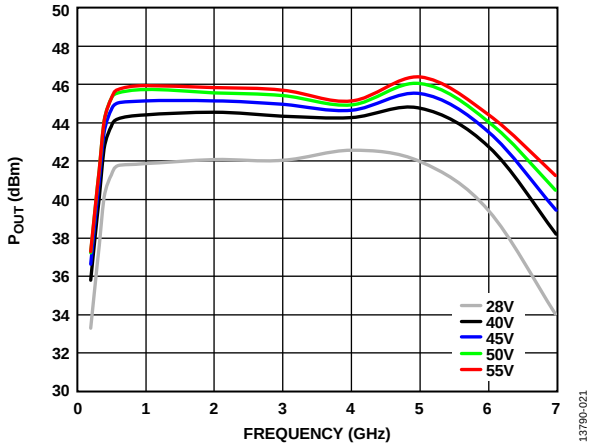


Figure 22. P_{OUT} vs. Frequency at Various Voltages, P_{IN} = 24 dBm

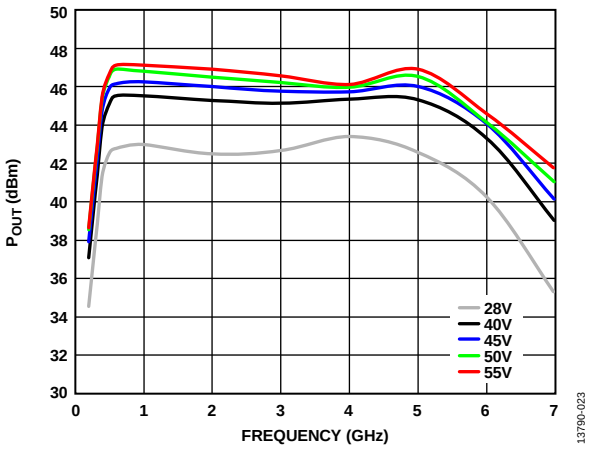


Figure 25. P_{OUT} vs. Frequency at Various Voltages, P_{IN} = 28 dBm

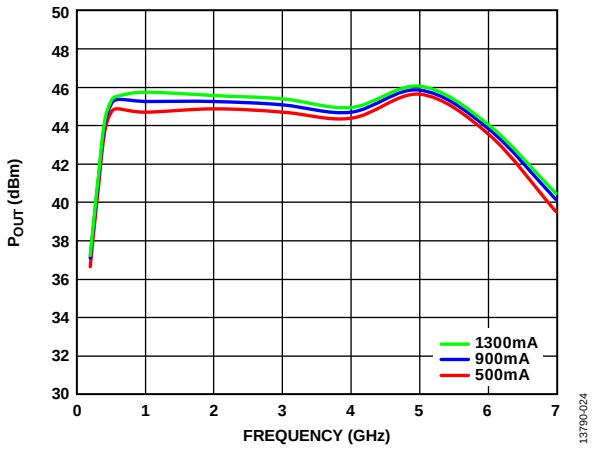


Figure 23. P_{OUT} vs. Frequency at Various Quiescent Currents ($I_{DD}1 + I_{DD}2$), P_{IN} = 24 dBm

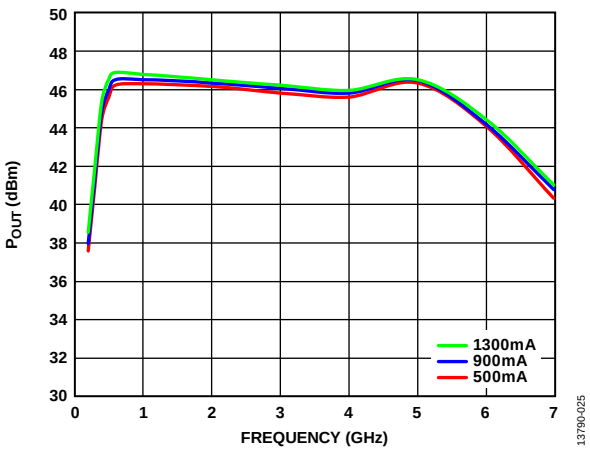


Figure 26. P_{OUT} vs. Frequency at Various Quiescent Currents ($I_{DD}1 + I_{DD}2$), P_{IN} = 28 dBm

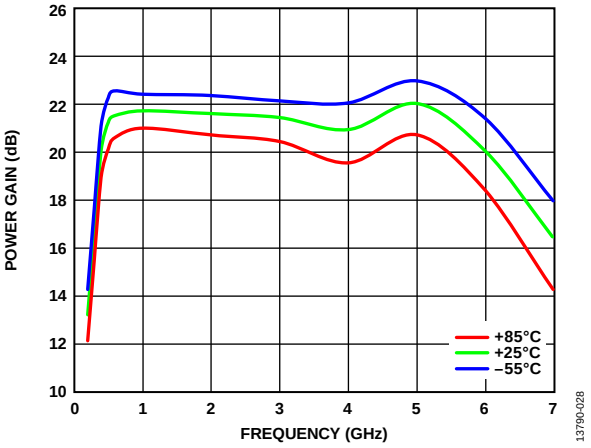


Figure 27. Power Gain vs. Frequency at Various Temperatures, Input Power = 24 dBm

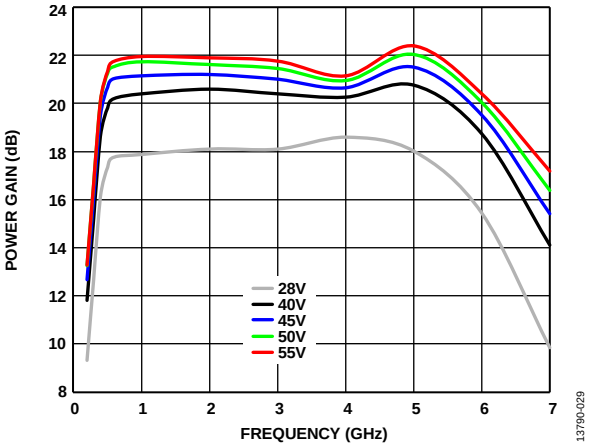


Figure 28. Power Gain vs. Frequency at Various Voltages, Input Power = 24 dBm

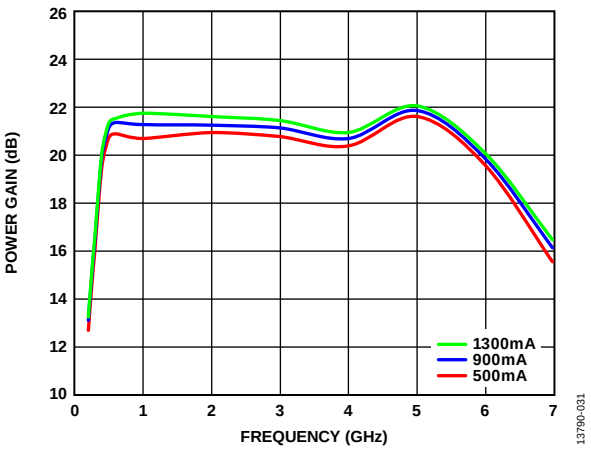


Figure 29. Power Gain vs. Frequency at Various Quiescent Currents ($I_{DD}1 + I_{DD}2$), Input Power = 24 dBm

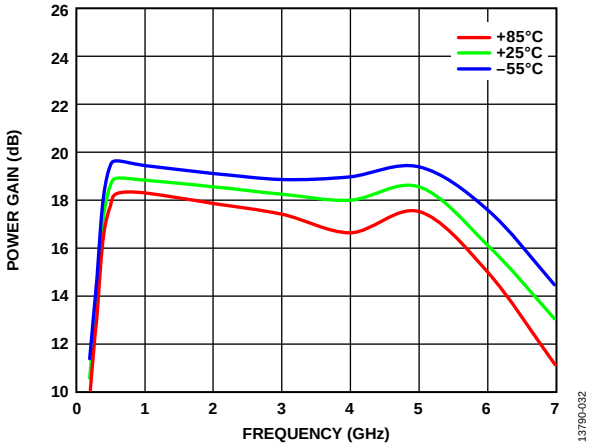


Figure 30. Power Gain vs. Frequency at Various Temperatures, Input Power = 28 dBm

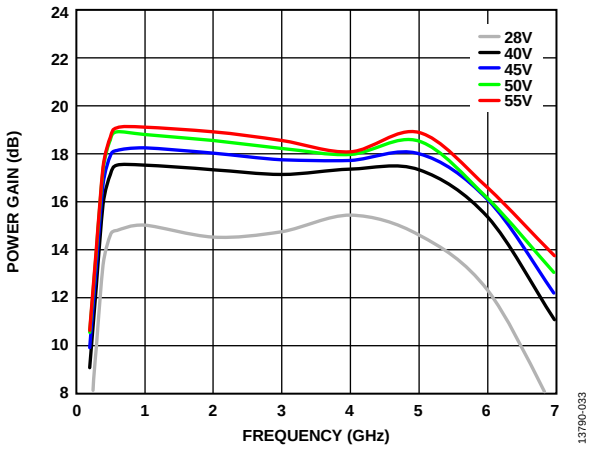


Figure 31. Power Gain vs. Frequency at Various Voltages, Input Power = 28 dBm

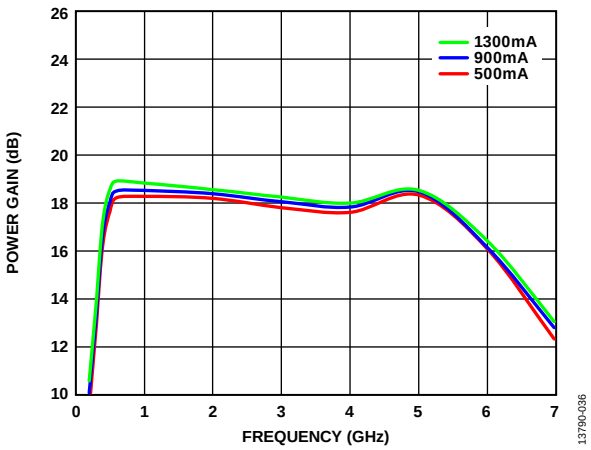


Figure 32. Power Gain vs. Frequency at Various Quiescent Currents ($I_{DD}1 + I_{DD}2$), Input Power = 28 dBm

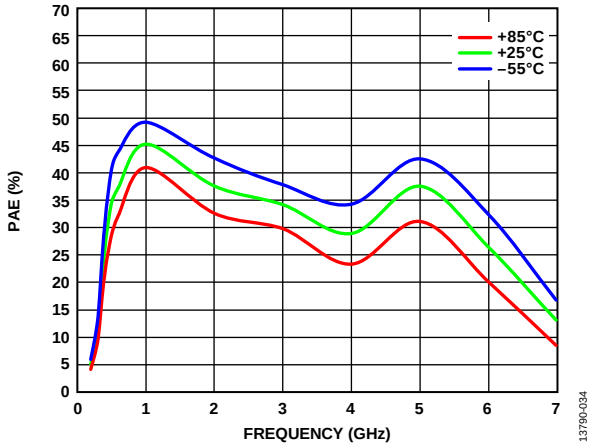


Figure 33. PAE vs. Frequency at Various Temperatures, Input Power = 24 dBm

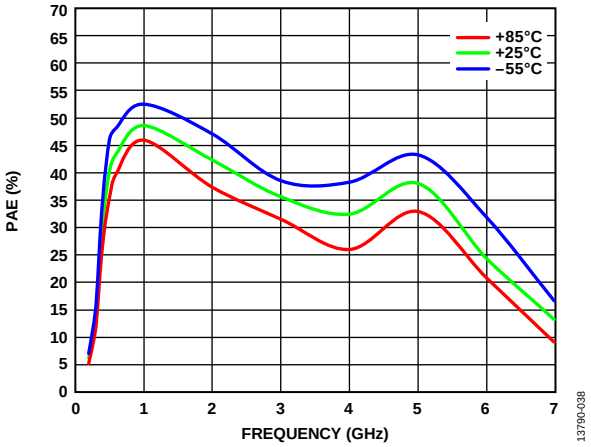


Figure 36. PAE vs. Frequency at Various Temperatures, Input Power = 28 dBm

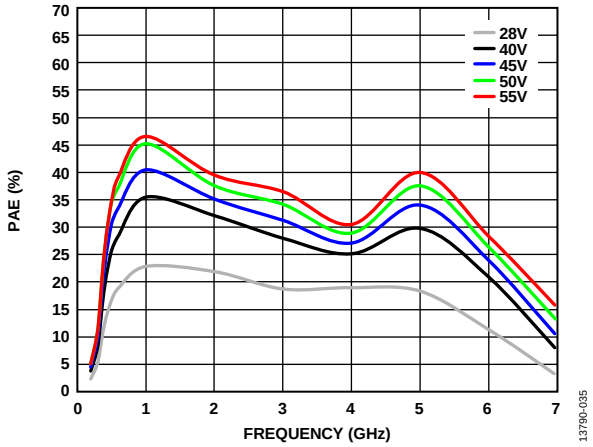


Figure 34. PAE vs. Frequency at Various Voltages, Input Power = 24 dBm

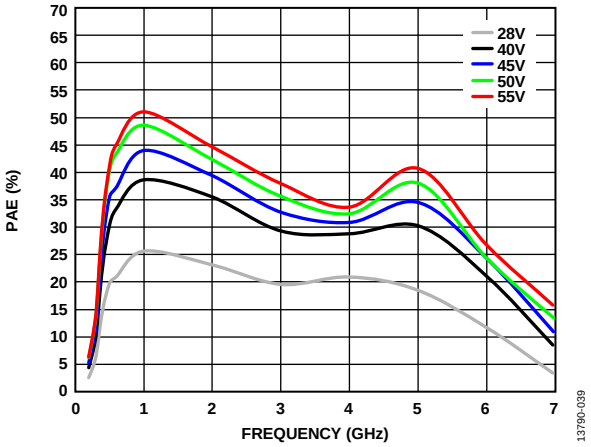


Figure 37. PAE vs. Frequency at Various Voltages, Input Power = 28 dBm

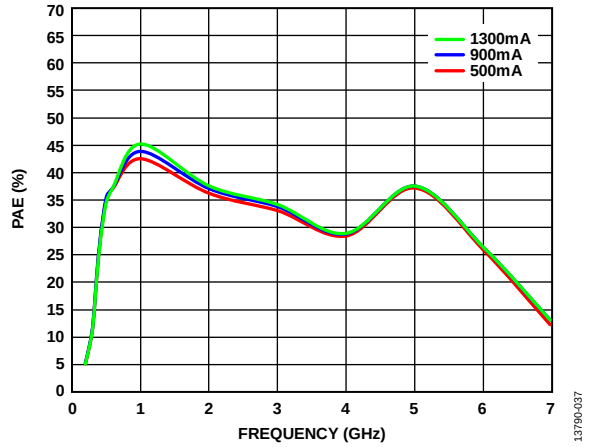


Figure 35. PAE vs. Frequency at Various Quiescent Currents ($I_{DD}1 + I_{DD}2$), Input Power = 24 dBm

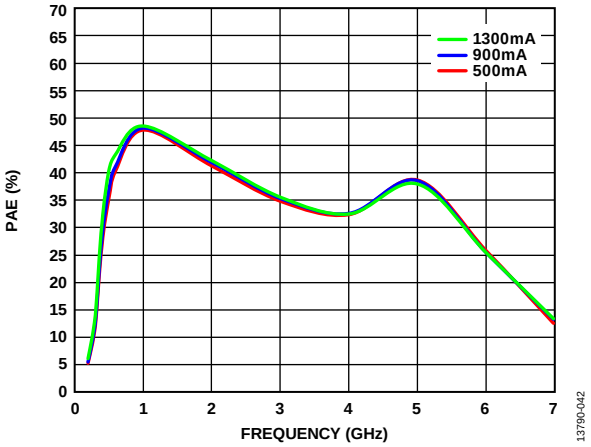


Figure 38. PAE vs. Frequency at Various Quiescent Currents ($I_{DD}1 + I_{DD}2$), Input Power = 28 dBm

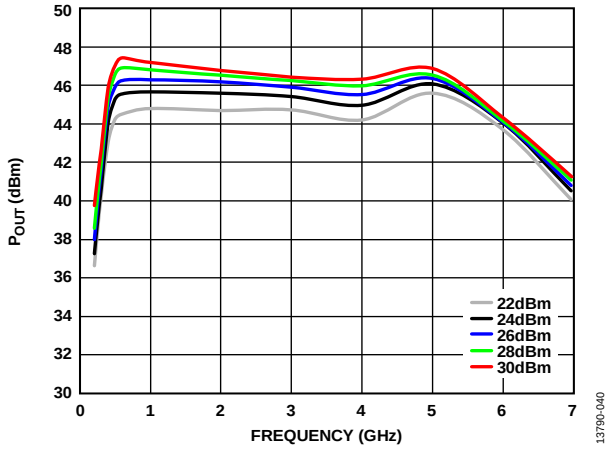


Figure 39. P_{OUT} vs. Frequency at Various Input Powers

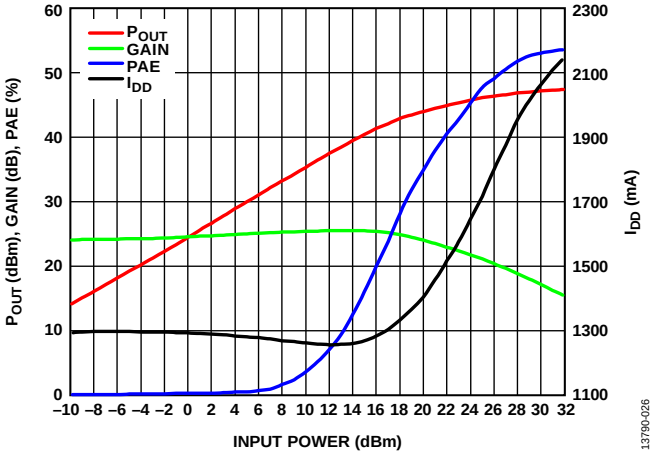


Figure 42. P_{OUT}, Gain, PAE, and Total Supply Current with RF Power Applied (I_{DD}) vs. Input Power, Frequency = 1 GHz

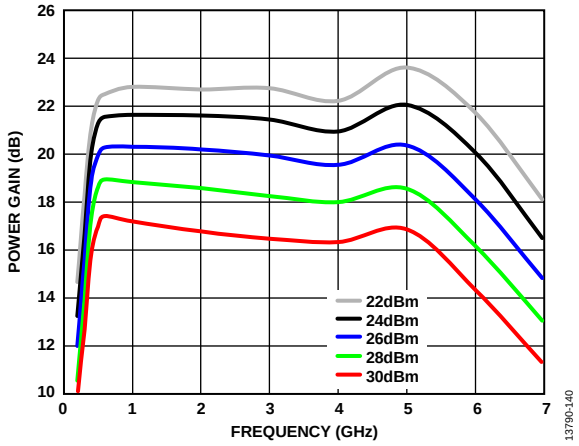


Figure 40. Power Gain vs. Frequency at Various Input Powers

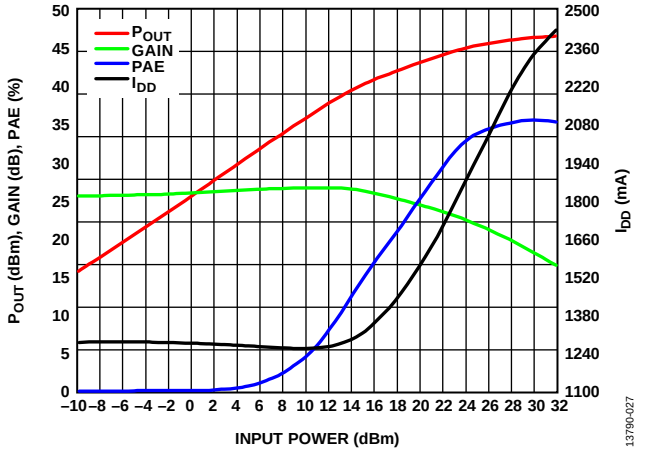


Figure 43. P_{OUT}, Gain, PAE, and Total Supply Current with RF Power Applied (I_{DD}) vs. Input Power, Frequency = 3 GHz

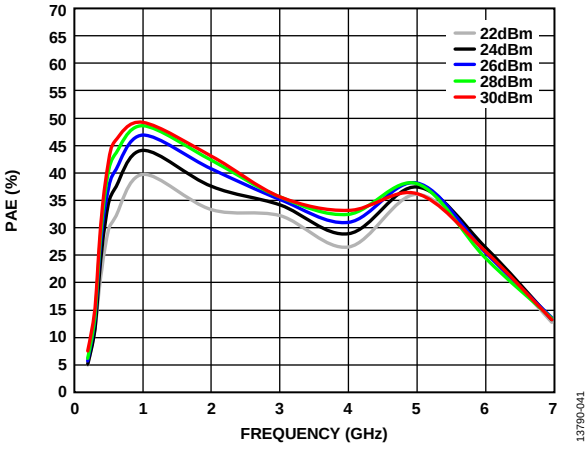


Figure 41. PAE vs. Frequency at Various Input Powers

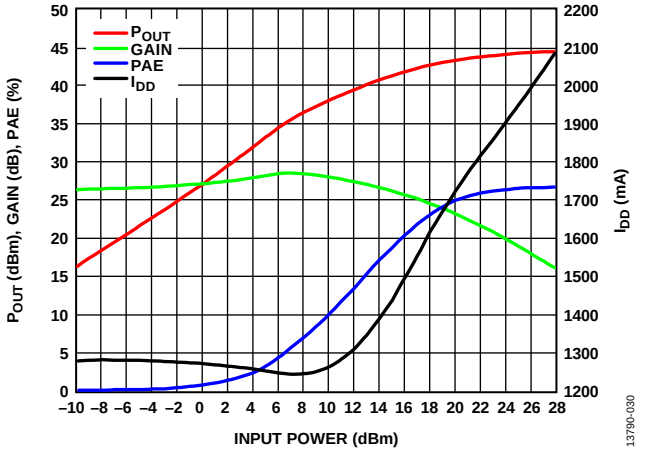


Figure 44. P_{OUT}, Gain, PAE, and Total Supply Current with RF Power Applied (I_{DD}) vs. Input Power, Frequency = 6 GHz

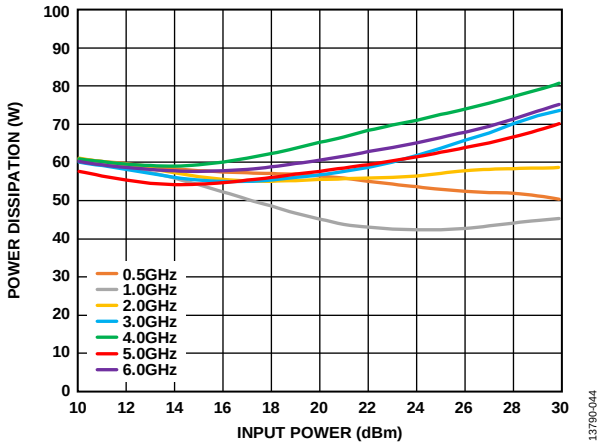


Figure 45. Power Dissipation vs. Input Power at 85°C

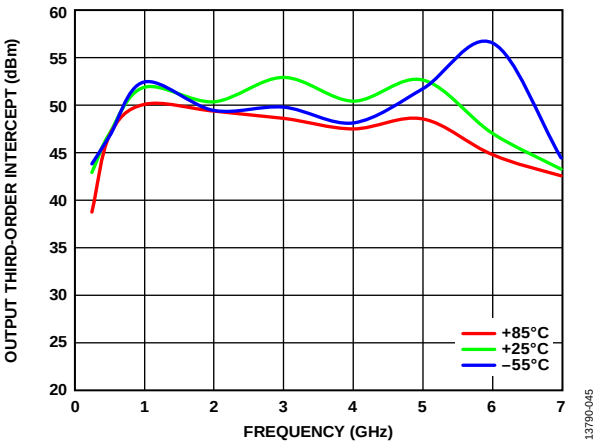


Figure 48. Output Third-Order Intercept Point (IP3) vs. Frequency at Various Temperatures, P_{OUT} per Tone = 32 dBm

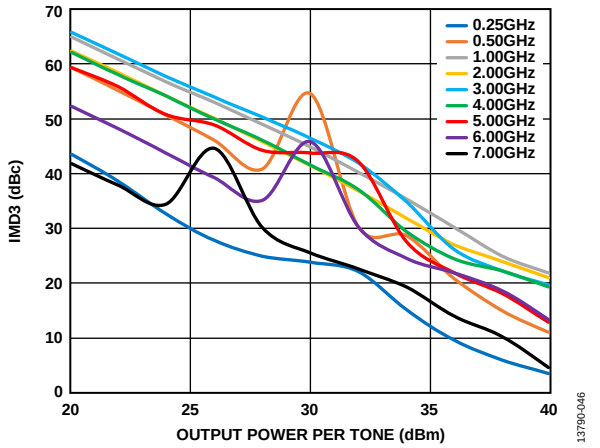


Figure 46. Upper Third-Order Intermodulation Distortion (IMD3) vs. Output Power per Tone at Various Frequencies

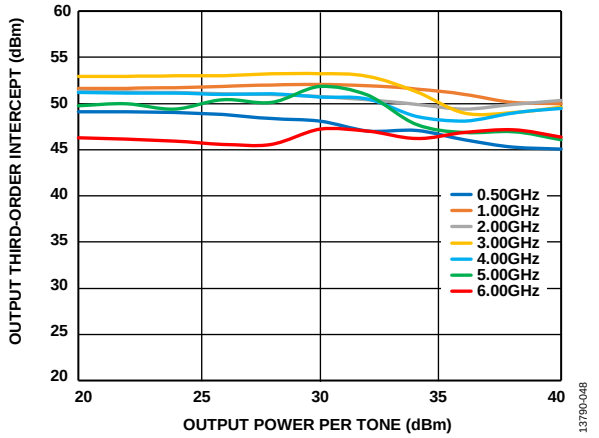


Figure 49. Output Third-Order Intercept Point (IP3) vs. Output Power per Tone at Various Frequencies

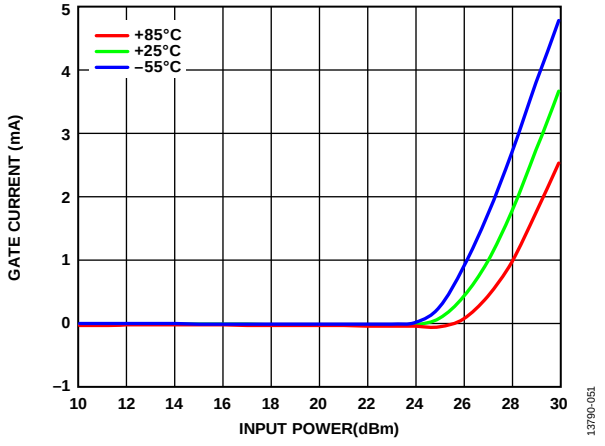


Figure 47. Gate Current vs. Input Power at Various Temperatures at 2 GHz

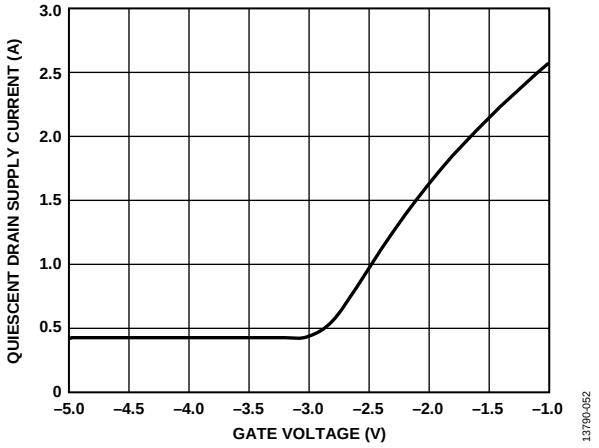


Figure 50. Quiescent Drain Supply Current vs. Gate Voltage

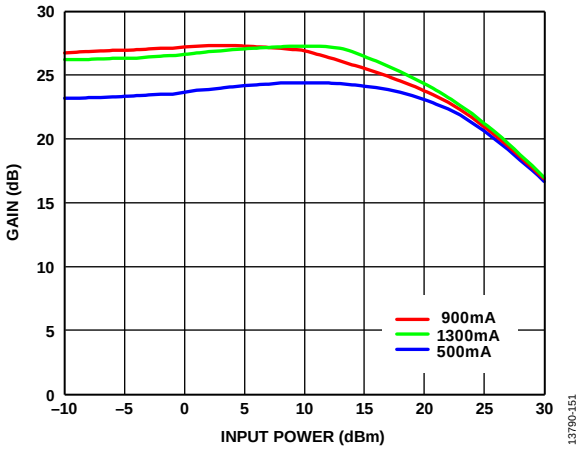


Figure 51. Gain vs. Input Power over I_{DQ} at 3 GHz

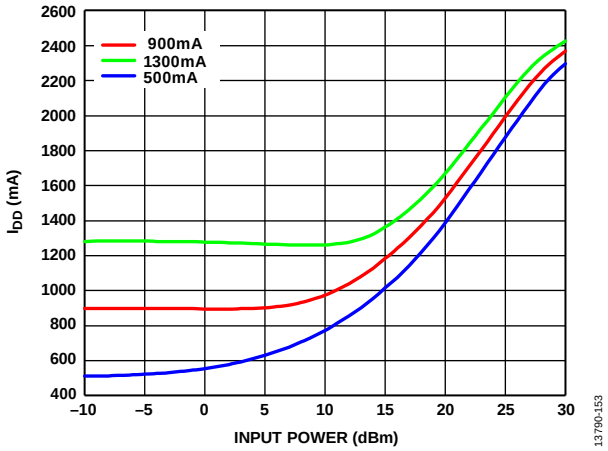


Figure 53. I_{DD} vs. Input Power over I_{DQ} at 3 GHz

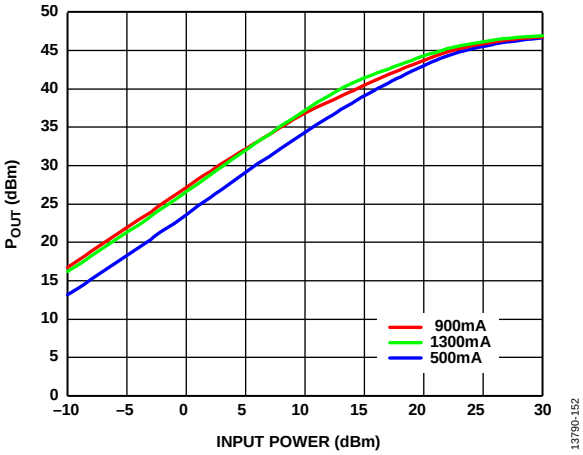


Figure 52. P_{OUT} vs. Input Power over I_{DQ} at 3 GHz

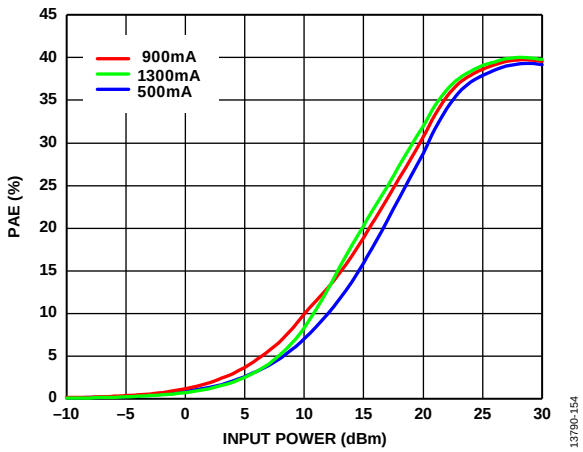


Figure 54. PAE vs. Input Power over I_{DQ} at 3 GHz

THEORY OF OPERATION

The HMC8205BCHIPS is a 35 W, GaN power amplifier consisting of two cascaded gain stages. The first stage requires only a single positive drain supply that is also used to internally generate gate bias such that a first stage drain current ($I_{DD}1$) of approximately 400 mA results for a 50 V drain voltage. The second stage is biased by a separate positive drain supply plus an externally applied negative gate supply. When using 50 V to bias the first and second stage drains together, adjust the negative voltage applied to $V_{GG}1$ such that a total quiescent drain current of 1300 mA is obtained. When biased as previously described, the HMC8205BCHIPS operates in Class A/Class B, resulting in maximum PAE at saturation. The inclusion of integrated RF chokes for each drain, on-chip dc blocking of the RFIN and RFOUT ports, and capacitive bypassing of the bias supplies improves performance, and simplifies use through the reduction in the required external component count.

APPLICATIONS INFORMATION

Figure 57 shows the basic connections for operating the HMC8205BCHIPS. The first and second stage drain bias voltages are applied via the $V_{DD}1$ and $V_{DD}2$ pads, respectively, while the second stage gate bias voltage is applied via the $V_{GG}1$ pad. A single supply can be used for both drains. Capacitive bypassing of all drain and gate pads is required as detailed in the Typical Application Circuit section. When used in a 50 Ω system, external matching components are not required for the RFIN and RFOUT ports.

RECOMMENDED BIAS SEQUENCING

The recommended power-up bias sequence follows:

1. Connect to ground.
2. Set $V_{GG}1$ to −8 V to pinch off the second stage drain current, $I_{DD}2$.
3. Set $V_{DD}1$ and $V_{DD}2$ to 50 V ($I_{DD}2$ is pinched off, while the first stage drain current, $I_{DD}1$, is approximately 400 mA).
4. Adjust $V_{GG}1$ more positive (to approximately −2.5 V) until a total supply current (I_{DQ}) = $I_{DD}1$ + $I_{DD}2$ = 1300 mA is obtained.
5. Apply the RF signal.

The recommended power-down bias sequence follows:

1. Turn off the RF signal.
2. Set $V_{GG}1$ to −8 V to pinch off $I_{DD}2$ ($I_{DD}1$ remains approximately 400 mA).
3. Set $V_{DD}1$ and $V_{DD}2$ to 0 V.
4. Set $V_{GG}1$ to 0 V.

All measurements for this device were taken using the typical application circuit (see Figure 57), configured as shown on the assembly diagram (see Figure 58). The bias conditions listed in Electrical Specifications section are the operating points recommended to optimize the overall performance. Unless otherwise noted, the data shown was taken using the recommended bias conditions (V_{DD} = 50 V and I_{DQ} = 1300 mA). Operation of the HMC8205BCHIPS at other bias conditions may provide performance that differs from what is shown in this data sheet. Some applications may benefit from the reduced power consumption afforded by the use of lower drain voltages and/or lower quiescent drain currents. Lower drain bias operating voltages result in overall lower saturated output power and diminished output linearity. For applications that require a lower overall power consumption, total supply drain currents as low as 500 mA can be used with minimal saturated performance degradation. To understand the trade-offs between dc bias and performance, see Figure 51 through Figure 54.

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

Attach the die directly to the ground plane eutectically or with high thermal conductive epoxy (see the Handling Precautions section).

To bring the radio frequency signal to and from the chip, it is recommended to implement 50 Ω transmission lines using microstrip or coplanar waveguide fabricated on 0.127 mm (0.005 inches) thick alumina thin film substrates (see Figure 55). When using 0.254 mm (0.010 inches) thick substrates, it is recommended that a 0.127 mm (0.005 inches) thick molybdenum (Mo) heat spreader (moly tab) be used to raise the die such that the additional height contributed by the moly tab and die attach layer result in coplanarity (see Figure 56).

Place microstrip substrates as close to the die as possible to minimize bond wire length. Typical die to substrate spacing is 0.076 mm to 0.127mm (0.003 inches to 0.005 inches).

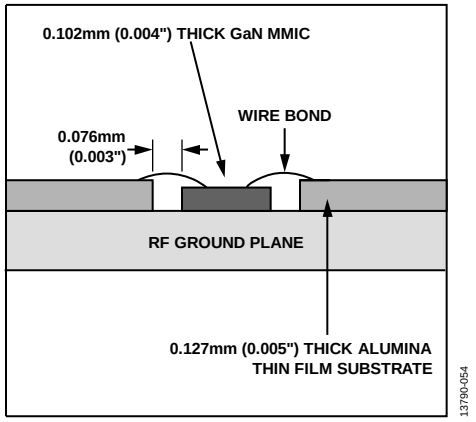


Figure 55. Die Without the Moly Tab

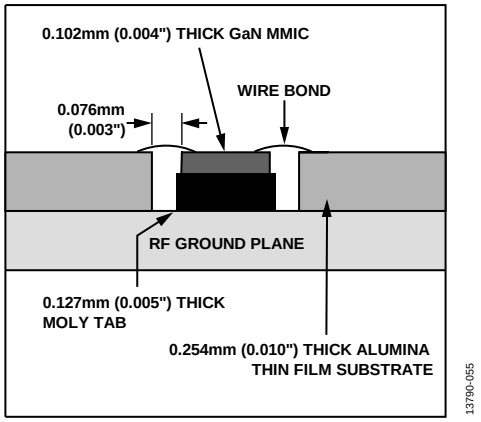


Figure 56. Die With the Moly Tab

Handling Precautions

To avoid permanent damage, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

- Place all bare die in either waffle or gel-based ESD protective containers and then seal the die in an ESD protective bag for shipment. After the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
- Handle the chips in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.
- Follow ESD precautions to protect against ESD strikes.
- While bias is applied, suppress instrument and bias supply transients. Use shielded signal and bias cables to minimize inductive pickup.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip can have fragile air bridges and must not be touched with a vacuum collet, tweezers, or fingers.

TYPICAL APPLICATION CIRCUIT

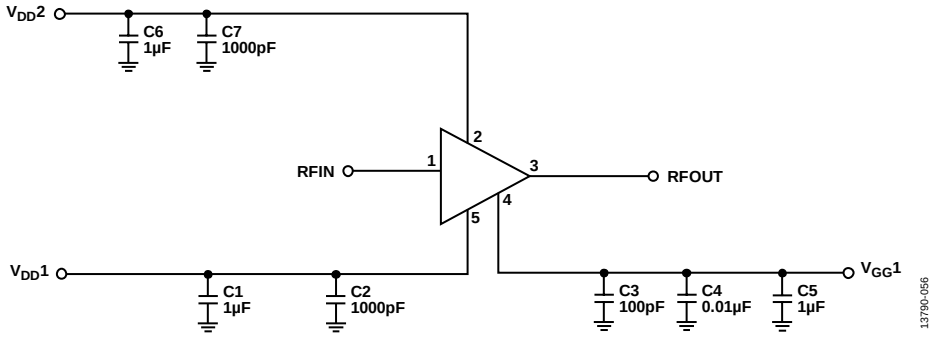


Figure 57. Typical Application Circuit

Table 8. Capacitor Values

Reference Designator	Description	Part Number	Manufacturer
C1, C5, and C6	1 µF capacitors, 100 V	GRM31CR72A105KA01	Murata
C2 and C7	1000 pF capacitors, 100 V	V30BZ102M6SX	Knowles Capacitors/Dielectric Laboratories
C3	100 pF capacitor, 16 V	SA1212B101MGH5N-L	Presidio Components
C4	0.01 µF capacitor, 16 V	MVL3030X103MGH5C	Presidio Components

ASSEMBLY DIAGRAM

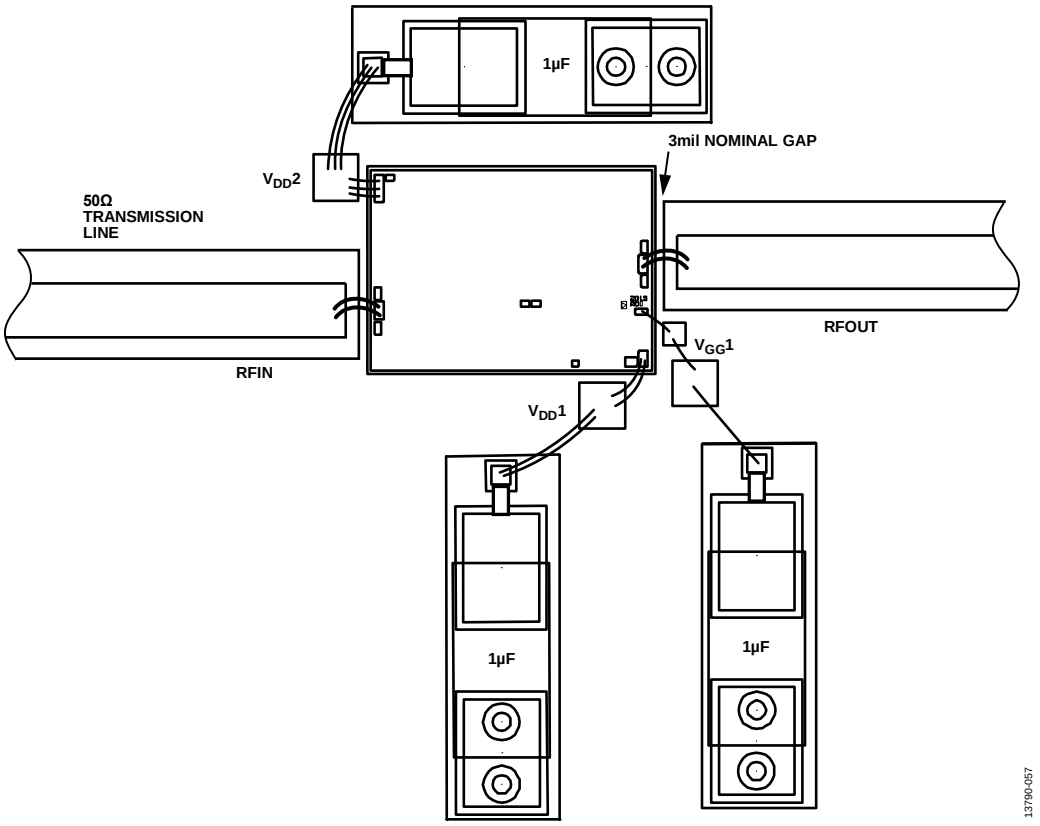


Figure 58. Assembly Diagram

OUTLINE DIMENSIONS

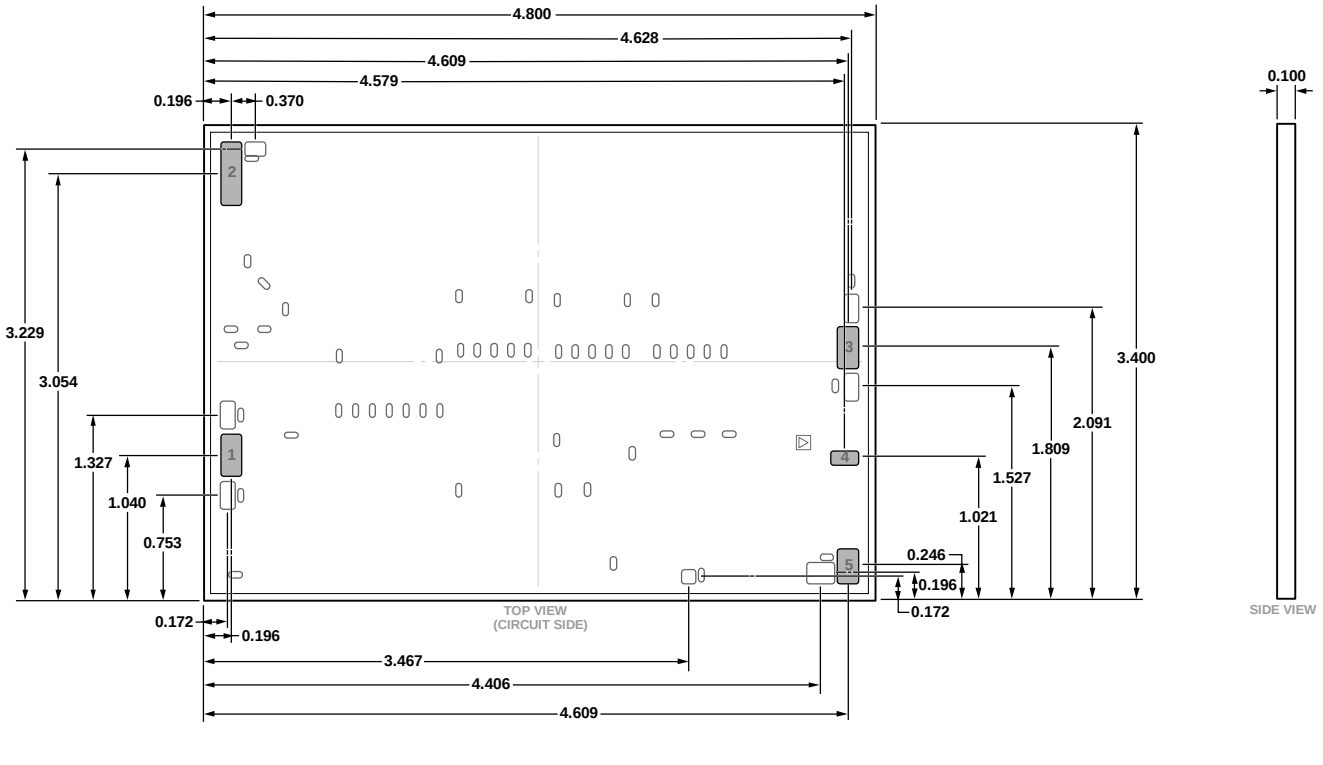


Figure 59. 5-Pad Bare Die [CHIP]
(C-5-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
HMC8205BCHIPS	−55°C to +85°C	5-Pad Bare Die [CHIP]	C-5-7

[1] The HMC8205BCHIPS is a RoHS compliant part.

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