CMOS, Low Voltage, 4 Ω Dual SPST Switches in 3 mm × 2 mm LFCSP

Data Sheet

ADG721/ADG722/ADG723

FEATURES

- 1.8 V to 5.5 V single supply
- 4 Ω (max) on resistance
- Low on resistance flatness
- −3 dB bandwidth >200 MHz
- Tiny package options
  - 8-lead MSOP
  - 3 mm × 2 mm LFCSP (A grade)
- Fast switching times
  - t_{ON}, 20 ns
  - t_{OFF}, 10 ns
- Low power consumption (<0.1 µW)
- TTL/CMOS compatible

APPLICATIONS

- USB 1.1 signal switching circuits
- Cell phones
- PDAs
- Battery-powered systems
- Communication systems
- Sample hold systems
- Audio signal routing
- Video switching
- Mechanical reed relay replacement

FUNCTIONAL BLOCK DIAGRAMS

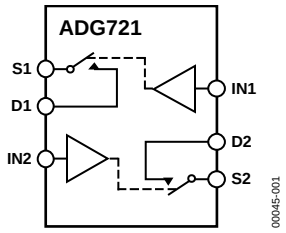

Figure 1.

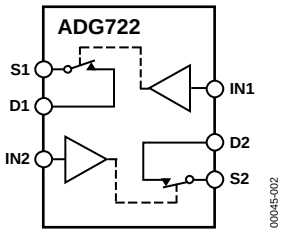

Figure 2.

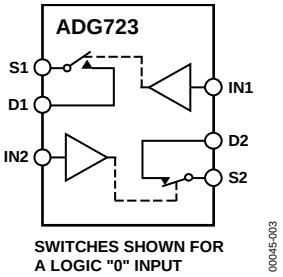

Figure 3.

GENERAL DESCRIPTION

The ADG721, ADG722, and ADG723 are monolithic CMOS SPST switches. These switches are designed on an advanced submicron process that provides low power dissipation yet gives high switching speed, low on resistance, and low leakage currents. The devices are packaged in both a tiny 3 mm × 2 mm LFCSP and an MSOP, making them ideal for space-constrained applications.

The ADG721, ADG722, and ADG723 are designed to operate from a single 1.8 V to 5.5 V supply, making them ideal for use in battery-powered instruments and with the new generation of DACs and ADCs from Analog Devices, Inc.

The ADG721, ADG722, and ADG723 contain two independent single-pole/single-throw (SPST) switches. The ADG721 and ADG722 differ only in that both switches are normally open and normally closed, respectively. In the ADG723, Switch 1 is normally open and Switch 2 is normally closed.

Each switch of the ADG721, ADG722, and ADG723 conducts equally well in both directions when on. The ADG723 exhibits break-before-make switching action.

PRODUCT HIGHLIGHTS

1. 1.8 V to 5.5 V single-supply operation.
2. Very low R_{ON} (4 Ω max at 5 V, 10 Ω max at 3 V).
3. Low on resistance flatness.
4. −3 dB bandwidth >200 MHz.
5. Low power dissipation. CMOS construction ensures low power dissipation.
6. 8-lead MSOP and 3 mm × 2 mm LFCSP.

Rev. E

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SPECIFICATIONS

V_{DD} = 5 V ± 10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	A, B Grade[1] +25°C	A, B Grade[1] −40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance, R_{ON}	2.5		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
	4	5	Ω max	See Figure 12
On Resistance Match Between Channels, ΔR_{ON}	0.3		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
		1.0	Ω max	
On Resistance Flatness, $R_{FLAT(ON)}$	0.85		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
		1.5	Ω max	
LEAKAGE CURRENTS – A Grade				V_{DD} = 5.5 V
Source off Leakage, I_S (OFF)	±0.01		nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V, see Figure 13
Drain off Leakage, I_D (OFF)	±0.01		nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V, see Figure 13
Channel on Leakage, I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = 1 V or V_S = V_D = 4.5 V, see Figure 14
LEAKAGE CURRENTS – B Grade				V_{DD} = 5.5 V
Source off Leakage, I_S (OFF)	±0.01		nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V
	±0.25	±0.35	nA max	Test Circuit 2
Drain off Leakage, I_D (OFF)	±0.01		nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V
	±0.25	±0.35	nA max	See Figure 13
Channel on Leakage, I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = 1 V or V_S = V_D = 4.5 V
	±0.25	±0.35	nA max	See Figure 14
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	14		ns typ	R_L = 300 Ω, C_L = 35 pF
		20	ns max	V_S = 3 V, see Figure 15
t_{OFF}	6		ns typ	R_L = 300 Ω, C_L = 35 pF
		10	ns max	V_S = 3 V, see Figure 15
Break-Before-Make Time Delay, t_D (ADG723 Only)	7		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_{S1} = V_{S2} = 3 V, see Figure 16
Charge Injection	2		pC typ	V_S = 2 V, R_S = 0 Ω, C_L = 1 nF, see Figure 17
Off Isolation	−60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 18
Channel-to-Channel Crosstalk	−77		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−97		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 19
Bandwidth −3 dB	200		MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 20
C_S (OFF)	7		pF typ	
C_D (OFF)	7		pF typ	
C_D, C_S (ON)	18		pF typ	
POWER REQUIREMENTS				V_{DD} = 5.5 V
I_{DD}	0.001		μA typ	Digital inputs = 0 V or 5 V
		1.0	μA max	

[1] Temperature range: A, B grades, −40°C to +85°C. All specifications apply to both grades unless otherwise stated.
[2] Guaranteed by design; not subject to production test.

V_{DD} = 3 V ± 10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	A, B Grades[1] +25°C	A, B Grades[1] −40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance, R_{ON}	6.5		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
		10	Ω max	See Figure 12
On Resistance Match Between Channels, ΔR_{ON}	0.3		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
		1.0	Ω max	
On Resistance Flatness, $R_{FLAT(ON)}$	3.5		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
LEAKAGE CURRENTS – A Grade				V_{DD} = 3.3 V
Source off Leakage, I_S (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V, see Figure 13
Drain off Leakage, I_D (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V, see Figure 13
Channel on Leakage, I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = 1 V or 3 V, Figure 14
LEAKAGE CURRENTS – B Grade				V_{DD} = 3.3 V
Source off Leakage, I_S (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V
	±0.25	±0.35	nA max	See Figure 13
Drain off Leakage, I_D (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V
	±0.25	±0.35	nA max	See Figure 13
Channel on Leakage, I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = 1 V or 3 V
	±0.25	±0.35	nA max	See Figure 14
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.4	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	16		ns typ	R_L = 300 Ω, C_L = 35 pF
		24	ns max	V_S = 2 V, see Figure 15
t_{OFF}	7		ns typ	R_L = 300 Ω, C_L = 35 pF
		11	ns max	V_S = 2 V, see Figure 15
Break-Before-Make Time Delay, t_D (ADG723 Only)	7		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_{S1} = V_{S2} = 2 V, see Figure 16
Charge Injection	2		pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF, see Figure 17
Off Isolation	−60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 18
Channel-to-Channel Crosstalk	−77		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−97		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 19
Bandwidth −3 dB	200		MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 20
C_S (OFF)	7		pF typ	
C_D (OFF)	7		pF typ	
C_D, C_S (ON)	18		pF typ	
POWER REQUIREMENTS				V_{DD} = 3.3 V
I_{DD}	0.001		μA typ	Digital inputs = 0 V or 3 V
		1.0	μA max	

[1] Temperature range: A, B Grades, −40°C to +85°C. All specifications apply to both grades unless otherwise stated.
[2] Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog, Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Continuous Current, S or D	30 mA
Operating Temperature Range	
Industrial (A, B Grade)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
8-Lead MSOP	
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
8-Lead LFCSP (4-Layer Board)	
θ_{JA} Thermal Impedance[1]	50.8°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Lead-Free Temperature, Soldering	
IR Reflow, Peak Temperature	260°C (+0/−5°C)
Time at Peak Temperature	10 sec to 40 sec
ESD	2 kV

[1]Assumes exposed paddle is tied to ground.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND PIN DESCRIPTIONS

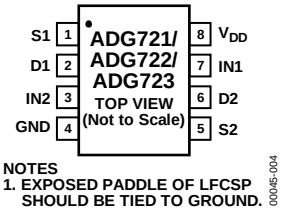

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Descriptions
1	S1	Source Pin 1. May be an input or an output.
2	D1	Drain Pin 1. May be an input or an output.
3	IN2	Logic Control Input for Switch S2→D2.
4	GND	Ground (0 V) Reference.
5	S2	Source Pin 2. May be an input or an output.
6	D2	Drain Pin 2. May be an input or an output.
7	IN1	Logic Control Input for Switch S1→D1.
8	V_{DD}	Positive Power Supply Input.

Table 5. Truth Table (ADG721/ADG722)

ADG721 In	ADG722 In	Switch Condition
0	1	Off
1	0	On

Table 6. Truth Table (ADG723)

Logic	Switch 1	Switch 2
0	Off	On
1	On	Off

TERMINOLOGY

V_{DD}
Most positive power supply potential.

GND
Ground (0 V) reference.

S
Source terminal. May be an input or output.

D
Drain terminal. May be an input or output.

IN
Logic control input.

R_{ON}
Ohmic resistance between D and S.

ΔR_{ON}
On resistance match between any two channels, that is, R_{ON} max − R_{ON} min.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (OFF)
Source leakage current with the switch off.

I_D (OFF)
Drain leakage current with the switch off.

I_D, I_S (ON)
Channel leakage current with the switch on.

V_D (V_S)
Analog voltage on the D and S terminals.

C_S (OFF)
Off switch source capacitance.

C_D (OFF)
Off switch drain capacitance.

C_D, C_S (ON)
On switch capacitance.

t_{ON}
Delay between applying the digital control input and the output switching on.

t_{OFF}
Delay between applying the digital control input and the output switching off.

t_D
Off time or on time measured between the 90% points of both switches, when switching from one address state to another (ADG723 only).

Crosstalk
A measure of unwanted signal that is the result of parasitic capacitance.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Charge Injection
A measure of the glitch impulse transferred during switching.

TYPICAL PERFORMANCE CHARACTERISTICS

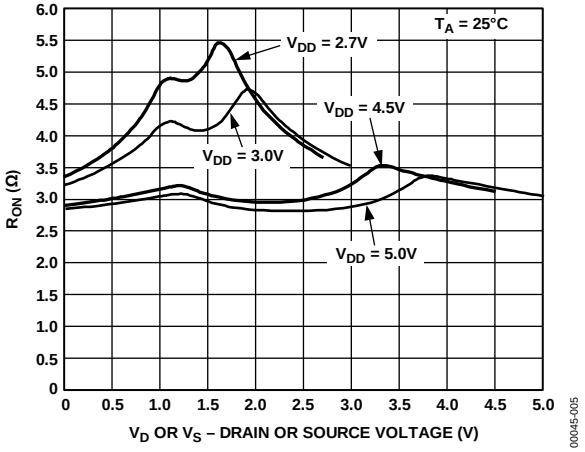

Figure 5. On Resistance as a Function of V_D (V_S), Single Supplies

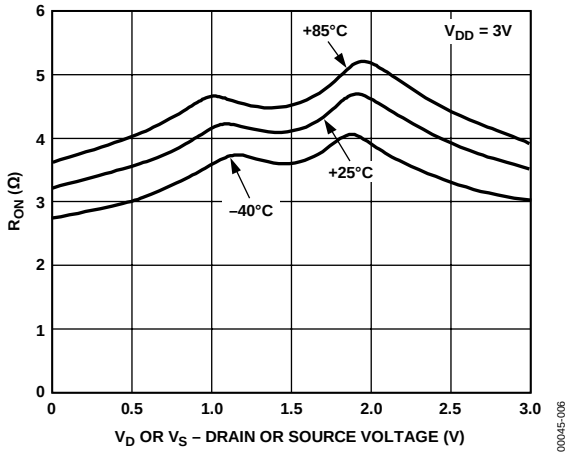

Figure 6. On Resistance as a Function of a V_D (V_S) for Different Temperatures, V_{DD} = 3 V

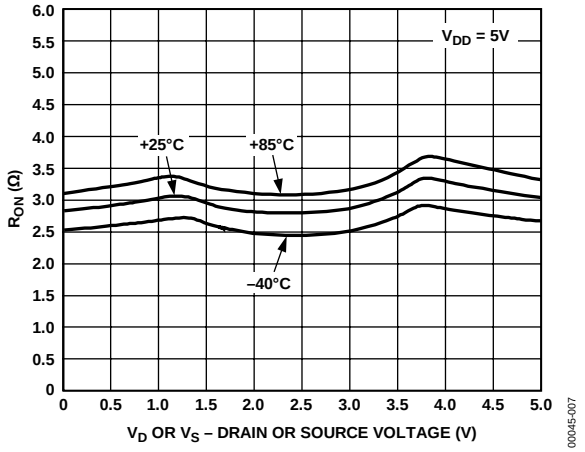

Figure 7. On Resistance as a Function of V_D (V_S) for Different Temperatures, V_{DD} = 5 V

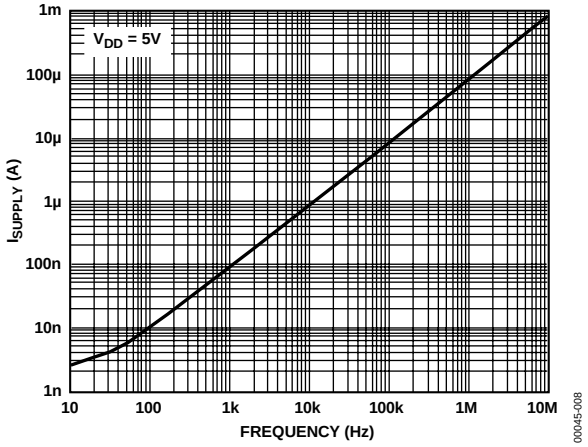

Figure 8. Supply Current vs. Input Switching Frequency

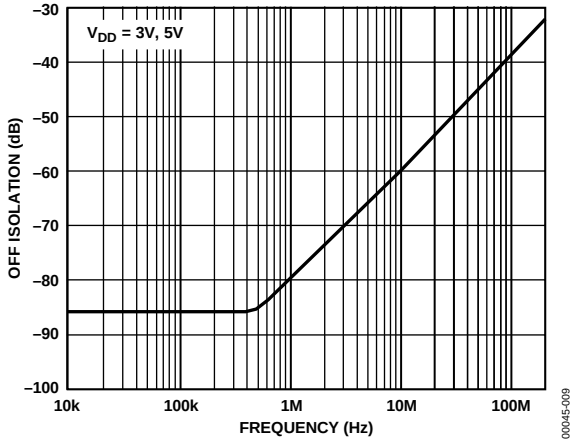

Figure 9. Off Isolation vs. Frequency

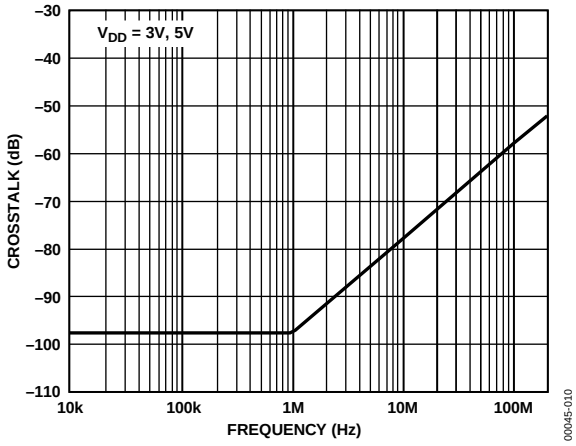

Figure 10. Crosstalk vs. Frequency

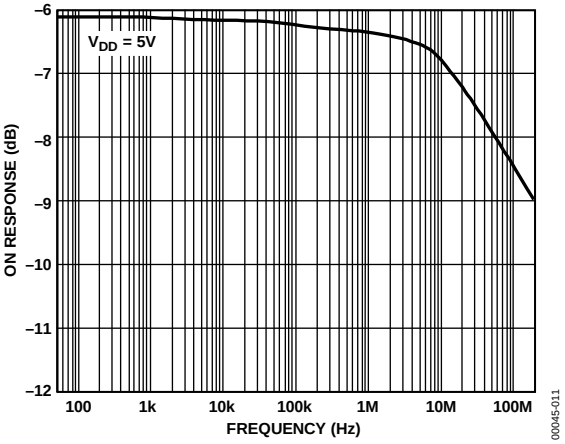

Figure 11. On Response vs. Frequency

TEST CIRCUITS

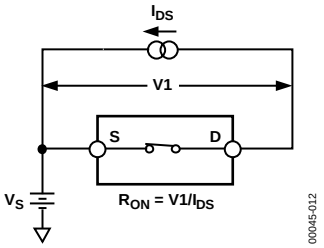

Figure 12. On Resistance

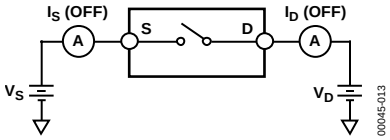

Figure 13. Off Leakage

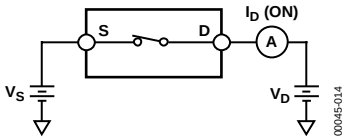

Figure 14. On Leakage

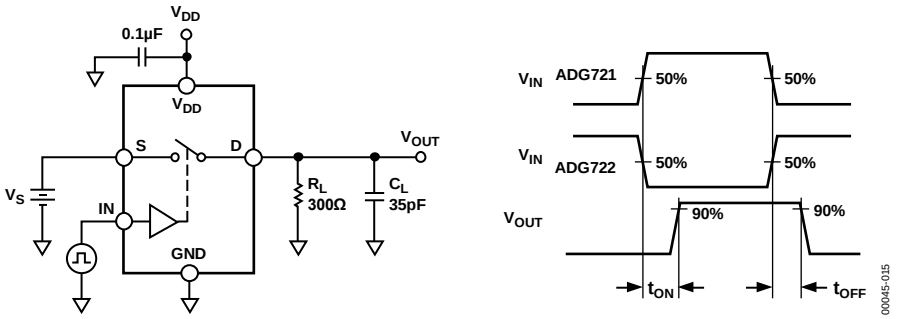

Figure 15. Switching Times

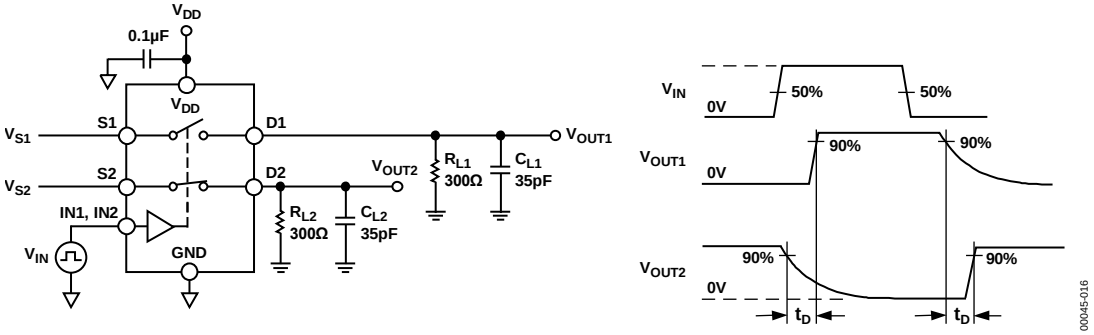

Figure 16. Break-Before-Make Time Delay, t_D (ADG723 Only)

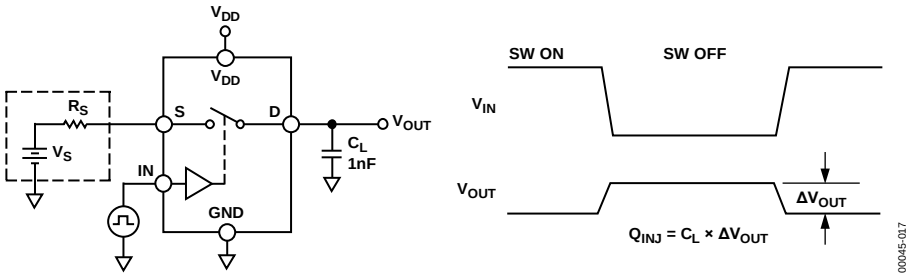

Figure 17. Charge Injection

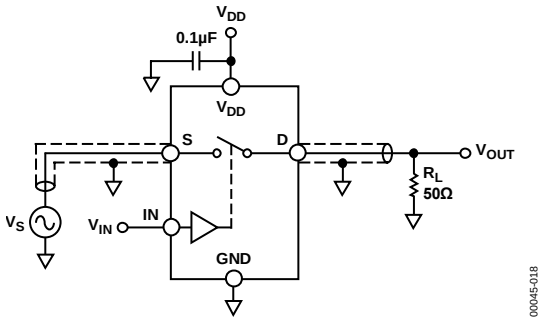

Figure 18. Off Isolation

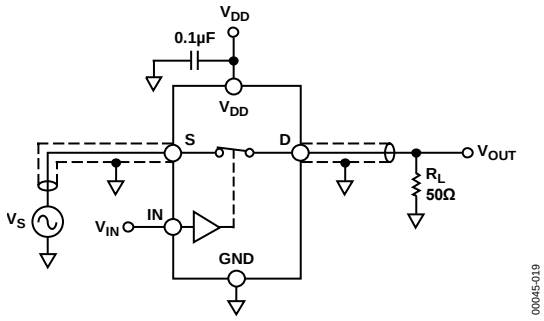

Figure 19. Channel-to-Channel Crosstalk

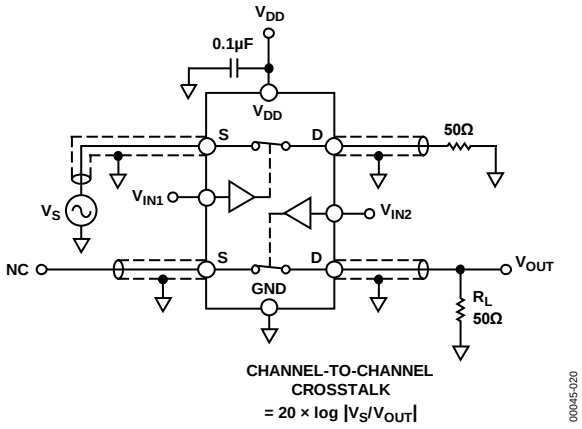

Figure 20. Bandwidth

APPLICATIONS

The ADG721/ADG722/ADG723 belong to a new family of Analog Devices CMOS switches. This series of general-purpose switches has improved switching times, lower on resistance, higher bandwidths, low power consumption, and low leakage currents.

ADG721/ADG722/ADG723 SUPPLY VOLTAGES

Functionality of the ADG721/ADG722/ADG723 extends from a 1.8 V to a 5.5 V single supply, which makes it ideal for battery-powered instruments, where important design parameters are power efficiency and performance.

It is important to note that the supply voltage affects the input signal range, the on resistance, and the switching times of the part. The typical performance characteristics and the specifications clearly show the effects of the power supplies.

For V_{DD} = 1.8 V, on resistance is typically 40 Ω over the temperature range.

ON RESPONSE VS. FREQUENCY

Figure 21 illustrates the parasitic components that affect the ac performance of CMOS switches (the switch is shown surrounded by a box). Additional external capacitances further degrade some aspects of performance. These capacitances affect feedthrough, crosstalk, and system bandwidth.

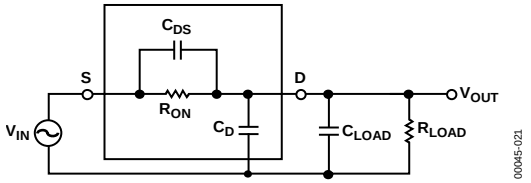

Figure 21. Switch Represented by Equivalent Parasitic Components

The transfer function that describes the equivalent diagram of the switch (Figure 21) is of the form (A)s, as shown in the following equation:

$$A(s) = R_T\left[\frac{s(R_{ON}\ C_{DS})+1}{s(R_{ON}\ C_T\ R_T)+1}\right]$$

where:
$C_T = C_{LOAD} + C_D + C_{DS}$
$R_T = R_{LOAD}/(R_{LOAD} + R_{ON})$

The signal transfer characteristic is dependent on the switch channel capacitance, C_{DS}. This capacitance creates a frequency zero in the numerator of the transfer function A(s). Because the switch on resistance is small, this zero usually occurs at high frequencies. The bandwidth is a function of the switch output capacitance combined with C_{DS} and the load capacitance. The frequency pole corresponding to these capacitances appears in the denominator of A(s).

The dominant effect of the output capacitance, C_D, causes the pole breakpoint frequency to occur first. Therefore, in order to maximize bandwidth, a switch must have a low input and output capacitance and low on resistance (see Figure 11).

OFF ISOLATION

Off isolation is a measure of the input signal coupled through an off switch to the switch output. The capacitance, C_{DS}, couples the input signal to the output load, when the switch is off, as shown in Figure 22.

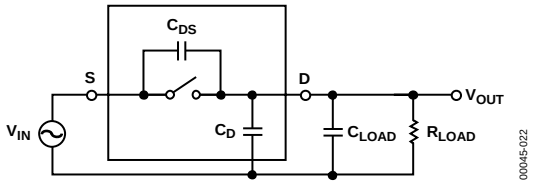

Figure 22. Off Isolation Is Affected by External Load Resistance and Capacitance

The larger the value of C_{DS}, the larger the value of feedthrough produced. Figure 9 illustrates the drop in off isolation as a function of frequency. From dc to roughly 1 MHz, the switch shows better than −80 dB isolation. Up to frequencies of 10 MHz, the off isolation remains better than −60 dB. As the frequency increases, more and more of the input signal is coupled through to the output. Off isolation can be maximized by choosing a switch with the smallest C_{DS} possible. The values of load resistance and capacitance also affect off isolation because they contribute to the coefficients of the poles and zeros in the transfer function of the switch when open.

$$A(s) = \left[\frac{s(R_{LOAD}\ C_{DS})}{s(R_{LOAD})(C_{LOAD} + C_D + C_{DS})+1}\right]$$

OUTLINE DIMENSIONS

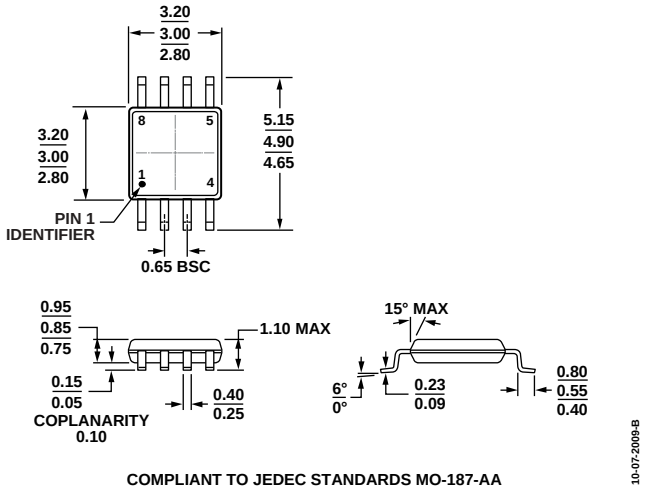

Figure 23. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

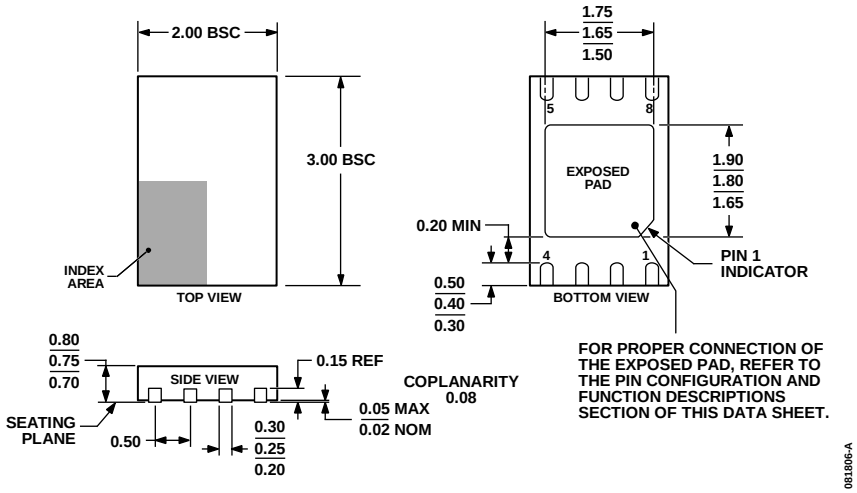

Figure 24. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 2 mm Body, Very Very Thin, Dual Lead
(CP-8-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding[2]
ADG721BRM	−40°C to +85°C	8-Lead MSOP	RM-8	S6B
ADG721BRM-REEL	−40°C to +85°C	8-Lead MSOP	RM-8	S6B
ADG721BRM-REEL7	−40°C to +85°C	8-Lead MSOP	RM-8	S6B
ADG721BRMZ	−40°C to +85°C	8-Lead MSOP	RM-8	#S6B
ADG721BRMZ-REEL	−40°C to +85°C	8-Lead MSOP	RM-8	#S6B
ADG721BRMZ-REEL7	−40°C to +85°C	8-Lead MSOP	RM-8	#S6B
ADG721ACPZ-REEL	−40°C to +85°C	8-Lead LFCSP_WD	CP-8-4	17
ADG721ACPZ-REEL7	−40°C to +85°C	8-Lead LFCSP_WD	CP-8-4	17
ADG722BRM	−40°C to +85°C	8-Lead MSOP	RM-8	S7B
ADG722BRM-REEL7	−40°C to +85°C	8-Lead MSOP	RM-8	S7B
ADG722BRMZ	−40°C to +85°C	8-Lead MSOP	RM-8	#S7B
ADG722BRMZ-REEL	−40°C to +85°C	8-Lead MSOP	RM-8	#S7B
ADG722BRMZ-REEL7	−40°C to +85°C	8-Lead MSOP	RM-8	#S7B
ADG722ACPZ-REEL	−40°C to +85°C	8-Lead LFCSP_WD	CP-8-4	0U
ADG722ACPZ-REEL7	−40°C to +85°C	8-Lead LFCSP_WD	CP-8-4	0U
ADG723BRM	−40°C to +85°C	8-Lead MSOP	RM-8	S8B
ADG723BRM-REEL	−40°C to +85°C	8-Lead MSOP	RM-8	S8B
ADG723BRM-REEL7	−40°C to +85°C	8-Lead MSOP	RM-8	S8B
ADG723BRMZ	−40°C to +85°C	8-Lead MSOP	RM-8	#S8B
ADG723BRMZ-REEL	−40°C to +85°C	8-Lead MSOP	RM-8	#S8B
ADG723BRMZ-REEL7	−40°C to +85°C	8-Lead MSOP	RM-8	#S8B
ADG723ACPZ-REEL	−40°C to +85°C	8-Lead LFCSP_WD	CP-8-4	S2N
ADG723ACPZ-REEL7	−40°C to +85°C	8-Lead LFCSP_WD	CP-8-4	S2N

[1] Z = RoHS Compliant Part; # denotes lead-free product may be top or bottom marked.
[2] Branding = due to package size limitations, these three characters represent the part number.

NOTES

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