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APPLICATION NOTE 3939

DC-DC Controllers Use Average-Current-Mode Control for Infotainment Applications

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Abstract: Auto infotainment products (multimedia and telematics) are demanding more power and challenging a vehicle's power-management systems. This application note explains average-current-mode control (ACMC) technology for power management. The article demonstrates that this technology minimizes several power-management problems, including efficiency, size, EMI, transient response, design complexity, and overall cost. The MAX5060/MAX5061 will serve as examples of the technique.

Introduction

As high-performance microprocessors demand more power in auto multimedia and telematics, (e.g., infotainment products), so do some of the well-known design problems like noise susceptibility, EMI, and loop compensation. Average-current-mode control (ACMC) helps to relieve these problems, especially in auto infotainment applications. This application note describes ACMC and explains its benefits over a current-mode control design for infotainment applications. The MAX5060/MAX5061 illustrate ACMC, and the information presented here supplements the basic narrative in the product data sheet.

Define the Design Goals

Each auto infotainment application presents a unique set of technical and commercial requirements for power management. The most important design considerations are efficiency, size, EMI, transient response, design complexity, and cost. All of these parameters are indirectly related to the power-supply switching frequency, an important parameter which is chosen to balance all these requirements.

Advantage of ACMC

For converters with relatively high output currents (5A to 25A), lowering the value of the current-sense resistor in current-mode control (CMC) techniques helps boost efficiency. In this article, CMC implies constant-frequency with peak current-sensing. There is, however, a drawback to this approach: CMC makes the converter increasingly susceptible to noise. In extreme high-current cases, even the best PCB layout cannot adequately suppress noise superimposed on the current-sense signal. One way to circumvent this problem is by using voltage-mode control, VMC, an old but proven technique. VMC improves noise immunity and efficiency, but requires a certain amount of loop compensation design to achieve acceptable performance.

ACMC Design Basics

The ACMC technique combines the noise immunity and efficiency of VMC with the stability and performance characteristics of CMC. **Figure 1** illustrates a functional block diagram of a buck converter operated in ACMC.

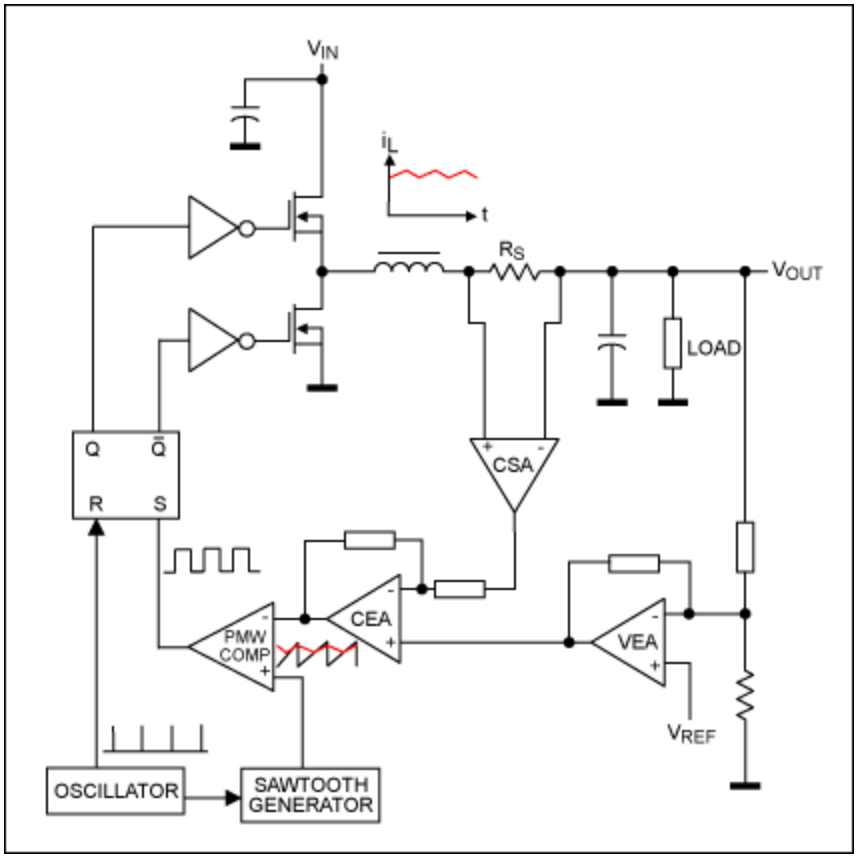

Figure 1. Functional block diagram of a buck converter operated in ACMC. In the diagram, CEA = current-error amplifier, CSA = current-sense amplifier, VEA = voltage-error amplifier. The inductor current signal, i_L, is discussed below and in Figure 2.

To better understand ACMC, one begins by reviewing the principle of CMC. By inspection of Figure 1, if the current-error amplifier (CEA) and the sawtooth generator are eliminated, the output of the current-sense amplifier (CSA) could be fed into the inverting terminal of the PWM comparator. Similarly, the output of the voltage-error amplifier (VEA) could then feed into the noninverting terminal. The result is a two-loop system which controls the inductor current (the *inner* loop) and the output voltage (the *outer* loop).

As mentioned earlier, in high-output current applications it is desirable to make the current-sense resistor, R_S (see Figure 1), as small as possible to minimize power dissipation in the converter. But the result of doing this is a shallower signal into which noise creeps and appears as jitter in the system.

With ACMC, however, the current-sense signal is fed into the inverting input of the CEA (Figure 1), whereas the VEA programs the inductor current at the CEA's noninverting input. By compensating the CEA with a feedback network, one accomplishes several things: tailor the current-sense signal to exhibit maximum gain at DC (for a buck converter, the inductor's DC current is equivalent to the converter's output current); allow the actual current-sense signal to pass unimpeded through the amplifier; and finally, dampen the high-frequency switching noise which is superimposed on the signal. The high gain

of the CEA at DC allows this control scheme to accurately program the output current. In contrast, the current-sense signal in CMC has a flat gain, causing the system to exhibit a peak-to-average current error as a result of input voltage variations. Finally from Figure 1, the CEA output is then compared to a voltage ramp, resulting in the desired PWM signal to drive the power MOSFETs.

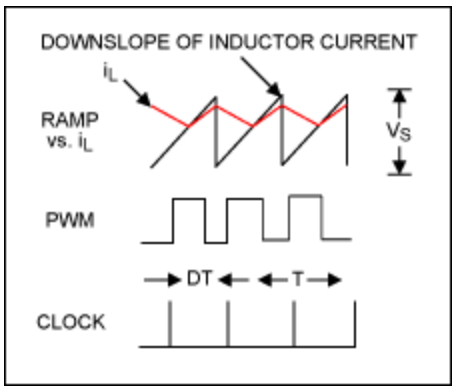

Figure 2. Control waveforms for Figure 1.

Figure 2 shows the Figure 1 control waveforms. Notice that the inductor current signal, i_L (in red), which is compared with the sawtooth waveform, is inverted. An SR latch following the PWM comparator prevents signal-bounce from occurring as a result of noise. Similarly, the clock signal resets the sawtooth ramp, virtually eliminating any possibility that noise spikes will prematurely turn off the MOSFET. Another important feature of this control technique is that no slope compensation is required when the duty-cycle exceeds 50%. This is because the sawtooth ramp already provides this compensation.

For the buck converter example in Figure 1, the inner loop compensates against variations in the input voltage. As the input voltage increases, the downslope of the current signal from the CEA becomes steeper (Figure 2), causing the duty-cycle to become narrow. The outer loop, however, compensates against changes in the output voltage, which in turn are caused by changes in the load. Since the inductor current is programmed by the VEA, the power section exhibits a single-pole response, thus simplifying the voltage-loop compensation.

Compensating the CEA is a straightforward task, provided that the recommended guidelines in the MAX5060/MAX5061 data sheet are followed. The MAX5060/MAX5061 are DC-DC controllers which address all the above design issues and contain all the features necessary for implementing an efficient, quiet, and cost-effective DC-DC converter. **Figure 3** depicts the CEA in the devices with a suggested compensation network. This network is recommended because the CEA does not offer direct access to its inverting input. Note that the CEA is a transconductance amplifier, i.e., it has a relatively high output impedance when compared to standard operational amplifiers.

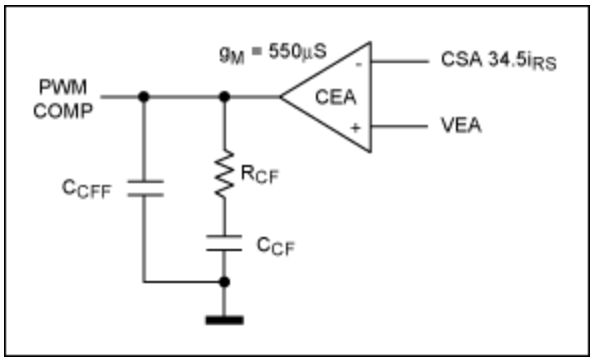

Figure 3. Suggested compensation network for the CEA in the MAX5060/MAX5061 DC-DC converters.

To optimize the current loop, the downslope of the inductor current, i_L, (the red signal in Figure 2) is made to follow the slope of the sawtooth ramp. It is also important that i_L does not exceed the ramp, otherwise subharmonic oscillations and instability can occur.

Neglecting the voltage drop across the synchronous rectifier, the downslope of the inductor current for a buck converter is given by:

$$\Delta I_L = \frac{V_O}{L} \qquad \text{(Eq. 1)}$$

This current goes through current-sense resistor, RS. The voltage across RS is measured and amplified with a gain of 34.5 by the CSA (see Figure 1). If we multiply this by the gain of the CEA, G_{CEA}, and equate it to the sawtooth slope, which is equal to V_{SfS}, we obtain the expression:

$$34.5R_S\left(\frac{V_O}{L}\right)G_{CEA} \le V_S f_S \qquad \text{(Eq. 2)}$$

Now, the gain of a transconductance amplifier is defined as $g_M R_L$. Substituting this for G_{CEA} and solving for R_L, we obtain:

$$R_L \le \frac{V_S f_S L}{34.5 R_S V_O g_M} \qquad \text{(Eq. 3)}$$

The CEA transconductance for the MAX5060/MAX5061 is given in the data sheet as 550µS; R_L in this case becomes R_{CF}, as shown in Figure 3. This resistor sets the CEA gain to unity at about the crossover frequency of the current-loop. The sawtooth ramp, V_S, in the MAX5060/MAX5061 has a peak-to-peak amplitude of 2V. Substituting these constants into the above equation, we obtain:

$$R_{CF} \le 105\frac{f_S L}{R_S V_O} \qquad \text{(Eq. 4)}$$

The DC gain of the CEA should be as high as possible to accurately program the DC output current. At DC the capacitors in the compensation network are equivalent to open circuits, thus allowing the CEA to have maximum gain at DC. Placing a zero just below the minimum crossover frequency and a pole at least one decade above the zero, causes the current-loop to exhibit a high bandwith while simultaneously attenuating unwanted switching noise.

The pole and zero are calculated by:

$$f_Z = \frac{1}{2\pi R_{CF} C_{CF}} \quad f_P = \frac{1}{2\pi R_{CF} C_{CFF}} \quad C_{CF} >> C_{CFF} \qquad \text{(Eq. 5)}$$

For the pole frequency expression in Equation 5 to hold true, C_{CF} needs to be at least 10 times greater than C_{CFF}. If this ratio is not 10:1, replace C_{CFF} with $C_{CF}||C_{CFF}$ for the pole expression. Note that there is a pole at the origin and, as one can imagine, an infinite impedance appearing across C_{CFF}. The capacitor values required are solved using the equations above.

Compensating the VEA can be a very complicated task depending on the desired level of performance. The MAX5060/MAX5061 data sheet describes a simple, yet practical compensation approach that recommends only a resistor feedback network. This forms part of an active voltage positioning technique which reduces the size of the output capacitance while providing good load transient response. If the output voltage is set slightly higher than its nominal value under minimum load conditions and allowed to fall below nominal by the same amount under full-load conditions, the DC regulation droops. Nonetheless, the maximum voltage deviation during a load transient is significantly lower than when the VEA is compensated for high low-frequency gain. In addition, the power consumption of the load also reduces.

Compensating the voltage loop for the otherwise *optimum response* requires knowledge of the gain vs. frequency characteristic of the VEA, and knowledge of the large-signal behavior of the overall loop, both over load and temperature. The knowledge of gain vs. frequency can be obtained experimentally. The VEA can then be compensated to achieve the desired performance. Enough phase margin should be allowed for stability; 45° to 60° is generally good. VEA compensating networks are derived the same way as with the CEA. The DC-DC converter should be subjected to transients like startup, load changes, recovery from short-circuit, no load conditions, and input voltage changes. If the output voltage exhibits a well-damped response over temperature for all these transient conditions, one can assume that the system is stable.

Application Hints

Adjusting the Input Voltage Range

The MAX5060/MAX5061 have an internal 5V linear regulator, which can be overridden with an external 5V source. If one feeds the input voltage to IN, the input range is specified from 7V to 28V. Feeding the input voltage to V_{CC} limits the input range from 4.75V to 5.50V. In the latter case it is recommended that IN be shorted to V_{CC} to bypass the internal regulator. To operate continuously over both input ranges, one can use the bootstrap circuit of **Figure 4**. The coupled winding in the choke is designed to create a voltage, for example, 8V, which takes over the supply to the IC, even when the voltage at IN falls under 7V. This bootstrap circuit also helps to reduce the power dissipation in the IC.

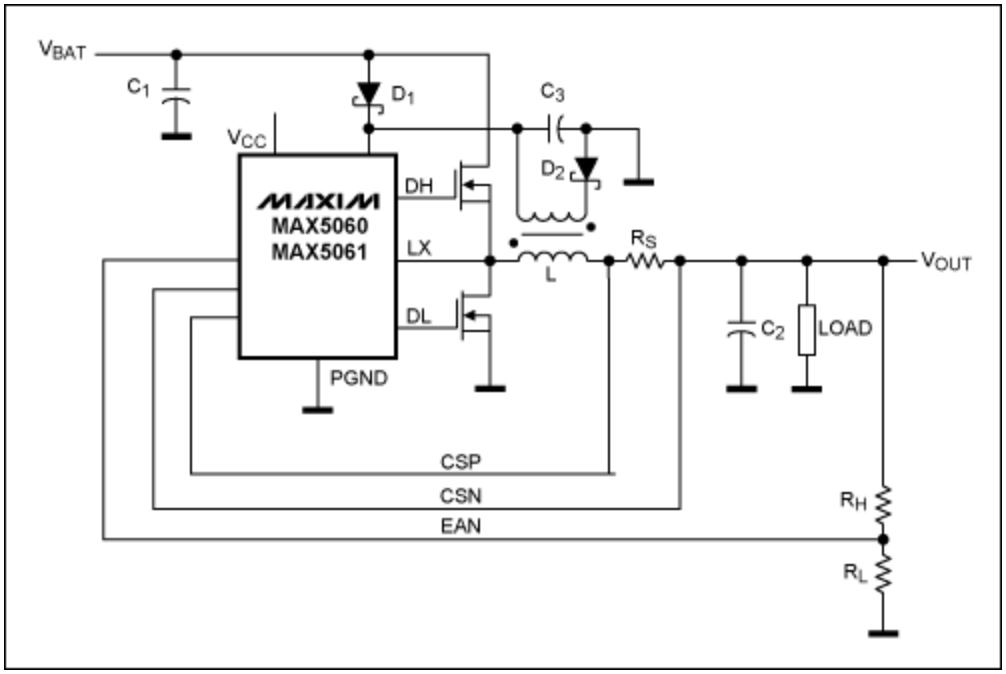

Figure 4. Example of a bootstrap circuit which extends MAX5060/MAX5061's input voltage range.

The maximum input voltage to the IC is 28V. If the converter needs to withstand a higher voltage up to 72V, the circuit of **Figure 5** is recommended. This circuit also provides reversed input-voltage protection.

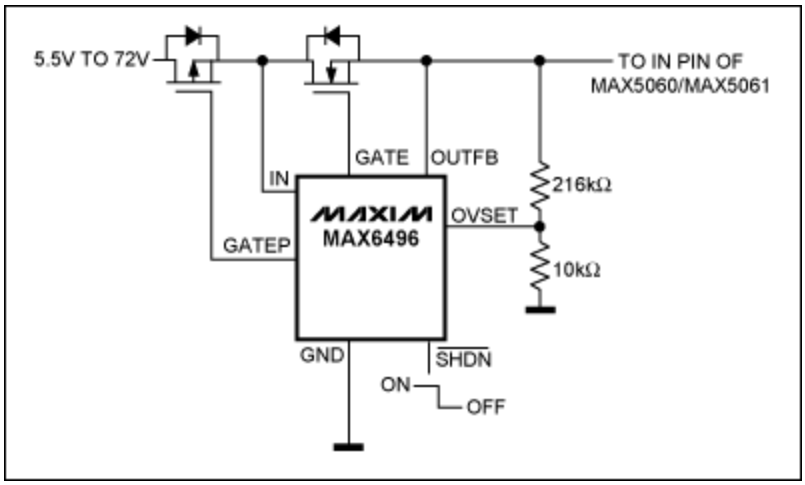

Figure 5. Use this circuit to limit the voltage to the MAX5060/MAX5061 to 28V, and to protect its circuit from reverse-battery fault conditions.

Synchronizing a Switching Frequency

Switching frequency synchronization is a very important requirement for infotainment systems to avoid interference from the DC-DC converter on sensitive loads like the car radio, TV tuner, the display monitor, or navigation system. Synchronization is usually implemented in these units is by letting the DC-DC controller's frequency free run and then by having the high-performance processor synchronize it to the desired frequency. The MAX5060/MAX5061 offer a frequency range from 125kHz to 1.5MHz which is also synchronizable.

If it is not possible to synchronize the MAX5060/MAX5061 to an external clock, or if the converter's switching frequency creates excessive EMI, a practical solution is to drive the SYNC pin by a spread-spectrum oscillator like the DS1090U-16 spread-spectrum oscillator, as shown in **Figure 6**. In this example, a switching frequency of 300kHz is programmed through a single resistor on the DS1090U-16. The dither amount is ±4% and the dither rate 1.2kHz. The dither rate should not be too high, since spread-spectrum causes a phase-shift in the system loop which needs to be compensated. A frequency calculator for the DS1090 is available free for downloading in application note 3692, "Frequency Calculator for the DS1090".

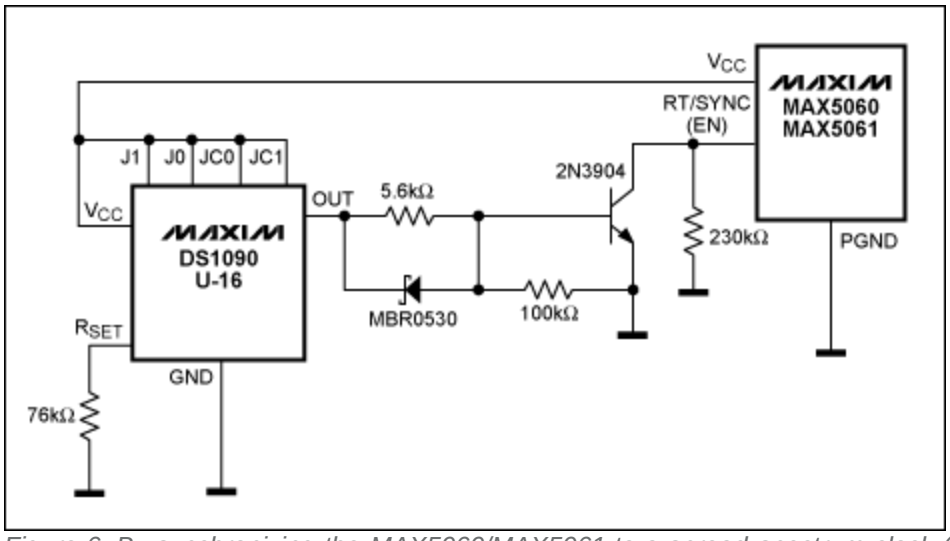

Figure 6. By synchronizing the MAX5060/MAX5061 to a spread-spectrum clock (DS1090), peak radiated emissions are significantly reduced.

Buck-Boost Operation

The MAX5060/MAX5061 also lends itself to implementing a buck-boost converter (**Figure 7**).

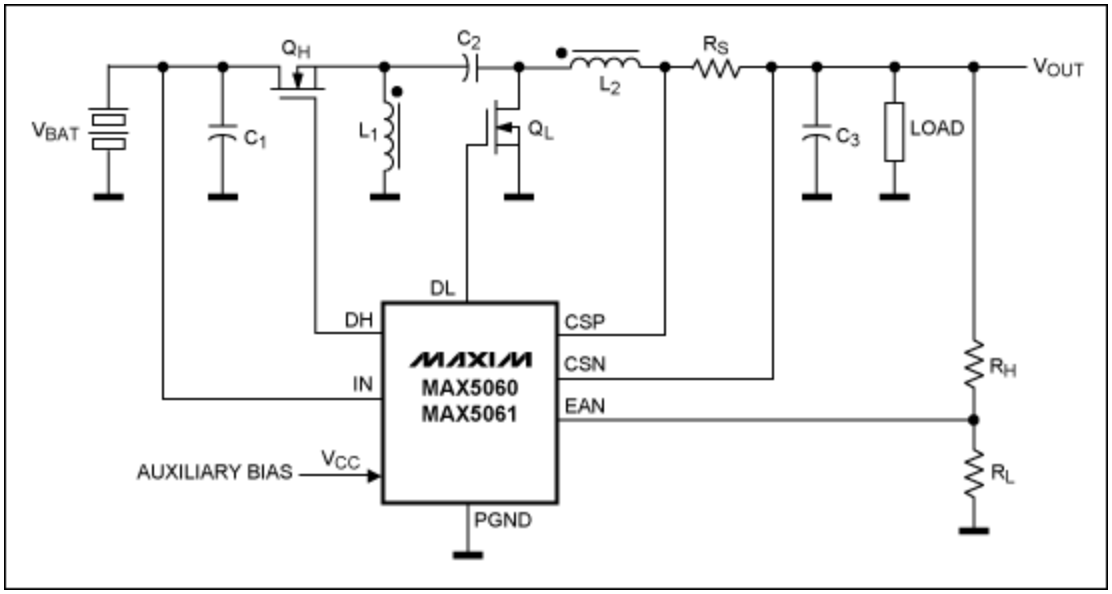

Figure 7. Simplified buck-boost converter implemented by using the MAX5060/MAX5061.

Note that in Figure 7 capacitors C_1 and C_2 need to withstand a greater ripple current than the output capacitor of a buck converter of an equivalent output current. Notice also that the two inductors shown can be wound on the same core; if this is done, note the orientation dots by L_1 and L_2 in Figure 7. These dots can be ignored if two separate inductors are used.

The common-mode range of the CSA in the MAX5060/MAX5061 extends from 0 to 5.5V. When designing converters for an output voltage greater than 5V, two circuits can be recommended. The circuit in **Figure 8** employs an off-the-shelf current-sense transformer, while the one in **Figure 9** uses a resistor bridge. Use 0.1% resistors for the design. To reduce the size and power dissipation of resistor kR_S, V_{RS} is biased up to 5V. Because the EAN input should be set to 0.6V, a separate voltage-divider is required.

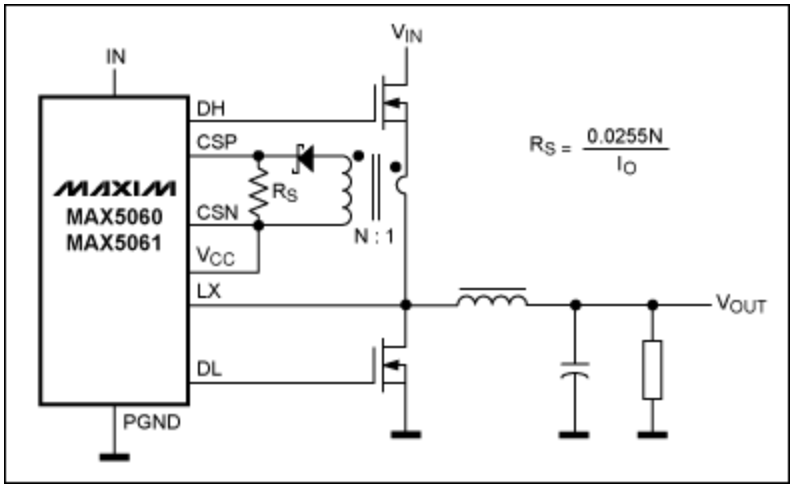

Figure 8. Current-sense method using a current-sense transformer.

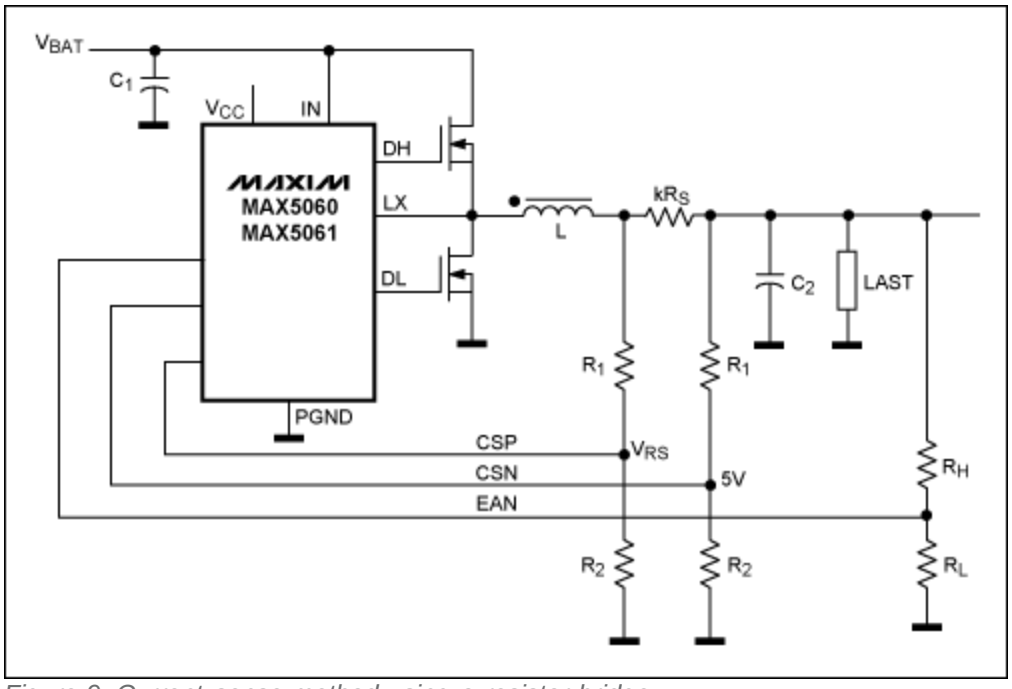

Figure 9. Current-sense method using a resistor bridge.

Conclusion

Although CMC has been advocated by designers as an excellent technique for operating DC-DC converters, the requirement for increased efficiency from inexpensive current-sense resistors has exposed one of CMC's major shortcomings: noise susceptibility. The technique of ACMC employed in the MAX5060/MAX5061 solves this noise concern and other problems. ACMC enables the design of DC-DC converters that meet the requirements of high-performance microprocessors, especially those found in automotive multimedia and telematics systems.

A similar article appeared in the March, 2006 issue of *Elektronik Informationen*.

Related Parts		
DS1090	Low-Frequency, Spread-Spectrum EconOscillator	Free Samples
MAX5060	0.6V to 5.5V Output, Parallelable, Average-Current-Mode DC-DC Controllers	Free Samples
MAX5061	0.6V to 5.5V Output, Parallelable, Average-Current-Mode DC-DC Controllers	Free Samples
MAX6496	72V, Overvoltage-Protection Switches/Limiter Controllers with an External MOSFET	Free Samples

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