

**DUT CONNECTIONS**

The diagram illustrates the pin connections for the SI5332-40-QFN integrated circuit. The chip is connected to several power supplies and ground:

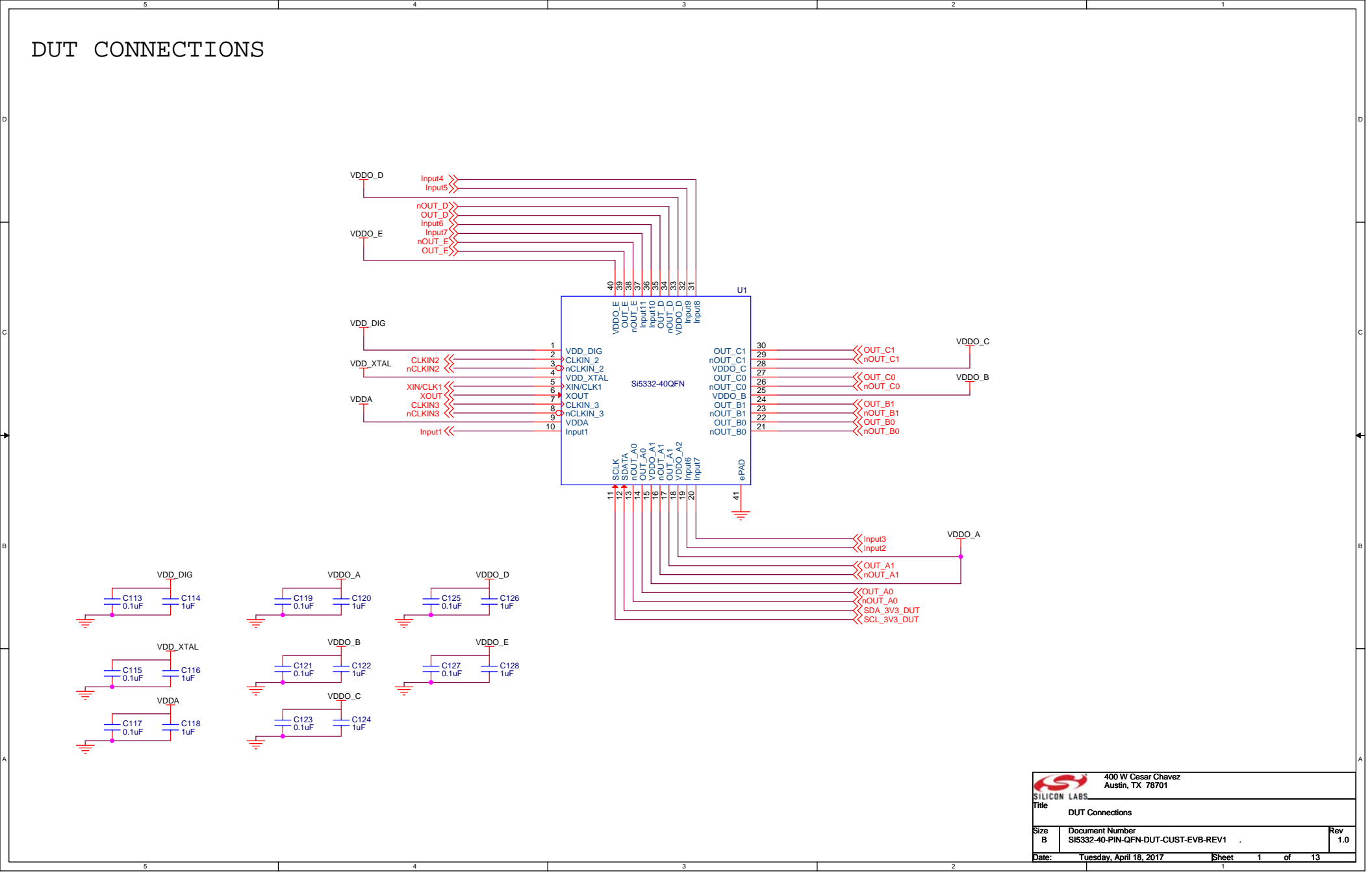
- VDDO\_D** and **VDDO\_E** are connected to pins 39, 38, 37, 36, 35, 34, 33, 32, and 31.
- VDD\_DIG** is connected to pin 1.
- VDD\_XTAL** is connected to pins 2 and 3.
- VDDA** is connected to pins 4, 5, 6, 7, 8, 9, and 10.
- VDDO\_C** is connected to pins 30, 29, 28, 27, 26, 25, 24, 23, 22, and 21.
- VDDO\_B** is connected to pins 20, 19, 18, 17, 16, 15, 14, 13, 12, and 11.
- VDDO\_A** is connected to pins 10, 9, 8, 7, 6, 5, 4, 3, 2, and 1.

The chip also has several input/output pins for digital signals, clocks, and control:

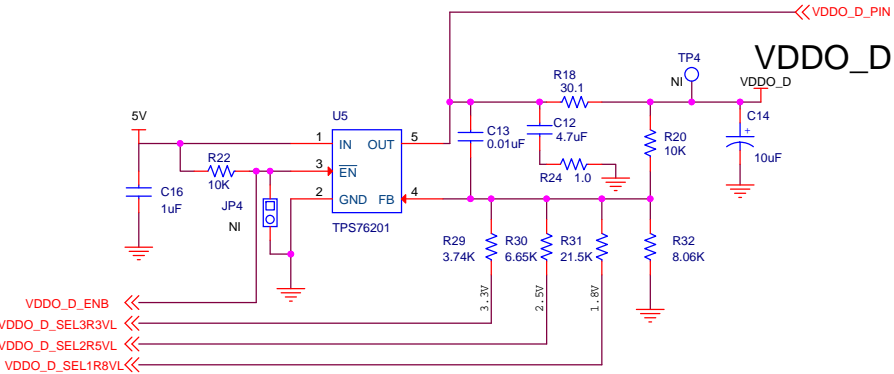
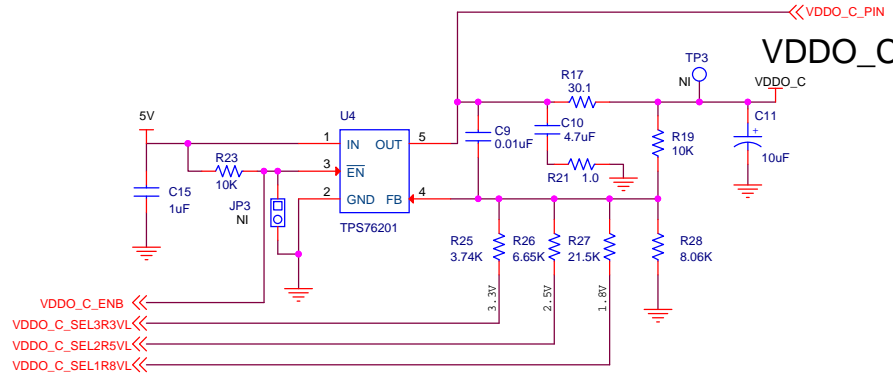
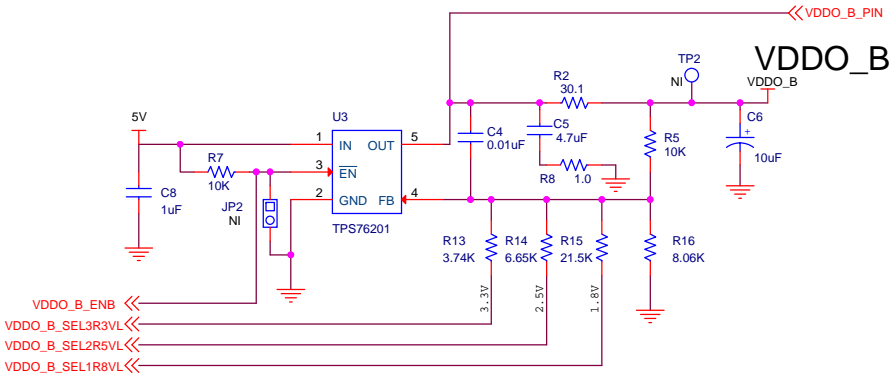
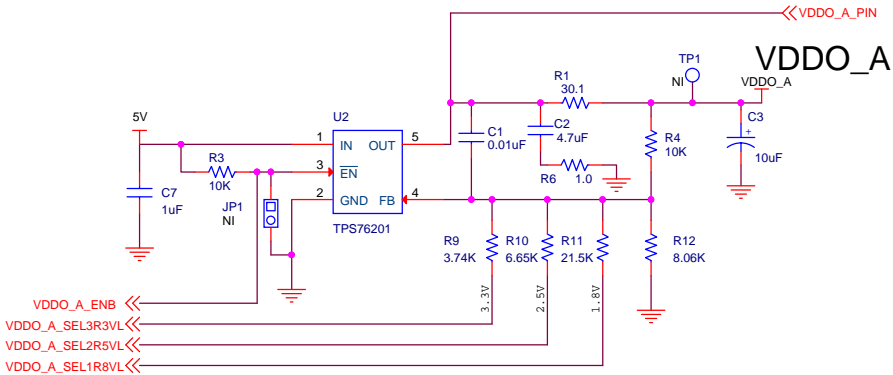
- Inputs:** Input4, Input5, Input6, Input7, Input8, Input9, Input10, Input11, Input12, Input13, Input14, Input15, Input16, Input17, Input18, Input19, Input20, Input21, Input22, Input23, Input24, Input25, Input26, Input27, Input28, Input29, Input30, Input31, Input32, Input33, Input34, Input35, Input36, Input37, Input38, Input39, Input40, Input41, Input42, Input43, Input44, Input45, Input46, Input47, Input48, Input49, Input50, Input51, Input52, Input53, Input54, Input55, Input56, Input57, Input58, Input59, Input60, Input61, Input62, Input63, Input64, Input65, Input66, Input67, Input68, Input69, Input70, Input71, Input72, Input73, Input74, Input75, Input76, Input77, Input78, Input79, Input80, Input81, Input82, Input83, Input84, Input85, Input86, Input87, Input88, Input89, Input90, Input91, Input92, Input93, Input94, Input95, Input96, Input97, Input98, Input99, Input100.
- Outputs:** OUT\_D, OUT\_E, OUT\_F, OUT\_G, OUT\_H, OUT\_I, OUT\_J, OUT\_K, OUT\_L, OUT\_M, OUT\_N, OUT\_O, OUT\_P, OUT\_Q, OUT\_R, OUT\_S, OUT\_T, OUT\_U, OUT\_V, OUT\_W, OUT\_X, OUT\_Y, OUT\_Z, OUT\_AA, OUT\_AB, OUT\_AC, OUT\_AD, OUT\_AE, OUT\_AF, OUT\_AG, OUT\_AH, OUT\_AI, OUT\_AJ, OUT\_AK, OUT\_AL, OUT\_AM, OUT\_AN, OUT\_AO, OUT\_AP, OUT\_AQ, OUT\_AR, OUT\_AS, OUT\_AT, OUT\_AU, OUT\_AV, OUT\_AW, OUT\_AX, OUT\_AY, OUT\_AZ, OUT\_BA, OUT\_BB, OUT\_BC, OUT\_BD, OUT\_BE, OUT\_BF, OUT\_BG, OUT\_BH, OUT\_BI, OUT\_BJ, OUT\_BK, OUT\_BL, OUT\_BM, OUT\_BN, OUT\_BO, OUT\_BP, OUT\_BQ, OUT\_BR, OUT\_BS, OUT\_BT, OUT\_BU, OUT\_BV, OUT\_BW, OUT\_BX, OUT\_BY, OUT\_BZ, OUT\_CA, OUT\_CB, OUT\_CC, OUT\_CD, OUT\_CE, OUT\_CF, OUT.CG, OUT\_CH, OUT\_CI, OUT\_CJ, OUT\_CK, OUT\_CL, OUT\_CM, OUT\_CN, OUT\_CO, OUT\_CP, OUT\_CQ, OUT\_CR, OUT\_CS, OUT\_CT, OUT\_CU, OUT\_CV, OUT\_CW, OUT\_CX, OUT\_CY, OUT\_CZ, OUT\_DA, OUT\_DB, OUT\_DC, OUT\_DD, OUT\_DE, OUT\_DF, OUT\_DG, OUT\_DH, OUT\_DI, OUT\_DJ, OUT\_DK, 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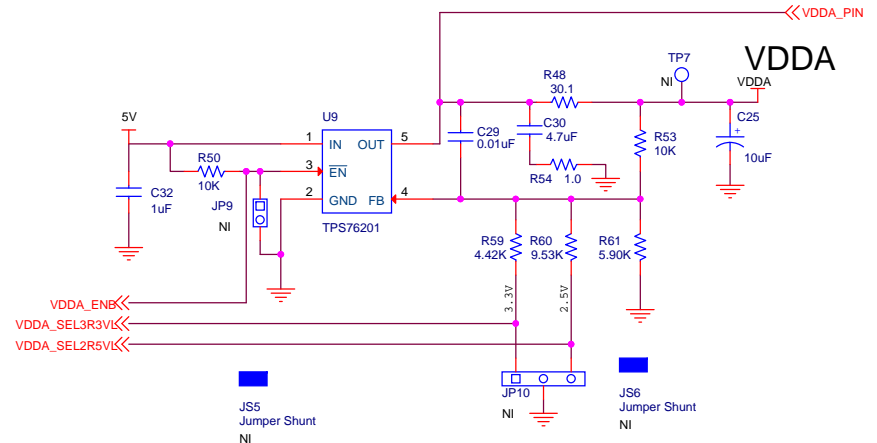
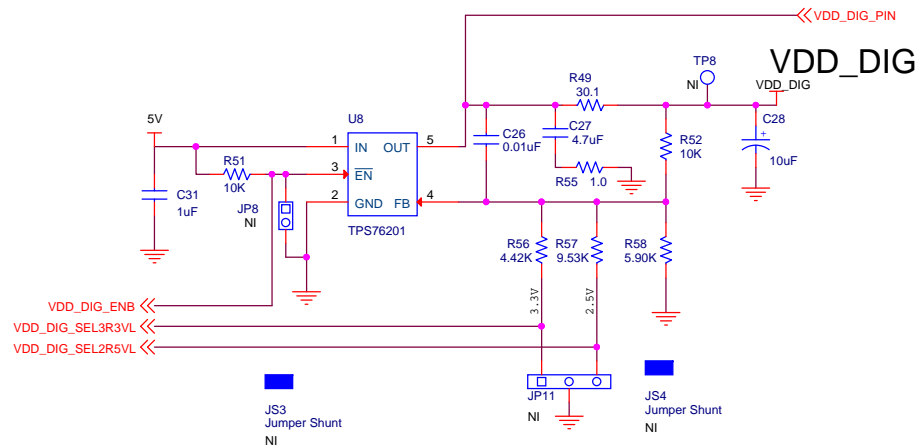
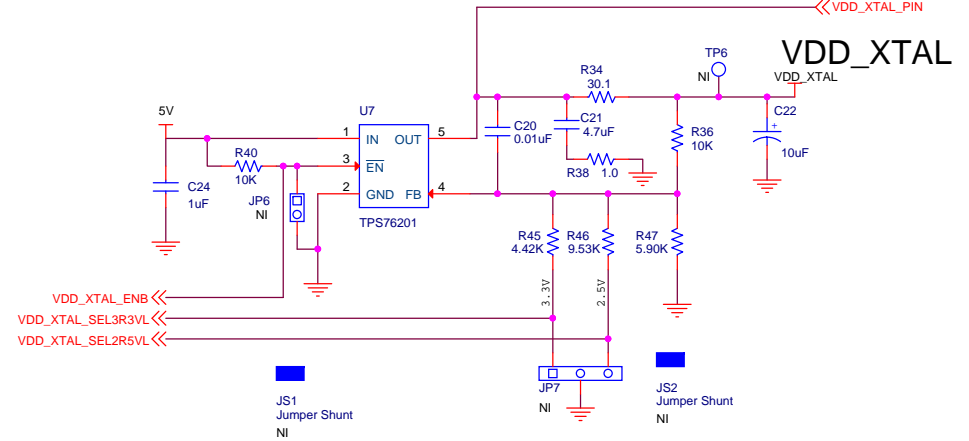
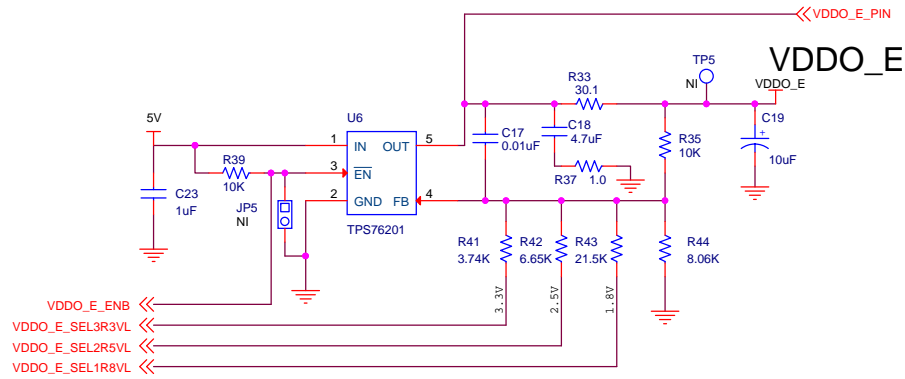
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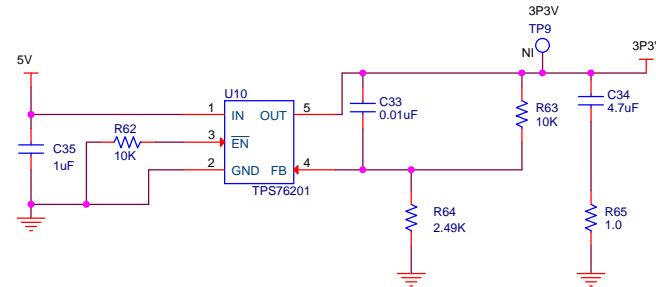
# 100 mA Adjustable Voltage Regulator



# 100 mA Adjustable Voltage Regulator

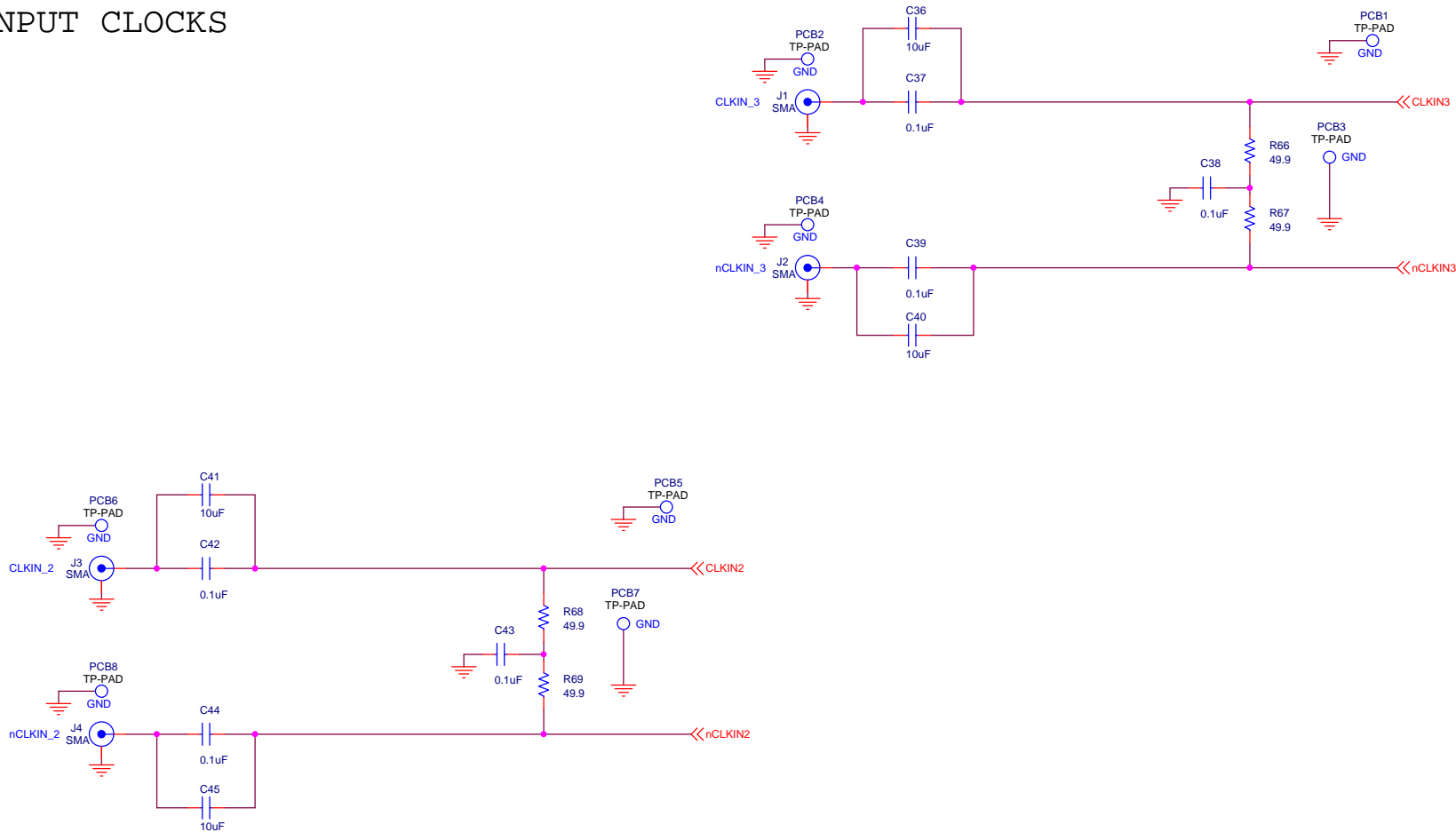


# Fixed 3.3V 100 mA Voltage Regulator (Enabled, no current measurement supported.)

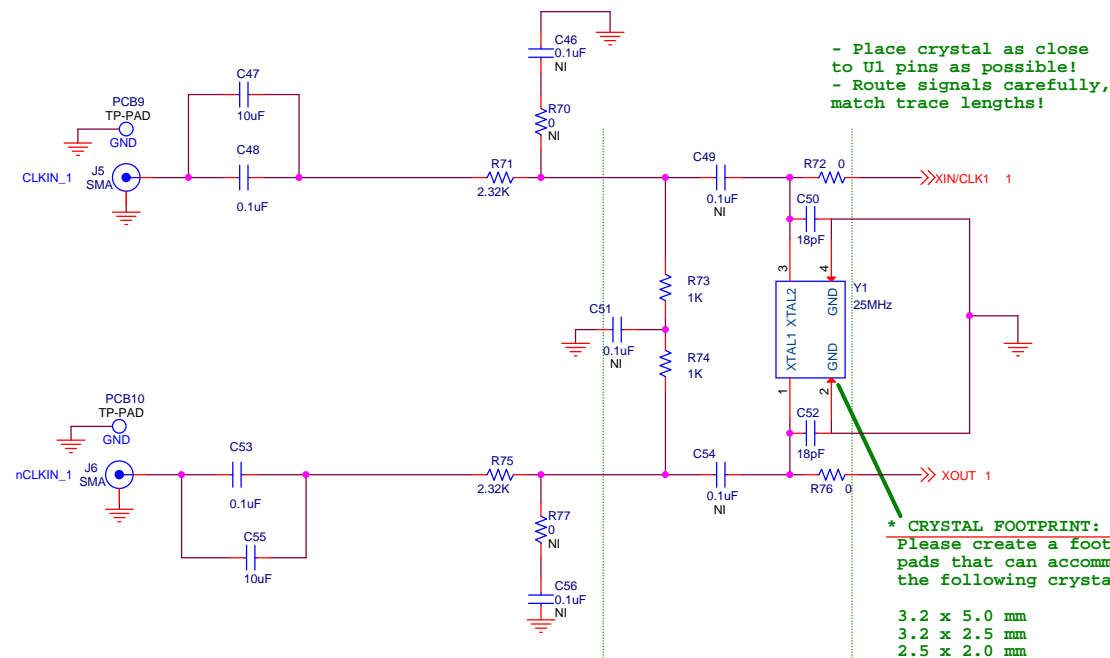


3P3V (In Schematic)  
3P3V (Board Silkscreen)

INPUT CLOCKS



# Crystal Input Connections



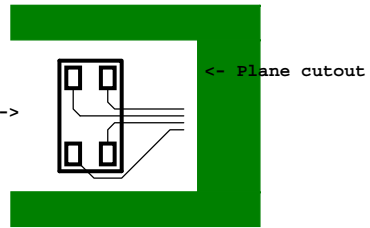
\* CRYSTAL FOOTPRINT:  
Please create a footprint with pads that can accommodate the following crystal sizes:

- 3.2 x 5.0 mm
- 3.2 x 2.5 mm
- 2.5 x 2.0 mm

Keep X as short as possible by placing all components close to the XA/XB pins

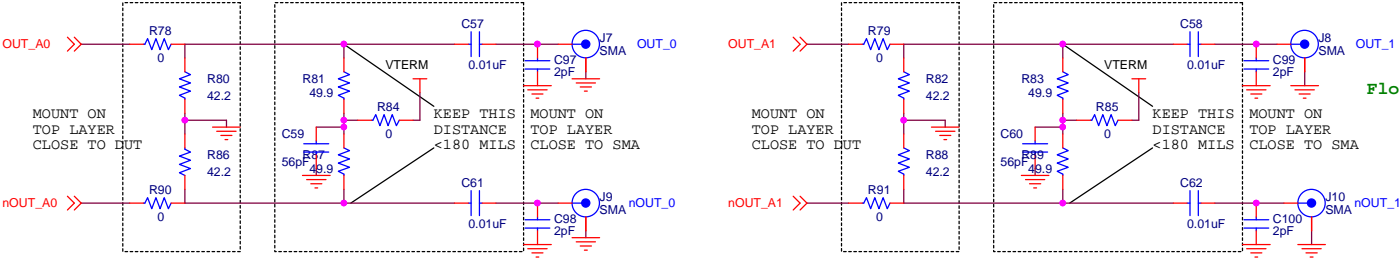
Cut planes underneath crystal to reduce capacitive coupling!

90 degree placement ->

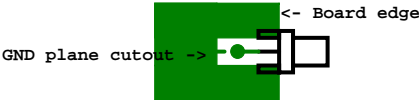
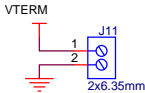


Traces are just an illustration!

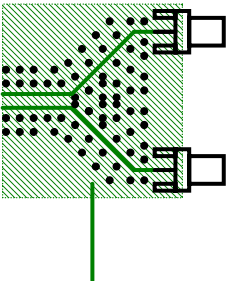
# OUTPUT CONNECTIONS, PART 1



SMA FOOTPRINT NOTE:  
Make sure pad for center pin on SMA matches exactly  
the actual width of the center pin in order to improve performance



Flood top and bottom layers with copper as shown

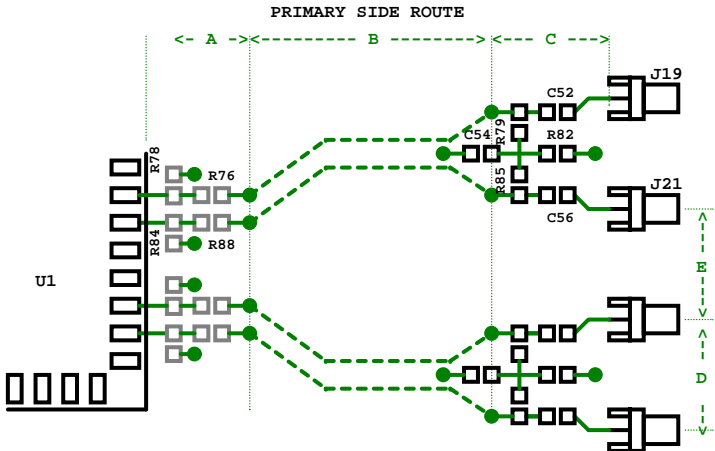


A sufficient number of via holes connected  
to ground should be used around all input/output  
traces!

OUTPUT SIGNALS LAYOUT NOTES - APPLIES TO THIS PAGE AND NEXT PAGE AS WELL!  
(Refer to image on left):

- ROUTING: route each differential pair loosely coupled. Trombone only when absolutely necessary and preserve symmetry on diff. pair. Keep bending at a minimum
- IMPEDANCE: all traces to have 50 ohms of controlled impedance
  - In order to reduce capacitance please cut-out ground planes underneath the microstrip launches on the SMA connectors as needed
- BANDWIDTH: all traces need a bandwidth of 9 GHz! (20-80% RT ~ 25ps)
- GEOMETRY: maintain the trace symmetry across all output differential pairs
- TOPOLOGY: use microstrip for SMA-to-trace and DUT-to-resistor launches, stripline for rest of traces
- COMPONENT PLACEMENT:
  - Separate each pair of SMA connectors by 750 mils between them (center to center, and also pair to pair) on flat edge, and by 785 mils on arc edge
- DIMENSIONS:
  - Use via-in-pad to drop to bottom layer to place termination resistors (49.9) and decoupling cap;
  - Make trace <A> as short as possible, then use via after resistor to launch into inner layer
  - Match trace length <B> on all output signals. Use shortest possible length
  - Make <C> and <F> distances as short as possible
  - Keep <D> at 0.75" (750 mils) on flat edge, 0.785" on arc edge

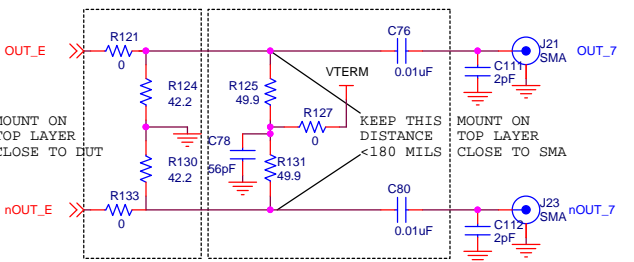
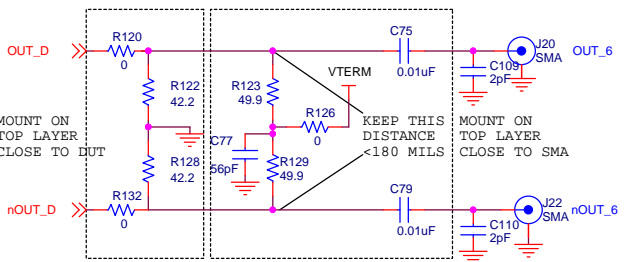
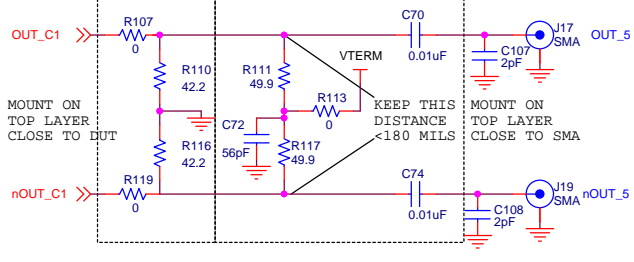
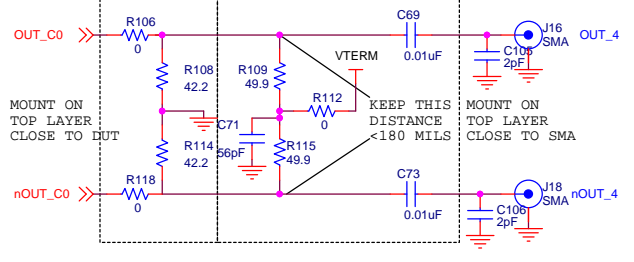
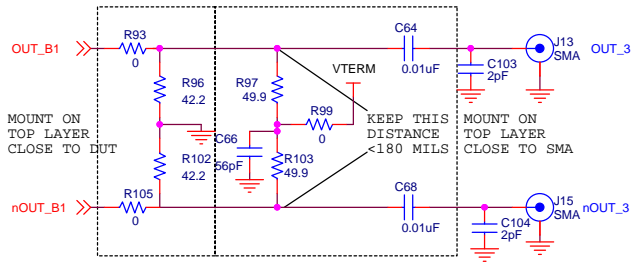
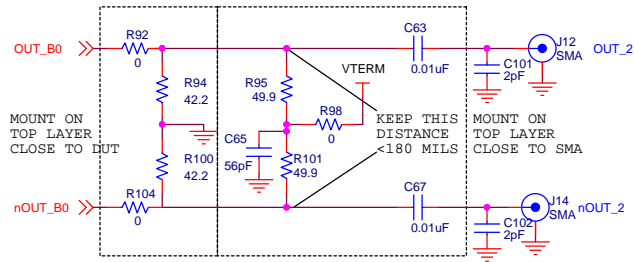
- LAYERS:
  - Top Layer: microstrips for SMA to components and DUT-to-snub resistor (953);
  - Layer 7: striplines for <B> traces
  - Bottom Layer: termination Res's (49.9) and decoupling cap;



OUTPUT CONNECTIONS, PART 2

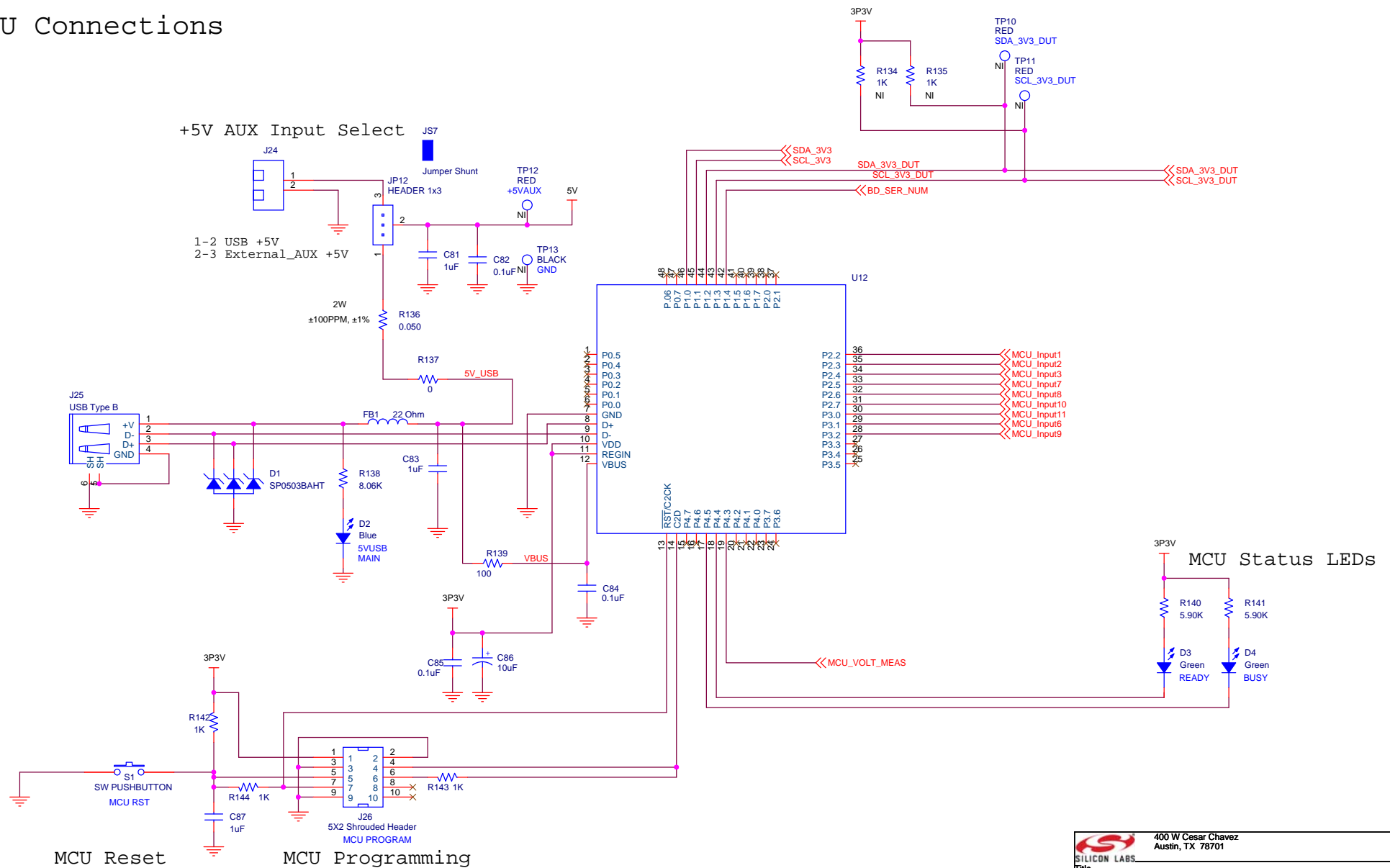
FORMAT	R572/573	R515/516	R524/525	R526/527	VTERM_x
LVDS (DC)	NI	0	49.9	0	NI
LVDS (AC)	NI	0.01uF	49.9	0	NI
HCSL (EXT)	49.9	0	NI	0	NI
LVPECL (DC)	NI	0	49.9	0	VDDOx-2
CMOS (33)	NI	27	4pF	0	GND
CMOS (25)	NI	20	4pF	0	GND

SEE PREVIOUS PAGE FOR LAYOUT INSTRUCTIONS!

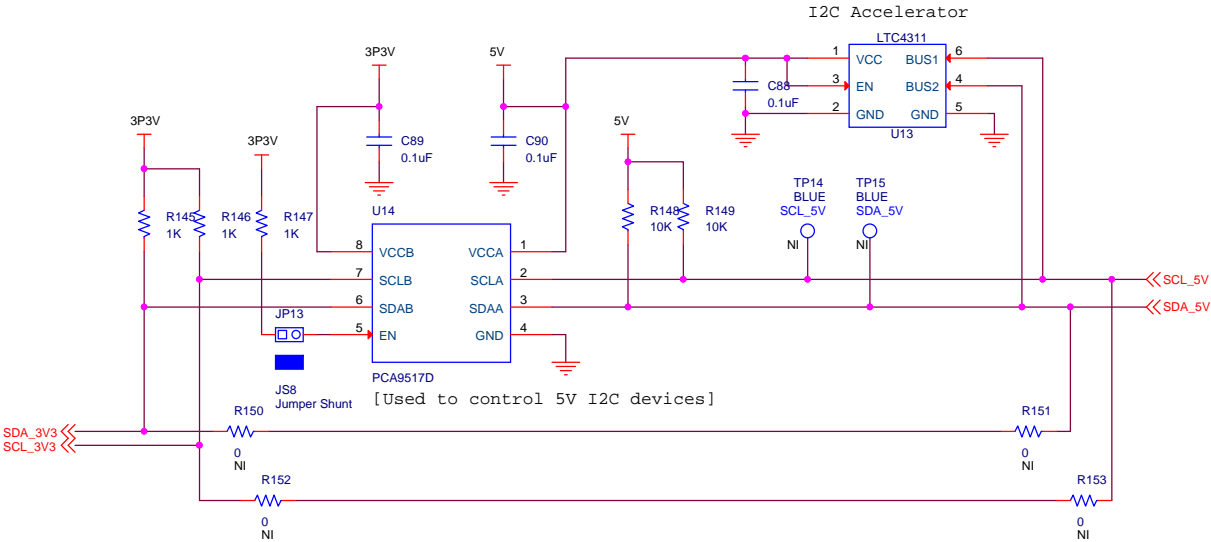


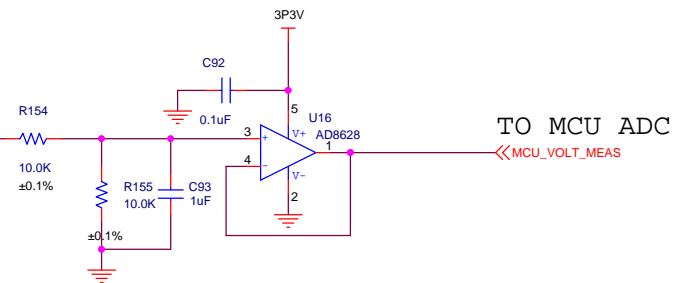
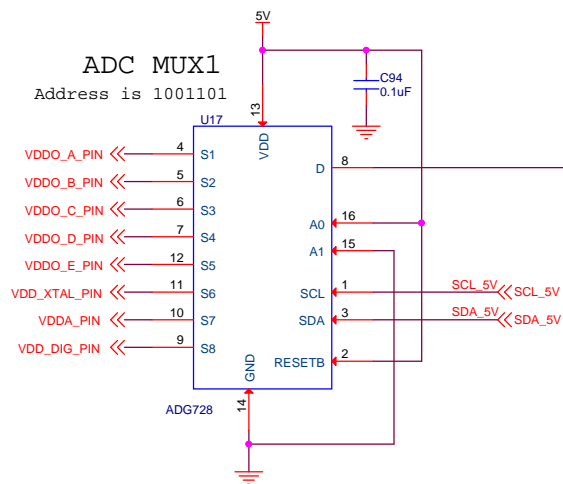
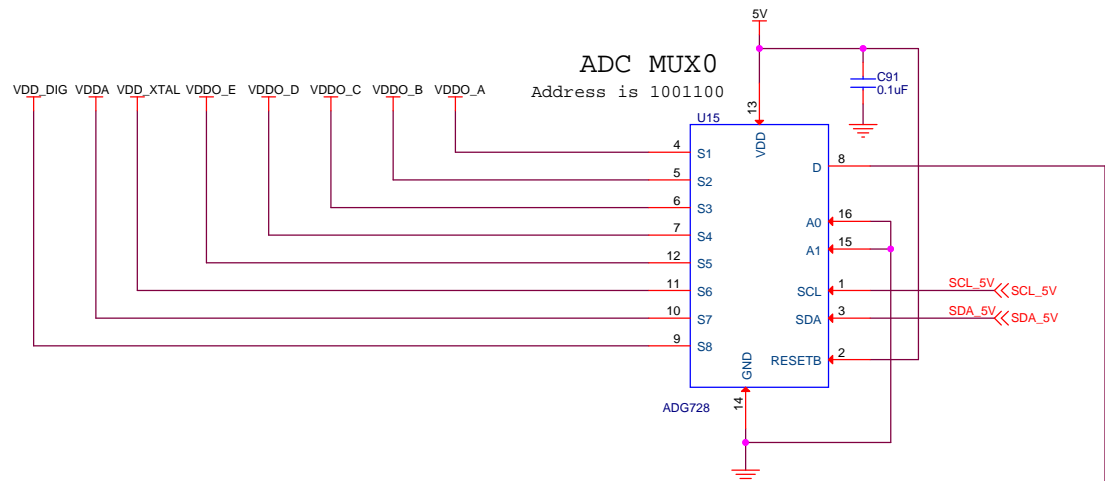


# MCU Connections



I2C LEVEL TRANSLATOR





VDD Enables and SN

