# TMS570LS1224 16- and 32-Bit RISC Flash Microcontroller

## 1 Device Overview

### 1.1 Features

- High-Performance Automotive-Grade Microcontroller for Safety-Critical Applications
  - Dual CPUs Running in Lockstep
  - ECC on Flash and RAM Interfaces
  - Built-In Self-Test (BIST) for CPU and On-chip RAMs
  - Error Signaling Module With Error Pin
  - Voltage and Clock Monitoring
- ARM® Cortex®-R4F 32-Bit RISC CPU
  - 1.66 DMIPS/MHz With 8-Stage Pipeline
  - FPU With Single- and Double-Precision
  - 12-Region Memory Protection Unit (MPU)
  - Open Architecture With Third-Party Support
- Operating Conditions
  - Up to 180-MHz System Clock
  - Core Supply Voltage (VCC): 1.14 to 1.32 V
  - I/O Supply Voltage (VCCIO): 3.0 to 3.6 V
- Integrated Memory
  - 1.25MB of Program Flash With ECC
  - 192KB of RAM With ECC
  - 64KB of Flash for Emulated EEPROM With ECC
- 16-Bit External Memory Interface (EMIF)
- Common Platform Architecture
  - Consistent Memory Map Across Family
  - Real-Time Interrupt (RTI) Timer (OS Timer)
  - 128-Channel Vectored Interrupt Module (VIM)
  - 2-Channel Cyclic Redundancy Checker (CRC)
- Direct Memory Access (DMA) Controller
  - 16 Channels and 32 Control Packets
  - Parity Protection for Control Packet RAM
  - DMA Accesses Protected by Dedicated MPU
- Frequency-Modulated Phase-Locked Loop (FMPLL) With Built-In Slip Detector
- Separate Nonmodulating PLL
- IEEE 1149.1 JTAG, Boundary Scan and ARM CoreSight™ Components
- Advanced JTAG Security Module (AJSM)
- Calibration Capabilities
  - Parameter Overlay Module (POM)
- 16 General-Purpose Input/Output (GPIO) Pins Capable of Generating Interrupts
- Enhanced Timing Peripherals for Motor Control
  - 7 Enhanced Pulse Width Modulator (ePWM) Modules
  - 6 Enhanced Capture (eCAP) Modules
  - 2 Enhanced Quadrature Encoder Pulse (eQEP) Modules
- Two Next Generation High-End Timer (N2HET) Modules
  - N2HET1: 32 Programmable Channels
  - N2HET2: 18 Programmable Channels
  - 160-Word Instruction RAM Each With Parity Protection
  - Each N2HET Includes Hardware Angle Generator
  - Dedicated High-End Timer Transfer Unit (HTU) for Each N2HET
- Two 12-Bit Multibuffered Analog-to-Digital Converter (MibADC) Modules
  - ADC1: 24 Channels
  - ADC2: 16 Channels Shared With ADC1
  - 64 Result Buffers Each With Parity Protection
- Multiple Communication Interfaces
  - Three CAN Controllers (DCANs)
    - 64 Mailboxes Each With Parity Protection
    - Compliant to CAN Protocol Version 2.0A and 2.0B
  - Inter-Integrated Circuit ($I^2C$)
  - Three Multibuffered Serial Peripheral Interface (MibSPI) Modules
    - 128 Words Each With Parity Protection
    - 8 Transfer Groups
  - Up to Two Standard Serial Peripheral Interface (SPI) Modules
  - Two UART (SCI) Interfaces, One With Local Interconnect Network (LIN 2.1) Interface Support
- Packages
  - 144-Pin Quad Flatpack (PGE) [Green]
  - 337-Ball Grid Array (ZWT) [Green]

## 1.2 Applications

- Braking Systems (ABS and ESC)
- Electric Power Steering (EPS)
- HEV and EV Inverter Systems
- Battery Management Systems
- Active Driver Assistance Systems
- Aerospace and Avionics
- Railway Communications
- Off-road Vehicles

## 1.3 Description

The TMS570LS1224 device is a high-performance automotive-grade microcontroller family for safety systems. The safety architecture includes dual CPUs in lockstep, CPU and memory BIST logic, ECC on both the flash and the data SRAM, parity on peripheral memories, and loopback capability on peripheral I/Os.

The TMS570LS1224 device integrates the ARM Cortex-R4F floating-point CPU which offers an efficient 1.66 DMIPS/MHz, and has configurations which can run up to 180 MHz providing up to 298 DMIPS. The device supports the word-invariant big-endian [BE32] format.

The TMS570LS1224 device has 1.25MB of integrated flash and 192KB of data RAM with single-bit error correction and double-bit error detection. The flash memory on this device is a nonvolatile, electrically erasable and programmable memory, implemented with a 64-bit-wide data bus interface. The flash operates on a 3.3-V supply input (same level as I/O supply) for all read, program, and erase operations. When in pipeline mode, the flash operates with a system clock frequency of up to 180 MHz. The SRAM supports single-cycle read and write accesses in byte, halfword, word, and double-word modes throughout the supported frequency range.

The TMS570LS1224 device features peripherals for real-time control-based applications, including two Next Generation High-End Timer (N2HET) timing coprocessors with up to 44 I/O terminals, seven Enhanced Pulse Width Modulator (ePWM) modules with up to 14 outputs, six Enhanced Capture (eCAP) modules, two Enhanced Quadrature Encoder Pulse (eQEP) modules, and two 12-bit Analog-to-Digital Converters (ADCs) supporting up to 24 inputs.

The N2HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The N2HET can be used for pulse-width-modulated outputs, capture or compare inputs, or general-purpose I/O (GIO). The N2HET is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses. A High-End Timer Transfer Unit (HTU) can perform DMA-type transactions to transfer N2HET data to or from main memory. A Memory Protection Unit (MPU) is built into the HTU.

The ePWM module can generate complex pulse width waveforms with minimal CPU overhead or intervention. The ePWM is easy to use and it supports both high-side and low-side PWM and deadband generation. With integrated trip zone protection and synchronization with the on-chip MibADC, the ePWM module is ideal for digital motor control applications.

The eCAP module is essential in systems where the accurately timed capture of external events is important. The eCAP can also be used to monitor the ePWM outputs or for simple PWM generation when the eCAP is not needed for capture applications.

The eQEP module is used for direct interface with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine as used in high-performance motion and position-control systems.

The device has two 12-bit-resolution MibADCs with 24 total inputs and 64 words of parity-protected buffer RAM each. The MibADC channels can be converted individually or can be grouped by software for sequential conversion sequences. Sixteen inputs are shared between the two MibADCs. Each MibADC supports three separate groupings of channels. Each group can be converted once when triggered or configured for continuous conversion mode. The MibADC has a 10-bit mode for use when compatibility with older devices or faster conversion time is desired. MibADC1 also supports the use of external analog multiplexers.

The device has multiple communication interfaces: three MibSPIs, two SPIs, one LIN, one SCI, three DCANs, and one $I^2C$. The SPI provides a convenient method of serial high-speed communications between similar shift-register type devices. The LIN supports the Local Interconnect standard 2.0 and can be used as a UART in full-duplex mode using the standard Non-Return-to-Zero (NRZ) format. The DCAN supports the CAN 2.0 (A and B) protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 Mbps. The DCAN is ideal for systems operating in noisy and harsh environments (for example, automotive and industrial fields) that require reliable serial communication or multiplexed wiring.

The I2C module is a multimaster communication module providing an interface between the microcontroller and an $I^2C$-compatible device through the $I^2C$ serial bus. The $I^2C$ supports speeds of 100 and 400 Kbps.

A Frequency-Modulated Phase-Locked Loop (FMPLL) clock module is used to multiply the external frequency reference to a higher frequency for internal use. The Global Clock Module (GCM) manages the mapping between the available clock sources and the device clock domains.

The device also has an External Clock Prescaler (ECP) module that when enabled, outputs a continuous external clock on the ECLK terminal. The ECLK frequency is a user-programmable ratio of the peripheral interface clock (VCLK) frequency. This low-frequency output can be monitored externally as an indicator of the device operating frequency.

The Direct Memory Access (DMA) controller has 16 channels, 32 control packets, and parity protection on its memory. An MPU is built into the DMA to protect memory against erroneous transfers.

The Error Signaling Module (ESM) monitors all device errors and determines whether an interrupt or external error pin (ball) is triggered when a fault is detected. The nERROR terminal can be monitored externally as an indicator of a fault condition in the microcontroller.

The External Memory Interface (EMIF) provides a memory extension to asynchronous and synchronous memories or other slave devices.

A Parameter Overlay Module (POM) enhances the calibration capabilities of application code. The POM can reroute flash accesses to internal memory or to the EMIF, thus avoiding the reprogramming steps necessary for parameter updates in flash.

With integrated safety features and a wide choice of communication and control peripherals, the TMS570LS1224 device is an ideal solution for high-performance real-time control applications with safety-critical requirements.

**Table 1-1. Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE |
|---|---|---|
| TMS570LS1224ZWT | NFBGA (337) | 16.0 mm × 16.0 mm |
| TMS570LS1224PGE | LQFP (144) | 20.0 mm × 20.0 mm |

(1) For more information, see Section 9, *Mechanical Packaging and Orderable Information*.

## 1.4 Functional Block Diagram

**NOTE**

The block diagram reflects the 337BGA package. Some pins are multiplexed or not available in the 144QFP. For details, see the respective terminal functions tables in Section 4.3.

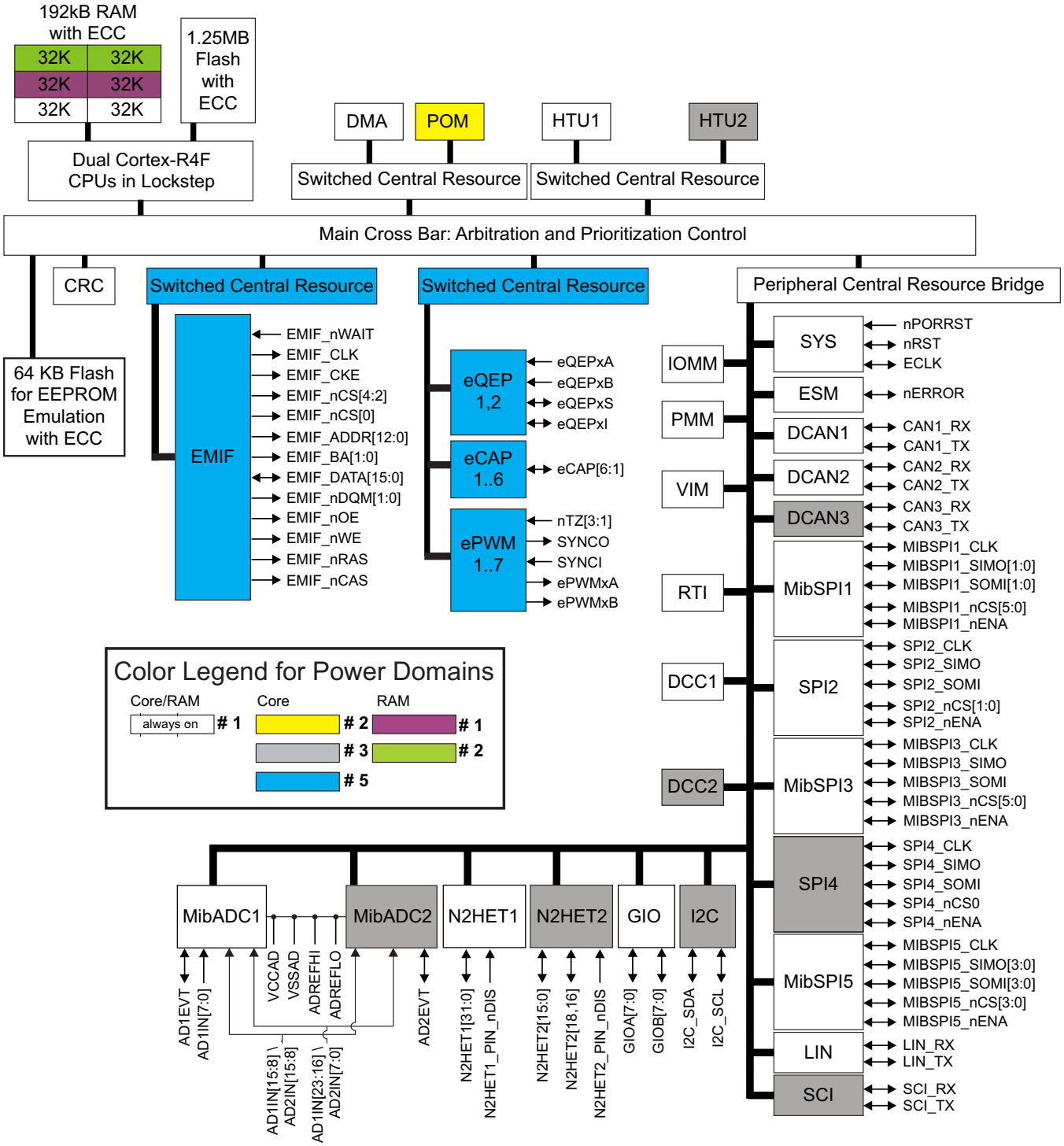


**Figure 1-1. Functional Block Diagram**

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## 2 Revision History

This data manual revision history highlights the technical changes made to the SPNS190A device-specific data manual addendum to make it an SPNS190B revision.

**Scope:** Applicable updates to the Hercules™ TMS570 MCU device family, specifically relating to the TMS570LS1224 devices, which are now in the production data (PD) stage of development have been incorporated.

**Changes from September 1, 2013 to February 28, 2015 (from A Revision (September 2013) to B Revision)** **Page**

- Updated/Changed section title to "Device Overview" ..... 1
- Updated/changed the N2HET feature ..... 1
- Added Table 1-1, *Device Information* ..... 3
- Added Section 3, *Device Comparison* ..... 8
- Updated/Changed section title to "Terminal Configuration and Functions" ..... 9
- Table 4-2 (PGE Enhanced High-End Timer Modules (N2HET)) Updated/Changed N2HET1 time input capture or output compare pin description ..... 13
- Table 4-2 Updated/Changed N2HET2 time input capture or output compare pin description ..... 14
- Table 4-5Updated/Changed the EPWM1SYNCI Signal Type from "Output" to "Input" ..... 15
- Table 4-5Updated/Changed the EPWM1SYNCI pin description from "Output" to "Input" ..... 15
- Table 4-15 (PGE Test and Debug Modules Interface): Updated/Changed TEST pin description ..... 20
- Table 4-21 (ZWT Enhanced High-End Timer Modules (N2HET)) Updated/Changed N2HET1 time input capture or output compare pin description ..... 24
- Table 4-21 Updated/Changed N2HET2 time input capture or output compare pin description ..... 25
- Updated/Changed the EPWM1SYNCI pin description from "Output" to "Input" ..... 27
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- Table 4-35 (ZWT Test and Debug Modules Interface): Updated/Changed TEST pin description ..... 35
- Table 4-37 Changed six BGA balls from NC to Reserved ..... 35
- Updated/Changed section title to "Specifications" ..... 41
- Moved Storage temperature range, $T_{stg}$ back to Section 5.1, *Absolute Maximum Ratings Over Operating Free-Air Temperature Range* ..... 41
- Added Section 5.2, *Handling Ratings (Automotive)* ..... 41
- Added Section 5.3, *Power-On-Hours (POH)* ..... 41
- Moved *Thermal Data* section here. ..... 45
- Section 5.9 (Thermal Resistance Characteristics): Updated/Changed title from "Thermal Data" to "Thermal Resistance Characteristics" ..... 45
- Added $\Theta_{JA}$ test conditions and added $\Psi_{JT}$ for PGE package ..... 45
- Added $\Theta_{JA}$ test conditions and added $\Psi_{JT}$ for ZWT package ..... 45
- Clarified impact of SPI2PC9 register on drive strength of SPI2SOMI pin ..... 47
- Changed the number of cycles of $t_{v(RST)}$ from 2252 to 2256 ..... 54
- Table 6-22 (Flash Memory Banks and Sectors): Added associated footnotes ..... 75
- Figure 6-10 (TCRAM Block Diagram): Updated/Changed figure ..... 78
- Added table notes identifying address ranges of ESRAM PBIST groups ..... 80
- Updated/Changed N2HET2 RAM ending address from "0xFF**57**FFFF" to "0xFF**45**FFFF" in Table 6-26, *Memory Initialization* ..... 81
- Updated EMIF Timings ..... 82
- Changed maximum addressable size of asynchronous memories from 16MB to 32KB ..... 82
- Updated/Changed the EMIF address bus signals from "EMIF_ADDR[21:0]" to "EMIF_ADDR[12:0]" for all figures in Section 6.14.2, *Electrical and Timing Specifications* ..... 82
- Updated/Changed EMIF address from "EMIF_ADDR[21:0]" to "EMIF_ADDR[12:0]" ..... 82
- Changed EMIF $t_{su(EMDV-EMOEH)}$ from 30nS to 9nS ..... 84
- Changed EMIF $t_{h(EMOEH-EMDIV)}$ from 0.5nS to 0nS ..... 84
- Changed EMIF $t_{su(EMOEL-EMWAIT)}$ from 4E+30nS to 4E+9nS ..... 84
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- Changed EMIF $t_{su(EMCEL-EMOEL)}$ from (RS)*E-5 to (RS)*E-6 ..... 85
- Changed EMIF $t_{su(EMCEL-EMOEL)}$ from -5 to -6 ..... 85
- Changed EMIF $t_{h(EMOEH-EMCEH)}$ from (RH)*E -4 to (RH)*E -3 ..... 85
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- Changed EMIF $t_{h(EMOEH-EMCEH)}$ from +4 to +5 ..... 85
- Changed EMIF $t_{su(EMBAV-EMOEL)}$ from (RS)*E-5 to (RS)*E-6 ..... 85
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- Changed EMIF $t_{d(EMWAITH-EMOEH)}$ from 3E-3 to 3E+9 ..... 85
- Changed EMIF $t_{d(EMWAITH-EMOEH)}$ from 4E+30 to 4E+20 ..... 85
- Changed EMIF $t_{su(EMDQMV-EMOEL)}$ from (RS)*E-5 to (RS)*E-6 ..... 85
- Changed EMIF $t_{h(EMOEH-EMDQMIV)}$ from (RS)*E-4 to (RS)*E-3 ..... 85
- Changed EMIF $t_{su(EMCEL-EMWEL)}$ from (WS)*E -4 to (WS)*E -3 ..... 86
- Changed EMIF $t_{su(EMCEL-EMWEL)}$ from -4 to -3 ..... 86
- Changed EMIF $t_{h(EMWEH-EMCEH)}$ from (WS)*E -4 to (WS)*E -3 ..... 86
- Changed EMIF $t_{h(EMWEH-EMCEH)}$ from -4 to -3 ..... 86
- Changed EMIF $t_{su(EMDQMV-EMWEL)}$ from (WS)*E -4 to (WS)*E -3 ..... 86
- Changed EMIF $t_{h(EMWEH-EMDQMIV)}$ from (WS)*E -4 to (WS)*E -3 ..... 86
- Changed EMIF $t_{su(EMBAV-EMWEL)}$ from (WS)*E -4 to (WS)*E -3 ..... 86
- Changed EMIF $t_{h(EMWEH-EMBAIV)}$ from (WS)*E -4 to (WS)*E -3 ..... 86
- Changed EMIF $t_{su(EMAV-EMWEL)}$ from (WS)*E -4 to (WS)*E -3 ..... 86
- Changed EMIF $t_{h(EMWEH-EMAIV)}$ from (WS)*E -4 to (WS)*E -3 ..... 86
- Changed EMIF $t_{d(EMWAITH-EMWEH)}$ from 3E-4 to 3E+11 ..... 86
- Changed EMIF $t_{d(EMWAITH-EMWEH)}$ from 4E+30 to 4E+24 ..... 86
- Changed EMIF $t_{su(EMDV-EMWEL)}$ from (WS)*E -4 to (WS)*E -3 ..... 86
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- Added JTAG ID for revision C silicon ..... 106
- Revised description of ePWM Trip Zone Timing Requirement $t_{w(TZ)}$ ..... 115
- Corrected SPI table note describing Master mode, phase = 0 condition ..... 146
- Added Device Identification code for revision C silicon ..... 157
- Changed address of die identification registers ..... 157
- Updated/Changed the section title to "Mechanical Packaging and Orderable Information" ..... 164
- Section 9.1 (Packaging Information): Updated/Changed paragraph ..... 164

# 3 Device Comparison

Table 3-1 lists the features of the TMS570LS1224 devices.

**Table 3-1. TMS570LS1224 Device Comparison(1)(2)**

| FEATURES | DEVICES | | | | | | |
|---|---|---|---|---|---|---|---|
| Generic Part Number | TMS570LS3137ZWT(3) | TMS570LS1227ZWT(3) | TMS570LS1224ZWT | TMS570LS1224PGE | TMS570LS0714PGE | TMS570LS0714PZ | TMS570LS0432PZ |
| Package | 337 BGA | 337 BGA | 337 BGA | 144 QFP | 144 QFP | 100 QFP | 100 QFP |
| CPU | ARM Cortex-R4F | ARM Cortex-R4F | ARM Cortex-R4F | ARM Cortex-R4F | ARM Cortex-R4F | ARM Cortex-R4F | ARM Cortex-R4 |
| Frequency (MHz) | 180 | 180 | 180 | 160 | 160 | 100 | 80 |
| Flash (KB) | 3072 | 1280 | 1280 | 1280 | 768 | 768 | 384 |
| RAM (KB) | 256 | 192 | 192 | 192 | 128 | 128 | 32 |
| Data Flash [EEPROM] (KB) | 64 | 64 | 64 | 64 | 64 | 64 | 16 |
| EMAC | 10/100 | 10/100 | – | – | – | – | – |
| FlexRay | 2-ch | 2-ch | – | – | – | – | – |
| CAN | 3 | 3 | 3 | 3 | 3 | 2 | 2 |
| MibADC 12-bit (Ch) | 2 (24ch) | 2 (24ch) | 2 (24ch) | 2 (24ch) | 2 (24ch) | 2 (16ch) | 1 (16ch) |
| N2HET (Ch) | 2 (44) | 2 (44) | 2 (44) | 2 (40) | 2 (40) | 2 (21) | 1 (19) |
| ePWM Channels | – | 14 | 14 | 14 | 14 | 8 | – |
| eCAP Channels | – | 6 | 6 | 6 | 6 | 4 | 0 |
| eQEP Channels | – | 2 | 2 | 2 | 2 | 1 | 1 |
| MibSPI (CS) | 3 (6 + 6 + 4) | 3 (6 + 6 + 4) | 3 (6 + 6 + 4) | 3 (5 + 6 + 1) | 3 (5 + 6 + 4) | 2 (5 + 1) | 1 (4) |
| SPI (CS) | 2 (2 + 1) | 2 (2 + 1) | 2 (2 + 1) | 1 (1) | 1 (1) | 1 (1) | 2 |
| SCI (LIN) | 2 (1 with LIN) | 2 (1 with LIN) | 2 (1 with LIN) | 2 (1 with LIN) | 2 (1 with LIN) | 1 (with LIN) | 1 (with LIN) |
| I2C | 1 | 1 | 1 | 1 | 1 | – | – |
| GPIO (INT)(4) | 144 (with 16 interrupt capable) | 101 (with 16 interrupt capable) | 101 (with 16 interrupt capable) | 64 (with 10 interrupt capable) | 64 (with 10 interrupt capable) | 45 (with 9 interrupt capable) | 45 (with 8 interrupt capable) |
| EMIF | 16-bit data | 16-bit data | 16-bit data | – | – | – | – |
| ETM (Trace) | 32-bit | – | – | – | – | – | – |
| RTP/DMM | YES | – | – | – | – | – | – |
| Operating Temperature | -40ºC to 125ºC | -40ºC to 125ºC | -40ºC to 125ºC | -40ºC to 125ºC | -40ºC to 125ºC | -40ºC to 125ºC | -40ºC to 125ºC |
| Core Supply (V) | 1.14 V – 1.32 V | 1.14 V – 1.32 V | 1.14 V – 1.32 V | 1.14 V – 1.32 V | 1.14 V – 1.32 V | 1.14 V – 1.32 V | 1.14 V – 1.32 V |
| I/O Supply (V) | 3.0 V – 3.6 V | 3.0 V – 3.6 V | 3.0 V – 3.6 V | 3.0 V – 3.6 V | 3.0 V – 3.6 V | 3.0 V – 3.6 V | 3.0 V – 3.6 V |

(1) For additional device variants, see www.ti.com/tms570
(2) This table reflects the maximum configuration for each peripheral. Some functions are multiplexed and not all pins are available at the same time.
(3) Superset device.
(4) Total number of pins that can be used as general purpose input or output when not used as part of a peripheral.

# 4 Terminal Configuration and Functions

## 4.1 PGE QFP Package Pinout (144-Pin)

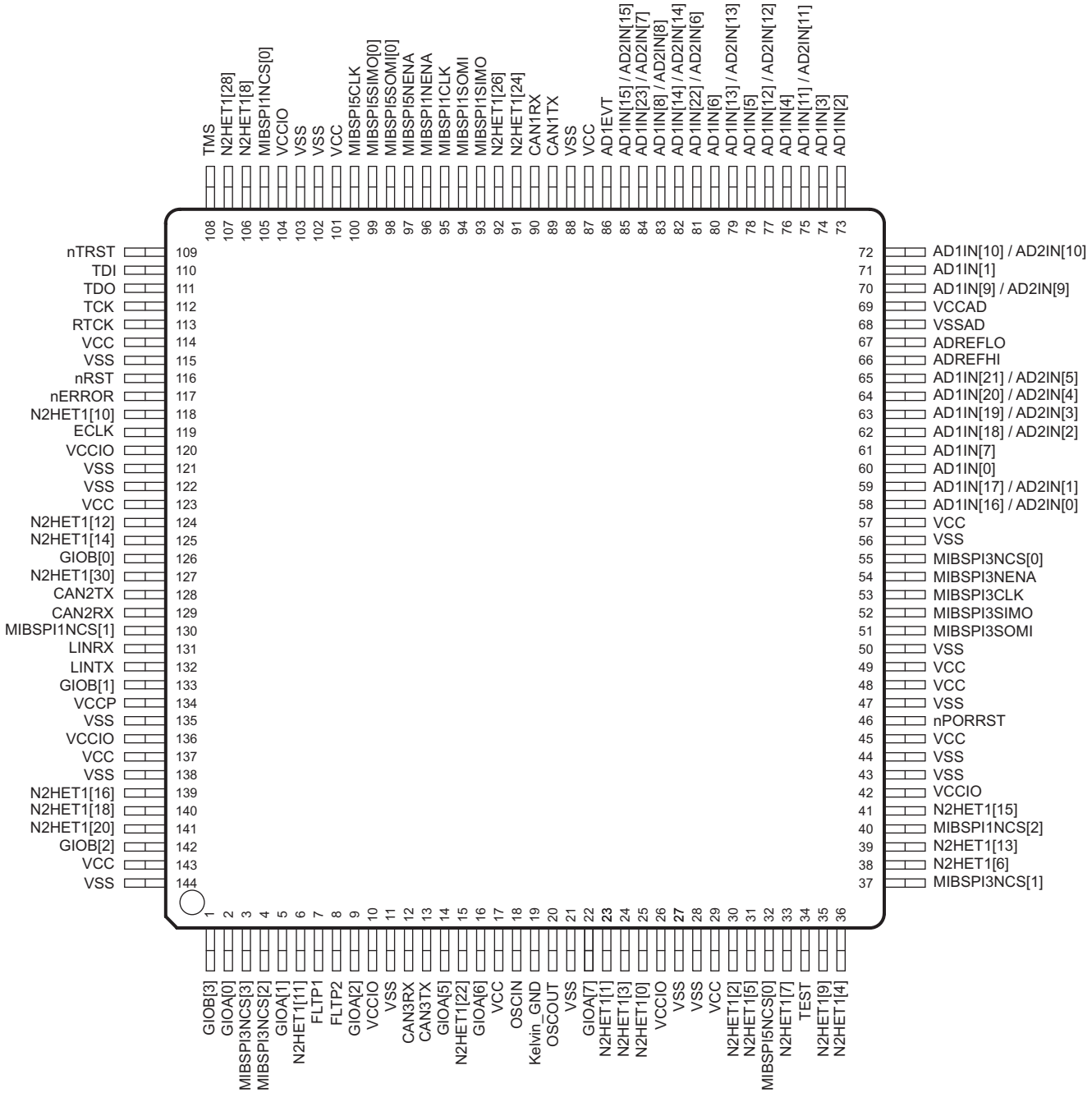



**Figure 4-1. PGE QFP Package Pinout (144-Pin)**

Note: Pins can have multiplexed functions. Only the default function is depicted in above diagram.

## 4.2 ZWT BGA Package Ball-Map (337 Ball Grid Array)

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T | U | V | W | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 19 | VSS | VSS | TMS | N2HET1 [10] | MIBSPI5 NCS[0] | MIBSPI1 SIMO | MIBSPI1 NENA | MIBSPI5 CLK | MIBSPI5 SIMO[0] | N2HET1 [28] | NC | CAN3RX | AD1EVT | AD1IN[15] / AD2IN[15] | AD1IN[22] / AD2IN[6] | AD1IN [6] | AD1IN[11] / AD2IN[11] | VSSAD | VSSAD | 19 |
| 18 | VSS | TCK | TDO | nTRST | N2HET1 [8] | MIBSPI1 CLK | MIBSPI1 SOMI | MIBSPI5 NENA | MIBSPI5 SOMI[0] | N2HET1 [0] | NC | CAN3TX | NC | AD1IN[8] / AD2IN[8] | AD1IN[14] / AD2IN[14] | AD1IN[13] / AD2IN[13] | AD1IN [4] | AD1IN [2] | VSSAD | 18 |
| 17 | TDI | nRST | NC | EMIF_ nWE | MIBSPI5 SOMI[1] | NC | MIBSPI5 SIMO[3] | MIBSPI5 SIMO[2] | N2HET1 [31] | EMIF_ nCS[3] | EMIF_ nCS[2] | EMIF_ nCS[4] | EMIF_ nCS[0] | NC | AD1IN [5] | AD1IN [3] | AD1IN[10] / AD2IN[10] | AD1IN [1] | AD1IN[9] / AD2IN[9] | 17 |
| 16 | RTCK | NC | NC | EMIF_ BA[1] | MIBSPI5 SIMO[1] | NC | MIBSPI5 SOMI[3] | MIBSPI5 SOMI[2] | NC | NC | NC | NC | NC | NC | AD1IN[23] / AD2IN[7] | AD1IN[12] / AD2IN[12] | AD1IN[19] / AD2IN[3] | ADREFLO | VSSAD | 16 |
| 15 | NC | NC | NC | NC | NC | NC | NC | NC | NC | EMIF_ DATA[0] | EMIF_ DATA[1] | EMIF_ DATA[2] | EMIF_ DATA[3] | NC | NC | AD1IN[21] / AD2IN[5] | AD1IN[20] / AD2IN[4] | ADREFHI | VCCAD | 15 |
| 14 | N2HET1 [26] | nERROR | NC | NC | NC | VCCIO | VCCIO | VCCIO | VCC | VCC | VCCIO | VCCIO | VCCIO | VCCIO | NC | NC | AD1IN[18] / AD2IN[2] | AD1IN [7] | AD1IN [0] | 14 |
| 13 | N2HET1 [17] | N2HET1 [19] | NC | NC | EMIF_BA[0] | VCCIO | | | | | | | | VCCIO | NC | NC | AD1IN[17] / AD2IN[1] | AD1IN[16] / AD2IN[0] | NC | 13 |
| 12 | ECLK | N2HET1 [4] | NC | NC | EMIF_nOE | VCCIO | | VSS | VSS | VCC | VSS | VSS | | VCCIO | NC | MIBSPI5 NCS[3] | NC | NC | NC | 12 |
| 11 | N2HET1 [14] | N2HET1 [30] | NC | NC | EMIF_ nDQM[1] | VCCIO | | VSS | VSS | VSS | VSS | VSS | | VCCPLL | NC | NC | NC | NC | NC | 11 |
| 10 | CAN1TX | CAN1RX | EMIF_ ADDR[12] | NC | EMIF_ nDQM[0] | VCC | | VCC | VSS | VSS | VSS | VCC | | VCC | NC | NC | NC | MIBSPI3 NCS[0] | GIOB[3] | 10 |
| 9 | N2HET1 [27] | NC | EMIF_ ADDR[11] | NC | EMIF_ ADDR[5] | VCC | | VSS | VSS | VSS | VSS | VSS | | VCCIO | EXTCLKIN2 | NC | NC | MIBSPI3 CLK | MIBSPI3 NENA | 9 |
| 8 | NC | NC | EMIF_ ADDR[10] | NC | EMIF_ ADDR[4] | VCCP | | VSS | VSS | VCC | VSS | VSS | | VCCIO | EMIF_ DATA[15] | NC | NC | MIBSPI3 SOMI | MIBSPI3 SIMO | 8 |
| 7 | LINRX | LINTX | EMIF_ ADDR[9] | NC | EMIF_ ADDR[3] | VCCIO | | | | | | | | VCCIO | EMIF_ DATA[14] | NC | NC | N2HET1 [9] | nPORRST | 7 |
| 6 | GIOA[4] | MIBSPI5 NCS[1] | EMIF_ ADDR[8] | NC | EMIF_ ADDR[2] | VCCIO | VCCIO | VCCIO | VCCIO | VCC | VCC | VCCIO | VCCIO | VCCIO | EMIF_ DATA[13] | NC | NC | N2HET1 [5] | MIBSPI5 NCS[2] | 6 |
| 5 | GIOA[0] | GIOA[5] | EMIF_ ADDR[7] | EMIF_ ADDR[1] | EMIF_ DATA[4] | EMIF_ DATA[5] | EMIF_ DATA[6] | FLTP2 | FLTP1 | EMIF_ DATA[7] | EMIF_ DATA[8] | EMIF_ DATA[9] | EMIF_ DATA[10] | EMIF_ DATA[11] | EMIF_ DATA[12] | NC | NC | MIBSPI3 NCS[1] | N2HET1 [2] | 5 |
| 4 | N2HET1 [16] | N2HET1 [12] | EMIF_ ADDR[6] | EMIF_ ADDR[0] | NC | NC | NC | N2HET1 [21] | N2HET1 [23] | NC | NC | NC | NC | NC | EMIF_ nCAS | NC | NC | NC | NC | 4 |
| 3 | N2HET1 [29] | N2HET1 [22] | MIBSPI3 NCS[3] | SPI2 NENA | N2HET1 [11] | MIBSPI1 NCS[1] | MIBSPI1 NCS[2] | GIOA[6] | MIBSPI1 NCS[3] | EMIF_ CLK | EMIF_ CKE | N2HET1 [25] | SPI2 NCS[0] | EMIF_ nWAIT | EMIF_ nRAS | NC | NC | NC | N2HET1 [6] | 3 |
| 2 | VSS | MIBSPI3 NCS[2] | GIOA[1] | SPI2 SOMI | SPI2 CLK | GIOB[2] | GIOB[5] | CAN2TX | GIOB[6] | GIOB[1] | KELVIN_ GND | GIOB[0] | N2HET1 [13] | N2HET1 [20] | MIBSPI1 NCS[0] | NC | TEST | N2HET1 [1] | VSS | 2 |
| 1 | VSS | VSS | GIOA[2] | SPI2 SIMO | GIOA[3] | GIOB[7] | GIOB[4] | CAN2RX | N2HET1 [18] | OSCIN | OSCOUT | GIOA[7] | N2HET1 [15] | N2HET1 [24] | NC | N2HET1 [7] | N2HET1 [3] | VSS | VSS | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T | U | V | W | |

**Figure 4-2. ZWT Package Pinout. Top View**

Note: Balls can have multiplexed functions. Only the default function is depicted in above diagram.

## 4.3 Terminal Functions

Section 4.3.1 and Section 4.3.2 identify the external signal names, the associated pin/ball numbers along with the mechanical package designator, the pin/ball type (Input, Output, IO, Power or Ground), whether the pin/ball has any internal pullup/pulldown, whether the pin/ball can be configured as a GPIO, and a functional pin/ball description. The first signal name listed is the primary function for that terminal. The signal name in **Bold** is the function being described. Refer to the I/O Multiplexing Module (IOMM) chapter of the TMS570LS12x/11x Technical Reference Manual (SPNU515).

**NOTE**

In the Terminal Functions table below, the "Reset Pull State" is the state of the pull applied to the terminal while nPORRST is low and immediately after nPORRST goes High. The default pull direction may change when software configures the pin for an alternate function. The "Pull Type" is the type of pull asserted when the signal name in bold is enabled for the given terminal by the IOMM control registers.

All I/O signals except nRST are configured as inputs while nPORRST is low and immediately after nPORRST goes High. While nPORRST is low, the input buffers are disabled, and the output buffers are disabled with the default pulls enabled.

All output-only signals have the output buffer disabled and the default pull enabled while nPORRST is low, and are configured as outputs with the pulls disabled immediately after nPORRST goes High.

### *4.3.1 PGE Package*

#### 4.3.1.1 Multibuffered Analog-to-Digital Converters (MibADC)

**Table 4-1. PGE Multibuffered Analog-to-Digital Converters (MibADC1, MibADC2)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| **ADREFHI**(1) | 66 | Power | N/A | None | ADC high reference supply |
| **ADREFLO**(1) | 67 | Power | | | ADC low reference supply |
| **VCCAD**(1) | 69 | Power | | | Operating supply for ADC |
| **VSSAD**(1) | 68 | Ground | | | |
| **AD1EVT** | 86 | I/O | Pull Down | Programmable, 20 µA | ADC1 event trigger input, or GPIO |
| MIBSPI3NCS[0]/**AD2EVT**/GIOB[2]/ EQEP1I/N2HET2_PIN_nDIS | 55 | I/O | Pull Up | Programmable, 20 µA | ADC2 event trigger input, or GPIO |
| **AD1IN[0]** | 60 | Input | N/A | None | ADC1 analog input |
| **AD1IN[1]** | 71 | | | | |
| **AD1IN[2]** | 73 | | | | |
| **AD1IN[3]** | 74 | | | | |
| **AD1IN[4]** | 76 | | | | |
| **AD1IN[5]** | 78 | | | | |
| **AD1IN[6]** | 80 | | | | |
| **AD1IN[7]** | 61 | | | | |

(1) The ADREFHI, ADREFLO, VCCAD and VSSAD connections are common for both ADC cores.

**Table 4-1. PGE Multibuffered Analog-to-Digital Converters (MibADC1, MibADC2) (continued)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| **AD1IN[8]** / AD2IN[8] | 83 | Input | N/A | None | ADC1/ADC2 shared analog inputs |
| **AD1IN[9]** / AD2IN[9] | 70 | | | | |
| **AD1IN[10]** / AD2IN[10] | 72 | | | | |
| **AD1IN[11]** / AD2IN[11] | 75 | | | | |
| **AD1IN[12]** / AD2IN[12] | 77 | | | | |
| **AD1IN[13]** / AD2IN[13] | 79 | | | | |
| **AD1IN[14]** / AD2IN[14] | 82 | | | | |
| **AD1IN[15]** / AD2IN[15] | 85 | | | | |
| **AD1IN[16]** / AD2IN[0] | 58 | | | | |
| **AD1IN[17]** / AD2IN[1] | 59 | | | | |
| **AD1IN[18]** / AD2IN[2] | 62 | | | | |
| **AD1IN[19]** / AD2IN[3] | 63 | | | | |
| **AD1IN[20]** / AD2IN[4] | 64 | | | | |
| **AD1IN[21]** / AD2IN[5] | 65 | | | | |
| **AD1IN[22]** / AD2IN[6] | 81 | | | | |
| **AD1IN[23]** / AD2IN[7] | 84 | | | | |
| MIBSPI3SOMI[0]/**AWM1_EXT_ENA**/ECAP2 | 51 | Output | Pull Up | None | AWM1 external analog mux enable |
| MIBSPI3SIMO[0]/**AWM1_EXT_SEL[0]**/ECAP3 | 52 | Output | Pull Up | None | AWM1 external analog mux select line0 |
| MIBSPI3CLK/**AWM1_EXT_SEL[1]**/EQEP1A | 53 | Output | Pull Up | None | AWM1 external analog mux select line0 |

#### 4.3.1.2 Enhanced High-End Timer Modules (N2HET)

**Table 4-2. PGE Enhanced High-End Timer Modules (N2HET)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| **N2HET1[0]**/SPI4CLK/EPWM2B | 25 | I/O | Pull Down | Programmable, 20 µA | N2HET1 time input capture or output compare, or GIO.<br>Each terminal has a suppression filter with a programmable duration. |
| **N2HET1[1]**/SPI4NENA/N2HET2[8]/EQEP2A | 23 | | | | |
| **N2HET1[2]**/SPI4SIMO[0]/EPWM3A | 30 | | | | |
| **N2HET1[3]**/SPI4NCS[0]/N2HET2[10]/EQEP2B | 24 | | | | |
| **N2HET1[4]**/EPWM4B | 36 | | | | |
| **N2HET1[5]**/SPI4SOMI[0]/N2HET2[12]/EPWM3B | 31 | | | | |
| **N2HET1[6]**/SCIRX/EPWM5A | 38 | | | | |
| **N2HET1[7]**/N2HET2[14]/EPWM7B | 33 | | | | |
| **N2HET1[8]**/MIBSPI1SIMO[1] | 106 | | | | |
| **N2HET1[9]**/N2HET2[16]/EPWM7A | 35 | | | | |
| **N2HET1[10]**/nTZ3 | 118 | | | | |
| **N2HET1[11]**/MIBSPI3NCS[4]/N2HET2[18]/ EPWM1SYNCO | 6 | | | | |
| **N2HET1[12]** | 124 | | | | |
| **N2HET1[13]**/SCITX/EPWM5B | 39 | | | | |
| **N2HET1[14]** | 125 | | | | |
| **N2HET1[15]**/MIBSPI1NCS[4]/ECAP1 | 41 | | | | |
| **N2HET1[16]**/EPWM1SYNCI/EPWM1SYNCO | 139 | | | | |
| MIBSPI1NCS[1]/**N2HET1[17]**/EQEP1S | 130 | | Pull Up | | |
| **N2HET1[18]**/EPWM6A | 140 | | Pull Down | | |
| MIBSPI1NCS[2]/**N2HET1[19]** | 40 | | Pull Up | | |
| **N2HET1[20]**/EPWM6B | 141 | | Pull Down | | |
| **N2HET1[22]** | 15 | | | | |
| MIBSPI1NENA/**N2HET1[23]**/ECAP4 | 96 | | Pull Up | | |
| **N2HET1[24]**/MIBSPI1NCS[5] | 91 | | Pull Down | | |
| MIBSPI3NCS[1]/**N2HET1[25]**/MDCLK | 37 | | Pull Up | | |
| **N2HET1[26]** | 92 | | Pull Down | | |
| MIBSPI3NCS[2]/I2C_SDA/**N2HET1[27]**/nTZ2 | 4 | | Pull Up | | |
| **N2HET1[28]** | 107 | | Pull Down | | |
| MIBSPI3NCS[3]/I2C_SCL/**N2HET1[29]**/nTZ1 | 3 | | Pull Up | | |
| **N2HET1[30]**/EQEP2S | 127 | | Pull Down | | |
| MIBSPI3NENA/MIBSPI3NCS[5]/**N2HET1[31]**/EQEP1B | 54 | | Pull Up | | |

**Table 4-2. PGE Enhanced High-End Timer Modules (N2HET) (continued)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| GIOA[5]/EXTCLKIN/EPWM1A/**N2HET1_PIN_nDIS** | 14 | I/O | Pull Down | Programmable, 20 µA(1) | Disable selected PWM outputs |
| GIOA[2]/**N2HET2[0]**/ EQEP2I | 9 | I/O | Pull Down | Programmable, 20 µA | N2HET2 time input capture or output compare, or GPIO<br>Each terminal has a suppression filter with a programmable duration. |
| GIOA[6]/**N2HET2[4]**/EPWM1B | 16 | | | | |
| GIOA[7]/**N2HET2[6]**/EPWM2A | 22 | | | | |
| N2HET1[1]/SPI4NENA/**N2HET2[8]**/EQEP2A | 23 | | | | |
| N2HET1[3]/SPI4NCS[0]/**N2HET2[10]**/EQEP2B | 24 | | | | |
| N2HET1[5]/SPI4SOMI[0]/**N2HET2[12]**/EPWM3B | 31 | | | | |
| N2HET1[7]/**N2HET2[14]**/EPWM7B | 33 | | | | |
| N2HET1[9]/**N2HET2[16]**/EPWM7A | 35 | | | | |
| N2HET1[11]/MIBSPI3NCS[4]/**N2HET2[18]**/ EPWM1SYNCO | 6 | | | | |
| MIBSPI3NCS[0]/AD2EVT/GIOB[2]/ EQEP1I/**N2HET2_PIN_nDIS** | 55 | I/O | Pull Up | Programmable, 20 µA(1) | Disable selected PWM outputs |

(1) The N2HETx_PIN_nDIS function is always available on this terminal. There is no mux control to select this function. The pull direction is controlled by the function which is selected by the output mux control for this terminal.

### 4.3.1.3 Enhanced Capture Modules (eCAP)

**Table 4-3. PGE Enhanced Capture Modules (eCAP)(1)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| N2HET1[15]/MIBSPI1NCS[4]/**ECAP1** | 41 | I/O | Pull Down | Fixed 20 µA Pull Up | Enhanced Capture Module 1 I/O |
| MIBSPI3SOMI[0]/AWM1_EXT_ENA/**ECAP2** | 51 | | Pull Up | | Enhanced Capture Module 2 I/O |
| MIBSPI3SIMO[0]/AWM1_EXT_SEL[0]/**ECAP3** | 52 | | | | Enhanced Capture Module 3 I/O |
| MIBSPI1NENA/N2HET1[23]/**ECAP4** | 96 | | | | Enhanced Capture Module 4 I/O |
| MIBSPI5NENA/MIBSPI5SOMI[1]/ **ECAP5** | 97 | | | | Enhanced Capture Module 5 I/O |
| MIBSPI1NCS[0]/MIBSPI1SOMI[1]/**ECAP6** | 105 | | | | Enhanced Capture Module 6 I/O |

(1) These signals, when used as inputs, are double-synchronized and then optionally filtered with a 6-cycle VCLK4-based counter.

#### 4.3.1.4 Enhanced Quadrature Encoder Pulse Modules (eQEP)

**Table 4-4. PGE Enhanced Quadrature Encoder Pulse Modules (eQEP)(1)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| MIBSPI3CLK/AWM1_EXT_SEL[1]/**EQEP1A** | 53 | Input | Pull Up | Fixed 20 µA Pull Up | Enhanced QEP1 Input A |
| MIBSPI3NENA/MIBSPI3NCS[5]/N2HET1[31]/**EQEP1B** | 54 | Input | | | Enhanced QEP1 Input B |
| MIBSPI3NCS[0]/AD2EVT/GIOB[2]/ **EQEP1I**/N2HET2_PIN_nDIS | 55 | I/O | | | Enhanced QEP1 Index |
| MIBSPI1NCS[1]/N2HET1[17]/**EQEP1S** | 130 | I/O | | | Enhanced QEP1 Strobe |
| N2HET1[1]/SPI4NENA/N2HET2[8]/**EQEP2A** | 23 | Input | Pull Down | | Enhanced QEP2 Input A |
| N2HET1[3]/SPI4NCS[0]/N2HET2[10]/**EQEP2B** | 24 | Input | | | Enhanced QEP2 Input B |
| GIOA[2]/N2HET2[0]/ **EQEP2I** | 9 | I/O | | | Enhanced QEP2 Index |
| N2HET1[30]/**EQEP2S** | 127 | I/O | | | Enhanced QEP2 Strobe |

(1) These signals are double-synchronized and then optionally filtered with a 6-cycle VCLK4-based counter.

#### 4.3.1.5 Enhanced Pulse-Width Modulator Modules (ePWM)

**Table 4-5. PGE Enhanced Pulse-Width Modulator Modules (ePWM)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| GIOA[5]/EXTCLKIN/**EPWM1A**/N2HET1_PIN_nDIS | 14 | Output | Pull Down | None | Enhanced PWM1 Output A |
| GIOA[6]/N2HET2[4]/**EPWM1B** | 16 | | | | Enhanced PWM1 Output B |
| N2HET1[11]/MIBSPI3NCS[4]/N2HET2[18]/**EPWM1SYNCO** | 6 | | | | External ePWM Sync Pulse Output |
| N2HET1[16]/**EPWM1SYNCI**/EPWM1SYNCO | 139 | Input | | Fixed 20 µA Pull Up | External ePWM Sync Pulse Input |
| GIOA[7]/N2HET2[6]/**EPWM2A** | 22 | Output | | None | Enhanced PWM2 Output A |
| N2HET1[0]/SPI4CLK/**EPWM2B** | 25 | | | | Enhanced PWM2 Output B |
| N2HET1[2]/SPI4SIMO[0]/**EPWM3A** | 30 | | | | Enhanced PWM3 Output A |
| N2HET1[5]/SPI4SOMI[0]/N2HET2[12]/**EPWM3B** | 31 | | | | Enhanced PWM3 Output B |
| MIBSPI5NCS[0]/**EPWM4A** | 32 | | Pull Up | | Enhanced PWM4 Output A |
| N2HET1[4]/**EPWM4B** | 36 | | Pull Down | | Enhanced PWM4 Output B |
| N2HET1[6]/SCIRX/**EPWM5A** | 38 | | | | Enhanced PWM5 Output A |
| N2HET1[13]/SCITX/**EPWM5B** | 39 | | | | Enhanced PWM5 Output B |
| N2HET1[18]/**EPWM6A** | 140 | | | | Enhanced PWM6 Output A |
| N2HET1[20]/**EPWM6B** | 141 | | | | Enhanced PWM6 Output B |
| N2HET1[9]/N2HET2[16]/**EPWM7A** | 35 | | | | Enhanced PWM7 Output A |
| N2HET1[7]/N2HET2[14]/**EPWM7B** | 33 | | | | Enhanced PWM7 Output B |

**Table 4-5. PGE Enhanced Pulse-Width Modulator Modules (ePWM) (continued)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| MIBSPI3NCS[3]/I2C_SCL/N2HET1[29]/**nTZ1** | 3 | Input | Pull Up | Fixed 20 µA Pull Up | Trip Zone Inputs 1, 2 and 3. These signals are either connected asynchronously to the ePWMx trip zone inputs, or double-synchronized with VCLK4, or double-synchronized and then filtered with a 6-cycle VCLK4-based counter before connecting to the ePWMx trip zone inputs. |
| MIBSPI3NCS[2]/I2C_SDA/N2HET1[27]/**nTZ2** | 4 | | | | |
| N2HET1[10]/**nTZ3** | 118 | | Pull Down | | |

### 4.3.1.6 General-Purpose Input / Output (GPIO)

**Table 4-6. PGE General-Purpose Input / Output (GPIO)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| **GIOA[0]** | 2 | I/O | Pull Down | Programmable, 20 µA | General-purpose I/O. All GPIO terminals are capable of generating interrupts to the CPU on rising / falling / both edges. |
| **GIOA[1]** | 5 | | | | |
| **GIOA[2]**/N2HET2[0] /EQEP2I | 9 | | | | |
| **GIOA[5]**/EXTCLKIN/EPWM1A/N2HET1_PIN_nDIS | 14 | | | | |
| **GIOA[6]**/N2HET2[4]/EPWM1B | 16 | | | | |
| **GIOA[7]**/N2HET2[6]/EPWM2A | 22 | | | | |
| **GIOB[0]** | 126 | | | | |
| **GIOB[1]** | 133 | | | | |
| **GIOB[2]** | 142 | | | | |
| MIBSPI3NCS[0]/AD2EVT/**GIOB[2]**/ EQEP1I/N2HET2_PIN_nDIS | 55 (1) | | Pull Up | | |
| **GIOB[3]** | 1 | | Pull Down | | |

(1) GIOB[2] cannot output a level on to pin 55. Only the input functionality is supported so that the application can generate an interrupt whenever the N2HET2_PIN_nDIS is asserted (driven low). Also, a pull up is enabled on the input. This is not programmable using the GIO module control registers.

### 4.3.1.7 Controller Area Network Controllers (DCAN)

**Table 4-7. PGE Controller Area Network Controllers (DCAN)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| **CAN1RX** | 90 | I/O | Pull Up | Programmable, 20 µA | CAN1 receive, or GPIO |
| **CAN1TX** | 89 | | | | CAN1 transmit, or GPIO |
| **CAN2RX** | 129 | | | | CAN2 receive, or GPIO |
| **CAN2TX** | 128 | | | | CAN2 transmit, or GPIO |
| **CAN3RX** | 12 | | | | CAN3 receive, or GPIO |
| **CAN3TX** | 13 | | | | CAN3 transmit, or GPIO |

#### 4.3.1.8 Local Interconnect Network Interface Module (LIN)

**Table 4-8. PGE Local Interconnect Network Interface Module (LIN)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| **LINRX** | 131 | I/O | Pull Up | Programmable, 20 µA | LIN receive, or GPIO |
| **LINTX** | 132 | | | | LIN transmit, or GPIO |

#### 4.3.1.9 Standard Serial Communication Interface (SCI)

**Table 4-9. PGE Standard Serial Communication Interface (SCI)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| N2HET1[6]/**SCIRX**/EPWM5A | 38 | I/O | Pull Down | Programmable, 20 µA | SCI receive, or GPIO |
| N2HET1[13]/**SCITX**/EPWM5B | 39 | | | | SCI transmit, or GPIO |

#### 4.3.1.10 Inter-Integrated Circuit Interface Module (I2C)

**Table 4-10. PGE Inter-Integrated Circuit Interface Module (I2C)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| MIBSPI3NCS[2]/**I2C_SDA**/N2HET1[27]/nTZ2 | 4 | I/O | Pull Up | Programmable, 20 µA | I2C serial data, or GPIO |
| MIBSPI3NCS[3]/**I2C_SCL**/N2HET1[29]/nTZ1 | 3 | | | | I2C serial clock, or GPIO |

#### 4.3.1.11 Standard Serial Peripheral Interface (SPI)

**Table 4-11. PGE Standard Serial Peripheral Interface (SPI)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| N2HET1[0]/**SPI4CLK**/EPWM2B | 25 | I/O | Pull Down | Programmable, 20 µA | SPI4 clock, or GPIO |
| N2HET1[3]/**SPI4NCS[0]**/N2HET2[10]/EQEP2B | 24 | | | | SPI4 chip select, or GPIO |
| N2HET1[1]/**SPI4NENA**/N2HET2[8]/EQEP2A | 23 | | | | SPI4 enable, or GPIO |
| N2HET1[2]/**SPI4SIMO[0]**/EPWM3A | 30 | | | | SPI4 slave-input master-output, or GPIO |
| N2HET1[5]/**SPI4SOMI[0]**/N2HET2[12]/EPWM3B | 31 | | | | SPI4 slave-output master-input, or GPIO |

#### 4.3.1.12 Multibuffered Serial Peripheral Interface Modules (MibSPI)

**Table 4-12. PGE Multibuffered Serial Peripheral Interface Modules (MibSPI)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| **MIBSPI1CLK** | 95 | I/O | Pull Up | Programmable, 20 µA | MibSPI1 clock, or GPIO |
| **MIBSPI1NCS[0]**/MIBSPI1SOMI[1]/ECAP6 | 105 | | | | MibSPI1 chip select, or GPIO |
| **MIBSPI1NCS[1]**/N2HET1[17]/EQEP1S | 130 | | | | |
| **MIBSPI1NCS[2]**/N2HET1[19] | 40 | | | | |
| N2HET1[15]/**MIBSPI1NCS[4]**/ECAP1 | 41 | | Pull Down | Programmable, 20 µA | MibSPI1 chip select, or GPIO |
| N2HET1[24]/**MIBSPI1NCS[5]** | 91 | | | | |
| **MIBSPI1NENA**/N2HET1[23]/ECAP4 | 96 | | Pull Up | Programmable, 20 µA | MibSPI1 enable, or GPIO |
| **MIBSPI1SIMO[0]** | 93 | | | | MibSPI1 slave-in master-out, or GPIO |
| N2HET1[8]/**MIBSPI1SIMO[1]** | 106 | | Pull Down | Programmable, 20 µA | MibSPI1 slave-in master-out, or GPIO |
| **MIBSPI1SOMI[0]** | 94 | | Pull Up | Programmable, 20 µA | MibSPI1 slave-out master-in, or GPIO |
| MIBSPI1NCS[0]/**MIBSPI1SOMI[1]**/ECAP6 | 105 | | | | |
| **MIBSPI3CLK**/AWM1_EXT_SEL[1]/EQEP1A | 53 | I/O | Pull Up | Programmable, 20 µA | MibSPI3 clock, or GPIO |
| **MIBSPI3NCS[0]**/AD2EVT/GIOB[2]/ EQEP1I/N2HET2_PIN_nDIS | 55 | | | | MibSPI3 chip select, or GPIO |
| **MIBSPI3NCS[1]**/N2HET1[25]/MDCLK | 37 | | | | |
| **MIBSPI3NCS[2]**/I2C_SDA/N2HET1[27]/nTZ2 | 4 | | | | |
| **MIBSPI3NCS[3]**/I2C_SCL/N2HET1[29]/nTZ1 | 3 | | | | |
| N2HET1[11]/**MIBSPI3NCS[4]**/N2HET2[18]/EPWM1SYNCO | 6 | | Pull Down | Programmable, 20 µA | MibSPI3 chip select, or GPIO |
| MIBSPI3NENA /**MIBSPI3NCS[5]**/N2HET1[31]/EQEP1B | 54 | | Pull Up | Programmable, 20 µA | MibSPI3 chip select, or GPIO |
| **MIBSPI3NENA**/MIBSPI3NCS[5]/N2HET1[31]/EQEP1B | 54 | | | | MibSPI3 enable, or GPIO |
| **MIBSPI3SIMO[0]**/AWM1_EXT_SEL[0]/ECAP3 | 52 | | | | MibSPI3 slave-in master-out, or GPIO |
| **MIBSPI3SOMI[0]**/AWM1_EXT_ENA/ECAP2 | 51 | | | | MibSPI3 slave-out master-in, or GPIO |
| **MIBSPI5CLK** | 100 | I/O | Pull Up | Programmable, 20 µA | MibSPI5 clock, or GPIO |
| **MIBSPI5NCS[0]**/EPWM4A | 32 | | | | MibSPI5 chip select, or GPIO |
| **MIBSPI5NENA**/MIBSPI5SOMI[1]/ ECAP5 | 97 | | | | MibSPI5 enable, or GPIO |
| **MIBSPI5SIMO[0]**/MIBSPI5SOMI[2] | 99 | | | | MibSPI5 slave-in master-out, or GPIO |
| **MIBSPI5SOMI[0]** | 98 | | | | MibSPI5 slave-out master-in, or GPIO |
| MIBSPI5NENA/**MIBSPI5SOMI[1]**/ ECAP5 | 97 | | | | MibSPI5 slave-out master-in, or GPIO |
| MIBSPI5SIMO[0]/**MIBSPI5SOMI[2]** | 99 | | | | MibSPI5 slave-out master-in, or GPIO |

#### 4.3.1.13 System Module Interface

**Table 4-13. PGE System Module Interface**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| **nPORRST** | 46 | Input | Pull Down | Fixed 100 µA Pull Down | Power-on reset, cold reset External power supply monitor circuitry must drive nPORRST low when any of the supplies to the microcontroller fall out of the specified range. This terminal has a glitch filter. See Section 6.8. |
| **nRST** | 116 | I/O | Pull Up | Fixed 100 µA Pull Up | System reset, warm reset, bidirectional. The internal circuitry indicates any reset condition by driving nRST low. The external circuitry can assert a system reset by driving nRST low. To ensure that an external reset is not arbitrarily generated, TI recommends that an external pull-up resistor is connected to this terminal. This terminal has a glitch filter. See Section 6.8. |
| **nERROR** | 117 | I/O | Pull Down | Fixed 20 µA Pull Down | ESM Error Signal Indicates error of high severity. See Section 6.18. |

#### 4.3.1.14 Clock Inputs and Outputs

**Table 4-14. PGE Clock Inputs and Outputs**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| **OSCIN** | 18 | Input | N/A | None | From external crystal/resonator, or external clock input |
| **KELVIN_GND** | 19 | Input | | | Kelvin ground for oscillator |
| **OSCOUT** | 20 | Output | | | To external crystal/resonator |
| **ECLK** | 119 | I/O | Pull Down | Programmable, 20 µA | External prescaled clock output, or GPIO. |
| GIOA[5]/**EXTCLKIN**/EPWM1A /N2HET1_PIN_nDIS | 14 | Input | Pull Down | Fixed 20 µA Pull Down | External clock input #1 |

#### 4.3.1.15 Test and Debug Modules Interface

**Table 4-15. PGE Test and Debug Modules Interface**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| **TEST** | 34 | Input | Pull Down | Fixed 100 µA Pull Down | Test enable. This terminal must be connected to ground directly or via a pull-down resistor. |
| **nTRST** | 109 | Input | | | JTAG test hardware reset |
| **RTCK** | 113 | Output | N/A | None | JTAG return test clock |
| **TCK** | 112 | Input | Pull Down | Fixed 100 µA Pull Down | JTAG test clock |
| **TDI** | 110 | Input | Pull Up | Fixed 100 µA Pull Up | JTAG test data in |
| **TDO** | 111 | Output | 100 µA Pull Down | None | JTAG test data out |
| **TMS** | 108 | Input | Pull Up | Fixed 100 µA Pull Up | JTAG test select |

#### 4.3.1.16 Flash Supply and Test Pads

**Table 4-16. PGE Flash Supply and Test Pads**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| **VCCP** | 134 | 3.3V Power | N/A | None | Flash pump supply |
| **FLTP1** | 7 | - | N/A- | None | Flash test pads. These terminals are reserved for TI use only. For proper operation these terminals must connect only to a test pad or not be connected at all [no connect (NC)]. |
| **FLTP2** | 8 | | | | |

#### 4.3.1.17 Supply for Core Logic: 1.2V nominal

**Table 4-17. PGE Supply for Core Logic: 1.2V nominal**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| **VCC** | 17 | 1.2V Power | N/A | None | Core supply |
| **VCC** | 29 | | | | |
| **VCC** | 45 | | | | |
| **VCC** | 48 | | | | |
| **VCC** | 49 | | | | |
| **VCC** | 57 | | | | |
| **VCC** | 87 | | | | |
| **VCC** | 101 | | | | |
| **VCC** | 114 | | | | |
| **VCC** | 123 | | | | |
| **VCC** | 137 | | | | |
| **VCC** | 143 | | | | |

#### 4.3.1.18 Supply for I/O Cells: 3.3V nominal

**Table 4-18. PGE Supply for I/O Cells: 3.3V nominal**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| **VCCIO** | 10 | 3.3V Power | N/A | None | Operating supply for I/Os |
| **VCCIO** | 26 | | | | |
| **VCCIO** | 42 | | | | |
| **VCCIO** | 104 | | | | |
| **VCCIO** | 120 | | | | |
| **VCCIO** | 136 | | | | |

#### 4.3.1.19 Ground Reference for All Supplies Except VCCAD

**Table 4-19. PGE Ground Reference for All Supplies Except VCCAD**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 144 PGE | | | | |
| **VSS** | 11 | Ground | N/A | None | Ground reference |
| **VSS** | 21 | | | | |
| **VSS** | 27 | | | | |
| **VSS** | 28 | | | | |
| **VSS** | 43 | | | | |
| **VSS** | 44 | | | | |
| **VSS** | 47 | | | | |
| **VSS** | 50 | | | | |
| **VSS** | 56 | | | | |
| **VSS** | 88 | | | | |
| **VSS** | 102 | | | | |
| **VSS** | 103 | | | | |
| **VSS** | 115 | | | | |
| **VSS** | 121 | | | | |
| **VSS** | 122 | | | | |
| **VSS** | 135 | | | | |
| **VSS** | 138 | | | | |
| **VSS** | 144 | | | | |

## 4.3.2 ZWT Package

### 4.3.2.1 Multibuffered Analog-to-Digital Converters (MibADC)

**Table 4-20. ZWT Multibuffered Analog-to-Digital Converters (MibADC1, MibADC2)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| **ADREFHI**(1) | V15 | Power | N/A | None | ADC high reference supply |
| **ADREFLO**(1) | V16 | Power | | | ADC low reference supply |
| **VCCAD**(1) | W15 | Power | | | Operating supply for ADC |
| **VSSAD** | V19 | Ground | N/A | None | ADC supply power |
| **VSSAD** | W16 | | | | |
| **VSSAD** | W18 | | | | |
| **VSSAD** | W19 | | | | |
| **AD1EVT** | N19 | I/O | Pull Down | Programmable, 20 µA | ADC1 event trigger input, or GPIO |
| MIBSPI3NCS[0]/**AD2EVT**/GIOB[2]/ EQEP1I/N2HET2_PIN_nDIS | V10 | I/O | Pull Up | Programmable, 20 µA | ADC2 event trigger input, or GPIO |
| **AD1IN[0]** | W14 | Input | N/A | None | ADC1 analog input |
| **AD1IN[1]** | V17 | | | | |
| **AD1IN[2]** | V18 | | | | |
| **AD1IN[3]** | T17 | | | | |
| **AD1IN[4]** | U18 | | | | |
| **AD1IN[5]** | R17 | | | | |
| **AD1IN[6]** | T19 | | | | |
| **AD1IN[7]** | V14 | | | | |
| **AD1IN[8]** / AD2IN[8] | P18 | Input | N/A | None | ADC1/ADC2 shared analog inputs |
| **AD1IN[9]** / AD2IN[9] | W17 | | | | |
| **AD1IN[10]** / AD2IN[10] | U17 | | | | |
| **AD1IN[11]** / AD2IN[11] | U19 | | | | |
| **AD1IN[12]** / AD2IN[12] | T16 | | | | |
| **AD1IN[13]** / AD2IN[13] | T18 | | | | |
| **AD1IN[14]** / AD2IN[14] | R18 | | | | |
| **AD1IN[15]** / AD2IN[15] | P19 | | | | |
| **AD1IN[16]** / AD2IN[0] | V13 | | | | |
| **AD1IN[17]** / AD2IN[1] | U13 | | | | |
| **AD1IN[18]** / AD2IN[2] | U14 | | | | |
| **AD1IN[19]** / AD2IN[3] | U16 | | | | |
| **AD1IN[20]** / AD2IN[4] | U15 | | | | |
| **AD1IN[21]** / AD2IN[5] | T15 | | | | |
| **AD1IN[22]** / AD2IN[6] | R19 | | | | |
| **AD1IN[23]** / AD2IN[7] | R16 | | | | |
| MIBSPI3SOMI[0]/**AWM1_EXT_ENA**/ECAP2 | V8 | Output | Pull Up | None | AWM1 external analog mux enable |
| MIBSPI3SIMO[0]/**AWM1_EXT_SEL[0]**/ECAP3 | W8 | | | | AWM1 external analog mux select line0 |
| MIBSPI3CLK/**AWM1_EXT_SEL[1]**/EQEP1A | V9 | | | | AWM1 external analog mux select line0 |

(1) The ADREFHI, ADREFLO, VCCAD and VSSAD connections are common for both ADC cores.

### 4.3.2.2 Enhanced High-End Timer Modules (N2HET)

**Table 4-21. ZWT Enhanced High-End Timer Modules (N2HET)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| **N2HET1[0]**/SPI4CLK/EPWM2B | K18 | I/O | Pull Down | Programmable, 20 µA | N2HET1 time input capture or output compare, or GIO.<br>Each terminal has a suppression filter with a programmable duration. |
| **N2HET1[1]**/SPI4NENA/N2HET2[8]/EQEP2A | V2 | | | | |
| **N2HET1[2]**/SPI4SIMO[0]/EPWM3A | W5 | | | | |
| **N2HET1[3]**/SPI4NCS[0]/N2HET2[10]/EQEP2B | U1 | | | | |
| **N2HET1[4]**/EPWM4B | B12 | | | | |
| **N2HET1[5]**/SPI4SOMI[0]/N2HET2[12]/EPWM3B | V6 | | | | |
| **N2HET1[6]**/SCIRX/EPWM5A | W3 | | | | |
| **N2HET1[7]**/N2HET2[14]/EPWM7B | T1 | | | | |
| **N2HET1[8]**/MIBSPI1SIMO[1] | E18 | | | | |
| **N2HET1[9]**/N2HET2[16]/EPWM7A | V7 | | | | |
| **N2HET1[10]**/nTZ3 | D19 | | | | |
| **N2HET1[11]**/MIBSPI3NCS[4]/N2HET2[18]/EPWM1SYNCO | E3 | | | | |
| **N2HET1[12]** | B4 | | | | |
| **N2HET1[13]**/SCITX/EPWM5B | N2 | | | | |
| **N2HET1[14]** | A11 | | | | |
| **N2HET1[15]**/MIBSPI1NCS[4]/ECAP1 | N1 | | | | |
| **N2HET1[16]**/EPWM1SYNCI/EPWM1SYNCO | A4 | | | | |
| **N2HET1[17]** | A13 | | | | |
| MIBSPI1NCS[1]/**N2HET1[17]**/ EQEP1S | F3 | | | | |
| **N2HET1[18]**/EPWM6A | J1 | | | | |
| **N2HET1[19]** | B13 | | | | |
| MIBSPI1NCS[2]/**N2HET1[19]** | G3 | | | | |
| **N2HET1[20]**/EPWM6B | P2 | | | | |
| **N2HET1[21]** | H4 | | | | |
| MIBSPI1NCS[3]/**N2HET1[21]** | J3 | | | | |
| **N2HET1[22]** | B3 | | | | |
| **N2HET1[23]** | J4 | | | | |
| MIBSPI1NENA/**N2HET1[23]**/ECAP4 | G19 | | Pull Up | | |
| **N2HET1[24]**/MIBSPI1NCS[5] | P1 | | Pull Down | | |
| **N2HET1[25]** | M3 | | | | |
| MIBSPI3NCS[1]/**N2HET1[25]**/MDCLK | V5 | | | | |
| **N2HET1[26]** | A14 | | | | |
| **N2HET1[27]** | A9 | | | | |
| MIBSPI3NCS[2]/I2C_SDA/**N2HET1[27]**/nTZ2 | B2 | | Pull Up | | |
| **N2HET1[28]** | K19 | | Pull Down | | |
| **N2HET1[29]** | A3 | | | | |
| MIBSPI3NCS[3]/I2C_SCL/**N2HET1[29]**/nTZ1 | C3 | | | | |

**Table 4-21. ZWT Enhanced High-End Timer Modules (N2HET) (continued)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| **N2HET1[30]**/EQEP2S | B11 | I/O | Pull Down | Programmable, 20 µA | |
| **N2HET1[31]** | J17 | | | | |
| MIBSPI3NENA/MIBSPI3NCS[5]/**N2HET1[31]**/EQEP1B | W9 | | Pull Up | | |
| GIOA[5]/EXTCLKIN/EPWM1A/**N2HET1_PIN_nDIS** | B5 | input | Pull Down | Programmable, 20 µA(1) | Disable selected PWM outputs |
| GIOA[2]/**N2HET2[0]** /EQEP2I | C1 | I/O | Pull Down | Programmable, 20 µA | N2HET2 time input capture or output compare, or GIO.<br>Each terminal has a suppression filter with a programmable duration. |
| EMIF_ADDR[0]/**N2HET2[1]** | D4 | | | | |
| GIOA[3]/**N2HET2[2]** | E1 | | | | |
| EMIF_ADDR[1]/**N2HET2[3]** | D5 | | | | |
| GIOA[6]/**N2HET2[4]**/EPWM1B | H3 | | | | |
| EMIF_BA[1]/**N2HET2[5]** | D16 | | | | |
| GIOA[7]/**N2HET2[6]**/EPWM2A | M1 | | | | |
| EMIF_nCS[0]/**N2HET2[7]** | N17 | | | | |
| N2HET1[1]/SPI4NENA/ **N2HET2[8]**/EQEP2A | V2 | | | | |
| EMIF_nCS[3]/**N2HET2[9]** | K17 | | | | |
| N2HET1[3]/SPI4NCS[0]/**N2HET2[10]**/EQEP2B | U1 | | | | |
| EMIF_ADDR[6]/**N2HET2[11]** | C4 | | | | |
| N2HET1[5]/SPI4SOMI[0]/**N2HET2[12]**/EPWM3B | V6 | | | | |
| EMIF_ADDR[7]/**N2HET2[13]** | C5 | | | | |
| N2HET1[7]/**N2HET2[14]**/EPWM7B | T1 | | | | |
| EMIF_ADDR[8]/**N2HET2[15]** | C6 | | | | |
| N2HET1[9]/**N2HET2[16]**/EPWM7A | V7 | | | | |
| N2HET1[11]/MIBSPI3NCS[4]/**N2HET2[18]**/EPWM1SYNCO | E3 | | | | |
| MIBSPI3NCS[0]/AD2EVT/GIOB[2]/ EQEP1I/**N2HET2_PIN_nDIS** | V10 | I/O | Pull Up | Programmable, 20 µA(1) | Disable selected PWM outputs |

(1) The N2HETx_PIN_nDIS function is always available on this terminal. There is no mux control to select this function. The pull direction is controlled by the function which is selected by the output mux control for this terminal.

### 4.3.2.3 Enhanced Capture Modules (eCAP)

**Table 4-22. ZWT Enhanced Capture Modules (eCAP)(1)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| N2HET1[15]/MIBSPI1NCS[4]/**ECAP1** | N1 | I/O | Pull Down | Fixed 20 µA Pull Up | Enhanced Capture Module 1 I/O |
| MIBSPI3SOMI[0]/AWM1_EXT_ENA/**ECAP2** | V8 | I/O | Pull Up | | Enhanced Capture Module 2 I/O |
| MIBSPI3SIMO[0]/AWM1_EXT_SEL[0]/**ECAP3** | W8 | I/O | | | Enhanced Capture Module 3 I/O |
| MIBSPI1NENA/N2HET1[23]/**ECAP4** | G19 | I/O | | | Enhanced Capture Module 4 I/O |
| MIBSPI5NENA/MIBSPI5SOMI[1]/ **ECAP5** | H18 | I/O | | | Enhanced Capture Module 5 I/O |
| MIBSPI1NCS[0]/MIBSPI1SOMI[1]/ **ECAP6** | R2 | I/O | | | Enhanced Capture Module 6 I/O |

(1) These signals, when used as inputs, are double-synchronized and then optionally filtered with a 6-cycle VCLK4-based counter.

### 4.3.2.4 Enhanced Quadrature Encoder Pulse Modules (eQEP)

**Table 4-23. ZWT Enhanced Quadrature Encoder Pulse Modules (eQEP)(1)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| MIBSPI3CLK/AWM1_EXT_SEL[1]/**EQEP1A** | V9 | Input | Pull Up | Fixed 20 µA Pull Up | Enhanced QEP1 Input A |
| MIBSPI3NENA/MIBSPI3NCS[5]/N2HET1[31]/**EQEP1B** | W9 | Input | | | Enhanced QEP1 Input B |
| MIBSPI3NCS[0]/AD2EVT/GIOB[2]/ **EQEP1I**/N2HET2_PIN_nDIS | V10 | I/O | | | Enhanced QEP1 Index |
| MIBSPI1NCS[1]/N2HET1[17]/ **EQEP1S** | F3 | I/O | | | Enhanced QEP1 Strobe |
| N2HET1[1]/SPI4NENA/N2HET2[8]/**EQEP2A** | V2 | Input | Pull Down | | Enhanced QEP2 Input A |
| N2HET1[3]/SPI4NCS[0]/N2HET2[10]/**EQEP2B** | U1 | Input | Pull Down | | Enhanced QEP2 Input B |
| GIOA[2]/N2HET2[0]/ **EQEP2I** | C1 | I/O | Pull Down | | Enhanced QEP2 Index |
| N2HET1[30]/**EQEP2S** | B11 | I/O | Pull Down | | Enhanced QEP2 Strobe |

(1) These signals are double-synchronized and then optionally filtered with a 6-cycle VCLK4-based counter.

#### 4.3.2.5 Enhanced Pulse-Width Modulator Modules (ePWM)

**Table 4-24. ZWT Enhanced Pulse-Width Modulator Modules (ePWM)**

| TERMINAL | | SIGNAL TYPE | Reset Pull State | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| GIOA[5]/EXTCLKIN/**EPWM1A**/N2HET1_PIN_nDIS | B5 | Output | Pull Down | None | Enhanced PWM1 Output A |
| GIOA[6]/N2HET2[4]/**EPWM1B** | H3 | | | | Enhanced PWM1 Output B |
| N2HET1[11]/MIBSPI3NCS[4]/N2HET2[18]/**EPWM1SYNCO** | E3 | | | | External ePWM Sync Pulse Output |
| N2HET1[16]/**EPWM1SYNCI**/EPWM1SYNCO | A4 | Input | | Fixed 20 µA Pull Up | External ePWM Sync Pulse Input |
| GIOA[7]/N2HET2[6]/**EPWM2A** | M1 | Output | | None | Enhanced PWM2 Output A |
| N2HET1[0]/SPI4CLK/**EPWM2B** | K18 | | | | Enhanced PWM2 Output B |
| N2HET1[2]/SPI4SIMO[0]/**EPWM3A** | W5 | | | | Enhanced PWM3 Output A |
| N2HET1[5]/SPI4SOMI[0]/N2HET2[12]/**EPWM3B** | V6 | | | | Enhanced PWM3 Output B |
| MIBSPI5NCS[0]/**EPWM4A** | E19 | | Pull Up | | Enhanced PWM4 Output A |
| N2HET1[4]/**EPWM4B** | B12 | | Pull Down | | Enhanced PWM4 Output B |
| N2HET1[6]/SCIRX/**EPWM5A** | W3 | | | | Enhanced PWM5 Output A |
| N2HET1[13]/SCITX/**EPWM5B** | N2 | | | | Enhanced PWM5 Output B |
| N2HET1[18]/**EPWM6A** | J1 | | | | Enhanced PWM6 Output A |
| N2HET1[20]/**EPWM6B** | P2 | | | | Enhanced PWM6 Output B |
| N2HET1[9]/N2HET2[16]/**EPWM7A** | V7 | | | | Enhanced PWM7 Output A |
| N2HET1[7]/N2HET2[14]/**EPWM7B** | T1 | | | | Enhanced PWM7 Output B |
| MIBSPI3NCS[3]/I2C_SCL/N2HET1[29]/**nTZ1** | C3 | Input | Pull Up | Fixed 20 µA Pull Up | Trip Zone Inputs 1, 2 and 3. These signals are either connected asynchronously to the ePWMx trip zone inputs, or double-synchronized with VCLK4, or double-synchronized and then filtered with a 6-cycle VCLK4-based counter before connecting to the ePWMx trip zone inputs. |
| MIBSPI3NCS[2]/I2C_SDA/N2HET1[27]/**nTZ2** | B2 | | | | |
| N2HET1[10]/**nTZ3** | D19 | | Pull Down | | |

#### 4.3.2.6 General-Purpose Input / Output (GPIO)

**Table 4-25. ZWT General-Purpose Input / Output (GPIO)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| **GIOA[0]** | A5 | I/O | Pull Down | Programmable, 20 µA | General-purpose I/O. All GPIO terminals are capable of generating interrupts to the CPU on rising / falling / both edges. |
| **GIOA[1]** | C2 | | | | |
| **GIOA[2]**/N2HET2[0] /EQEP2I | C1 | | | | |
| **GIOA[3]**/N2HET2[2] | E1 | | | | |
| **GIOA[4]** | A6 | | | | |
| **GIOA[5]**/EXTCLKIN/EPWM1A/N2HET1_PIN_nDIS | B5 | | | | |
| **GIOA[6]**/N2HET2[4]/EPWM1B | H3 | | | | |
| **GIOA[7]**/N2HET2[6]/EPWM2A | M1 | | | | |
| **GIOB[0]** | M2 | | | | |
| **GIOB[1]** | K2 | | | | |
| **GIOB[2]** | F2 | | | | |
| MIBSPI3NCS[0]/AD2EVT/**GIOB[2]**/ EQEP1I/N2HET2_PIN_nDIS | V10(1) | | | | |
| **GIOB[3]** | W10 | | | | |
| **GIOB[4]** | G1 | | | | |
| **GIOB[5]** | G2 | | | | |
| **GIOB[6]** | J2 | | | | |
| **GIOB[7]** | F1 | | | | |

(1) GIOB[2] cannot output a level on to terminal V10. Only the input functionality is supported so that the application can generate an interrupt whenever the N2HET2_PIN_nDIS is asserted (driven low). Also, a pull up is enabled on the input. This is not programmable using the GIO module control registers.

#### 4.3.2.7 Controller Area Network Controllers (DCAN)

**Table 4-26. ZWT Controller Area Network Controllers (DCAN)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| **CAN1RX** | B10 | I/O | Pull Up | Programmable, 20 µA | CAN1 receive, or GPIO |
| **CAN1TX** | A10 | | | | CAN1 transmit, or GPIO |
| **CAN2RX** | H1 | | | | CAN2 receive, or GPIO |
| **CAN2TX** | H2 | | | | CAN2 transmit, or GPIO |
| **CAN3RX** | M19 | | | | CAN3 receive, or GPIO |
| **CAN3TX** | M18 | | | | CAN3 transmit, or GPIO |

#### 4.3.2.8 Local Interconnect Network Interface Module (LIN)

**Table 4-27. ZWT Local Interconnect Network Interface Module (LIN)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| **LINRX** | A7 | I/O | Pull Up | Programmable, 20 µA | LIN receive, or GPIO |
| **LINTX** | B7 | | | | LIN transmit, or GPIO |

#### 4.3.2.9 Standard Serial Communication Interface (SCI)

**Table 4-28. ZWT Standard Serial Communication Interface (SCI)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| N2HET1[6]/**SCIRX**/EPWM5A | W3 | I/O | Pull Down | Programmable, 20 µA | SCI receive, or GPIO |
| N2HET1[13]/**SCITX**/EPWM5B | N2 | | | | SCI transmit, or GPIO |

#### 4.3.2.10 Inter-Integrated Circuit Interface Module (I2C)

**Table 4-29. ZWT Inter-Integrated Circuit Interface Module (I2C)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| MIBSPI3NCS[2]/**I2C_SDA**/N2HET1[27]/nTZ2 | B2 | I/O | Pull Up | Programmable, 20 µA | I2C serial data, or GPIO |
| MIBSPI3NCS[3]/**I2C_SCL**/N2HET1[29]/nTZ1 | C3 | | | | I2C serial clock, or GPIO |

#### 4.3.2.11 Standard Serial Peripheral Interface (SPI)

**Table 4-30. ZWT Standard Serial Peripheral Interface (SPI)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| **SPI2CLK** | E2 | I/O | Pull Up | Programmable, 20 µA | SPI2 clock, or GPIO |
| **SPI2NCS[0]** | N3 | | | | SPI2 chip select, or GPIO |
| SPI2NENA/**SPI2NCS[1]** | D3 | | | | SPI2 chip select, or GPIO |
| **SPI2NENA**/SPI2NCS[1] | D3 | | | | SPI2 enable, or GPIO |
| **SPI2SIMO[0]** | D1 | | | | SPI2 slave-input master-output, or GPIO |
| **SPI2SOMI[0]** | D2 | | | | SPI2 slave-output master-input, or GPIO |
| | | | | | |
| N2HET1[0]/**SPI4CLK**/EPWM2B | K18 | I/O | Pull Down | Programmable, 20 µA | SPI4 clock, or GPIO |
| N2HET1[3]/**SPI4NCS[0]**/N2HET2[10]/EQEP2B | U1 | | | | SPI4 chip select, or GPIO |
| N2HET1[1]/**SPI4NENA**/N2HET2[8]/EQEP2A | V2 | | | | SPI4 enable, or GPIO |
| N2HET1[2]/**SPI4SIMO[0]**/EPWM3A | W5 | | | | SPI4 slave-input master-output, or GPIO |
| N2HET1[5]/**SPI4SOMI[0]**/N2HET2[12]/EPWM3B | V6 | | | | SPI4 slave-output master-input, or GPIO |

#### 4.3.2.12 Multibuffered Serial Peripheral Interface Modules (MibSPI)

**Table 4-31. ZWT Multibuffered Serial Peripheral Interface Modules (MibSPI)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| **MIBSPI1CLK** | F18 | I/O | Pull Up | Programmable, 20 µA | MibSPI1 clock, or GPIO |
| **MIBSPI1NCS[0]**/MIBSPI1SOMI[1]/ECAP6 | R2 | | | | MibSPI1 chip select, or GPIO |
| **MIBSPI1NCS[1]**/N2HET1[17]/EQEP1S | F3 | | | | |
| **MIBSPI1NCS[2]**/N2HET1[19] | G3 | | | | |
| **MIBSPI1NCS[3]**/N2HET1[21] | J3 | | | | |
| N2HET1[15]/**MIBSPI1NCS[4]**/ECAP1 | N1 | | Pull Down | Programmable, 20 µA | MibSPI1 chip select, or GPIO |
| N2HET1[24]/**MIBSPI1NCS[5]** | P1 | | | | |
| **MIBSPI1NENA**/N2HET1[23]/ECAP4 | G19 | | Pull Up | Programmable, 20 µA | MibSPI1 enable, or GPIO |
| **MIBSPI1SIMO[0]** | F19 | | | | MibSPI1 slave-in master-out, or GPIO |
| N2HET1[8]/**MIBSPI1SIMO[1]** | E18 | | Pull Down | Programmable, 20 µA | MibSPI1 slave-in master-out, or GPIO |
| **MIBSPI1SOMI[0]** | G18 | | Pull Up | Programmable, 20 µA | MibSPI1 slave-out master-in, or GPIO |
| MIBSPI1NCS[0]/**MIBSPI1SOMI[1]**/ECAP6 | R2 | | | | |
| **MIBSPI3CLK**/AWM1_EXT_SEL[1]/EQEP1A | V9 | I/O | Pull Up | Programmable, 20 µA | MibSPI3 clock, or GPIO |
| **MIBSPI3NCS[0]**/AD2EVT/GIOB[2]/ EQEP1I/N2HET2_PIN_nDIS | V10 | | | | MibSPI3 chip select, or GPIO |
| **MIBSPI3NCS[1]**/N2HET1[25]/MDCLK | V5 | | | | |
| **MIBSPI3NCS[2]**/I2C_SDA/N2HET1[27]/nTZ2 | B2 | | | | |
| **MIBSPI3NCS[3]**/I2C_SCL/N2HET1[29]/nTZ1 | C3 | | | | |
| N2HET1[11]/**MIBSPI3NCS[4]**/N2HET2[18]/EPWM1SYNCO | E3 | | Pull Down | Programmable, 20 µA | MibSPI3 chip select, or GPIO |
| MIBSPI3NENA/**MIBSPI3NCS[5]**/N2HET1[31]/EQEP1B | W9 | | Pull Up | Programmable, 20 µA | MibSPI3 chip select, or GPIO |
| **MIBSPI3NENA**/MIBSPI3NCS[5]/N2HET1[31]/EQEP1B | W9 | | | | MibSPI3 enable, or GPIO |
| **MIBSPI3SIMO[0]**/AWM1_EXT_SEL[0]/ECAP3 | W8 | | | | MibSPI3 slave-in master-out, or GPIO |
| **MIBSPI3SOMI[0]**/AWM1_EXT_ENA/ECAP2 | V8 | | | | MibSPI3 slave-out master-in, or GPIO |
| **MIBSPI5CLK** | H19 | I/O | Pull Up | Programmable, 20 µA | MibSPI5 clock, or GPIO |
| **MIBSPI5NCS[0]**/EPWM4A | E19 | | | | MibSPI5 chip select, or GPIO |
| **MIBSPI5NCS[1]** | B6 | | | | |
| **MIBSPI5NCS[2]** | W6 | | | | |
| **MIBSPI5NCS[3]** | T12 | | | | |
| **MIBSPI5NENA**/MIBSPI5SOMI[1]/ECAP5 | H18 | | | | MibSPI5 enable, or GPIO |
| **MIBSPI5SIMO[0]**/MIBSPI5SOMI[2] | J19 | | | | MibSPI5 slave-in master-out, or GPIO |
| **MIBSPI5SIMO[1]** | E16 | | | | |
| **MIBSPI5SIMO[2]** | H17 | | | | |
| **MIBSPI5SIMO[3]** | G17 | | | | |
| **MIBSPI5SOMI[0]** | J18 | | | | MibSPI5 slave-out master-in, or GPIO |
| **MIBSPI5SOMI[1]** | E17 | | | | |
| MIBSPI5NENA/**MIBSPI5SOMI[1]**/ECAP5 | H18 | | | | |
| **MIBSPI5SOMI[2]** | H16 | | | | |
| MIBSPI5SIMO[0]/**MIBSPI5SOMI[2]** | J19 | | | | |
| **MIBSPI5SOMI[3]** | G16 | | | | |

### 4.3.2.13 External Memory Interface (EMIF)

**Table 4-32. External Memory Interface (EMIF)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| **EMIF_CKE** | L3 | Output | Pull Up | None | EMIF Clock Enable |
| **EMIF_CLK** | K3 | I/O | | None | EMIF clock. This is an output signal in functional mode. It is gated off by default, so that the signal is pulled up. PINMUX29[8] must be cleared to enable this output. |
| **EMIF_nOE** | E12 | Output | Pull Up | None | EMIF Read Enable |
| **EMIF_nWAIT** | P3 | I/O | Pull Up | Fixed 20 µA Pull Up | EMIF Extended Wait Signal |
| **EMIF_nWE** | D17 | Output | Pull Up | None | EMIF Write Enable |
| **EMIF_nCAS** | R4 | Output | | | EMIF column address strobe |
| **EMIF_nRAS** | R3 | Output | | | EMIF row address strobe |
| **EMIF_nCS[0]**/N2HET2[7](1) | N17 | Output | | | EMIF chip select, synchronous |
| **EMIF_nCS[2]** | L17 | Output | | | EMIF chip selects, asynchronous<br>This applies to chip selects 2, 3 and 4 |
| **EMIF_nCS[3]**/N2HET2[9](1) | K17 | Output | | | |
| **EMIF_nCS[4]** | M17 | Output | | | |
| **EMIF_nDQM[0]** | E10 | Output | | | EMIF Data Mask or Write Strobe.<br>Data mask for SDRAM devices, write strobe for connected asynchronous devices. |
| **EMIF_nDQM[1]** | E11 | Output | | | |
| **EMIF_BA[0]** | E13 | Output | | | EMIF bank address or address line |
| **EMIF_BA[1]**/N2HET2[5](1) | D16 | Output | | | EMIF bank address or address line |
| **EMIF_ADDR[0]**/N2HET2[1](1) | D4 | Output | | | EMIF address |
| **EMIF_ADDR[1]**/N2HET2[3](1) | D5 | Output | | | |
| **EMIF_ADDR[2]** | E6 | Output | | | |
| **EMIF_ADDR[3]** | E7 | Output | | | |
| **EMIF_ADDR[4]** | E8 | Output | | | |
| **EMIF_ADDR[5]** | E9 | Output | | | |
| **EMIF_ADDR[6]**/N2HET2[11](1) | C4 | Output | | | |
| **EMIF_ADDR[7]**/N2HET2[13](1) | C5 | Output | | | |
| **EMIF_ADDR[8]**/N2HET2[15](1) | C6 | Output | | | |
| **EMIF_ADDR[9]** | C7 | Output | | | |
| **EMIF_ADDR[10]** | C8 | Output | | | |
| **EMIF_ADDR[11]** | C9 | Output | | | |
| **EMIF_ADDR[12]** | C10 | Output | | | |

(1) These signals are tri-stated and pulled up by default after power-up. Any application that requires the EMIF must set the bit 31 of the system module general-purpose register GPREG1.

**Table 4-32. External Memory Interface (EMIF) (continued)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| **EMIF_DATA[0]** | K15 | I/O | Pull Up | Fixed 20 µA Pull Up | EMIF Data |
| **EMIF_DATA[1]** | L15 | I/O | | | |
| **EMIF_DATA[2]** | M15 | I/O | | | |
| **EMIF_DATA[3]** | N15 | I/O | | | |
| **EMIF_DATA[4]** | E5 | I/O | | | |
| **EMIF_DATA[5]** | F5 | I/O | | | |
| **EMIF_DATA[6]** | G5 | I/O | | | |
| **EMIF_DATA[7]** | K5 | I/O | | | |
| **EMIF_DATA[8]** | L5 | I/O | | | |
| **EMIF_DATA[9]** | M5 | I/O | | | |
| **EMIF_DATA[10]** | N5 | I/O | | | |
| **EMIF_DATA[11]** | P5 | I/O | | | |
| **EMIF_DATA[12]** | R5 | I/O | | | |
| **EMIF_DATA[13]** | R6 | I/O | | | |
| **EMIF_DATA[14]** | R7 | I/O | | | |
| **EMIF_DATA[15]** | R8 | I/O | | | |

#### 4.3.2.14 System Module Interface

**Table 4-33. ZWT System Module Interface**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| **nPORRST** | W7 | Input | Pull Down | Fixed 100 µA Pull Down | Power-on reset, cold reset External power supply monitor circuitry must drive nPORRST low when any of the supplies to the microcontroller fall out of the specified range. This terminal has a glitch filter. See Section 6.8. |
| **nRST** | B17 | I/O | Pull Up | Fixed 100 µA Pull Up | System reset, warm reset, bidirectional. The internal circuitry indicates any reset condition by driving nRST low. The external circuitry can assert a system reset by driving nRST low. To ensure that an external reset is not arbitrarily generated, TI recommends that an external pull-up resistor is connected to this terminal. This terminal has a glitch filter. See Section 6.8. |
| **nERROR** | B14 | I/O | Pull Down | Fixed 20 µA Pull Down | ESM Error Signal Indicates error of high severity. See Section 6.18. |

#### 4.3.2.15 Clock Inputs and Outputs

**Table 4-34. ZWT Clock Inputs and Outputs**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| **OSCIN** | K1 | Input | N/A | None | From external crystal/resonator, or external clock input |
| **KELVIN_GND** | L2 | Input | | | Kelvin ground for oscillator |
| **OSCOUT** | L1 | Output | | | To external crystal/resonator |
| **ECLK** | A12 | I/O | Pull Down | Programmable, 20 µA | External prescaled clock output, or GIO. |
| GIOA[5]/**EXTCLKIN**/EPWM1A/N2HET1_PIN_nDIS | B5 | Input | Pull Down | 20 µA | External clock input #1 |
| **EXTCLKIN2** | R9 | Input | | | External clock input #2 |
| **VCCPLL** | P11 | 1.2V Power | N/A | None | Dedicated core supply for PLL's |

#### 4.3.2.16 Test and Debug Modules Interface

**Table 4-35. ZWT Test and Debug Modules Interface**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| **TEST** | U2 | Input | Pull Down | Fixed 100 µA Pull Down | Test enable. This terminal must be connected to ground directly or via a pull-down resistor. |
| **nTRST** | D18 | Input | | | JTAG test hardware reset |
| **RTCK** | A16 | Output | N/A | None | JTAG return test clock |
| **TCK** | B18 | Input | Pull Down | Fixed 100 µA Pull Down | JTAG test clock |
| **TDI** | A17 | Input | Pull Up | Fixed 100 µA Pull Up | JTAG test data in |
| **TDO** | C18 | Output | 100 µA Pull Down | None | JTAG test data out |
| **TMS** | C19 | Input | Pull Up | Fixed 100 µA Pull Up | JTAG test select |

#### 4.3.2.17 Flash Supply and Test Pads

**Table 4-36. ZWT Flash Supply and Test Pads**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| **VCCP** | F8 | 3.3V Power | N/A | None | Flash pump supply |
| **FLTP1** | J5 | - | N/A | None | Flash test pads. These terminals are reserved for TI use only. For proper operation these terminals must connect only to a test pad or not be connected at all [no connect (NC)]. |
| **FLTP2** | H5 | | | | |

#### 4.3.2.18 Reserved

**Table 4-37. Reserved**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| Reserved | A15 | - | N/A | None | Reserved. These balls are connected to internal logic but are not outputs nor do they have internal pulls. They are subject to ±1 µA leakage current. |
| Reserved | B15 | - | N/A | None | |
| Reserved | B16 | - | N/A | None | |
| Reserved | A8 | - | N/A- | None | |
| Reserved | B8 | - | N/A | None | |
| Reserved | B9 | - | N/A | None | |

### 4.3.2.19 No Connects

**Table 4-38. No Connects**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| NC | C11 | - | N/A | None | No Connects. These balls are not connected to any internal logic and can be connected to the PCB ground without affecting the functionality of the device. |
| NC | C12 | - | N/A | None | |
| NC | C13 | - | N/A | None | |
| NC | C14 | - | N/A | None | |
| NC | C15 | - | N/A | None | |
| NC | C16 | - | N/A | None | |
| NC | C17 | - | N/A | None | |
| NC | D6 | - | N/A | None | |
| NC | D7 | - | N/A | None | |
| NC | D8 | - | N/A | None | |
| NC | D9 | - | N/A | None | |
| NC | D10 | - | N/A | None | |
| NC | D11 | - | N/A | None | |
| NC | D12 | - | N/A | None | |
| NC | D13 | - | N/A | None | |
| NC | D14 | - | N/A | None | |
| NC | D15 | - | N/A | None | |
| NC | E4 | - | N/A | None | |
| NC | E14 | - | N/A | None | |
| NC | E15 | - | N/A | None | |
| NC | F4 | - | N/A | None | |
| NC | F15 | - | N/A | None | |
| NC | F16 | - | N/A | None | |
| NC | F17 | - | N/A | None | |
| NC | G4 | - | N/A | None | |
| NC | G15 | - | N/A | None | |
| NC | H15 | - | N/A | None | |
| NC | J15 | - | N/A | None | |
| NC | J16 | - | N/A | None | |
| NC | K4 | - | N/A | None | |
| NC | K16 | - | N/A | None | |
| NC | L4 | - | N/A | None | |
| NC | L16 | - | N/A | None | |
| NC | L18 | - | N/A | None | |
| NC | L19 | - | N/A | None | |
| NC | M4 | - | N/A | None | |
| NC | M16 | - | N/A | None | |
| NC | N4 | - | N/A | None | |
| NC | N16 | - | N/A | None | |
| NC | N18 | - | N/A | None | |
| NC | P4 | - | N/A | None | |

**Table 4-38. No Connects (continued)**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| NC | P15 | - | N/A | None | No Connects. These balls are not connected to any internal logic and can be connected to the PCB ground without affecting the functionality of the device. |
| NC | P16 | - | N/A | None | |
| NC | P17 | - | N/A | None | |
| NC | R1 | - | N/A | None | |
| NC | R10 | - | N/A | None | |
| NC | R11 | - | N/A | None | |
| NC | R12 | - | N/A | None | |
| NC | R13 | - | N/A | None | |
| NC | R14 | - | N/A | None | |
| NC | R15 | - | N/A | None | |
| NC | T2 | - | N/A | None | |
| NC | T3 | - | N/A | None | |
| NC | T4 | - | N/A | None | |
| NC | T5 | - | N/A | None | |
| NC | T6 | - | N/A | None | |
| NC | T7 | - | N/A | None | |
| NC | T8 | - | N/A | None | |
| NC | T9 | - | N/A | None | |
| NC | T10 | - | N/A | None | |
| NC | T11 | - | N/A | None | |
| NC | T13 | - | N/A | None | |
| NC | T14 | - | N/A | None | |
| NC | U3 | - | N/A- | None | |
| NC | U4 | - | N/A | None | |
| NC | U5 | - | N/A | None | |
| NC | U6 | - | N/A | None | |
| NC | U7 | - | N/A | None | |
| NC | U8 | - | N/A | None | |
| NC | U9 | - | N/A | None | |
| NC | U10 | - | N/A | None | |
| NC | U11 | - | N/A | None | |
| NC | U12 | - | N/A | None | |
| NC | V3 | - | N/A | None | |
| NC | V4 | - | N/A | None | |
| NC | V11 | - | N/A | None | |
| NC | V12 | - | N/A | None | |
| NC | W4 | - | N/A | None | |
| NC | W11 | - | N/A | None | |
| NC | W12 | - | N/A | None | |
| NC | W13 | - | N/A | None | |

#### 4.3.2.20 Supply for Core Logic: 1.2V nominal

**Table 4-39. ZWT Supply for Core Logic: 1.2V nominal**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| **VCC** | F9 | 1.2V Power | N/A | None | Core supply |
| **VCC** | F10 | | | | |
| **VCC** | H10 | | | | |
| **VCC** | J14 | | | | |
| **VCC** | K6 | | | | |
| **VCC** | K8 | | | | |
| **VCC** | K12 | | | | |
| **VCC** | K14 | | | | |
| **VCC** | L6 | | | | |
| **VCC** | M10 | | | | |
| **VCC** | P10 | | | | |

#### 4.3.2.21 Supply for I/O Cells: 3.3V nominal

**Table 4-40. ZWT Supply for I/O Cells: 3.3V nominal**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| **VCCIO** | F6 | 3.3V Power | N/A | None | Operating supply for I/Os |
| **VCCIO** | F7 | | | | |
| **VCCIO** | F11 | | | | |
| **VCCIO** | F12 | | | | |
| **VCCIO** | F13 | | | | |
| **VCCIO** | F14 | | | | |
| **VCCIO** | G6 | | | | |
| **VCCIO** | G14 | | | | |
| **VCCIO** | H6 | | | | |
| **VCCIO** | H14 | | | | |
| **VCCIO** | J6 | | | | |
| **VCCIO** | L14 | | | | |
| **VCCIO** | M6 | | | | |
| **VCCIO** | M14 | | | | |
| **VCCIO** | N6 | | | | |
| **VCCIO** | N14 | | | | |
| **VCCIO** | P6 | | | | |
| **VCCIO** | P7 | | | | |
| **VCCIO** | P8 | | | | |
| **VCCIO** | P9 | | | | |
| **VCCIO** | P12 | | | | |
| **VCCIO** | P13 | | | | |
| **VCCIO** | P14 | | | | |

#### 4.3.2.22 Ground Reference for All Supplies Except VCCAD

**Table 4-41. ZWT Ground Reference for All Supplies Except VCCAD**

| Terminal | | Signal Type | Reset Pull State | Pull Type | Description |
|---|---|---|---|---|---|
| Signal Name | 337 ZWT | | | | |
| **VSS** | A1 | Ground | N/A | None | Ground reference |
| **VSS** | A2 | | | | |
| **VSS** | A18 | | | | |
| **VSS** | A19 | | | | |
| **VSS** | B1 | | | | |
| **VSS** | B19 | | | | |
| **VSS** | H8 | | | | |
| **VSS** | H9 | | | | |
| **VSS** | H11 | | | | |
| **VSS** | H12 | | | | |
| **VSS** | J8 | | | | |
| **VSS** | J9 | | | | |
| **VSS** | J10 | | | | |
| **VSS** | J11 | | | | |
| **VSS** | J12 | | | | |
| **VSS** | K9 | | | | |
| **VSS** | K10 | | | | |
| **VSS** | K11 | | | | |
| **VSS** | L8 | | | | |
| **VSS** | L9 | | | | |
| **VSS** | L10 | | | | |
| **VSS** | L11 | | | | |
| **VSS** | L12 | | | | |
| **VSS** | M8 | | | | |
| **VSS** | M9 | | | | |
| **VSS** | M11 | | | | |
| **VSS** | M12 | | | | |
| **VSS** | V1 | | | | |
| **VSS** | W1 | | | | |
| **VSS** | W2 | | | | |

# 5 Specifications

## 5.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage range: | $V_{CC}$ (2) | -0.3 | 1.43 | V |
| | $V_{CCIO}$, $V_{CCP}$ (2) | -0.3 | 4.6 | V |
| | $V_{CCAD}$ | -0.3 | 6.25 | V |
| Input voltage range: | All input pins, with exception of ADC pins | -0.3 | 4.6 | V |
| | ADC input pins | -0.3 | 6.25 | V |
| Input clamp current: | $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CCIO}$) All pins, except AD1IN[23:0] or AD2IN[15:0] | -20 | +20 | mA |
| | $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CCAD}$) AD1IN[23:0] or AD2IN[15:0] | -10 | +10 | mA |
| | Total | -40 | +40 | mA |
| Operating free-air temperature range, $T_A$: | | -40 | 125 | °C |
| Operating junction temperature range, $T_J$: | | -40 | 150 | °C |
| Storage temperature range, $T_{stg}$ | | -65 | 150 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to their associated grounds.

## 5.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{ESD}$ | Electrostatic discharge (ESD) performance: | Human body model (HBM), per AEC Q100-002 (1) | | ±2 | kV |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | V |
| | | | Corner pins on 144-pin PGE (1, 36, 37, 72, 73, 108, 109, 144) | ±750 | V |
| | | | Corner balls on 337-ball ZWT (A1, A19, W1, W19) | ±750 | V |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Power-On Hours (POH) (1) (2)

| NOMINAL CORE VOLTAGE ($V_{CC}$) | JUNCTION TEMPERATURE (Tj) | LIFETIME POH |
|---|---|---|
| 1.2 | 105ºC | 100K |

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) To avoid significant degradation, the device power-on hours (POH) must be limited to those specified in this table. To convert to equivalent POH for a specific temperature profile, see the *Calculating Equivalent Power-on-Hours for Hercules Safety MCUs* Application Report (SPNA207).

## 5.4 Device Recommended Operating Conditions(1)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Digital logic supply voltage (Core) | 1.14 | 1.2 | 1.32 | V |
| $V_{CCPLL}$ | PLL Supply Voltage | 1.14 | 1.2 | 1.32 | V |
| $V_{CCIO}$ | Digital logic supply voltage (I/O) | 3 | 3.3 | 3.6 | V |
| $V_{CCAD}$ | MibADC supply voltage | 3 | | 5.25 | V |
| $V_{CCP}$ | Flash pump supply voltage | 3 | 3.3 | 3.6 | V |
| $V_{SS}$ | Digital logic supply ground | | 0 | | V |
| $V_{SSAD}$ | MibADC supply ground | -0.1 | | 0.1 | V |
| $V_{ADREFHI}$ | A-to-D high-voltage reference source | $V_{SSAD}$ | | $V_{CCAD}$ | V |
| $V_{ADREFLO}$ | A-to-D low-voltage reference source | $V_{SSAD}$ | | $V_{CCAD}$ | V |
| $V_{SLEW}$ | Maximum positive slew rate for $V_{CCIO}$, $V_{CCAD}$ and $V_{CCP}$ supplies | | | 1 | V/µs |
| $T_A$ | Operating free-air temperature | -40 | | 125 | °C |
| $T_J$ | Operating junction temperature(2) | -40 | | 150 | °C |

(1) All voltages are with respect to $V_{SS}$, except $V_{CCAD}$, which is with respect to $V_{SSAD}$
(2) Reliability data is based upon a temperature profile that is equivalent to 100,000 power-on hours at 105°C junction temperature.

## 5.5 Switching Characteristics Over Recommended Operating Conditions for Clock Domains

**Table 5-1. Clock Domain Timing Specifications**

| PARAMETER | DESCRIPTION | CONDITIONS | | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{HCLK}$ | HCLK - System clock frequency | PGE | Pipeline mode enabled | 160 | MHz |
| | | | Pipeline mode disabled | 50 | MHz |
| | | ZWT | Pipeline mode enabled | 180 | MHz |
| | | | Pipeline mode disabled | 50 | MHz |
| $f_{GCLK}$ | GCLK - CPU clock frequency | | | $f_{HCLK}$ | MHz |
| $f_{VCLK}$ | VCLK - Primary peripheral clock frequency | | | 100 | MHz |
| $f_{VCLK2}$ | VCLK2 - Secondary peripheral clock frequency | | | 100 | MHz |
| $f_{VCLK3}$ | VCLK3 - Secondary peripheral clock frequency | | | 100 | MHz |
| $f_{VCLK4}$ | VCLK4 - Secondary peripheral clock frequency | | | 150 | MHz |
| $f_{VCLKA1}$ | VCLKA1 - Primary asynchronous peripheral clock frequency | | | 100 | MHz |
| $f_{VCLKA2}$ | VCLKA2 - Secondary asynchronous peripheral clock frequency | | | 100 | MHz |
| $f_{VCLKA3}$ | VCLKA3 - Primary asynchronous peripheral clock frequency | | | 100 | MHz |
| $f_{VCLKA4}$ | VCLKA4 - Secondary asynchronous peripheral clock frequency | | | 100 | MHz |
| $f_{RTICLK}$ | RTICLK - clock frequency | | | $f_{VCLK}$ | MHz |

## 5.6 Wait States Required

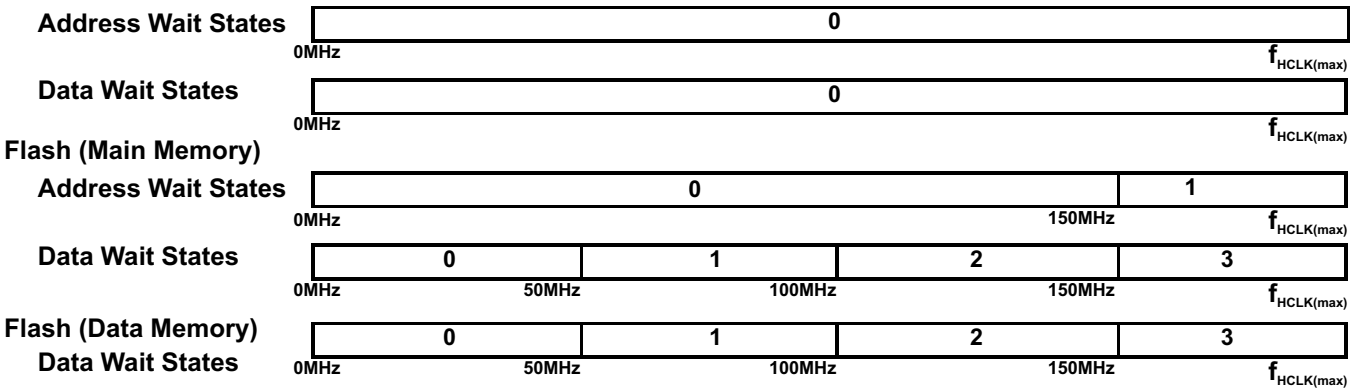



**Figure 5-1. Wait States Scheme**

As shown in the figure above, the TCM RAM can support program and data fetches at full CPU speed without any address or data wait states required.

The TCM flash can support zero address and data wait states up to a CPU speed of 50 MHz in nonpipelined mode. The flash supports a maximum CPU clock speed of 160 MHz in pipelined mode for the PGE Package and 180 MHz for the ZWT package, with one address wait state and three data wait states.

The flash wrapper defaults to non-pipelined mode with zero address wait state and one random-read data wait state.

## 5.7 Power Consumption Over Recommended Operating Conditions

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CC}$ | $V_{CC}$ digital supply current (operating mode) $f_{VCLK} = f_{HCLK}/2$; Flash in pipelined mode; $V_{CCmax}$ | $f_{HCLK}$ = 160MHz | | 170 (1) | 350 (2) | mA |
| | | $f_{HCLK}$ = 180MHz | | 190(1) | 370(2) | |
| | $V_{CC}$ Digital supply current (LBIST/PBIST mode) | LBIST/PBIST clock frequency = 80MHz | | 215(1) | 470(3)(4) | mA |
| | | LBIST/PBIST clock frequency = 90MHz | | 240(1) | 470 (3)(4) | mA |
| $I_{CCPLL}$ | $V_{CCPLL}$ digital supply current (operating mode) | $V_{CCPLL} = V_{CCPLLmax}$ | | | 10 | mA |
| $I_{CCIO}$ | $V_{CCIO}$ Digital supply current (operating mode. | No DC load, $V_{CCmax}$ | | | 10 | mA |
| $I_{CCAD}$ | $V_{CCAD}$ supply current (operating mode) | Single ADC operational, $V_{CCADmax}$ | | | 15 | mA |
| | | Both ADCs operational, $V_{CCADmax}$ | | | 30 | |
| $I_{ADREFHI}$ | $AD_{REFHI}$ supply current (operating mode) | Single ADC operational, $AD_{REFHImax}$ | | | 3 | mA |
| | | Both ADCs operational, $AD_{REFHImax}$ | | | 6 | |
| $I_{CCP}$ | $V_{CCP}$ supply current | read from 1 bank and program another bank, $V_{CCPmax}$ | | | 55 | mA |

(1) The typical value is the average current for the nominal process corner and junction temperature of 25C.
(2) The maximum $I_{CC,}$ value can be derated
- linearly with voltage
- by 1 ma/MHz for lower operating frequency when $f_{HCLK} = 2 * f_{VCLK}$
- for lower junction temperature by the equation below where $T_{JK}$ is the junction temperature in Kelvin and the result is in milliamperes. **$170 - 0.068\ e^{0.0185\ T_{JK}}$**

(3) The maximum $I_{CC,}$ value can be derated
- linearly with voltage
- by 1.5 ma/MHz for lower operating frequency
- for lower junction temperature by the equation below where $T_{JK}$ is the junction temperature in Kelvin and the result is in milliamperes. **$170 - 0.068\ e^{0.0185\ T_{JK}}$**

(4) LBIST and PBIST currents are for a short duration, typically less than 10ms. They are usually ignored for thermal calculations for the device and the voltage regulator

## 5.8 Input/Output Electrical Characteristics Over Recommended Operating Conditions(1)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{hys}$ | Input hysteresis | All inputs | | 180 | | | mV |
| $V_{IL}$ | Low-level input voltage | All inputs | | -0.3 | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | All inputs | | 2 | | $V_{CCIO}$ + 0.3 | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL} = I_{OLmax}$ | | | 0.2 $V_{CCIO}$ | V |
| | | | $I_{OL}$ = 50 µA, standard output mode | | | 0.2 | |
| | | | $I_{OL}$ = 50 µA, low-EMI output mode (see Section 5.13) | | | 0.2 $V_{CCIO}$ | |
| $V_{OH}$ | High-level output voltage | | $I_{OH} = I_{OHmax}$ | 0.8 $V_{CCIO}$ | | | V |
| | | | $I_{OH}$ = 50 µA, standard output mode | $V_{CCIO}$ -0.3 | | | |
| | | | $I_{OH}$ = 50 µA, low-EMI output mode (see Section 5.13) | 0.8 $V_{CCIO}$ | | | |
| $I_{IK}$ | Input clamp current (I/O pins)(2) | | $V_I < V_{SSIO}$ - 0.3 or $V_I > V_{CCIO}$ + 0.3 | -3.5 | | 3.5 | mA |
| $I_I$ | Input current (I/O pins) | $I_{IH}$ Pulldown 20µA | $V_I = V_{CCIO}$ | 5 | | 40 | µA |
| | | $I_{IH}$ Pulldown 100µA | $V_I = V_{CCIO}$ | 40 | | 195 | |
| | | $I_{IL}$ Pullup 20µA | $V_I = V_{SS}$ | -40 | | -5 | |
| | | $I_{IL}$ Pullup 100µA | $V_I = V_{SS}$ | -195 | | -40 | |
| | | All other pins | No pullup or pulldown | -1 | | 1 | |
| $C_I$ | Input capacitance | | | | 2 | | pF |
| $C_O$ | Output capacitance | | | | 3 | | pF |

(1) Source currents (out of the device) are negative while sink currents (into the device) are positive.
(2) If the input voltage extends outside of the range $V_{IL}$ to $V_{IH}$ then the input current must be limited to $I_{IK}$ to maintain proper operation. See the application note SPNA201 for more information on limiting input clamp currents.

## 5.9 Thermal Resistance Characteristics

Table 5-2 shows the thermal resistance characteristics for the QFP - PGE mechanical package.

Table 5-3 shows the thermal resistance characteristics for the BGA - ZWT mechanical package.

**Table 5-2. Thermal Resistance Characteristics (PGE Package)**

| | | °C/W |
|---|---|---|
| $R\Theta_{JA}$ | Junction-to-free air thermal resistance, Still air using JEDEC 2S2P test board | 40 |
| $R\Theta_{JB}$ | Junction-to-board thermal resistance | 27.2 |
| $R\Theta_{JC}$ | Junction-to-case thermal resistance | 7.3 |
| $\Psi_{JT}$ | Junction-to-package top, Still air | 0.10 |

**Table 5-3. Thermal Resistance Characteristics (ZWT Package)**

| | | °C/W |
|---|---|---|
| $R\Theta_{JA}$ | Junction-to-free air thermal resistance, Still air (includes 5x5 thermal via cluster in 2s2p PCB connected to 1st ground plane) | 18.8 |
| $R\Theta_{JB}$ | Junction-to-board thermal resistance | 14.1 |
| $R\Theta_{JC}$ | Junction-to-case thermal resistance | 7.1 |

**Table 5-3. Thermal Resistance Characteristics (ZWT Package) (continued)**

| | | °C/W |
|---|---|---|
| $\Psi_{JT}$ | Junction-to-package top, Still air (includes 5x5 thermal via cluster in 2s2p PCB connected to 1st ground plane) | 0.33 |

## 5.10 Output Buffer Drive Strengths

**Table 5-4. Output Buffer Drive Strengths**

| LOW-LEVEL OUTPUT CURRENT, $I_{OL}$ for $V_I=V_{OLmax}$ or HIGH-LEVEL OUTPUT CURRENT, $I_{OH}$ for $V_I=V_{OHmin}$ | SIGNALS |
|---|---|
| 8 mA | MIBSPI5CLK, MIBSPI5SOMI[0], MIBSPI5SOMI[1], MIBSPI5SOMI[2], MIBSPI5SOMI[3], MIBSPI5SIMO[0], MIBSPI5SIMO[1], MIBSPI5SIMO[2], MIBSPI5SIMO[3],<br>TMS, TDI, TDO, RTCK,<br>SPI4CLK, SPI4SIMO, SPI4SOMI, nERROR,<br>N2HET2[1], N2HET2[3], N2HET2[5], N2HET2[7], N2HET2[9], N2HET2[11], N2HET2[13], N2HET2[15]<br>ECAP1, ECAP4, ECAP5, ECAP6<br>EQEP1I, EQEP1S, EQEP2I, EQEP2S<br>EPWM1A, EPWM1B, EPWM1SYNCO, ETPW2A, EPWM2B, EPWM3A, EPWM3B, EPWM4A, EPWM4B, EPWM5A, EPWM5B, EPWM6A, EPWM6B, EPWM7A, EPWM7B<br>EMIF_ADDR[0:12], EMIF_BA[0:1], EMIF_CKE, EMIF_CLK, EMIF_DATA[0:15], EMIF_nCAS, EMIF_nCS[0:4], EMIF_nDQM[0:1], EMIF_nOE, EMIF_nRAS, EMIF_nWAIT, EMIF_nWE, EMIF_RNW |
| 4 mA | TEST,<br>MIBSPI3SOMI, MIBSPI3SIMO, MIBSPI3CLK, MIBSPI1SIMO, MIBSPI1SOMI, MIBSPI1CLK,<br>ECAP2, ECAP3<br>nRST |
| 2 mA zero-dominant | AD1EVT,<br>CAN1RX, CAN1TX, CAN2RX, CAN2TX, CAN3RX, CAN3TX,<br>GIOA[0-7], GIOB[0-7],<br>LINRX, LINTX,<br>MIBSPI1nCS[0], MIBSPI1nCS[1-3], MIBSPI1nENA, MIBSPI3nCS[0-3], MIBSPI3nENA, MIBSPI5nCS[0-3], MIBSPI5nENA,<br>N2HET1[0-31], N2HET2[0], N2HET2[2], N2HET2[4], N2HET2[5], N2HET2[6], N2HET2[7], N2HET2[8], N2HET2[9], N2HET2[10], N2HET2[11], N2HET2[12], N2HET2[13], N2HET2[14], N2HET2[15], N2HET2[16], N2HET2[18],<br>SPI2nCS[0], SPI2nENA, SPI4nCS[0], SPI4nENA |
| selectable 8 mA / 2 mA | ECLK,<br>SPI2CLK, SPI2SIMO, SPI2SOMI<br>The default output buffer drive strength is 8 mA for these signals. |

**Table 5-5. Selectable 8 mA/2 mA Control**

| Signal | Control Bit | Address | 8 mA | 2 mA |
|---|---|---|---|---|
| ECLK | SYSPC10[0] | 0xFFFF FF78 | 0 | 1 |
| SPI2CLK | SPI2PC9[9] | 0xFFF7 F668 | 0 | 1 |
| SPI2SIMO | SPI2PC9[10] | 0xFFF7 F668 | 0 | 1 |

**Table 5-5. Selectable 8 mA/2 mA Control (continued)**

| Signal | Control Bit | Address | 8 mA | 2 mA |
|---|---|---|---|---|
| SPI2SOMI | SPI2PC9[11] (1) | 0xFFF7 F668 | 0 | 1 |

(1) Either SPI2PC9[11] or SPI2PC9[24] can change the output strength of the SPI2SOMI pin. In case of a 32-bit write where these two bits differ, SPI2PC9[11] determines the drive strength.

## 5.11 Input Timings

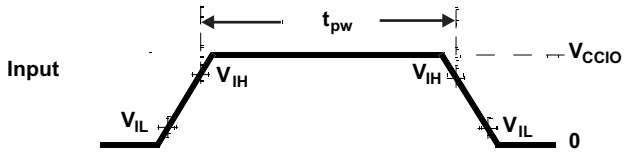



**Figure 5-2. TTL-Level Inputs**

**Table 5-6. Timing Requirements for Inputs (1)**

| Parameter | | MIN | MAX | Unit |
|---|---|---|---|---|
| $t_{pw}$ | Input minimum pulse width | $t_{c(VCLK)}$ + 10 (2) | | ns |
| $t_{in\_slew}$ | Time for input signal to go from $V_{IL}$ to $V_{IH}$ or from $V_{IH}$ to $V_{IL}$ | | 1 | ns |

(1) $t_{c(VCLK)}$ = peripheral VBUS clock cycle time = 1 / $f_{(VCLK)}$
(2) The timing shown above is only valid for pin used in general-purpose input mode.

## 5.12 Output Timings

**Table 5-7. Switching Characteristics for Output Timings versus Load Capacitance ©$_L$)**

| Parameter | | | MIN | MAX | Unit |
|---|---|---|---|---|---|
| Rise time, $t_r$ | 8 mA low EMI pins (see Table 5-4) | CL = 15 pF | | 2.5 | ns |
| | | CL = 50 pF | | 4 | |
| | | CL = 100 pF | | 7.2 | |
| | | CL = 150 pF | | 12.5 | |
| Fall time, $t_f$ | | CL = 15 pF | | 2.5 | ns |
| | | CL = 50 pF | | 4 | |
| | | CL = 100 pF | | 7.2 | |
| | | CL = 150 pF | | 12.5 | |
| Rise time, $t_r$ | 4 mA low EMI pins (see Table 5-4) | CL = 15 pF | | 5.6 | ns |
| | | CL = 50 pF | | 10.4 | |
| | | CL = 100 pF | | 16.8 | |
| | | CL = 150 pF | | 23.2 | |
| Fall time, $t_f$ | | CL = 15 pF | | 5.6 | ns |
| | | CL= 50 pF | | 10.4 | |
| | | CL = 100 pF | | 16.8 | |
| | | CL = 150 pF | | 23.2 | |

**Table 5-7. Switching Characteristics for Output Timings versus Load Capacitance ($C_L$) (continued)**

| Parameter | | | | MIN | MAX | Unit |
|---|---|---|---|---|---|---|
| Rise time, $t_r$ | 2 mA-z low EMI pins (see Table 5-4) | | CL = 15 pF | | 8 | ns |
| | | | CL = 50 pF | | 15 | |
| | | | CL = 100 pF | | 23 | |
| | | | CL = 150 pF | | 33 | |
| Fall time, $t_f$ | | | CL = 15 pF | | 8 | ns |
| | | | CL = 50 pF | | 15 | |
| | | | CL = 100 pF | | 23 | |
| | | | CL = 150 pF | | 33 | |
| Rise time, $t_r$ | Selectable 8 mA / 2 mA-z pins (see Table 5-4) | 8 mA mode | CL = 15 pF | | 2.5 | ns |
| | | | CL = 50 pF | | 4 | |
| | | | CL = 100 pF | | 7.2 | |
| | | | CL = 150 pF | | 12.5 | |
| Fall time, $t_f$ | | | CL = 15 pF | | 2.5 | ns |
| | | | CL = 50 pF | | 4 | |
| | | | CL = 100 pF | | 7.2 | |
| | | | CL = 150 pF | | 12.5 | |
| Rise time, $t_r$ | | 2 mA-z mode | CL = 15 pF | | 8 | ns |
| | | | CL = 50 pF | | 15 | |
| | | | CL = 100 pF | | 23 | |
| | | | CL = 150 pF | | 33 | |
| Fall time, $t_f$ | | | CL = 15 pF | | 8 | ns |
| | | | CL = 50 pF | | 15 | |
| | | | CL = 100 pF | | 23 | |
| | | | CL = 150 pF | | 33 | |

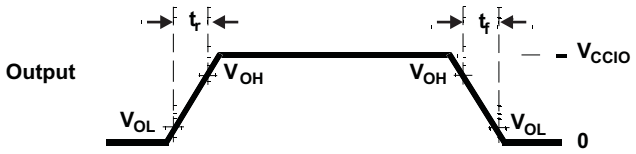



**Figure 5-3. CMOS-Level Outputs**

**Table 5-8. Timing Requirements for Outputs (1)**

| Parameter | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{d(parallel\_out)}$ | Delay between low to high, or high to low transition of general-purpose output signals that can be configured by an application in parallel, e.g. all signals in a GIOA port, or all N2HET1 signals, etc. | | 6 | ns |

(1) This specification does not account for any output buffer drive strength differences or any external capacitive loading differences. Check Table 5-4 for output buffer drive strength information on each signal.

## 5.13 Low-EMI Output Buffers

The low-EMI output buffer has been designed explicitly to address the issue of decoupling sources of emissions from the pins which they drive. This is accomplished by adaptively controlling the impedance of the output buffer, and is particularly effective with capacitive loads.

This is not the default mode of operation of the low-EMI output buffers and must be enabled by setting the system module GPCR1 register for the desired module or signal, as shown in . The adaptive impedance control circuit monitors the DC bias point of the output signal. The buffer internally generates two reference levels, VREFLOW and VREFHIGH, which are set to approximately 10% and 90% of $V_{CCIO}$, respectively.

Once the output buffer has driven the output to a low level, if the output voltage is below VREFLOW, then the output buffer's impedance will increase to hi-Z. A high degree of decoupling between the internal ground bus and the output pin will occur with capacitive loads, or any load in which no current is flowing, e.g. the buffer is driving low on a resistive path to ground. Current loads on the buffer which attempt to pull the output voltage above VREFLOW will be opposed by the buffer's output impedance so as to maintain the output voltage at or below VREFLOW.

Conversely, once the output buffer has driven the output to a high level, if the output voltage is above VREFHIGH then the output buffer's impedance will again increase to hi-Z. A high degree of decoupling between internal power bus ad output pin will occur with capacitive loads or any loads in which no current is flowing, e.g. buffer is driving high on a resistive path to VCCIO. Current loads on the buffer which attempt to pull the output voltage below VREFHIGH will be opposed by the buffer's output impedance so as to maintain the output voltage at or above VREFHIGH.

The bandwidth of the control circuitry is relatively low, so that the output buffer in adaptive impedance control mode cannot respond to high-frequency noise coupling into the buffer's power buses. In this manner, internal bus noise approaching 20% peak-to-peak of VCCIO can be rejected.

Unlike standard output buffers which clamp to the rails, an output buffer in impedance control mode will allow a positive current load to pull the output voltage up to VCCIO + 0.6V without opposition. Also, a negative current load will pull the output voltage down to VSSIO – 0.6V without opposition. This is not an issue since the actual clamp current capability is always greater than the IOH / IOL specifications.

The low-EMI output buffers are automatically configured to be in the standard buffer mode when the device enters a low-power mode.

**Table 5-9. Low-EMI Output Buffer Hookup**

| Module or Signal Name | Control Register to Enable Low-EMI Mode |
|---|---|
| Module: MibSPI1 | GPREG1.0 |
| Module: SPI2 | GPREG1.1 |
| Module: MibSPI3 | GPREG1.2 |
| Reserved | GPREG1.3 |
| Module: MibSPI5 | GPREG1.4 |
| Reserved | GPREG1.5 |
| Module: EMIF | GPREG1.6 |
| Reserved | GPREG1.7 |
| Signal: TMS | GPREG1.8 |
| Signal: TDI | GPREG1.9 |
| Signal: TDO | GPREG1.10 |
| Signal: RTCK | GPREG1.11 |
| Signal: TEST | GPREG1.12 |
| Signal: nERROR | GPREG1.13 |
| Signal: AD1EVT | GPREG1.14 |

# 6 System Information and Electrical Specifications

## 6.1 Device Power Domains

The device core logic is split up into multiple power domains to optimize the Self-Test Clock Configuration power for a given application use case. There are 7 power domains in total: PD1, PD2, PD3, PD5, RAM_PD1, and RAM_PD2. Refer to Section 1.4 for more information.

PD1 is an "always-ON" power domain, which cannot be turned off. Each of the other power domains can be turned OFF one time during device initialization as per the application requirement. Refer to the Power Management Module (PMM) chapter of TMS570LS12x/11x Technical Reference Manual (SPNU515) for more details.

**NOTE**

The clocks to a module must be turned off before powering down the core domain that contains the module.

**NOTE**

The logic in the modules that are powered down loses its power completely. Any access to modules that are powered down results in an abort being generated. When power is restored, the modules power-up to their default states (after normal power-up). No register or memory contents are preserved in the core domains that are turned off.

## 6.2 Voltage Monitor Characteristics

A voltage monitor is implemented on this device. The purpose of this voltage monitor is to eliminate the requirement for a specific sequence when powering up the core and I/O voltage supplies.

### *6.2.1 Important Considerations*

- The voltage monitor does not eliminate the need of a voltage supervisor circuit to ensure that the device is held in reset when the voltage supplies are out of range.
- The voltage monitor only monitors the core supply (VCC) and the I/O supply (VCCIO). The other supplies are not monitored by the VMON. For example, if the VCCAD or VCCP are supplied from a source different from that for VCCIO, then there is no internal voltage monitor for the VCCAD and VCCP supplies.

### *6.2.2 Voltage Monitor Operation*

The voltage monitor generates the Power Good MCU signal (PGMCU) as well as the I/Os Power Good IO signal (PGIO) on the device. During power-up or power-down, the PGMCU and PGIO are driven low when the core or I/O supplies are lower than the specified minimum monitoring thresholds. The PGIO and PGMCU being low isolates the core logic as well as the I/O controls during the power-up or power-down of the supplies. This allows the core and I/O supplies to be powered up or down in any order.

When the voltage monitor detects a low voltage on the I/O supply, it will assert a power-on reset. When the voltage monitor detects an out-of-range voltage on the core supply, it asynchronously makes all output pins high impedance, and asserts a power-on reset. The voltage monitor is disabled when the device enters a low power mode.

The VMON also incorporates a glitch filter for the nPORRST input. Refer to Section 6.3.3.1 for the timing information on this glitch filter.

**Table 6-1. Voltage Monitoring Specifications**

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{MON}$ | Voltage monitoring thresholds | VCC low - VCC level below this threshold is detected as too low. | 0.75 | 0.9 | 1.13 | V |
| | | VCC high - VCC level above this threshold is detected as too high. | 1.40 | 1.7 | 2.1 | |
| | | VCCIO low - VCCIO level below this threshold is detected as too low. | 1.85 | 2.4 | 2.9 | |

### 6.2.3 Supply Filtering

The VMON has the capability to filter glitches on the VCC and VCCIO supplies.

The following table shows the characteristics of the supply filtering. Glitches in the supply larger than the maximum specification cannot be filtered.

**Table 6-2. VMON Supply Glitch Filtering Capability**

| Parameter | MIN | MAX |
|---|---|---|
| Width of glitch on VCC that can be filtered | 250 ns | 1 µs |
| Width of glitch on VCCIO that can be filtered | 250 ns | 1 µs |

## 6.3 Power Sequencing and Power On Reset

### 6.3.1 Power-Up Sequence

There is no timing dependency between the ramp of the VCCIO and the VCC supply voltage. The power-up sequence starts with the I/O voltage rising above the minimum I/O supply threshold, (see Table 6-4 for more details), core voltage rising above the minimum core supply threshold and the release of power-on reset. The high frequency oscillator will start up first and its amplitude will grow to an acceptable level. The oscillator start up time is dependent on the type of oscillator and is provided by the oscillator vendor. The different supplies to the device can be powered up in any order.

The device goes through the following sequential phases during power up.

**Table 6-3. Power-Up Phases**

| | |
|---|---|
| Oscillator start-up and validity check | 1032 oscillator cycles |
| eFuse autoload | 1160 oscillator cycles |
| Flash pump power-up | 688 oscillator cycles |
| Flash bank power-up | 617 oscillator cycles |
| **Total** | **3497 oscillator cycles** |

The CPU reset is released at the end of the above sequence and fetches the first instruction from address 0x00000000.

### 6.3.2 Power-Down Sequence

The different supplies to the device can be powered down in any order.

### 6.3.3 Power-On Reset: nPORRST

This is the power-on reset. This reset must be asserted by an external circuitry whenever the I/O or core supplies are outside the specified recommended range. This signal has a glitch filter on it. It also has an internal pulldown.

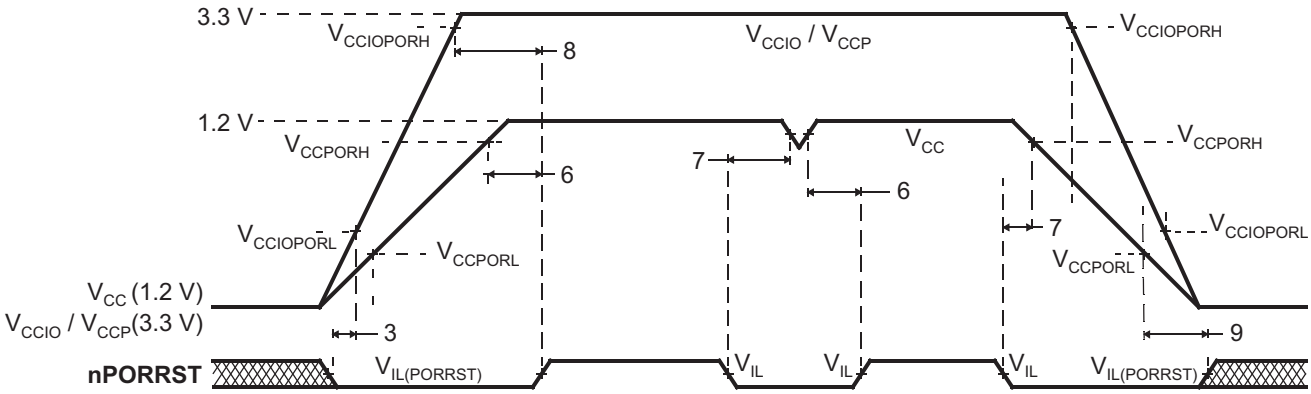
#### 6.3.3.1 nPORRST Electrical and Timing Requirements

**Table 6-4. Electrical Requirements for nPORRST**

| NO | Parameter | | MIN | MAX | Unit |
|---|---|---|---|---|---|
| | $V_{CCPORL}$ | $V_{CC}$ low supply level when nPORRST must be active during power-up | | 0.5 | V |
| | $V_{CCPORH}$ | $V_{CC}$ high supply level when nPORRST must remain active during power-up and become active during power down | 1.14 | | V |
| | $V_{CCIOPORL}$ | $V_{CCIO}$ / $V_{CCP}$ low supply level when nPORRST must be active during power-up | | 1.1 | V |
| | $V_{CCIOPORH}$ | $V_{CCIO}$ / $V_{CCP}$ high supply level when nPORRST must remain active during power-up and become active during power down | 3.0 | | V |
| | $V_{IL(PORRST)}$ | Low-level input voltage of nPORRST $V_{CCIO}$ > 2.5V | | 0.2 * $V_{CCIO}$ | V |
| | | Low-level input voltage of nPORRST $V_{CCIO}$ < 2.5V | | 0.5 | V |
| 3 | $t_{su(PORRST)}$ | Setup time, nPORRST active before $V_{CCIO}$ and $V_{CCP}$ > $V_{CCIOPORL}$ during power-up | 0 | | ms |
| 6 | $t_{h(PORRST)}$ | Hold time, nPORRST active after $V_{CC}$ > $V_{CCPORH}$ | 1 | | ms |
| 7 | $t_{su(PORRST)}$ | Setup time, nPORRST active before $V_{CC}$ < $V_{CCPORH}$ during power down | 2 | | µs |
| 8 | $t_{h(PORRST)}$ | Hold time, nPORRST active after $V_{CCIO}$ and $V_{CCP}$ > $V_{CCIOPORH}$ | 1 | | ms |
| 9 | $t_{h(PORRST)}$ | Hold time, nPORRST active after $V_{CC}$ < $V_{CCPORL}$ | 0 | | ms |

**Table 6-4. Electrical Requirements for nPORRST (continued)**

| NO | Parameter | | MIN | MAX | Unit |
|---|---|---|---|---|---|
| | $t_{f(nPORRST)}$ | Filter time nPORRST pin;<br>pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset. | 475 | 2000 | ns |




NOTE: There is no timing dependency between the ramp of the VCCIO and the VCC supply voltage; this is just an exemplary drawing.

**Figure 6-1. nPORRST Timing Diagram**

## 6.4 Warm Reset (nRST)

This is a bidirectional reset signal. The internal circuitry drives the signal low on detecting any device reset condition. An external circuit can assert a device reset by forcing the signal low. On this terminal, the output buffer is implemented as an open drain (drives low only). To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor is connected to this terminal.

This terminal has a glitch filter. It also has an internal pullup.

### 6.4.1 Causes of Warm Reset

**Table 6-5. Causes of Warm Reset**

| DEVICE EVENT | SYSTEM STATUS FLAG |
|---|---|
| Power-Up Reset | Exception Status Register, bit 15 |
| Oscillator fail | Global Status Register, bit 0 |
| PLL slip | Global Status Register, bits 8 and 9 |
| Watchdog exception / Debugger reset | Exception Status Register, bit 13 |
| Software Reset | Exception Status Register, bit 4 |
| External Reset | Exception Status Register, bit 3 |

### 6.4.2 nRST Timing Requirements

**Table 6-6. nRST Timing Requirements**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{v(RST)}$ | Valid time, nRST active after nPORRST inactive | 2256 $t_{c(OSC)}$ (1) | | ns |
| | Valid time, nRST active (all other System reset conditions) | 32 $t_{c(VCLK)}$ | | |
| $t_{f(nRST)}$ | Filter time nRST pin;<br>pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset | 475 | 2000 | ns |

(1) Assumes the oscillator has started up and stabilized before nPORRST is released ..

## 6.5 ARM Cortex-R4F CPU Information

### 6.5.1 Summary of ARM Cortex-R4F CPU Features

The features of the ARM Cortex-R4F CPU include:

- An integer unit with integral Embedded ICE-RT logic.
- High-speed Advanced Microprocessor Bus Architecture (AMBA) Advanced eXtensible Interfaces (AXI) for Level two (L2) master and slave interfaces.
- Floating Point Coprocessor
- Dynamic branch prediction with a global history buffer, and a 4-entry return stack
- Low interrupt latency.
- Non-maskable interrupt.
- A Harvard Level one (L1) memory system with:
  - Tightly-Coupled Memory (TCM) interfaces with support for error correction or parity checking memories
  - ARMv7-R architecture Memory Protection Unit (MPU) with 12 regions
- Dual core logic for fault detection in safety-critical applications.
- An L2 memory interface:
  - Single 64-bit master AXI interface
  - 64-bit slave AXI interface to TCM RAM blocks
- A debug interface to a CoreSight Debug Access Port (DAP).
- A Performance Monitoring Unit (PMU).
- A Vectored Interrupt Controller (VIC) port.

For more information on the ARM Cortex-R4F CPU, see www.arm.com.

### 6.5.2 ARM Cortex-R4F CPU Features Enabled by Software

The following CPU features are disabled on reset and must be enabled by the application if required.

- ECC On Tightly-Coupled Memory (TCM) Accesses
- Hardware Vectored Interrupt (VIC) Port
- Floating Point Coprocessor
- Memory Protection Unit (MPU)

### 6.5.3 Dual Core Implementation

The device has two Cortex-R4F cores, where the output signals of both CPUs are compared in the CCM-R4 unit. To avoid common mode impacts the signals of the CPUs to be compared are delayed by 2 clock cycles as shown in Figure 6-3.

The CPUs have a diverse CPU placement given by following requirements:

- different orientation; for example, CPU1 = "north" orientation, CPU2 = "flip west" orientation
- dedicated guard ring for each CPU


**Figure 6-2. Dual - CPU Orientation**

### 6.5.4 Duplicate clock tree after GCLK

The CPU clock domain is split into two clock trees, one for each CPU, with the clock of the 2nd CPU running at the same frequency and in phase to the clock of CPU1. See Figure 6-3.

### 6.5.5 ARM Cortex-R4F CPU Compare Module (CCM-R4) for Safety

This device has two ARM Cortex-R4F CPU cores, where the output signals of both CPUs are compared in the CCM-R4 unit. To avoid common mode impacts the signals of the CPUs to be compared are delayed in a different way as shown in the figure below.

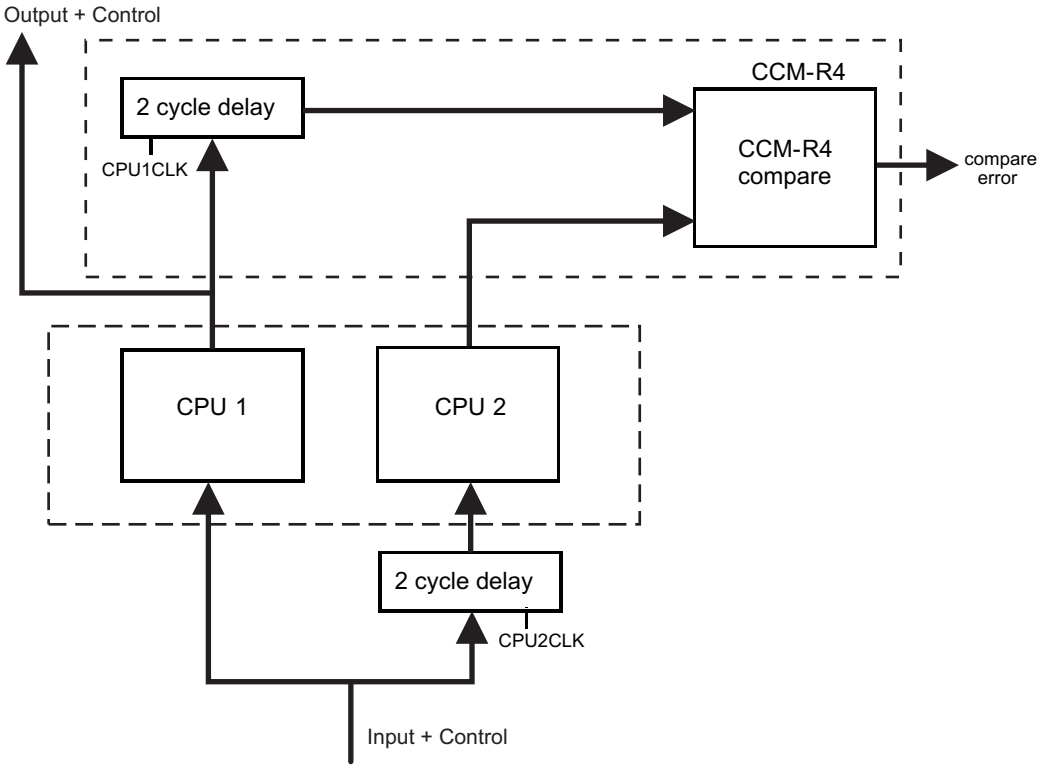



**Figure 6-3. Dual Core Implementation**

To avoid an erroneous CCM-R4 compare error, the application software must initialize the registers of both CPUs before the registers are used, including function calls where the register values are pushed onto the stack.

### 6.5.6 CPU Self-Test

The CPU STC (Self-Test Controller) is used to test the two Cortex-R4F CPU Cores using the Deterministic Logic BIST Controller as the test engine.

The main features of the self-test controller are:

- Ability to divide the complete test run into independent test intervals
- Capable of running the complete test as well as running few intervals at a time
- Ability to continue from the last executed interval (test set) as well as ability to restart from the beginning (First test set)
- Complete isolation of the self-tested CPU core from rest of the system during the self-test run
- Ability to capture the Failure interval number
- Timeout counter for the CPU self-test run as a fail-safe feature

#### 6.5.6.1 Application Sequence for CPU Self-Test

1. Configure clock domain frequencies.
2. Select number of test intervals to be run.
3. Configure the timeout period for the self-test run.
4. Enable self-test.
5. Wait for CPU reset.
6. In the reset handler, read CPU self-test status to identify any failures.
7. Retrieve CPU state if required.

For more information see TMS570LS12x/11x Technical Reference Manual (SPNU515).

#### 6.5.6.2 CPU Self-Test Clock Configuration

The maximum clock rate for the self-test is 90MHz. The STCCLK is divided down from the CPU clock. This divider is configured by the STCCLKDIV register at address 0xFFFFE108.

For more information see TMS570LS12x/11x Technical Reference Manual (SPNU515).

#### 6.5.6.3 CPU Self-Test Coverage

Table 6-7 shows CPU test coverage achieved for each self-test interval. It also lists the cumulative test cycles. The test time can be calculated by multiplying the number of test cycles with the STC clock period.

**Table 6-7. CPU Self-Test Coverage**

| INTERVALS | TEST COVERAGE, % | TEST CYCLES |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 62.13 | 1365 |
| 2 | 70.09 | 2730 |
| 3 | 74.49 | 4095 |
| 4 | 77.28 | 5460 |
| 5 | 79.28 | 6825 |
| 6 | 80.90 | 8190 |
| 7 | 82.02 | 9555 |
| 8 | 83.10 | 10920 |
| 9 | 84.08 | 12285 |
| 10 | 84.87 | 13650 |
| 11 | 85.59 | 15015 |
| 12 | 86.11 | 16380 |
| 13 | 86.67 | 17745 |
| 14 | 87.16 | 19110 |
| 15 | 87.61 | 20475 |
| 16 | 87.98 | 21840 |
| 17 | 88.38 | 23205 |
| 18 | 88.69 | 24570 |
| 19 | 88.98 | 25935 |
| 20 | 89.28 | 27300 |
| 21 | 89.50 | 28665 |
| 22 | 89.76 | 30030 |
| 23 | 90.01 | 31395 |
| 24 | 90.21 | 32760 |

## 6.6 Clocks

### 6.6.1 Clock Sources

The table below lists the available clock sources on the device. Each of the clock sources can be enabled or disabled using the CSDISx registers in the system module. The clock source number in the table corresponds to the control bit in the CSDISx register for that clock source.

The table also shows the default state of each clock source.

**Table 6-8. Available Clock Sources**

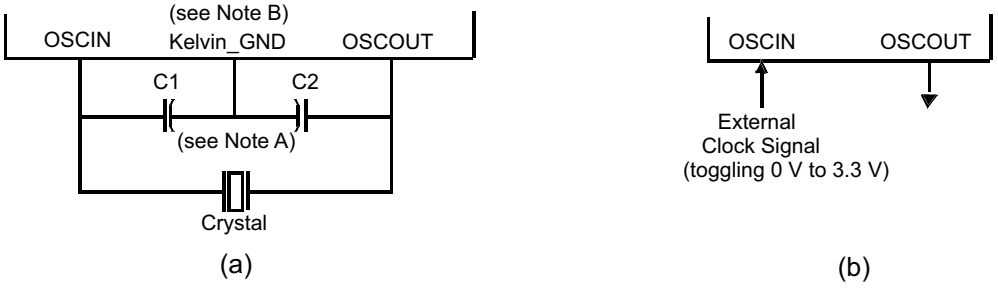
| Clock Source # | Name | Description | Default State |
|---|---|---|---|
| 0 | OSCIN | Main Oscillator | Enabled |
| 1 | PLL1 | Output From PLL1 | Disabled |
| 2 | Reserved | Reserved | Disabled |
| 3 | EXTCLKIN1 | External Clock Input #1 | Disabled |
| 4 | LFLPO | Low Frequency Output of Internal Reference Oscillator | Enabled |
| 5 | HFLPO | High Frequency Output of Internal Reference Oscillator | Enabled |
| 6 | PLL2 | Output From PLL2 | Disabled |
| 7 | EXTCLKIN2 | External Clock Input #2 | Disabled |

#### 6.6.1.1 Main Oscillator

The oscillator is enabled by connecting the appropriate fundamental resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in Figure 6-4. The oscillator is a single stage inverter held in bias by an integrated bias resistor. This resistor is disabled during leakage test measurement and low power modes.

**TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.**

An external oscillator source can be used by connecting a 3.3 V clock signal to the OSCIN pin and leaving the OSCOUT pin unconnected (open) as shown in the figure below.




Note A: The values of C1 and C2 should be provided by the resonator/crystal vendor.
Note B: Kelvin_GND should not be connected to any other GND.

**Figure 6-4. Recommended Crystal/Clock Connection**

#### 6.6.1.1.1 Timing Requirements for Main Oscillator

**Table 6-9. Timing Requirements for Main Oscillator**

| Parameter | | MIN | Type | MAX | Unit |
|---|---|---|---|---|---|
| tc(OSC) | Cycle time, OSCIN (when using a sine-wave input) | 50 | | 200 | ns |
| tc(OSC_SQR) | Cycle time, OSCIN, (when input to the OSCIN is a square wave ) | 50 | | 200 | ns |
| tw(OSCIL) | Pulse duration, OSCIN low (when input to the OSCIN is a square wave) | 15 | | | ns |
| tw(OSCIH) | Pulse duration, OSCIN high (when input to the OSCIN is a square wave) | 15 | | | ns |

### 6.6.1.2 Low Power Oscillator

The Low Power Oscillator (LPO) is comprised of two oscillators — HF LPO and LF LPO, in a single macro.

#### *6.6.1.2.1 Features*

The main features of the LPO are:

- Supplies a clock at extremely low power for power-saving modes. This is connected as clock source # 4 of the Global Clock Module.
- Supplies a high-frequency clock for non-timing-critical systems. This is connected as clock source # 5 of the Global Clock Module.
- Provides a comparison clock for the crystal oscillator failure detection circuit.

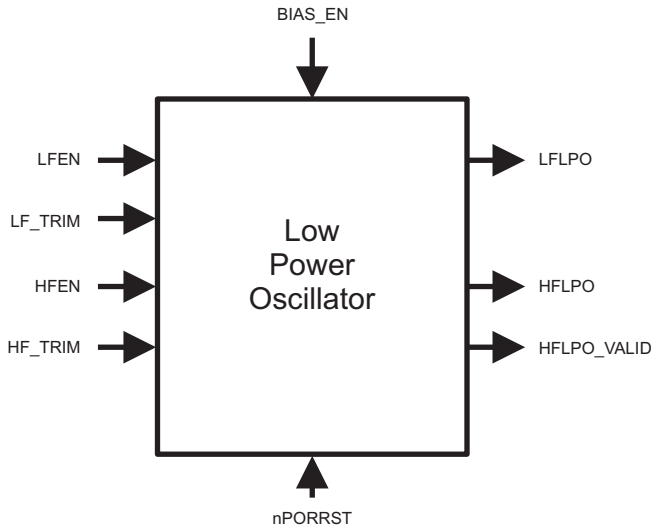



**Figure 6-5. LPO Block Diagram**

Figure 6-5 shows a block diagram of the internal reference oscillator. This is a low power oscillator (LPO) and provides two clock sources: one nominally 80KHz and one nominally 10MHz.

**Table 6-10. LPO Specifications**

| Parameter | | MIN | Typical | MAX | Unit |
|---|---|---|---|---|---|
| Clock Detection | oscillator fail frequency - lower threshold, using untrimmed LPO output | 1.375 | 2.4 | 4.875 | MHz |
| | oscillator fail frequency - higher threshold, using untrimmed LPO output | 22 | 38.4 | 78 | MHz |
| LPO - HF oscillator ($f_{HFLPO}$) | untrimmed frequency | 5.5 | 9 | 19.5 | MHz |
| | trimmed frequency | 8 | 9.6 | 11 | MHz |
| | startup time from STANDBY (LPO BIAS_EN High for at least 900µs) | | | 10 | µs |
| | cold startup time | | | 900 | µs |
| LPO - LF oscillator | untrimmed frequency | 36 | 85 | 180 | kHz |
| | startup time from STANDBY (LPO BIAS_EN High for at least 900µs) | | | 100 | µs |
| | cold startup time | | | 2000 | µs |

#### 6.6.1.3 Phase Locked Loop (PLL) Clock Modules

The PLL is used to multiply the input frequency to some higher frequency.

The main features of the PLL are:

- Frequency modulation can be optionally superimposed on the synthesized frequency of PLL1. The frequency modulation capability of PLL2 is permanently disabled.
- Configurable frequency multipliers and dividers.
- Built-in PLL Slip monitoring circuit.
- Option to reset the device on a PLL slip detection.

##### *6.6.1.3.1 Block Diagram*

Figure 6-6 shows a high-level block diagram of the two PLL macros on this microcontroller. PLLCTL1 and PLLCTL2 are used to configure the multiplier and dividers for the PLL1. PLLCTL3 is used to configure the multiplier and dividers for PLL2.

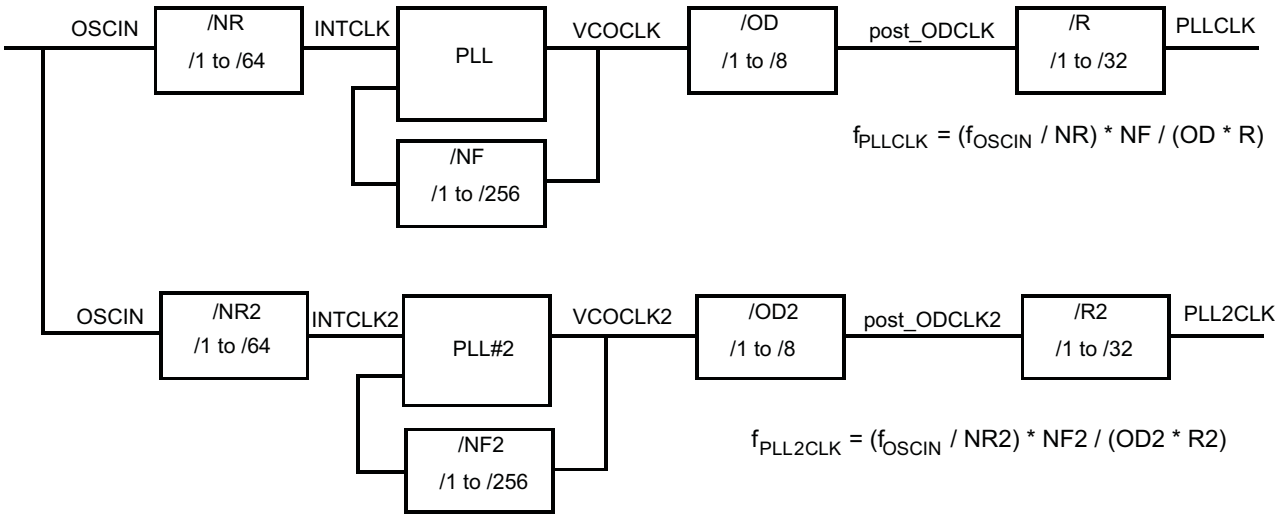



**Figure 6-6. PLLx Block Diagram**

##### *6.6.1.3.2 PLL Timing Specifications*

**Table 6-11. PLL Timing Specifications**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $f_{INTCLK}$ | PLL1 Reference Clock frequency | 1 | $f_{(OSC\_SQR)}$ | MHz |
| $f_{post\_ODCLK}$ | Post-ODCLK – PLL1 Post-divider input clock frequency | | 400 | MHz |
| $f_{VCOCLK}$ | VCOCLK – PLL1 Output Divider (OD) input clock frequency | 150 | 550 | MHz |
| $f_{INTCLK2}$ | PLL2 Reference Clock frequency | 1 | $f_{(OSC\_SQR)}$ | MHz |
| $f_{post\_ODCLK2}$ | Post-ODCLK – PLL2 Post-divider input clock frequency | | 400 | MHz |
| $f_{VCOCLK2}$ | VCOCLK – PLL2 Output Divider (OD) input clock frequency | 150 | 550 | MHz |

#### 6.6.1.4 External Clock Inputs

The device supports up to two external clock inputs. This clock input must be a square wave input. The electrical and timing requirements for these clock inputs are specified below. The external clock sources are not checked for validity. They are assumed valid when enabled.

**Table 6-12. External Clock Timing and Electrical Specifications**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $f_{EXTCLKx}$ | External clock input frequency | | 80 | MHz |
| $t_{w(EXTCLKIN)H}$ | EXTCLK high-pulse duration | 6 | | ns |
| $t_{w(EXTCLKIN)L}$ | EXTCLK low-pulse duration | 6 | | ns |
| $v_{iL(EXTCLKIN)}$ | Low-level input voltage | -0.3 | 0.8 | V |
| $v_{iH(EXTCLKIN)}$ | High-level input voltage | 2 | VCCIO + 0.3 | V |

### 6.6.2 Clock Domains

#### 6.6.2.1 Clock Domain Descriptions

The table below lists the device clock domains and their default clock sources. The table also shows the system module control register that is used to select an available clock source for each clock domain.

**Table 6-13. Clock Domain Descriptions**

| Clock Domain Name | Default Clock Source | Clock Source Selection Register | Description |
|---|---|---|---|
| HCLK | OSCIN | GHVSRC | • Is disabled through the CDDISx registers bit 1<br>• Used for all system modules including DMA, ESM |
| GCLK | OSCIN | GHVSRC | • Always the same frequency as HCLK<br>• In phase with HCLK<br>• Is disabled separately from HCLK through the CDDISx registers bit 0<br>• Can be divided by 1up to 8 when running CPU self-test (LBIST) using the CLKDIV field of the STCCLKDIV register at address 0xFFFFE108 |
| GCLK2 | OSCIN | GHVSRC | • Always the same frequency as GCLK<br>• 2 cycles delayed from GCLK<br>• Is disabled along with GCLK<br>• Gets divided by the same divider setting as that for GCLK when running CPU self-test (LBIST) |
| VCLK | OSCIN | GHVSRC | • Divided down from HCLK<br>• Can be HCLK/1, HCLK/2, ... or HCLK/16<br>• Is disabled separately from HCLK through the CDDISx registers bit 2 |
| VCLK2 | OSCIN | GHVSRC | • Divided down from HCLK<br>• Can be HCLK/1, HCLK/2, ... or HCLK/16<br>• Frequency must be an integer multiple of VCLK frequency<br>• Is disabled separately from HCLK through the CDDISx registers bit 3 |
| VCLK3 | OSCIN | GHVSRC | • Divided down from HCLK<br>• Can be HCLK/1, HCLK/2, ... or HCLK/16<br>• Is disabled separately from HCLK through the CDDISx registers bit 8 |
| VCLK4 | OSCIN | GHVSRC | • Divided down from HCLK<br>• Can be HCLK/1, HCLK/2, ... or HCLK/16<br>• Is disabled separately from HCLK through the CDDISx registers bit 9 |

**Table 6-13. Clock Domain Descriptions (continued)**

| Clock Domain Name | Default Clock Source | Clock Source Selection Register | Description |
|---|---|---|---|
| VCLKA1 | VCLK | VCLKASRC | • Defaults to VCLK as the source<br>• Is disabled through the CDDISx registers bit 4 |
| VCLKA2 | VCLK | VCLKASRC | • Defaults to VCLK as the source<br>• Is disabled through the CDDISx registers bit 5 |
| VCLKA4_S | VCLK | VCLKACON1 | • Defaults to VCLK as the source<br>• Frequency can be as fast as HCLK frequency<br>• Is disabled through the CDDISx registers bit 11 |
| VCLKA4_DIVR | VCLK | VCLKACON1 | • Divided down from the VCLKA4_S using the VCLKA4R field of the VCLKACON1 register at address 0xFFFFE140<br>• Frequency can be VCLKA4_S/1, VCLKA4_S/2, ..., or VCLKA4_S/8<br>• Default frequency is VCLKA4_S/2<br>• Is disabled separately through the VCLKACON1 register VCLKA4_DIV_CDDIS bit only if the VCLKA4_S clock is not disabled |
| RTICLK | VCLK | RCLKSRC | • Defaults to VCLK as the source<br>• If a clock source other than VCLK is selected for RTICLK, then the RTICLK frequency must be less than or equal to VCLK/3<br>– Application can ensure this by programming the RTI1DIV field of the RCLKSRC register, if necessary<br>• Is disabled through the CDDISx registers bit 6 |

### 6.6.2.2 Mapping of Clock Domains to Device Modules

Each clock domain has a dedicated functionality as shown in the figures below.

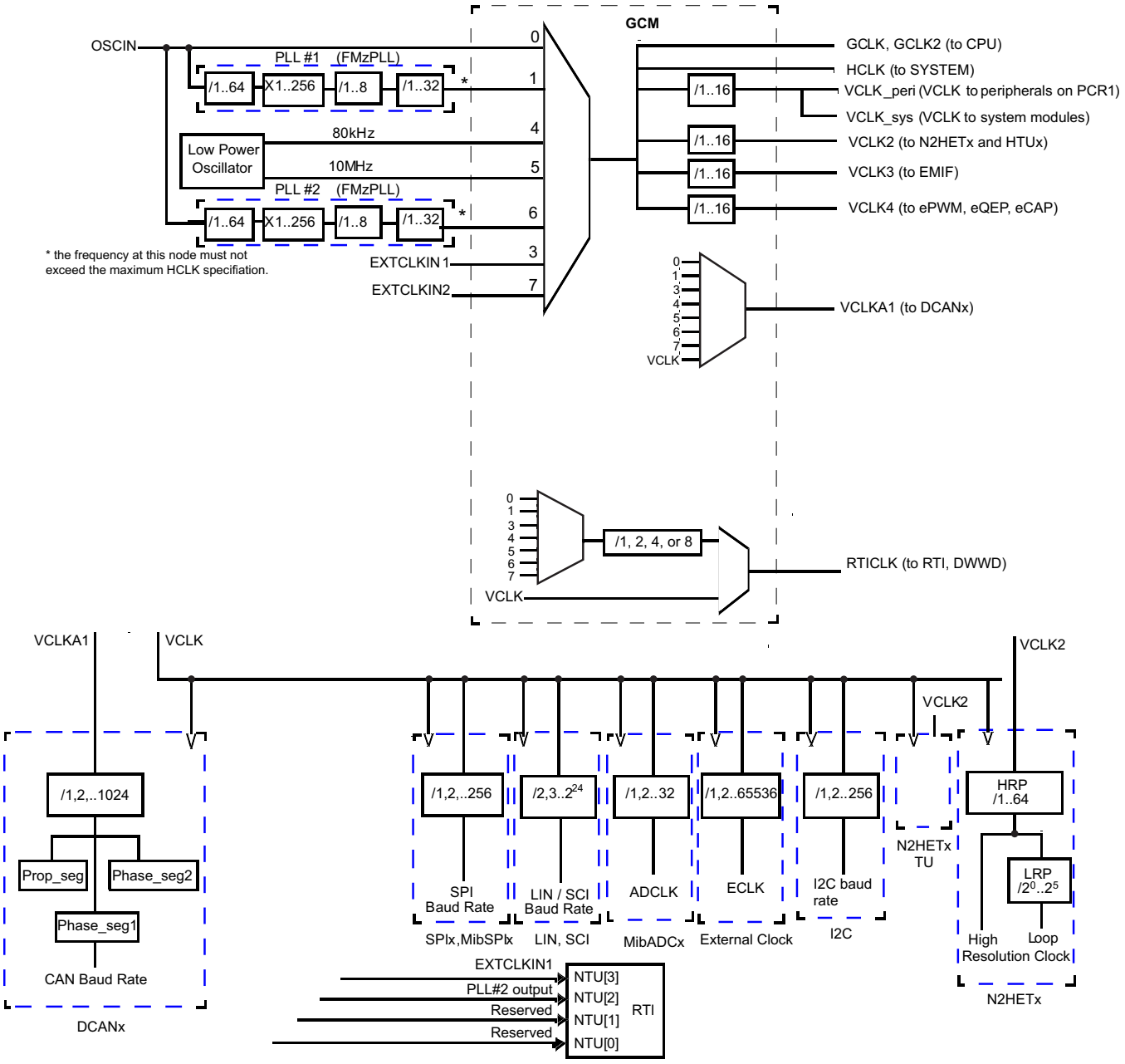



**Figure 6-7. Device Clock Domains**

### 6.6.3 Clock Test Mode

The platform architecture defines a special mode that allows various clock signals to be brought out on to the ECLK pin and N2HET1[12] device outputs. This mode is called the Clock Test mode. It is very useful for debugging purposes and can be configured through the CLKTEST register in the system module.

**Table 6-14. Clock Test Mode Options**

| SEL_ECP_PIN = CLKTEST[3-0] | SIGNAL ON ECLK | | SEL_GIO_PIN = CLKTEST[11-8] | SIGNAL ON N2HET1[12] |
|---|---|---|---|---|
| 0000 | Oscillator | | 0000 | Oscillator Valid Status |
| 0001 | Main PLL free-running clock output | | 0001 | Main PLL Valid status |
| 0010 | Reserved | | 0010 | Reserved |
| 0011 | EXTCLKIN1 | | 0011 | Reserved |
| 0100 | LFLPO | | 0100 | Reserved |
| 0101 | HFLPO | | 0101 | HFLPO Valid status |
| 0110 | Secondary PLL free-running clock output | | 0110 | Secondary PLL Valid Status |
| 0111 | EXTCLKIN2 | | 0111 | Reserved |
| 1000 | GCLK | | 1000 | LFLPO |
| 1001 | RTI Base | | 1001 | Oscillator Valid status |
| 1010 | Reserved | | 1010 | Oscillator Valid status |
| 1011 | VCLKA1 | | 1011 | Oscillator Valid status |
| 1100 | Reserved | | 1100 | Oscillator Valid status |
| 1101 | Reserved | | 1101 | Reserved |
| 1110 | VCLKA4_DIVR | | 1110 | VCLKA4_S |
| 1111 | Reserved | | 1111 | Oscillator Valid status |

## 6.7 Clock Monitoring

The LPO Clock Detect (LPOCLKDET) module consists of a clock monitor (CLKDET) and an internal low power oscillator (LPO).

The LPO provides two different clock sources – a low frequency (LFLPO) and a high frequency (HFLPO).

The CLKDET is a supervisor circuit for an externally supplied clock signal (OSCIN). In case the OSCIN frequency falls out of a frequency window, the CLKDET flags this condition in the global status register (GLBSTAT bit 0: OSC FAIL) and switches all clock domains sourced by OSCIN to the HFLPO clock (limp mode clock).

The valid OSCIN frequency range is defined as: $f_{HFLPO} / 4 < f_{OSCIN} < f_{HFLPO} * 4$.

### 6.7.1 Clock Monitor Timings

For more information on LPO and Clock detection, refer to Table 6-10.

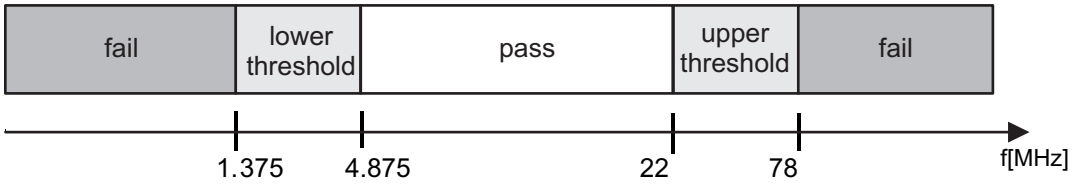



**Figure 6-8. LPO and Clock Detection, Untrimmed HFLPO**

### 6.7.2 External Clock (ECLK) Output Functionality

The ECLK pin can be configured to output a pre-scaled clock signal indicative of an internal device clock. This output can be externally monitored as a safety diagnostic.

### 6.7.3 Dual Clock Comparators

The Dual Clock Comparator (DCC) module determines the accuracy of selectable clock sources by counting the pulses of two independent clock sources (counter 0 and counter 1). If one clock is out of spec, an error signal is generated. For example, the DCC1 can be configured to use HFLPO as the reference clock (for counter 0) and VCLK as the "clock under test" (for counter 1). This configuration allows the DCC1 to monitor the PLL output clock when VCLK is using the PLL output as its source.

An additional use of this module is to measure the frequency of a selectable clock source, using the input clock as a reference, by counting the pulses of two independent clock sources. Counter 0 generates a fixed-width counting window after a preprogrammed number of pulses. Counter 1 generates a fixed-width pulse (1 cycle) after a pre-programmed number of pulses. This pulse sets as an error signal if counter 1 does not reach 0 within the counting window generated by counter 0.

#### 6.7.3.1 Features

- Takes two different clock sources as input to two independent counter blocks.
- One of the clock sources is the known-good, or reference clock; the second clock source is the "clock under test."
- Each counter block is programmable with initial, or seed values.
- The counter blocks start counting down from their seed values at the same time; a mismatch from the expected frequency for the clock under test generates an error signal which is used to interrupt the CPU.

#### 6.7.3.2 Mapping of DCC Clock Source Inputs

**Table 6-15. DCC1 Counter 0 Clock Sources**

| CLOCK SOURCE [3:0] | CLOCK NAME |
|---|---|
| others | oscillator (OSCIN) |
| 0x5 | high frequency LPO |

**Table 6-15. DCC1 Counter 0 Clock Sources (continued)**

| CLOCK SOURCE [3:0] | CLOCK NAME |
|---|---|
| 0xA | test clock (TCK) |

**Table 6-16. DCC1 Counter 1 Clock Sources**

| KEY [3:0] | CLOCK SOURCE [3:0] | CLOCK NAME |
|---|---|---|
| others | - | N2HET1[31] |
| 0xA | 0x0 | Main PLL free-running clock output |
| | 0x1 | PLL #2 free-running clock output |
| | 0x2 | low frequency LPO |
| | 0x3 | high frequency LPO |
| | 0x4 | reserved |
| | 0x5 | EXTCLKIN1 |
| | 0x6 | EXTCLKIN2 |
| | 0x7 | reserved |
| | 0x8 - 0xF | VCLK |

**Table 6-17. DCC2 Counter 0 Clock Sources**

| CLOCK SOURCE [3:0] | CLOCK NAME |
|---|---|
| others | oscillator (OSCIN) |
| 0xA | test clock (TCK) |

**Table 6-18. DCC2 Counter 1 Clock Sources**

| KEY [3:0] | CLOCK SOURCE [3:0] | CLOCK NAME |
|---|---|---|
| others | - | N2HET2[0] |
| 0xA | 00x0 - 0x7 | Reserved |
| | 0x8 - 0xF | VCLK |

## 6.8 Glitch Filters

A glitch filter is present on the following signals.

**Table 6-19. Glitch Filter Timing Specifications**

| Pin | Parameter | | MIN | MAX | Unit |
|---|---|---|---|---|---|
| nPORRST | $t_{f(nPORRST)}$ | Filter time nPORRST pin;<br>pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset(1) | 475 | 2000 | ns |
| nRST | $t_{f(nRST)}$ | Filter time nRST pin;<br>pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset | 475 | 2000 | ns |
| TEST | $t_{f(TEST)}$ | Filter time TEST pin;<br>pulses less than MIN will be filtered out, pulses greater than MAX will pass through | 475 | 2000 | ns |

(1) The glitch filter design on the nPORRST signal is designed such that no size pulse will reset any part of the microcontroller (flash pump, I/O pins, etc.) without also generating a valid reset signal to the CPU.

## 6.9 Device Memory Map

### 6.9.1 Memory Map Diagram

The figure below shows the device memory map.

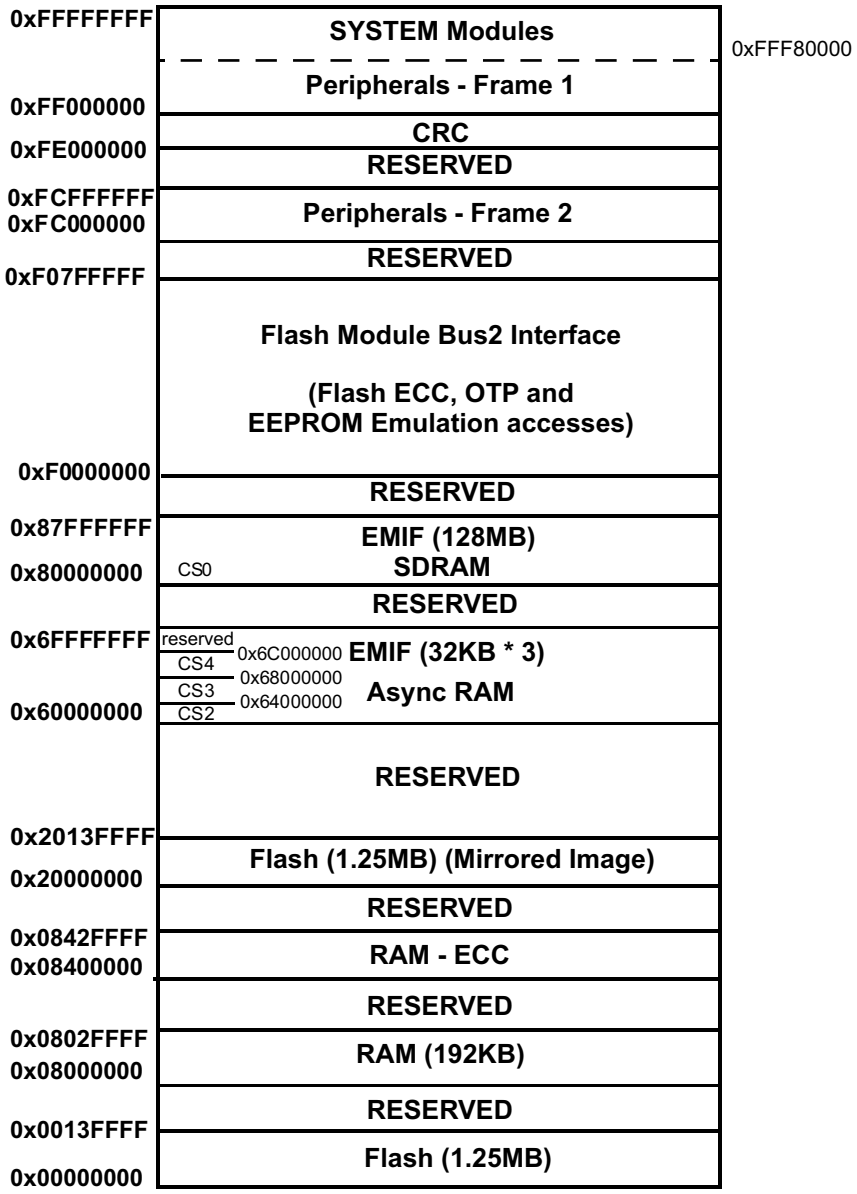



**Figure 6-9. Memory Map**

The Flash memory is mirrored to support ECC logic testing. The base address of the mirrored Flash image is 0x2000 0000.

### 6.9.2 Memory Map Table

**Table 6-20. Device Memory Map**

| MODULE NAME | FRAME CHIP SELECT | FRAME ADDRESS RANGE | | FRAME SIZE | ACTUAL SIZE | RESPNSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME |
|---|---|---|---|---|---|---|
| | | START | END | | | |
| **Memories tightly coupled to the ARM Cortex-R4F CPU** | | | | | | |
| TCM Flash | CS0 | 0x0000_0000 | 0x00FF_FFFF | 16MB | 1.25MB | Abort |
| TCM RAM + RAM ECC | CSRAM0 | 0x0800_0000 | 0x0BFF_FFFF | 64MB | 192KB | |
| Mirrored Flash | Flash mirror frame | 0x2000_0000 | 0x20FF_FFFF | 16MB | 1.25MB | |
| **External Memory Accesses** | | | | | | |
| EMIF Chip Select 2 (asynchronous) | EMIF select 2 | 0x6000_0000 | 0x63FF_FFFF | 64MB | 32KB | Access to "Reserved" space will generate Abort |
| EMIF Chip Select 3 (asynchronous) | EMIF select 3 | 0x6400_0000 | 0x67FF_FFFF | 64MB | 32KB | |
| EMIF Chip Select 4 (asynchronous) | EMIF select 4 | 0x6800_0000 | 0x6BFF_FFFF | 64MB | 32KB | |
| EMIF Chip Select 0 (synchronous) | EMIF select 0 | 0x8000_0000 | 0x87FF_FFFF | 128MB | 128MB | |
| **Flash Module Bus2 Interface** | | | | | | |
| Customer OTP, TCM Flash Banks | | 0xF000_0000 | 0xF000_1FFF | 8KB | 4KB | Abort |
| Customer OTP, Bank 7 | | 0xF000_E000 | 0xF000_FFFF | 8KB | 2KB | |
| Customer OTP–ECC, TCM Flash Banks | | 0xF004_0000 | 0xF004_03FF | 1KB | 512B | |
| Customer OTP–ECC, Bank 7 | | 0xF004_1C00 | 0xF004_1FFF | 1KB | 256B | |
| TI OTP, TCM Flash Banks | | 0xF008_0000 | 0xF008_1FFF | 8KB | 4KB | |
| TI OTP, Bank 7 | | 0xF008_E000 | 0xF008_FFFF | 8KB | 2KB | |
| TI OTP–ECC, TCM Flash Banks | | 0xF00C_0000 | 0xF00C_03FF | 1KB | 512B | |
| TI OTP–ECC, Bank 7 | | 0xF00C_1C00 | 0xF00C_1FFF | 1KB | 256B | |
| Bank 7 – ECC | | 0xF010_0000 | 0xF013_FFFF | 256KB | 8KB | |
| Bank 7 | | 0xF020_0000 | 0xF03F_FFFF | 2MB | 64KB | |
| Flash Data Space ECC | | 0xF040_0000 | 0xF04F_FFFF | 1MB | 160KB | |
| **EMIF slave interfaces** | | | | | | |
| EMIF Registers | | 0xFCFF_E800 | 0xFCFF_E8FF | 256B | 256B | Abort |
| **SCR5: Enhanced Timer Peripherals** | | | | | | |
| ePWM1 | | 0xFCF7_8C00 | 0xFCF7_8CFF | 256B | 256B | Abort |
| ePWM2 | | 0xFCF7_8D00 | 0xFCF7_8DFF | 256B | 256B | Abort |
| ePWM3 | | 0xFCF7_8E00 | 0xFCF7_8EFF | 256B | 256B | Abort |
| ePWM4 | | 0xFCF7_8F00 | 0xFCF7_8FFF | 256B | 256B | Abort |
| ePWM5 | | 0xFCF7_9000 | 0xFCF7_90FF | 256B | 256B | Abort |
| ePWM6 | | 0xFCF7_9100 | 0xFCF7_91FF | 256B | 256B | Abort |
| ePWM7 | | 0xFCF7_9200 | 0xFCF7_92FF | 256B | 256B | Abort |
| eCAP1 | | 0xFCF7_9300 | 0xFCF7_93FF | 256B | 256B | Abort |

**Table 6-20. Device Memory Map (continued)**

| MODULE NAME | FRAME CHIP SELECT | FRAME ADDRESS RANGE | | FRAME SIZE | ACTUAL SIZE | RESPNSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME |
|---|---|---|---|---|---|---|
| | | START | END | | | |
| eCAP2 | | 0xFCF7_9400 | 0xFCF7_94FF | 256B | 256B | Abort |
| eCAP3 | | 0xFCF7_9500 | 0xFCF7_95FF | 256B | 256B | Abort |
| eCAP4 | | 0xFCF7_9600 | 0xFCF7_96FF | 256B | 256B | Abort |
| eCAP5 | | 0xFCF7_9700 | 0xFCF7_97FF | 256B | 256B | Abort |
| eCAP6 | | 0xFCF7_9800 | 0xFCF7_98FF | 256B | 256B | Abort |
| eQEP1 | | 0xFCF7_9900 | 0xFCF7_99FF | 256B | 256B | Abort |
| eQEP2 | | 0xFCF7_9A00 | 0xFCF7_9AFF | 256B | 256B | Abort |
| **Cyclic Redundancy Checker (CRC) Module Registers** | | | | | | |
| CRC | CRC frame | 0xFE00_0000 | 0xFEFF_FFFF | 16MB | 512B | Accesses above 0x200 generate abort. |
| **Peripheral Memories** | | | | | | |
| MIBSPI5 RAM | PCS[5] | 0xFF0A_0000 | 0xFF0B_FFFF | 128KB | 2KB | Abort for accesses above 2KB |
| MIBSPI3 RAM | PCS[6] | 0xFF0C_0000 | 0xFF0D_FFFF | 128KB | 2KB | Abort for accesses above 2KB |
| MIBSPI1 RAM | PCS[7] | 0xFF0E_0000 | 0xFF0F_FFFF | 128KB | 2KB | Abort for accesses above 2KB |
| DCAN3 RAM | PCS[13] | 0xFF1A_0000 | 0xFF1B_FFFF | 128KB | 2KB | Wrap around for accesses to unimplemented address offsets lower than 0x7FF. Abort generated for accesses beyond offset 0x800. |
| DCAN2 RAM | PCS[14] | 0xFF1C_0000 | 0xFF1D_FFFF | 128KB | 2KB | Wrap around for accesses to unimplemented address offsets lower than 0x7FF. Abort generated for accesses beyond offset 0x800. |
| DCAN1 RAM | PCS[15] | 0xFF1E_0000 | 0xFF1F_FFFF | 128KB | 2KB | Wrap around for accesses to unimplemented address offsets lower than 0x7FF. Abort generated for accesses beyond offset 0x800. |
| MIBADC2 RAM | PCS[29] | 0xFF3A_0000 | 0xFF3B_FFFF | 128KB | 8KB | Wrap around for accesses to unimplemented address offsets lower than 0x1FFF. Abort generated for accesses beyond 0x1FFF. |
| MIBADC2 Look-Up Table | | | | | 384B | Look-Up Table for ADC2 wrapper. Starts at address offset 0x2000 and ends at address offset 0x217F. Wrap around for accesses between offsets 0x0180 and 0x3FFF. Abort generated for accesses beyond offset 0x4000. |
| MIBADC1 RAM | PCS[31] | 0xFF3E_0000 | 0xFF3F_FFFF | 128KB | 8KB | Wrap around for accesses to unimplemented address offsets lower than 0x1FFF. Abort generated for accesses beyond 0x1FFF. |
| MibADC1 Look-Up Table | | | | | 384B | Look-Up Table for ADC1 wrapper. Starts at address offset 0x2000 and ends at address offset 0x217F. Wrap around for accesses between offsets 0x0180 and 0x3FFF. Abort generated for accesses beyond offset 0x4000. |
| N2HET2 RAM | PCS[34] | 0xFF44_0000 | 0xFF45_FFFF | 128KB | 16KB | Wrap around for accesses to unimplemented address offsets lower than 0x3FFF. Abort generated for accesses beyond 0x3FFF. |
| N2HET1 RAM | PCS[35] | 0xFF46_0000 | 0xFF47_FFFF | 128KB | 16KB | Wrap around for accesses to unimplemented address offsets lower than 0x3FFF. Abort generated for accesses beyond 0x3FFF. |
| HTU2 RAM | PCS[38] | 0xFF4C_0000 | 0xFF4D_FFFF | 128KB | 1KB | Abort |
| HTU1 RAM | PCS[39] | 0xFF4E_0000 | 0xFF4F_FFFF | 128KB | 1KB | Abort |

**Table 6-20. Device Memory Map (continued)**

| MODULE NAME | FRAME CHIP SELECT | FRAME ADDRESS RANGE | | FRAME SIZE | ACTUAL SIZE | RESPNSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME |
|---|---|---|---|---|---|---|
| | | START | END | | | |
| **Debug Components** | | | | | | |
| CoreSight Debug ROM | CSCS0 | 0xFFA0_0000 | 0xFFA0_0FFF | 4KB | 4KB | Reads return zeros, writes have no effect |
| Cortex-R4F Debug | CSCS1 | 0xFFA0_1000 | 0xFFA0_1FFF | 4KB | 4KB | Reads return zeros, writes have no effect |
| POM | CSCS4 | 0xFFA0_4000 | 0xFFA0_4FFF | 4KB | 4KB | Abort |
| **Peripheral Control Registers** | | | | | | |
| HTU1 | PS[22] | 0xFFF7_A400 | 0xFFF7_A4FF | 256B | 256B | Reads return zeros, writes have no effect |
| HTU2 | PS[22] | 0xFFF7_A500 | 0xFFF7_A5FF | 256B | 256B | Reads return zeros, writes have no effect |
| N2HET1 | PS[17] | 0xFFF7_B800 | 0xFFF7_B8FF | 256B | 256B | Reads return zeros, writes have no effect |
| N2HET2 | PS[17] | 0xFFF7_B900 | 0xFFF7_B9FF | 256B | 256B | Reads return zeros, writes have no effect |
| GIO | PS[16] | 0xFFF7_BC00 | 0xFFF7_BDFF | 512B | 256B | Reads return zeros, writes have no effect |
| MIBADC1 | PS[15] | 0xFFF7_C000 | 0xFFF7_C1FF | 512B | 512B | Reads return zeros, writes have no effect |
| MIBADC2 | PS[15] | 0xFFF7_C200 | 0xFFF7_C3FF | 512B | 512B | Reads return zeros, writes have no effect |
| I2C | PS[10] | 0xFFF7_D400 | 0xFFF7_D4FF | 256B | 256B | Reads return zeros, writes have no effect |
| DCAN1 | PS[8] | 0xFFF7_DC00 | 0xFFF7_DDFF | 512B | 512B | Reads return zeros, writes have no effect |
| DCAN2 | PS[8] | 0xFFF7_DE00 | 0xFFF7_DFFF | 512B | 512B | Reads return zeros, writes have no effect |
| DCAN3 | PS[7] | 0xFFF7_E000 | 0xFFF7_E1FF | 512B | 512B | Reads return zeros, writes have no effect |
| LIN | PS[6] | 0xFFF7_E400 | 0xFFF7_E4FF | 256B | 256B | Reads return zeros, writes have no effect |
| SCI | PS[6] | 0xFFF7_E500 | 0xFFF7_E5FF | 256B | 256B | Reads return zeros, writes have no effect |
| MibSPI1 | PS[2] | 0xFFF7_F400 | 0xFFF7_F5FF | 512B | 512B | Reads return zeros, writes have no effect |
| SPI2 | PS[2] | 0xFFF7_F600 | 0xFFF7_F7FF | 512B | 512B | Reads return zeros, writes have no effect |
| MibSPI3 | PS[1] | 0xFFF7_F800 | 0xFFF7_F9FF | 512B | 512B | Reads return zeros, writes have no effect |
| SPI4 | PS[1] | 0xFFF7_FA00 | 0xFFF7_FBFF | 512B | 512B | Reads return zeros, writes have no effect |
| MibSPI5 | PS[0] | 0xFFF7_FC00 | 0xFFF7_FDFF | 512B | 512B | Reads return zeros, writes have no effect |
| **System Modules Control Registers and Memories** | | | | | | |
| DMA RAM | PPCS0 | 0xFFF8_0000 | 0xFFF8_0FFF | 4KB | 4KB | Abort |
| VIM RAM | PPCS2 | 0xFFF8_2000 | 0xFFF8_2FFF | 4KB | 1KB | Wrap around for accesses to unimplemented address offsets between 1KB and 4KB. |
| Flash Module | PPCS7 | 0xFFF8_7000 | 0xFFF8_7FFF | 4KB | 4KB | Abort |
| eFuse Controller | PPCS12 | 0xFFF8_C000 | 0xFFF8_CFFF | 4KB | 4KB | Abort |
| Power Management Module (PMM) | PPSE0 | 0xFFFF_0000 | 0xFFFF_01FF | 512B | 512B | Abort |

**Table 6-20. Device Memory Map (continued)**

| MODULE NAME | FRAME CHIP SELECT | FRAME ADDRESS RANGE | | FRAME SIZE | ACTUAL SIZE | RESPNSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME |
|---|---|---|---|---|---|---|
| | | START | END | | | |
| PCR registers | PPS0 | 0xFFFF_E000 | 0xFFFF_E0FF | 256B | 256B | Reads return zeros, writes have no effect |
| System Module - Frame 2 (see SPNU515) | PPS0 | 0xFFFF_E100 | 0xFFFF_E1FF | 256B | 256B | Reads return zeros, writes have no effect |
| PBIST | PPS1 | 0xFFFF_E400 | 0xFFFF_E5FF | 512B | 512B | Reads return zeros, writes have no effect |
| STC | PPS1 | 0xFFFF_E600 | 0xFFFF_E6FF | 256B | 256B | Generates address error interrupt, if enabled |
| IOMM Multiplexing Control Module | PPS2 | 0xFFFF_EA00 | 0xFFFF_EBFF | 512B | 512B | Reads return zeros, writes have no effect |
| DCC1 | PPS3 | 0xFFFF_EC00 | 0xFFFF_ECFF | 256B | 256B | Reads return zeros, writes have no effect |
| DMA | PPS4 | 0xFFFF_F000 | 0xFFFF_F3FF | 1KB | 1KB | Reads return zeros, writes have no effect |
| DCC2 | PPS5 | 0xFFFF_F400 | 0xFFFF_F4FF | 256B | 256B | Reads return zeros, writes have no effect |
| ESM | PPS5 | 0xFFFF_F500 | 0xFFFF_F5FF | 256B | 256B | Reads return zeros, writes have no effect |
| CCMR4 | PPS5 | 0xFFFF_F600 | 0xFFFF_F6FF | 256B | 256B | Reads return zeros, writes have no effect |
| RAM ECC even | PPS6 | 0xFFFF_F800 | 0xFFFF_F8FF | 256B | 256B | Reads return zeros, writes have no effect |
| RAM ECC odd | PPS6 | 0xFFFF_F900 | 0xFFFF_F9FF | 256B | 256B | Reads return zeros, writes have no effect |
| RTI + DWWD | PPS7 | 0xFFFF_FC00 | 0xFFFF_FCFF | 256B | 256B | Reads return zeros, writes have no effect |
| VIM Parity | PPS7 | 0xFFFF_FD00 | 0xFFFF_FDFF | 256B | 256B | Reads return zeros, writes have no effect |
| VIM | PPS7 | 0xFFFF_FE00 | 0xFFFF_FEFF | 256B | 256B | Reads return zeros, writes have no effect |
| System Module - Frame 1 (see SPNU515) | PPS7 | 0xFFFF_FF00 | 0xFFFF_FFFF | 256B | 256B | Reads return zeros, writes have no effect |

### 6.9.3 Special Consideration for CPU Access Errors Resulting in Imprecise Aborts

Any CPU write access to a Normal or Device type memory, which generates a fault, will generate an imprecise abort. The imprecise abort exception is disabled by default and must be enabled for the CPU to handle this exception. The imprecise abort handling is enabled by clearing the "A" bit in the CPU's program status register (CPSR).

### 6.9.4 Master/Slave Access Privileges

The table below lists the access permissions for each bus master on the device. A bus master is a module that can initiate a read or a write transaction on the device.

Each slave module on the main interconnect is listed in the table. A "Yes" indicates that the module listed in the "MASTERS" column can access that slave module.

**Table 6-21. Master / Slave Access Matrix**

| MASTERS | ACCESS MODE | SLAVES ON MAIN SCR | | | | |
|---|---|---|---|---|---|---|
| | | Flash Module Bus2 Interface: OTP, ECC, Bank 7 | Non-CPU Accesses to Program Flash and CPU Data RAM | CRC | EMIF Slave Interface | Peripheral Control Registers, All Peripheral Memories, And All System Module Control Registers And Memories |
| CPU READ | User/Privilege | Yes | Yes | Yes | Yes | Yes |
| CPU WRITE | User/Privilege | **No** | Yes | Yes | Yes | Yes |
| DMA | User | Yes | Yes | Yes | Yes | Yes |
| POM | User | Yes | Yes | Yes | Yes | Yes |
| DAP | Privilege | Yes | Yes | Yes | Yes | Yes |
| HTU1 | Privilege | **No** | Yes | Yes | Yes | Yes |
| HTU2 | Privilege | **No** | Yes | Yes | Yes | Yes |

### 6.9.5 Special Notes on Accesses to Certain Slaves

Write accesses to the Power Domain Management Module (PMM) control registers are limited to the CPU (master id = 1). The other masters can only read from these registers.

A debugger can also write to the PMM registers. The master-id check is disabled in debug mode.

The device contains dedicated logic to generate a bus error response on any access to a module that is in a power domain that has been turned OFF.

### 6.9.6 Parameter Overlay Module (POM) Considerations

- The POM can map onto up to 8MB of the internal or external memory space. The starting address and the size of the memory overlay are configurable through the POM control registers. Care must be taken to ensure that the overlay is mapped on to available memory.
- ECC must be disabled by software through CP15 in case POM overlay is enabled; otherwise ECC errors will be generated.
- POM overlay must not be enabled when the flash and internal RAM memories are swapped through the MEM SWAP field of the Bus Matrix Module Control Register 1 (BMMCR1).
- When POM is used to overlay the flash on to internal or external RAM, there is a bus contention possibility when another master accesses the TCM flash. This results in a system hang.
  - The POM implements a timeout feature to detect this exact scenario. The timeout needs to be enabled whenever POM overlay is enabled.
  - The timeout can be enabled by writing 1010 to the Enable TimeOut (ETO) field of the POM Global Control register (POMGLBCTRL, address = 0xFFA04000).
  - In case a read request by the POM cannot be completed within 32 HCLK cycles, the timeout (TO) flag is set in the POM Flag register (POMFLG, address = 0xFFA0400C). Also, an abort is generated to the CPU. This can be a prefetch abort for an instruction fetch or a data abort for a data fetch.
  - The prefetch- and data-abort handlers must be modified to check if the TO flag in the POM is set. If so, then the application can assume that the timeout is caused by a bus contention between the POM transaction and another master accessing the same memory region. The abort handlers need to clear the TO flag, so that any further aborts are not misinterpreted as having been caused due to a timeout from the POM.

## 6.10 Flash Memory

### 6.10.1 Flash Memory Configuration

**Flash Bank:** A separate block of logic consisting of 1 to 16 sectors. Each flash bank normally has a customer-OTP and a TI-OTP area. These flash sectors share input/output buffers, data paths, sense amplifiers, and control logic.

**Flash Sector:** A contiguous region of flash memory which must be erased simultaneously due to physical construction constraints.

**Flash Pump:** A charge pump which generates all the voltages required for reading, programming, or erasing the flash banks.

**Flash Module:** Interface circuitry required between the host CPU and the flash banks and pump module.

**Table 6-22. Flash Memory Banks and Sectors**

| Memory Arrays (or Banks) | Sector No. | Segment | Low Address | High Address |
|---|---|---|---|---|
| BANK0 (1.25MBytes)(1) | 0 | 16K Bytes | 0x0000_0000 | 0x0000_3FFF |
| | 1 | 16K Bytes | 0x0000_4000 | 0x0000_7FFF |
| | 2 | 16K Bytes | 0x0000_8000 | 0x0000_BFFF |
| | 3 | 16K Bytes | 0x0000_C000 | 0x0000_FFFF |
| | 4 | 16K Bytes | 0x0001_0000 | 0x0001_3FFF |
| | 5 | 16K Bytes | 0x0001_4000 | 0x0001_7FFF |
| | 6 | 32K Bytes | 0x0001_8000 | 0x0001_FFFF |
| | 7 | 128K Bytes | 0x0002_0000 | 0x0003_FFFF |
| | 8 | 128K Bytes | 0x0004_0000 | 0x0005_FFFF |
| | 9 | 128K Bytes | 0x0006_0000 | 0x0007_FFFF |
| | 10 | 128K Bytes | 0x0008_0000 | 0x0009_FFFF |
| | 11 | 128K Bytes | 0x000A_0000 | 0x000B_FFFF |
| | 12 | 128K Bytes | 0x000C_0000 | 0x000D_FFFF |
| | 13 | 128K Bytes | 0x000E_0000 | 0x000F_FFFF |
| | 14 | 128K Bytes | 0x0010_0000 | 0x0011_FFFF |
| | 15 | 128K Bytes | 0x0012_0000 | 0x0013_FFFF |
| BANK7 (64KBytes) for EEPROM emulation(2)(3) | 0 | 16K Bytes | 0xF020_0000 | 0xF020_3FFF |
| | 1 | 16K Bytes | 0xF020_4000 | 0xF020_7FFF |
| | 2 | 16K Bytes | 0xF020_8000 | 0xF020_BFFF |
| | 3 | 16K Bytes | 0xF020_C000 | 0xF020_FFFF |

(1) The Flash banks are 144-bit wide bank with ECC support.
(2) The flash bank7 can be programmed while executing code from flash bank0.
(3) Code execution is not allowed from flash bank7.

### 6.10.2 Main Features of Flash Module

- Support for multiple flash banks for program and/or data storage
- Simultaneous read access on a bank while performing program or erase operation on any other bank
- Integrated state machines to automate flash erase and program operations
- Pipelined mode operation to improve instruction access interface bandwidth
- Support for Single Error Correction Double Error Detection (SECDED) block inside Cortex-R4F CPU
  - Error address is captured for host system debugging
- Support for a rich set of diagnostic features

### 6.10.3 ECC Protection for Flash Accesses

All accesses to the program flash memory are protected by Single Error Correction Double Error Detection (SECDED) logic embedded inside the CPU. The flash module provides 8 bits of ECC code for 64 bits of instructions or data fetched from the flash memory. The CPU calculates the expected ECC code based on the 64 bits received and compares it with the ECC code returned by the flash module. A single-bit error is corrected and flagged by the CPU, while a multibit error is only flagged. The CPU signals an ECC error through its Event bus. This signaling mechanism is not enabled by default and must be enabled by setting the "X" bit of the Performance Monitor Control Register, c9.

```
MRC p15,#0,r1,c9,c12,#0    ;Enabling Event monitor states
ORR r1, r1, #0x00000010
MCR p15,#0,r1,c9,c12,#0    ;Set 4th bit (‘X’) of PMNC register
MRC p15,#0,r1,c9,c12,#0
```

The application must also explicitly enable the CPU's ECC checking for accesses on the CPU's ATCM and BTCM interfaces. These are connected to the program flash and data RAM respectively. ECC checking for these interfaces can be done by setting the B1TCMPCEN, B0TCMPCEN and ATCMPCEN bits of the System Control coprocessor's Auxiliary Control Register, c1.

```
MRC p15, #0, r1, c1, c0, #1
ORR r1, r1, #0x0e000000        ;Enable ECC checking for ATCM and BTCMs
DMB
MCR p15, #0, r1, c1, c0, #1
```

### 6.10.4 Flash Access Speeds

For information on flash memory access speeds and the relevant wait states required, refer to Section 5.6.

### 6.10.5 Program Flash

**Table 6-23. Timing Requirements for Program Flash**

| Parameter | | | MIN | NOM | MAX | Unit |
|---|---|---|---|---|---|---|
| $t_{prog(144bit)}$ | Wide Word (144bit) programming time | | | 40 | 300 | µs |
| $t_{prog(Total)}$ | 1.25MByte programming time(1) | -40°C to 125°C | | | 13 | s |
| | | 0°C to 60°C, for first 25 cycles | | 3.3 | 6.6 | s |
| $t_{erase(bank0)}$ | Sector/Bank erase time(2) | -40°C to 125°C | | 0.03 | 4 | s |
| | | 0°C to 60°C, for first 25 cycles | | 16 | 100 | ms |
| $t_{wec}$ | Write/erase cycles with 15 year Data Retention requirement | -40°C to 125°C | | | 1000 | cycles |

(1) This programming time includes overhead of state machine, but does not include data transfer time. The programming time assumes programming 144 bits at a time at the maximum specified operating frequency.
(2) During bank erase, the selected sectors are erased simultaneously. The time to erase the bank is specified as equal to the time to erase a sector.

### 6.10.6 Data Flash

**Table 6-24. Timing Requirements for Data Flash**

| Parameter | | | MIN | NOM | MAX | Unit |
|---|---|---|---|---|---|---|
| $t_{prog(144bit)}$ | Wide Word (144bit) programming time | | | 40 | 300 | µs |
| $t_{prog(Total)}$ | EEPROM Emulation (bank 7) 64KByte programming time(1) | -40°C to 125°C | | | 660 | ms |
| | | 0°C to 60°C, for first 25 cycles | | 165 | 330 | ms |
| $t_{erase(bank7)}$ | EEPROM Emulation (bank 7) Sector/Bank erase time (2) | -40°C to 125°C | | 0.2 | 8 | s |
| | | 0°C to 60°C, for first 25 cycles | | 14 | 100 | ms |
| $t_{wec}$ | Write/erase cycles with 15 year Data Retention requirement | -40°C to 125°C | | | 100000 | cycles |

(1) This programming time includes overhead of state machine, but does not include data transfer time. The programming time assumes programming 144 bits at a time at the maximum specified operating frequency.
(2) During bank erase, the selected sectors are erased simultaneously. The time to erase the bank is specified as equal to the time to erase a sector.

## 6.11 Tightly Coupled RAM Interface Module

Figure 6-10 illustrates the connection of the Tightly Coupled RAM (TCRAM) to the Cortex-R4F CPU.

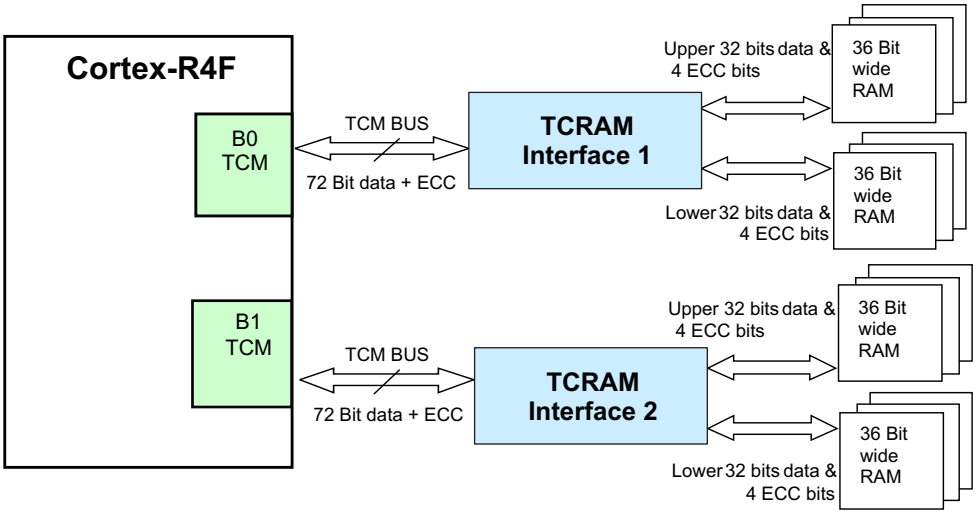



**Figure 6-10. TCRAM Block Diagram**

### *6.11.1 Features*

The features of the Tightly Coupled RAM (TCRAM) Module are:

- Acts as slave to the BTCM interface of the Cortex-R4F CPU
- Supports the internal ECC scheme of the CPU by providing 64-bit data and 8-bit ECC code
- Monitors CPU Event Bus and generates single or multibit error interrupts
- Stores addresses for single and multibit errors
- Supports RAM trace module
- Provides CPU address bus integrity checking by supporting parity checking on the address bus
- Performs redundant address decoding for the RAM bank chip select and ECC select generation logic
- Provides enhanced safety for the RAM addressing by implementing two 36-bit-wide byte-interleaved RAM banks and generating independent RAM access control signals to the two banks
- Supports auto-initialization of the RAM banks along with the ECC bits

### *6.11.2 TCRAM ECC Support*

The TCRAM interface passes on the ECC code for each data read by the Cortex-R4F CPU from the RAM. It also stores the contents of the CPU ECC port in the ECC RAM when the CPU does a write to the RAM. The TCRAM interface monitors the CPU event bus and provides registers for indicating single/multibit errors and also for identifying the address that caused the single or multibit error. The event signaling and the ECC checking for the RAM accesses must be enabled inside the CPU.

For more information see TMS570LS12x/11x Technical Reference Manual (SPNU515).

## 6.12 Parity Protection for Accesses to Peripheral RAMs

Accesses to some peripheral RAMs are protected by odd/even parity checking. During a read access the parity is calculated based on the data read from the peripheral RAM and compared with the good parity value stored in the parity RAM for that peripheral. If any word fails the parity check, the module generates a parity error signal that is mapped to the Error Signaling Module. The module also captures the peripheral RAM address that caused the parity error.

The parity protection for peripheral RAMs is not enabled by default and must be enabled by the application. Each individual peripheral contains control registers to enable the parity protection for accesses to its RAM.

**NOTE**

The CPU read access gets the actual data from the peripheral. The application can choose to generate an interrupt whenever a peripheral RAM parity error is detected.

## 6.13 On-Chip SRAM Initialization and Testing

### *6.13.1 On-Chip SRAM Self-Test Using PBIST*

#### 6.13.1.1 Features

- Extensive instruction set to support various memory test algorithms
- ROM-based algorithms allow application to run TI production-level memory tests
- Independent testing of all on-chip SRAM

#### 6.13.1.2 PBIST RAM Groups

**Table 6-25. PBIST RAM Grouping**

| Memory | RAM Group | Test Clock | MEM Type | Test Pattern (Algorithm) | | | |
|---|---|---|---|---|---|---|---|
| | | | | triple read slow read | triple read fast read | March 13N(1) two port (cycles) | March 13N(1) single port (cycles) |
| | | | | ALGO MASK 0x1 | ALGO MASK 0x2 | ALGO MASK 0x4 | ALGO MASK 0x8 |
| PBIST_ROM | 1 | ROM CLK | ROM | 24578 | 8194 | | |
| STC_ROM | 2 | ROM CLK | ROM | 19586 | 6530 | | |
| DCAN1 | 3 | VCLK | Dual Port | | | 25200 | |
| DCAN2 | 4 | VCLK | Dual Port | | | 25200 | |
| DCAN3 | 5 | VCLK | Dual Port | | | 25200 | |
| ESRAM1(2) | 6 | HCLK | Single Port | | | | 266280 |
| MIBSPI1 | 7 | VCLK | Dual Port | | | 33440 | |
| MIBSPI3 | 8 | VCLK | Dual Port | | | 33440 | |
| MIBSPI5 | 9 | VCLK | Dual Port | | | 33440 | |
| VIM | 10 | VCLK | Dual Port | | | 12560 | |
| MIBADC1 | 11 | VCLK | Dual Port | | | 4200 | |
| DMA | 12 | HCLK | Dual Port | | | 18960 | |
| N2HET1 | 13 | VCLK | Dual Port | | | 31680 | |
| HTU1 | 14 | VCLK | Dual Port | | | 6480 | |
| MIBADC2 | 18 | VCLK | Dual Port | | | 4200 | |
| N2HET2 | 19 | VCLK | Dual Port | | | 31680 | |
| HTU2 | 20 | VCLK | Dual Port | | | 6480 | |
| ESRAM5(3) | 21 | HCLK | Single Port | | | | 266280 |
| ESRAM6(4) | 22 | HCLK | Single Port | | | | 266280 |

(1) There are several memory testing algorithms stored in the PBIST ROM. However, TI recommends the March13N algorithm for application testing.
(2) ESRAM1: Address 0x08000000 - 0x0800FFFF
(3) ESRAM5: Address 0x08010000 - 0x0801FFFF
(4) ESRAM6: Address 0x08020000 - 0x0802FFFF

The PBIST ROM clock frequency is limited to 100MHz, if 100MHz < HCLK <= HCLKmax, or HCLK, if HCLK <= 100MHz.

The PBIST ROM clock is divided down from HCLK. The divider is selected by programming the ROM_DIV field of the Memory Self-Test Global Control Register (MSTGCR) at address 0xFFFFFF58.

### 6.13.2 On-Chip SRAM Auto Initialization

This microcontroller allows some of the on-chip memories to be initialized through the Memory Hardware Initialization mechanism in the System module. This hardware mechanism allows an application to program the memory arrays with error detection capability to a known state based on their error detection scheme (odd/even parity or ECC).

The MINITGCR register enables the memory initialization sequence, and the MSINENA register selects the memories that are to be initialized.

For more information on these registers see TMS570LS12x/11x Technical Reference Manual (SPNU515).

The mapping of the different on-chip memories to the specific bits of the MSINENA registers is shown in Table 6-26.

**Table 6-26. Memory Initialization**

| CONNECTING MODULE | ADDRESS RANGE | | MSINENA REGISTER BIT # |
|---|---|---|---|
| | BASE ADDRESS | ENDING ADDRESS | |
| RAM (PD#1) | 0x08000000 | 0x0800FFFF | 0(1) |
| RAM (RAM_PD#1) | 0x08010000 | 0x0801FFFF | 0(1) |
| RAM (RAM_PD#2) | 0x08020000 | 0x0802FFFF | 0(1) |
| MIBSPI5 RAM | 0xFF0A0000 | 0xFF0BFFFF | 12(2) |
| MIBSPI3 RAM | 0xFF0C0000 | 0xFF0DFFFF | 11(2) |
| MIBSPI1 RAM | 0xFF0E0000 | 0xFF0FFFFF | 7(2) |
| DCAN3 RAM | 0xFF1A0000 | 0xFF1BFFFF | 10 |
| DCAN2 RAM | 0xFF1C0000 | 0xFF1DFFFF | 6 |
| DCAN1 RAM | 0xFF1E0000 | 0xFF1FFFFF | 5 |
| MIBADC2 RAM | 0xFF3A0000 | 0xFF3BFFFF | 14 |
| MIBADC1 RAM | 0xFF3E0000 | 0xFF3FFFFF | 8 |
| N2HET2 RAM | 0xFF440000 | 0xFF45FFFF | 15 |
| N2HET1 RAM | 0xFF460000 | 0xFF47FFFF | 3 |
| HTU2 RAM | 0xFF4C0000 | 0xFF4DFFFF | 16 |
| HTU1 RAM | 0xFF4E0000 | 0xFF4FFFFF | 4 |
| DMA RAM | 0xFFF80000 | 0xFFF80FFF | 1 |
| VIM RAM | 0xFFF82000 | 0xFFF82FFF | 2 |

(1) The TCM RAM interface module has separate control bits to select the RAM power domain that is to be auto-initialized.
(2) The MibSPIx modules perform an initialization of the transmit and receive RAMs as soon as the module is released from its local reset.. This is independent of whether the application chooses to initialize the MibSPIx RAMs using the system module auto-initialization method. The MibSPIx module must be first brought out of its local reset in order to use the system module auto-initialization method.

## 6.14 External Memory Interface (EMIF)

### 6.14.1 Features

The EMIF includes many features to enhance the ease and flexibility of connecting to external asynchronous memories or SDRAM devices. The EMIF features includes support for:

- 3 addressable chip select for asynchronous memories of up to 32KB each
- 1 addressable chip select space for SDRAMs up to 128MB
- 8 or 16-bit data bus width
- Programmable cycle timings such as setup, strobe, and hold times as well as turnaround time
- Select strobe mode
- Extended Wait mode
- Data bus parking

### 6.14.2 Electrical and Timing Specifications

#### 6.14.2.1 Asynchronous RAM

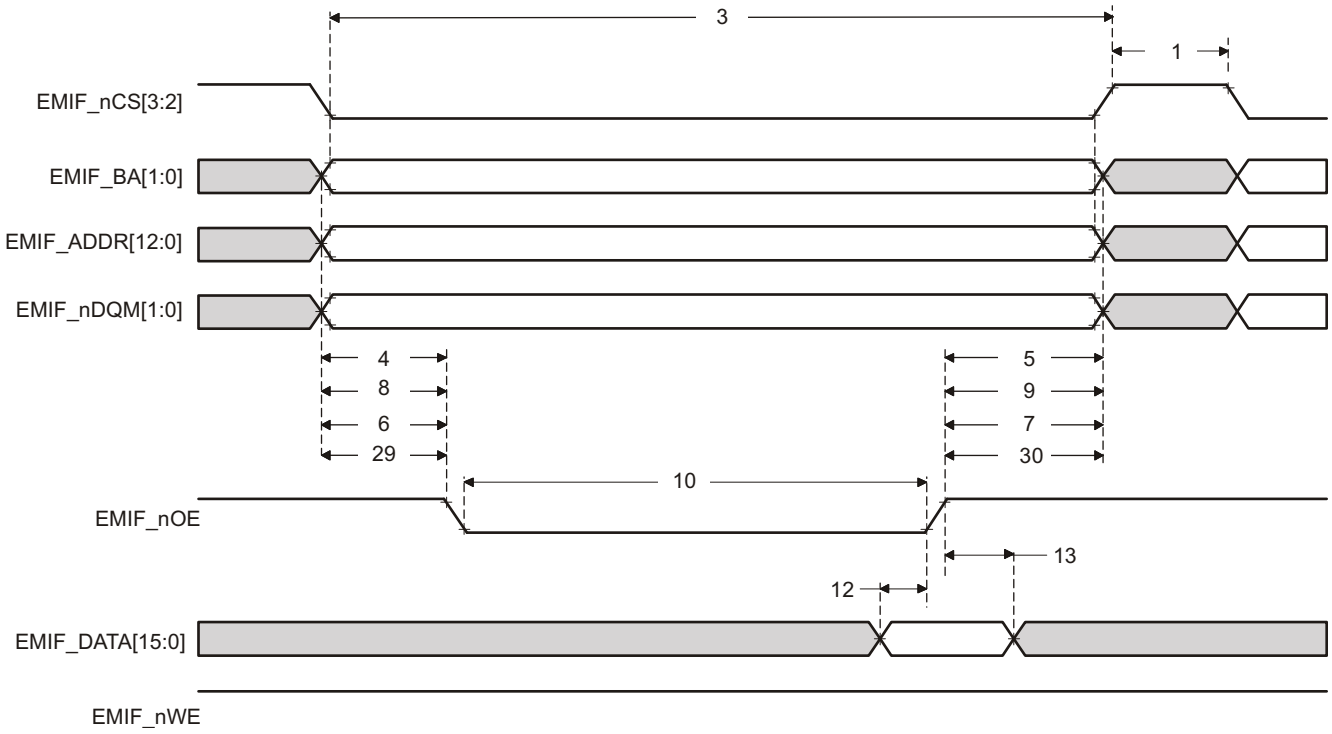



**Figure 6-11. Asynchronous Memory Read Timing**

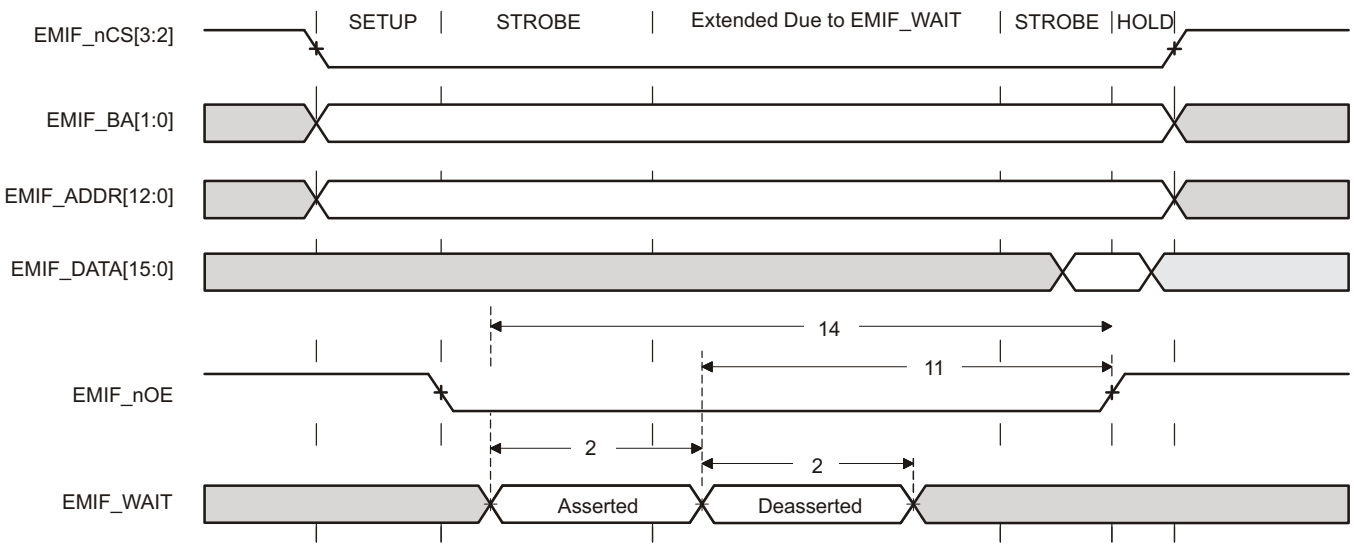



**Figure 6-12. EMIFnWAIT Read Timing Requirements**

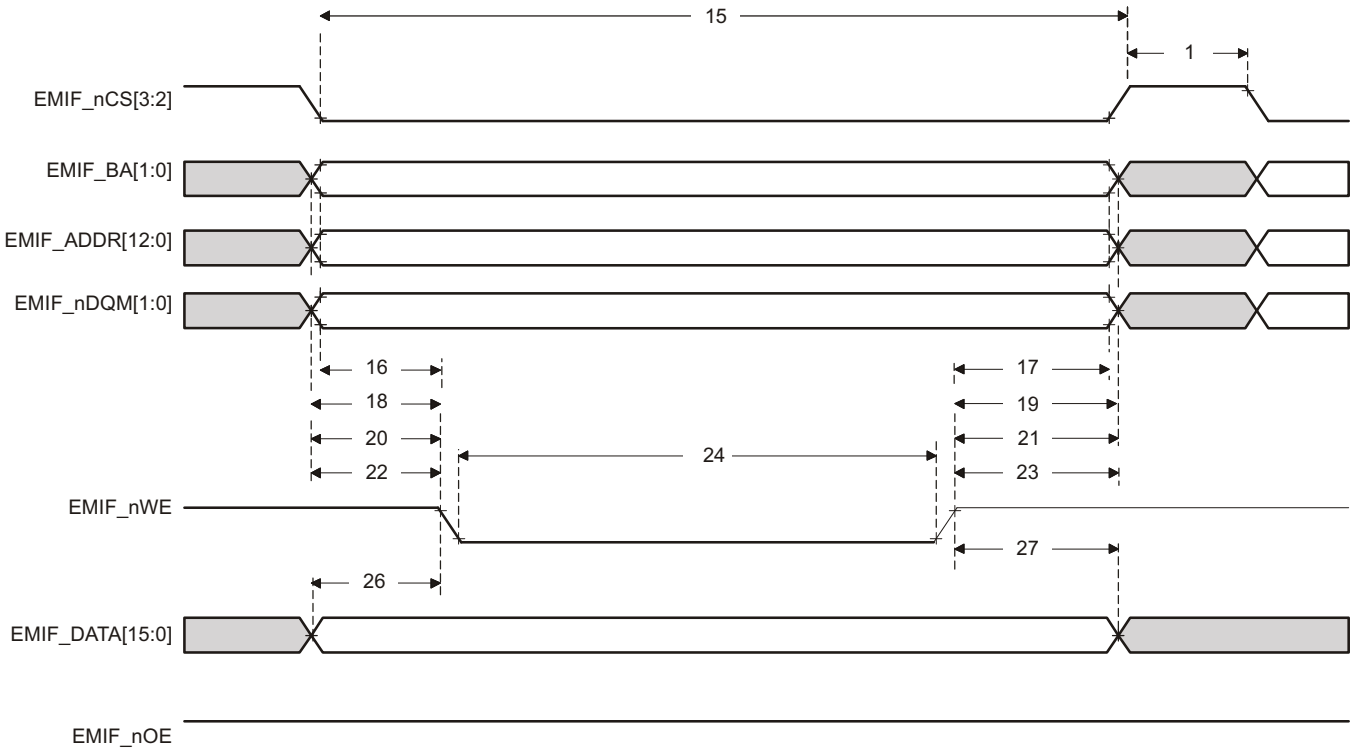



**Figure 6-13. Asynchronous Memory Write Timing**

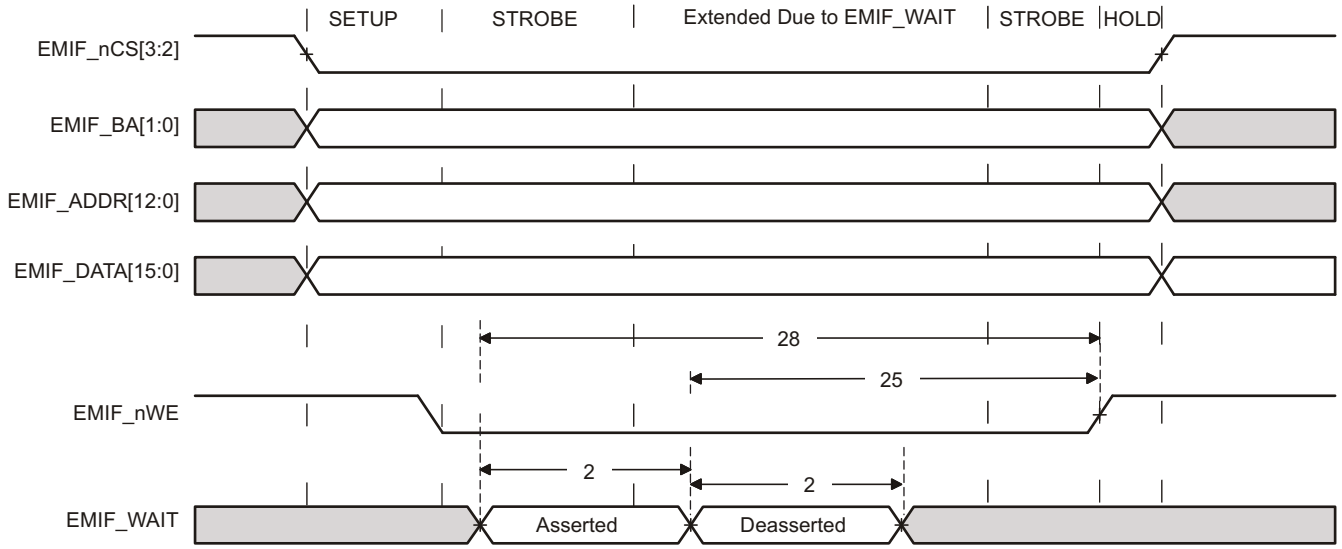



**Figure 6-14. EMIFnWAIT Write Timing Requirements**

**Table 6-27. EMIF Asynchronous Memory Timing Requirements(1)**

| NO. | | | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | |
| **Reads and Writes** | | | | | | |
| | E | EMIF clock period | 11 | | | ns |
| 2 | $t_{w(EM\_WAIT)}$ | Pulse duration, EMIF_nWAIT assertion and deassertion | 2E | | | ns |
| **Reads** | | | | | | |
| 12 | $t_{su(EMDV-EMOEH)}$ | Setup time, EMIF_DATA[15:0] valid before EMIFnOE high | 9 | | | ns |
| 13 | $t_{h(EMOEH-EMDIV)}$ | Hold time, EMIF_DATA[15:0] valid after EMIF_nOE high | 0 | | | ns |
| 14 | $t_{su(EMOEL-EMWAIT)}$ | Setup Time, EMIF_nWAIT asserted before end of Strobe Phase(2) | 4E+9 | | | ns |
| **Writes** | | | | | | |
| 28 | $t_{su(EMWEL-EMWAIT)}$ | Setup Time, EMIF_nWAIT asserted before end of Strobe Phase(2) | 4E+14 | | | ns |

(1) E = EMIF_CLK period in ns.
(2) Setup before end of STROBE phase (if no extended wait states are inserted) by which EMIFnWAIT must be asserted to add extended wait states. Figure 6-12 and Figure 6-14 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

## Table 6-28. EMIF Asynchronous Memory Switching Characteristics[1][2][3]

| NO | PARAMETER | | Value | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | |
| **Reads and Writes** | | | | | | |
| 1 | $t_{d(TURNAROUND)}$ | Turnaround time | (TA)*E - 4 | (TA)*E | (TA)*E + 3 | ns |
| **Reads** | | | | | | |
| 3 | $t_{c(EMRCYCLE)}$ | EMIF read cycle time (EW = 0) | (RS+RST+RH)*E -3 | (RS+RST+RH)*E | (RS+RST+RH)*E + 3 | ns |
| | | EMIF read cycle time (EW = 1) | (RS+RST+RH+(EWC*16))*E -3 | (RS+RST+RH+(EWC*16))*E | (RS+RST+RH+(EWC*16))*E + 3 | ns |
| 4 | $t_{su(EMCEL-EMOEL)}$ | Output setup time, EMIF_nCS[4:2] low to EMIF_nOE low (SS = 0) | (RS)*E-6 | (RS)*E | (RS)*E+3 | ns |
| | | Output setup time, EMIF_nCS[4:2] low to EMIF_nOE low (SS = 1) | -6 | 0 | +3 | ns |
| 5 | $t_{h(EMOEH-EMCEH)}$ | Output hold time, EMIF_nOE high to EMIF_nCS[4:2] high (SS = 0) | (RH)*E -3 | (RH)*E | (RH)*E + 5 | ns |
| | | Output hold time, EMIF_nOE high to EMIF_nCS[4:2] high (SS = 1) | -3 | 0 | +5 | ns |
| 6 | $t_{su(EMBAV-EMOEL)}$ | Output setup time, EMIF_BA[1:0] valid to EMIF_nOE low | (RS)*E-6 | (RS)*E | (RS)*E+3 | ns |
| 7 | $t_{h(EMOEH-EMBAIV)}$ | Output hold time, EMIF_nOE high to EMIF_BA[1:0] invalid | (RH)*E-3 | (RH)*E | (RH)*E+5 | ns |
| 8 | $t_{su(EMAV-EMOEL)}$ | Output setup time, EMIF_ADDR[12:0] valid to EMIFnOE low | (RS)*E-6 | (RS)*E | (RS)*E+3 | ns |
| 9 | $t_{h(EMOEH-EMAIV)}$ | Output hold time, EMIF_nOE high to EMIF_ADDR[12:0] invalid | (RH)*E-3 | (RH)*E | (RH)*E+5 | ns |
| 10 | $t_{w(EMOEL)}$ | EMIF_nOE active low width (EW = 0) | (RST)*E-3 | (RST)*E | (RST)*E+3 | ns |
| | | EMIF_nOE active low width (EW = 1) | (RST+(EWC*16)) *E-3 | (RST+(EWC*16))*E | (RST+(EWC*16)) *E+3 | ns |
| 11 | $t_{d(EMWAITH-EMOEH)}$ | Delay time from EMIF_nWAIT deasserted to EMIF_nOE high | 3E+9 | 4E | 4E+20 | ns |
| 29 | $t_{su(EMDQMV-EMOEL)}$ | Output setup time, EMIF_nDQM[1:0] valid to EMIF_nOE low | (RS)*E-6 | (RS)*E | (RS)*E+3 | ns |
| 30 | $t_{h(EMOEH-EMDQMIV)}$ | Output hold time, EMIF_nOE high to EMIF_nDQM[1:0] invalid | (RH)*E-3 | (RH)*E | (RH)*E+5 | ns |
| **Writes** | | | | | | |
| 15 | $t_{c(EMWCYCLE)}$ | EMIF write cycle time (EW = 0) | (WS+WST+WH)* E-3 | (WS+WST+WH)*E | (WS+WST+WH)* E+3 | ns |
| | | EMIF write cycle time (EW = 1) | (WS+WST+WH+( EWC*16))*E -3 | (WS+WST+WH+(E WC*16))*E | (WS+WST+WH+( EWC*16))*E + 3 | ns |

(1) TA = Turnaround, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed through the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers. These support the following ranges of values: TA[4–1], RS[16–1], RST[64–1], RH[8–1], WS[16–1], WST[64–1], WH[8–1], and MEWC[1–256]. See the TMS570LS12x/11x Technical Reference Manual (SPNU515) for more information.
(2) E = EMIF_CLK period in ns.
(3) EWC = external wait cycles determined by EMIF_nWAIT input signal. EWC supports the following range of values. EWC[256–1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register. See the TMS570LS12x/11x Technical Reference Manual (SPNU515) for more information.

**Table 6-28. EMIF Asynchronous Memory Switching Characteristics[1][2][3] (continued)**

| NO | PARAMETER | | Value | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | |
| 16 | $t_{su(EMCEL-EMWEL)}$ | Output setup time, EMIF_nCS[4:2] low to EMIF_nWE low (SS = 0) | (WS)*E -3 | (WS)*E | (WS)*E + 3 | ns |
| | | Output setup time, EMIF_nCS[4:2] low to EMIF_nWE low (SS = 1) | -3 | 0 | +3 | ns |
| 17 | $t_{h(EMWEH-EMCEH)}$ | Output hold time, EMIF_nWE high to EMIF_nCS[4:2] high (SS = 0) | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |
| | | Output hold time, EMIF_nWE high to EMIF_CS[4:2] high (SS = 1) | -3 | 0 | +3 | ns |
| 18 | $t_{su(EMDQMV-EMWEL)}$ | Output setup time, EMIF_BA[1:0] valid to EMIF_nWE low | (WS)*E-3 | (WS)*E | (WS)*E+3 | ns |
| 19 | $t_{h(EMWEH-EMDQMIV)}$ | Output hold time, EMIF_nWE high to EMIF_BA[1:0] invalid | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |
| 20 | $t_{su(EMBAV-EMWEL)}$ | Output setup time, EMIF_BA[1:0] valid to EMIF_nWE low | (WS)*E-3 | (WS)*E | (WS)*E+3 | ns |
| 21 | $t_{h(EMWEH-EMBAIV)}$ | Output hold time, EMIF_nWE high to EMIF_BA[1:0] invalid | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |
| 22 | $t_{su(EMAV-EMWEL)}$ | Output setup time, EMIF_ADDR[12:0] valid to EMIF_nWE low | (WS)*E-3 | (WS)*E | (WS)*E+3 | ns |
| 23 | $t_{h(EMWEH-EMAIV)}$ | Output hold time, EMIF_nWE high to EMIF_ADDR[12:0] invalid | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |
| 24 | $t_{w(EMWEL)}$ | EMIF_nWE active low width (EW = 0) | (WST)*E-3 | (WST)*E | (WST)*E+3 | ns |
| | | EMIF_nWE active low width (EW = 1) | (WST+(EWC*16)) *E-3 | (WST+(EWC*16))*E | (WST+(EWC*16)) *E+3 | ns |
| 25 | $t_{d(EMWAITH-EMWEH)}$ | Delay time from EMIF_nWAIT deasserted to EMIF_nWE high | 3E+11 | 4E | 4E+24 | ns |
| 26 | $t_{su(EMDV-EMWEL)}$ | Output setup time, EMIF_DATA[15:0] valid to EMIF_nWE low | (WS)*E-3 | (WS)*E | (WS)*E+3 | ns |
| 27 | $t_{h(EMWEH-EMDIV)}$ | Output hold time, EMIF_nWE high to EMIF_DATA[15:0] invalid | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |
| 31 | $t_{su(EMDQMV-EMWEL)}$ | Output setup time, EMIF_nDQM[1:0] valid to EMIF_nWE low | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |
| 32 | $t_{h(EMWEH-EMDQMIV)}$ | Output hold time, EMIF_nWE high to EMIF_nDQM[1:0] invalid | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |

### 6.14.2.2 Synchronous Timing

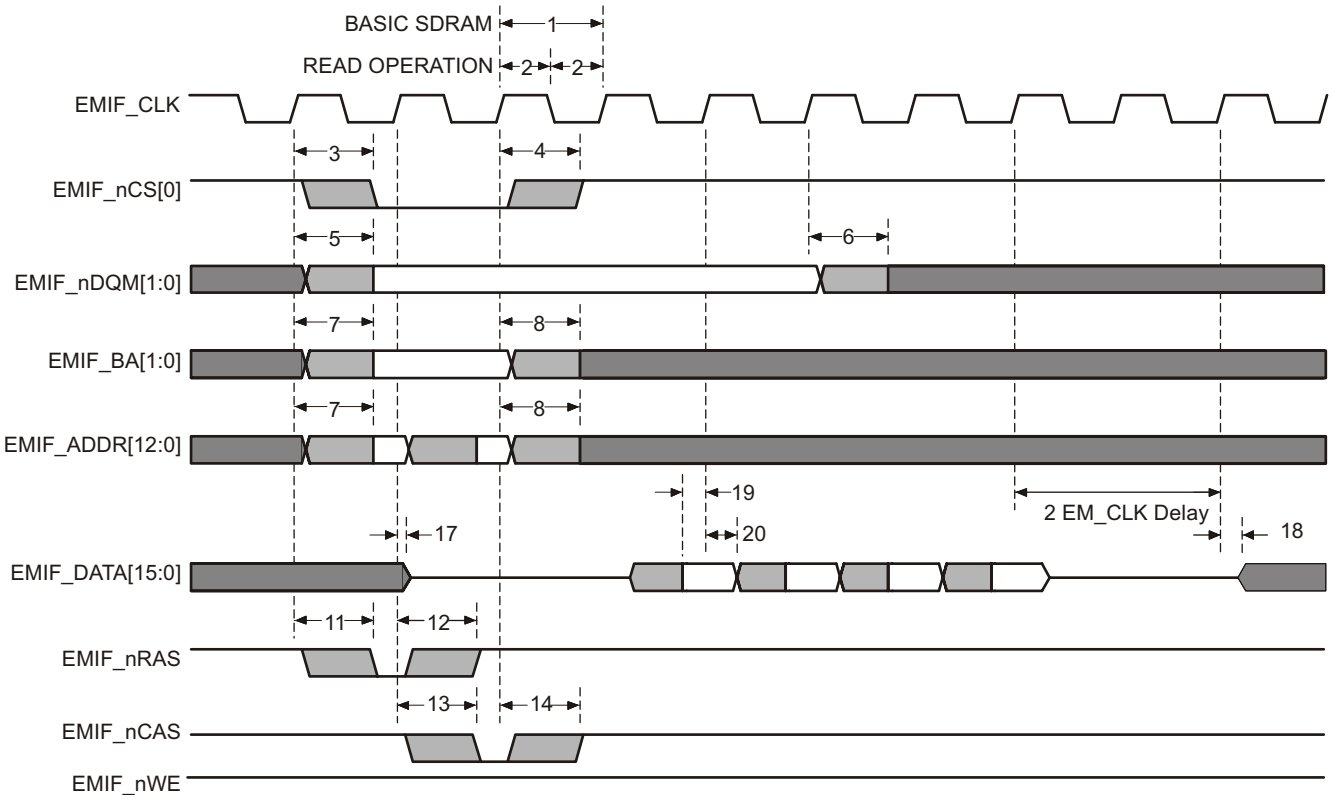



**Figure 6-15. Basic SDRAM Read Operation**

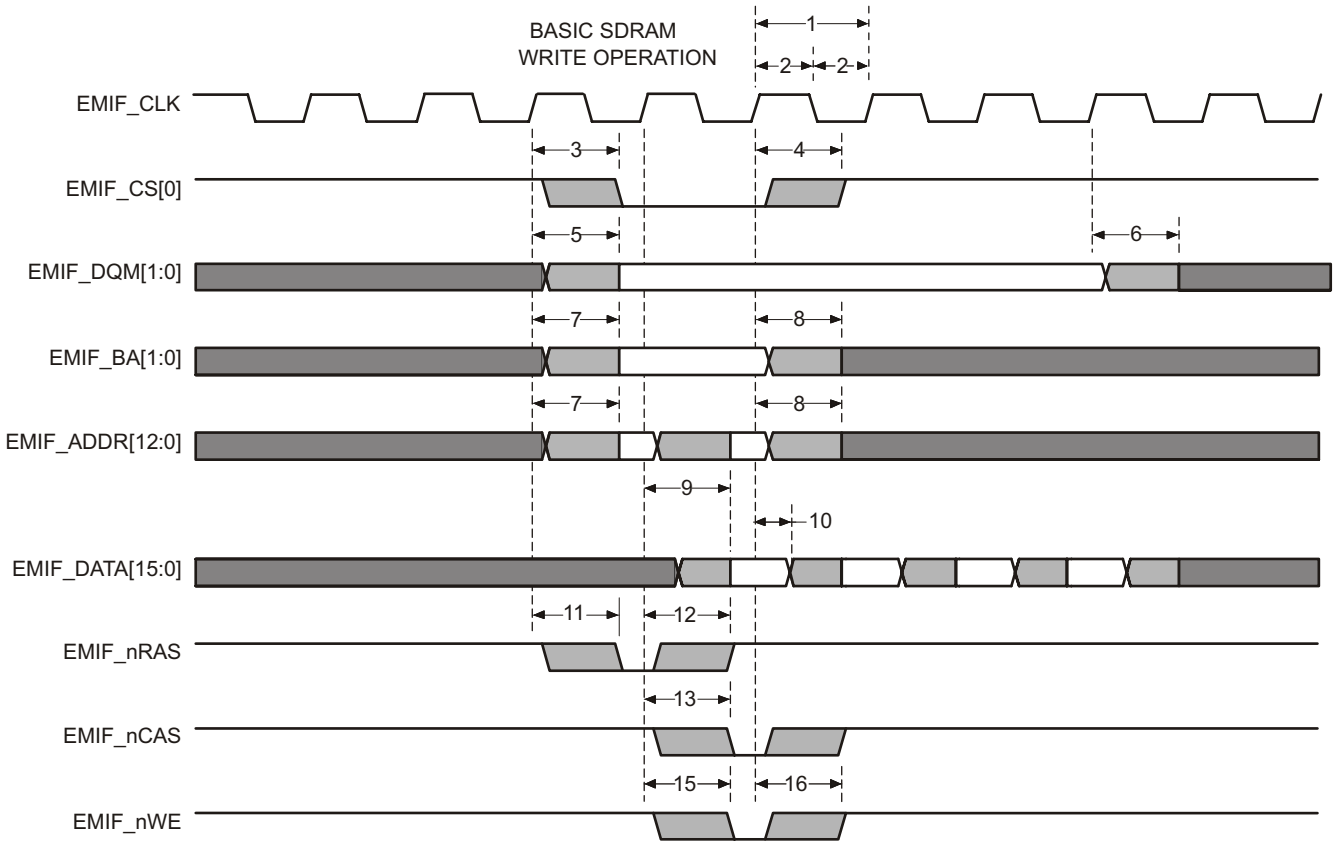



**Figure 6-16. Basic SDRAM Write Operation**

**Table 6-29. EMIF Synchronous Memory Timing Requirements**

| NO. | Parameter | | MIN | MAX | Unit |
|---|---|---|---|---|---|
| 19 | $t_{su(EMIFDV-EM\_CLKH)}$ | Input setup time, read data valid on EMIF_DATA[15:0] before EMIF_CLK rising | 2 | | ns |
| 20 | $t_{h(CLKH-DIV)}$ | Input hold time, read data valid on EMIF_DATA[15:0] after EMIF_CLK rising | 2 | | ns |

**Table 6-30. EMIF Synchronous Memory Switching Characteristics**

| NO. | Parameter | | MIN | MAX | Unit |
|---|---|---|---|---|---|
| 1 | $t_{c(CLK)}$ | Cycle time, EMIF clock EMIF_CLK | 22 | | ns |
| 2 | $t_{w(CLK)}$ | Pulse width, EMIF clock EMIF_CLK high or low | 5 | | ns |
| 3 | $t_{d(CLKH-CSV)}$ | Delay time, EMIF_CLK rising to EMIF_nCS[0] valid | | 13 | ns |
| 4 | $t_{oh(CLKH-CSIV)}$ | Output hold time, EMIF_CLK rising to EMIF_nCS[0] invalid | 1 | | ns |
| 5 | $t_{d(CLKH-DQMV)}$ | Delay time, EMIF_CLK rising to EMIF_nDQM[1:0] valid | | 13 | ns |
| 6 | $t_{oh(CLKH-DQMIV)}$ | Output hold time, EMIF_CLK rising to EMIF_nDQM[1:0] invalid | 1 | | ns |
| 7 | $t_{d(CLKH-AV)}$ | Delay time, EMIF_CLK rising to EMIF_ADDR[12:0] and EMIFBA[1:0] valid | | 13 | ns |

**Table 6-30. EMIF Synchronous Memory Switching Characteristics (continued)**

| NO. | Parameter | | MIN | MAX | Unit |
|---|---|---|---|---|---|
| 8 | $t_{oh(CLKH-AIV)}$ | Output hold time, EMIF_CLK rising to EMIF_ADDR[12:0] and EMIF_BA[1:0] invalid | 1 | | ns |
| 9 | $t_{d(CLKH-DV)}$ | Delay time, EMIF_CLK rising to EMIF_DATA[15:0] valid | | 13 | ns |
| 10 | $t_{oh(CLKH-DIV)}$ | Output hold time, EMIF_CLK rising to EMIF_DATA[15:0] invalid | 1 | | ns |
| 11 | $t_{d(CLKH-RASV)}$ | Delay time, EMIF_CLK rising to EMIF_nRAS valid | | 13 | ns |
| 12 | $t_{oh(CLKH-RASIV)}$ | Output hold time, EMIF_CLK rising to EMIF_nRAS invalid | 1 | | ns |
| 13 | $t_{d(CLKH-CASV)}$ | Delay time, EMIF_CLK rising to EMIF_nCAS valid | | 13 | ns |
| 14 | $t_{oh(CLKH-CASIV)}$ | Output hold time, EMIF_CLK rising to EMIF_nCAS invalid | 1 | | ns |
| 15 | $t_{d(CLKH-WEV)}$ | Delay time, EMIF_CLK rising to EMIF_nWE valid | | 13 | ns |
| 16 | $t_{oh(CLKH-WEIV)}$ | Output hold time, EMIF_CLK rising to EMIF_nWE invalid | 1 | | ns |
| 17 | $t_{dis(CLKH-DHZ)}$ | Delay time, EMIF_CLK rising to EMIF_DATA[15:0] tri-stated | | 7 | ns |
| 18 | $t_{ena(CLKH-DLZ)}$ | Output hold time, EMIF_CLK rising to EMIF_DATA[15:0] driving | 1 | | ns |

## 6.15 Vectored Interrupt Manager

The vectored interrupt manager (VIM) provides hardware assistance for prioritizing and controlling the many interrupt sources present on this device. Interrupts are caused by events outside of the normal flow of program execution. Normally, these events require a timely response from the central processing unit (CPU); therefore, when an interrupt occurs, the CPU switches execution from the normal program flow to an interrupt service routine (ISR).

### 6.15.1 VIM Features

The VIM module has the following features:

- Supports 128 interrupt channels.
  - Provides programmable priority and enable for interrupt request lines.
- Provides a direct hardware dispatch mechanism for fastest IRQ dispatch.
- Provides two software dispatch mechanisms when the CPU VIC port is not used.
  - Index interrupt
  - Register vectored interrupt
- Parity protected vector interrupt table against soft errors.

### 6.15.2 Interrupt Request Assignments

**Table 6-31. Interrupt Request Assignments**

| Modules | Interrupt Sources | Default VIM Interrupt Channel |
|---|---|---|
| ESM | ESM High level interrupt (NMI) | 0 |
| Reserved | Reserved | 1 |
| RTI | RTI compare interrupt 0 | 2 |
| RTI | RTI compare interrupt 1 | 3 |
| RTI | RTI compare interrupt 2 | 4 |
| RTI | RTI compare interrupt 3 | 5 |
| RTI | RTI overflow interrupt 0 | 6 |
| RTI | RTI overflow interrupt 1 | 7 |
| RTI | RTI timebase interrupt | 8 |
| GIO | GIO interrupt A | 9 |
| N2HET1 | N2HET1 level 0 interrupt | 10 |
| HTU1 | HTU1 level 0 interrupt | 11 |
| MIBSPI1 | MIBSPI1 level 0 interrupt | 12 |
| LIN | LIN level 0 interrupt | 13 |
| MIBADC1 | MIBADC1 event group interrupt | 14 |
| MIBADC1 | MIBADC1 sw group 1 interrupt | 15 |
| DCAN1 | DCAN1 level 0 interrupt | 16 |
| SPI2 | SPI2 level 0 interrupt | 17 |
| Reserved | Reserved | 18 |
| CRC | CRC Interrupt | 19 |
| ESM | ESM Low level interrupt | 20 |
| SYSTEM | Software interrupt (SSI) | 21 |
| CPU | PMU Interrupt | 22 |
| GIO | GIO interrupt B | 23 |
| N2HET1 | N2HET1 level 1 interrupt | 24 |
| HTU1 | HTU1 level 1 interrupt | 25 |
| MIBSPI1 | MIBSPI1 level 1 interrupt | 26 |

**Table 6-31. Interrupt Request Assignments (continued)**

| Modules | Interrupt Sources | Default VIM Interrupt Channel |
|---|---|---|
| LIN | LIN level 1 interrupt | 27 |
| MIBADC1 | MIBADC1 sw group 2 interrupt | 28 |
| DCAN1 | DCAN1 level 1 interrupt | 29 |
| SPI2 | SPI2 level 1 interrupt | 30 |
| MIBADC1 | MIBADC1 magnitude compare interrupt | 31 |
| Reserved | Reserved | 32 |
| DMA | FTCA interrupt | 33 |
| DMA | LFSA interrupt | 34 |
| DCAN2 | DCAN2 level 0 interrupt | 35 |
| Reserved | Reserved | 36 |
| MIBSPI3 | MIBSPI3 level 0 interrupt | 37 |
| MIBSPI3 | MIBSPI3 level 1 interrupt | 38 |
| DMA | HBCA interrupt | 39 |
| DMA | BTCA interrupt | 40 |
| EMIF | AEMIFINT3 | 41 |
| DCAN2 | DCAN2 level 1 interrupt | 42 |
| Reserved | Reserved | 43 |
| DCAN1 | DCAN1 IF3 interrupt | 44 |
| DCAN3 | DCAN3 level 0 interrupt | 45 |
| DCAN2 | DCAN2 IF3 interrupt | 46 |
| FPU | FPU interrupt | 47 |
| Reserved | Reserved | 48 |
| SPI4 | SPI4 level 0 interrupt | 49 |
| MIBADC2 | MibADC2 event group interrupt | 50 |
| MIBADC2 | MibADC2 sw group1 interrupt | 51 |
| Reserved | Reserved | 52 |
| MIBSPI5 | MIBSPI5 level 0 interrupt | 53 |
| SPI4 | SPI4 level 1 interrupt | 54 |
| DCAN3 | DCAN3 level 1 interrupt | 55 |
| MIBSPI5 | MIBSPI5 level 1 interrupt | 56 |
| MIBADC2 | MibADC2 sw group2 interrupt | 57 |
| Reserved | Reserved | 58 |
| MIBADC2 | MibADC2 magnitude compare interrupt | 59 |
| DCAN3 | DCAN3 IF3 interrupt | 60 |
| FMC | FSM_DONE interrupt | 61 |
| Reserved | Reserved | 62 |
| N2HET2 | N2HET2 level 0 interrupt | 63 |
| SCI | SCI level 0 interrupt | 64 |
| HTU2 | HTU2 level 0 interrupt | 65 |
| I2C | I2C level 0 interrupt | 66 |
| Reserved | Reserved | 67-72 |
| N2HET2 | N2HET2 level 1 interrupt | 73 |
| SCI | SCI level 1 interrupt | 74 |
| HTU2 | HTU2 level 1 interrupt | 75 |
| Reserved | Reserved | 76-79 |
| HWAG1 | HWA_INT_REQ_H | 80 |
| HWAG2 | HWA_INT_REQ_H | 81 |

**Table 6-31. Interrupt Request Assignments (continued)**

| Modules | Interrupt Sources | Default VIM Interrupt Channel |
|---|---|---|
| DCC1 | DCC done interrupt | 82 |
| DCC2 | DCC2 done interrupt | 83 |
| Reserved | Reserved | 84 |
| PBIST Controller | PBIST Done Interrupt | 85 |
| Reserved | Reserved | 86-87 |
| HWAG1 | HWA_INT_REQ_L | 88 |
| HWAG2 | HWA_INT_REQ_L | 89 |
| ePWM1INTn | ePWM1 Interrupt | 90 |
| ePWM1TZINTn | ePWM1 Trip Zone Interrupt | 91 |
| ePWM2INTn | ePWM2 Interrupt | 92 |
| ePWM2TZINTn | ePWM2 Trip Zone Interrupt | 93 |
| ePWM3INTn | ePWM3 Interrupt | 94 |
| ePWM3TZINTn | ePWM3 Trip Zone Interrupt | 95 |
| ePWM4INTn | ePWM4 Interrupt | 96 |
| ePWM4TZINTn | ePWM4 Trip Zone Interrupt | 97 |
| ePWM5INTn | ePWM5 Interrupt | 98 |
| ePWM5TZINTn | ePWM5 Trip Zone Interrupt | 99 |
| ePWM6INTn | ePWM6 Interrupt | 100 |
| ePWM6TZINTn | ePWM6 Trip Zone Interrupt | 101 |
| ePWM7INTn | ePWM7 Interrupt | 102 |
| ePWM7TZINTn | ePWM7 Trip Zone Interrupt | 103 |
| eCAP1INTn | eCAP1 Interrupt | 104 |
| eCAP2INTn | eCAP2 Interrupt | 105 |
| eCAP3INTn | eCAP3 Interrupt | 106 |
| eCAP4INTn | eCAP4 Interrupt | 107 |
| eCAP5INTn | eCAP5 Interrupt | 108 |
| eCAP6INTn | eCAP6 Interrupt | 109 |
| eQEP1INTn | eQEP1 Interrupt | 110 |
| eQEP2INTn | eQEP2 Interrupt | 111 |
| Reserved | Reserved | 112-127 |

**NOTE**

Address location 0x00000000 in the VIM RAM is reserved for the phantom interrupt ISR entry; therefore only request channels 0..126 can be used and are offset by 1 address in the VIM RAM.

**NOTE**

The EMIF_nWAIT signal has a pull-up on it. The EMIF module generates a "Wait Rise" interrupt whenever it detects a rising edge on the EMIF_nWAIT signal. This interrupt condition is indicated as soon as the device is powered up. This can be ignored if the EMIF_nWAIT signal is not used in the application. If the EMIF_nWAIT signal is actually used in the application, then the external slave memory must always drive the EMIF_nWAIT signal such that an interrupt is not caused due to the default pull-up on this signal.

**NOTE**

The lower-order interrupt channels are higher priority channels than the higher-order interrupt channels.

**NOTE**

The application can change the mapping of interrupt sources to the interrupt channels through the interrupt channel control registers (CHANCTRLx) inside the VIM module.

## 6.16 DMA Controller

The DMA controller is used to transfer data between two locations in the memory map in the background of CPU operations. Typically, the DMA is used to:

- Transfer blocks of data between external and internal data memories
- Restructure portions of internal data memory
- Continually service a peripheral

### *6.16.1 DMA Features*

- CPU independent data transfer
- One 64-bit master port that interfaces to the Memory System.
- FIFO buffer(4 entries deep and each 64bit wide)
- Channel control information is stored in RAM protected by parity
- 16 channels with individual enable
- Channel chaining capability
- 32 peripheral DMA requests
- Hardware and Software DMA requests
- 8, 16, 32 or 64-bit transactions supported
- Multiple addressing modes for source/destination (fixed, increment, offset)
- Auto-initiation
- Power-management mode
- Memory Protection with four configurable memory regions

### 6.16.2 Default DMA Request Map

The DMA module on this microcontroller has 16 channels and up to 32 hardware DMA requests. The module contains DREQASIx registers which are used to map the DMA requests to the DMA channels. By default, channel 0 is mapped to request 0, channel 1 to request 1, and so on.

Some DMA requests have multiple sources, as shown in Table 6-32. The application must ensure that only one of these DMA request sources is enabled at any time.

**Table 6-32. DMA Request Line Connection**

| Modules | DMA Request Sources | DMA Request |
|---|---|---|
| MIBSPI1 | MIBSPI1[1](1) | DMAREQ[0] |
| MIBSPI1 | MIBSPI1[0](2) | DMAREQ[1] |
| SPI2 | SPI2 receive | DMAREQ[2] |
| SPI2 | SPI2 transmit | DMAREQ[3] |
| MIBSPI1 / MIBSPI3 / DCAN2 | MIBSPI1[2] / MIBSPI3[2] / DCAN2 IF3 | DMAREQ[4] |
| MIBSPI1 / MIBSPI3 / DCAN2 | MIBSPI1[3] / MIBSPI3[3] / DCAN2 IF2 | DMAREQ[5] |
| DCAN1 / MIBSPI5 | DCAN1 IF2 / MIBSPI5[2] | DMAREQ[6] |
| MIBADC1 / MIBSPI5 | MIBADC1 event / MIBSPI5[3] | DMAREQ[7] |
| MIBSPI1 / MIBSPI3 / DCAN1 | MIBSPI1[4] / MIBSPI3[4] / DCAN1 IF1 | DMAREQ[8] |
| MIBSPI1 / MIBSPI3 / DCAN2 | MIBSPI1[5] / MIBSPI3[5] / DCAN2 IF1 | DMAREQ[9] |
| MIBADC1 / I2C / MIBSPI5 | MIBADC1 G1 / I2C receive / MIBSPI5[4] | DMAREQ[10] |
| MIBADC1 / I2C / MIBSPI5 | MIBADC1 G2 / I2C transmit / MIBSPI5[5] | DMAREQ[11] |
| RTI / MIBSPI1 / MIBSPI3 | RTI DMAREQ0 / MIBSPI1[6] / MIBSPI3[6] | DMAREQ[12] |
| RTI / MIBSPI1 / MIBSPI3 | RTI DMAREQ1 / MIBSPI1[7] / MIBSPI3[7] | DMAREQ[13] |
| MIBSPI3 / MibADC2 / MIBSPI5 | MIBSPI3[1](1) / MibADC2 event / MIBSPI5[6] | DMAREQ[14] |
| MIBSPI3 / MIBSPI5 | MIBSPI3[0](2) / MIBSPI5[7] | DMAREQ[15] |
| MIBSPI1 / MIBSPI3 / DCAN1 / MibADC2 | MIBSPI1[8] / MIBSPI3[8] / DCAN1 IF3 / MibADC2 G1 | DMAREQ[16] |
| MIBSPI1 / MIBSPI3 / DCAN3 / MibADC2 | MIBSPI1[9] / MIBSPI3[9] / DCAN3 IF1 / MibADC2 G2 | DMAREQ[17] |
| RTI / MIBSPI5 | RTI DMAREQ2 / MIBSPI5[8] | DMAREQ[18] |
| RTI / MIBSPI5 | RTI DMAREQ3 / MIBSPI5[9] | DMAREQ[19] |
| N2HET1 / N2HET2 / DCAN3 | N2HET1 DMAREQ[4] / N2HET2 DMAREQ[4] / DCAN3 IF2 | DMAREQ[20] |
| N2HET1 / N2HET2 / DCAN3 | N2HET1 DMAREQ[5] / N2HET2 DMAREQ[5] / DCAN3 IF3 | DMAREQ[21] |
| MIBSPI1 / MIBSPI3 / MIBSPI5 | MIBSPI1[10] / MIBSPI3[10] / MIBSPI5[10] | DMAREQ[22] |
| MIBSPI1 / MIBSPI3 / MIBSPI5 | MIBSPI1[11] / MIBSPI3[11] / MIBSPI5[11] | DMAREQ[23] |
| N2HET1 / N2HET2 / SPI4 / MIBSPI5 | N2HET1 DMAREQ[6] / N2HET2 DMAREQ[6] / SPI4 receive / MIBSPI5[12] | DMAREQ[24] |
| N2HET1 / N2HET2 / SPI4 / MIBSPI5 | N2HET1 DMAREQ[7] / N2HET2 DMAREQ[7] / SPI4 transmit / MIBSPI5[13] | DMAREQ[25] |
| CRC / MIBSPI1 / MIBSPI3 | CRC DMAREQ[0] / MIBSPI1[12] / MIBSPI3[12] | DMAREQ[26] |
| CRC / MIBSPI1 / MIBSPI3 | CRC DMAREQ[1] / MIBSPI1[13] / MIBSPI3[13] | DMAREQ[27] |
| LIN / MIBSPI5 | LIN receive / MIBSPI5[14] | DMAREQ[28] |
| LIN / MIBSPI5 | LIN transmit / MIBSPI5[15] | DMAREQ[29] |
| MIBSPI1 / MIBSPI3 / SCI / MIBSPI5 | MIBSPI1[14] / MIBSPI3[14] / SCI receive / MIBSPI5[1](1) | DMAREQ[30] |
| MIBSPI1 / MIBSPI3 / SCI / MIBSPI5 | MIBSPI1[15] / MIBSPI3[15] / SCI transmit / MIBSPI5[0](2) | DMAREQ[31] |

(1) Receive DMA when configured in standard SPI mode
(2) Transmit DMA when configured in standard SPI mode

## 6.17 Real Time Interrupt Module

The real-time interrupt (RTI) module provides timer functionality for operating systems and for benchmarking code. The RTI module can incorporate several counters that define the timebases needed for scheduling an operating system.

The timers also allow you to benchmark certain areas of code by reading the values of the counters at the beginning and the end of the desired code range and calculating the difference between the values.

### 6.17.1 Features

The RTI module has the following features:

- Two independent 64 bit counter blocks
- Four configurable compares for generating operating system ticks or DMA requests. Each event can be driven by either counter block 0 or counter block 1.
- Fast enabling/disabling of events
- Two time-stamp (capture) functions for system or peripheral interrupts, one for each counter block

### 6.17.2 Block Diagrams

Figure 6-17 shows a high-level block diagram for one of the two 64-bit counter blocks inside the RTI module. Both the counter blocks are identical except the Network Time Unit (NTUx) inputs are only available as time base inputs for the counter block 0.

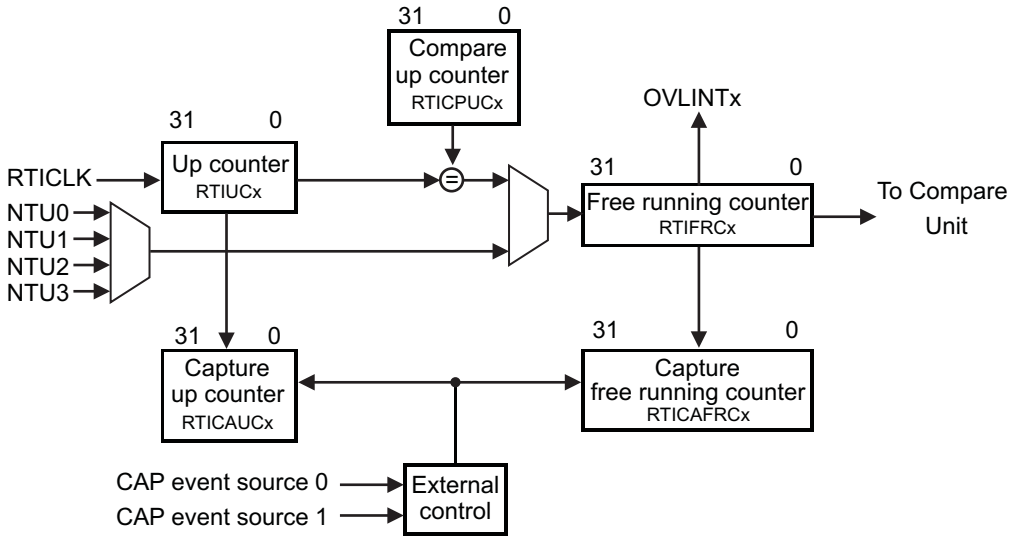



**Figure 6-17. Counter Block Diagram**

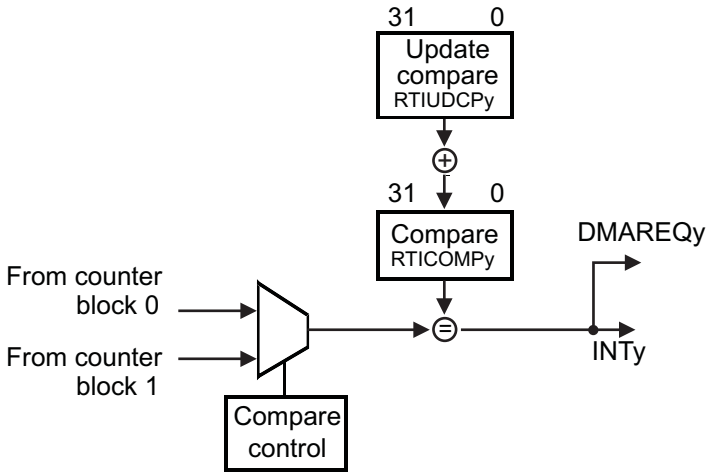



**Figure 6-18. Compare Block Diagram**

### 6.17.3 Clock Source Options

The RTI module uses the RTI1CLK clock domain for generating the RTI time bases.

The application can select the clock source for the RTI1CLK by configuring the RCLKSRC register in the System module at address 0xFFFFFF50. The default source for RTI1CLK is VCLK.

For more information on clock sources refer to Table 6-8 and Table 6-13.

### 6.17.4 Network Time Synchronization Inputs

The RTI module supports 4 Network Time Unit (NTU) inputs that signal internal system events, and which can be used to synchronize the time base used by the RTI module. On this device, these NTU inputs are connected as shown below.

**Table 6-33. Network Time Synchronization Inputs**

| NTU Input | Source |
|---|---|
| 0 | Reserved |
| 1 | Reserved |
| 2 | PLL2 Clock output |
| 3 | EXTCLKIN1 clock input |

## 6.18 Error Signaling Module

The Error Signaling Module (ESM) manages the various error conditions on the microcontroller. The error condition is handled based on a fixed severity level assigned to it. Any severe error condition can be configured to drive a low level on a dedicated device terminal called nERROR. This can be used as an indicator to an external monitor circuit to put the system into a safe state.

### 6.18.1 Features

The features of the Error Signaling Module are:

- 128 interrupt/error channels are supported, divided into 3 different groups
  - 64 channels with maskable interrupt and configurable error pin behavior
  - 32 error channels with non-maskable interrupt and predefined error pin behavior
  - 32 channels with predefined error pin behavior only
- Error pin to signal severe device failure
- Configurable timebase for error signal
- Error forcing capability

### 6.18.2 ESM Channel Assignments

The Error Signaling Module (ESM) integrates all the device error conditions and groups them in the order of severity. Group1 is used for errors of the lowest severity while Group3 is used for errors of the highest severity. The device response to each error is determined by the severity group it is connected to. Table 6-35 shows the channel assignment for each group.

**Table 6-34. ESM Groups**

| ERROR GROUP | INTERRUPT CHARACTERISTICS | INFLUENCE ON ERROR PIN |
|---|---|---|
| Group1 | maskable, low or high priority | configurable |
| Group2 | non-maskable, high priority | fixed |
| Group3 | no interrupt generated | fixed |

**Table 6-35. ESM Channel Assignments**

| ERROR Condition | Group | Channels |
|---|---|---|
| Reserved | Group1 | 0 |
| MibADC2 - RAM parity error | Group1 | 1 |
| DMA - MPU configuration violation | Group1 | 2 |
| DMA - control packet RAM parity error | Group1 | 3 |
| Reserved | Group1 | 4 |
| DMA - error on DMA read access, imprecise error | Group1 | 5 |
| FMC - correctable ECC error: bus1 and bus2 interfaces (does not include accesses to Bank 7) | Group1 | 6 |
| N2HET1 - RAM parity error | Group1 | 7 |
| HTU1/HTU2 - dual-control packet RAM parity error | Group1 | 8 |
| HTU1/HTU2 - MPU configuration violation | Group1 | 9 |
| PLL1 - Slip | Group1 | 10 |
| Clock Monitor - oscillator fail | Group1 | 11 |
| Reserved | Group1 | 12 |
| DMA - error on DMA write access, imprecise error | Group1 | 13 |
| Reserved | Group1 | 14 |
| VIM RAM - parity error | Group1 | 15 |
| Reserved | Group1 | 16 |
| MibSPI1 - RAM parity error | Group1 | 17 |
| MibSPI3 - RAM parity error | Group1 | 18 |

**Table 6-35. ESM Channel Assignments (continued)**

| ERROR Condition | Group | Channels |
|---|---|---|
| MibADC1 - RAM parity error | Group1 | 19 |
| Reserved | Group1 | 20 |
| DCAN1 - RAM parity error | Group1 | 21 |
| DCAN3 - RAM parity error | Group1 | 22 |
| DCAN2 - RAM parity error | Group1 | 23 |
| MibSPI5 - RAM parity error | Group1 | 24 |
| Reserved | Group1 | 25 |
| RAM even bank (B0TCM) - correctable ECC error | Group1 | 26 |
| CPU - self-test failed | Group1 | 27 |
| RAM odd bank (B1TCM) - correctable ECC error | Group1 | 28 |
| Reserved | Group1 | 29 |
| DCC1 - error | Group1 | 30 |
| CCM-R4 - self-test failed | Group1 | 31 |
| Reserved | Group1 | 32 |
| Reserved | Group1 | 33 |
| N2HET2 - RAM parity error | Group1 | 34 |
| FMC - correctable ECC error (Bank 7 access) | Group1 | 35 |
| FMC - uncorrectable ECC error (Bank 7 access) | Group1 | 36 |
| IOMM - Access to unimplemented location in IOMM frame, or write access detected in unprivileged mode | Group1 | 37 |
| Power domain controller compare error | Group1 | 38 |
| Power domain controller self-test error | Group1 | 39 |
| eFuse Controller Error – this error signal is generated when any bit in the eFuse controller error status register is set. The application can choose to generate an interrupt whenever this bit is set to service any eFuse controller error conditions. | Group1 | 40 |
| eFuse Controller - Self Test Error. This error signal is generated only when a self test on the eFuse controller generates an error condition. When an ECC self test error is detected, group 1 channel 40 error signal will also be set. | Group1 | 41 |
| PLL#2 - Slip | Group1 | 42 |
| Reserved | Group1 | 43 |
| Reserved | Group1 | 44 |
| Reserved | Group1 | 45 |
| Reserved | Group1 | 46 |
| Reserved | Group1 | 47 |
| Reserved | Group1 | 48 |
| Reserved | Group1 | 49 |
| Reserved | Group1 | 50 |
| Reserved | Group1 | 51 |
| Reserved | Group1 | 52 |
| Reserved | Group1 | 53 |
| Reserved | Group1 | 54 |
| Reserved | Group1 | 55 |
| Reserved | Group1 | 56 |
| Reserved | Group1 | 57 |
| Reserved | Group1 | 58 |
| Reserved | Group1 | 59 |
| Reserved | Group1 | 60 |
| Reserved | Group1 | 61 |
| DCC2 - error | Group1 | 62 |

**Table 6-35. ESM Channel Assignments (continued)**

| ERROR Condition | Group | Channels |
|---|---|---|
| Reserved | Group1 | 63 |
| Reserved | Group2 | 0 |
| Reserved | Group2 | 1 |
| CCMR4 - dual-CPU lock-step error | Group2 | 2 |
| Reserved | Group2 | 3 |
| FMC - uncorrectable address parity error on accesses to main flash | Group2 | 4 |
| Reserved | Group2 | 5 |
| RAM even bank (B0TCM) - uncorrectable redundant address decode error | Group2 | 6 |
| Reserved | Group2 | 7 |
| RAM odd bank (B1TCM) - uncorrectable redundant address decode error | Group2 | 8 |
| Reserved | Group2 | 9 |
| RAM even bank (B0TCM) - address bus parity error | Group2 | 10 |
| Reserved | Group2 | 11 |
| RAM odd bank (B1TCM) - address bus parity error | Group2 | 12 |
| Reserved | Group2 | 13 |
| Reserved | Group2 | 14 |
| Reserved | Group2 | 15 |
| TCM - ECC live lock detect | Group2 | 16 |
| Reserved | Group2 | 17 |
| Reserved | Group2 | 18 |
| Reserved | Group2 | 19 |
| Reserved | Group2 | 20 |
| Reserved | Group2 | 21 |
| Reserved | Group2 | 22 |
| Reserved | Group2 | 23 |
| Windowed Watchdog (WWD) violation | Group2 | 24 |
| Reserved | Group2 | 25 |
| Reserved | Group2 | 26 |
| Reserved | Group2 | 27 |
| Reserved | Group2 | 28 |
| Reserved | Group2 | 29 |
| Reserved | Group2 | 30 |
| Reserved | Group2 | 31 |
| Reserved | Group3 | 0 |
| eFuse Farm - autoload error | Group3 | 1 |
| Reserved | Group3 | 2 |
| RAM even bank (B0TCM) - ECC uncorrectable error | Group3 | 3 |
| Reserved | Group3 | 4 |
| RAM odd bank (B1TCM) - ECC uncorrectable error | Group3 | 5 |
| Reserved | Group3 | 6 |
| FMC - uncorrectable ECC error: ATCM and Flash OTP interfaces (does not include address parity error and errors on accesses to Bank 7 data memory) | Group3 | 7 |
| Reserved | Group3 | 8 |
| Reserved | Group3 | 9 |
| Reserved | Group3 | 10 |
| Reserved | Group3 | 11 |
| Reserved | Group3 | 12 |

**Table 6-35. ESM Channel Assignments (continued)**

| ERROR Condition | Group | Channels |
|---|---|---|
| Reserved | Group3 | 13 |
| Reserved | Group3 | 14 |
| Reserved | Group3 | 15 |
| Reserved | Group3 | 16 |
| Reserved | Group3 | 17 |
| Reserved | Group3 | 18 |
| Reserved | Group3 | 19 |
| Reserved | Group3 | 20 |
| Reserved | Group3 | 21 |
| Reserved | Group3 | 22 |
| Reserved | Group3 | 23 |
| Reserved | Group3 | 24 |
| Reserved | Group3 | 25 |
| Reserved | Group3 | 26 |
| Reserved | Group3 | 27 |
| Reserved | Group3 | 28 |
| Reserved | Group3 | 29 |
| Reserved | Group3 | 30 |
| Reserved | Group3 | 31 |

## 6.19 Reset / Abort / Error Sources

**Table 6-36. Reset/Abort/Error Sources**

| ERROR SOURCE | SYSTEM MODE | ERROR RESPONSE | ESM HOOKUP group.channel |
|---|---|---|---|
| **CPU TRANSACTIONS** | | | |
| Precise write error (NCNB/Strongly Ordered) | User/Privilege | Precise Abort (CPU) | n/a |
| Precise read error (NCB/Device or Normal) | User/Privilege | Precise Abort (CPU) | n/a |
| Imprecise write error (NCB/Device or Normal) | User/Privilege | Imprecise Abort (CPU) | n/a |
| Illegal instruction | User/Privilege | Undefined Instruction Trap (CPU)(1) | n/a |
| MPU access violation | User/Privilege | Abort (CPU) | n/a |
| **SRAM** | | | |
| B0 TCM (even) ECC single error (correctable) | User/Privilege | ESM | 1.26 |
| B0 TCM (even) ECC double error (non-correctable) | User/Privilege | Abort (CPU), ESM => nERROR | 3.3 |
| B0 TCM (even) uncorrectable error (for example, redundant address decode) | User/Privilege | ESM => NMI => nERROR | 2.6 |
| B0 TCM (even) address bus parity error | User/Privilege | ESM => NMI => nERROR | 2.10 |
| B1 TCM (odd) ECC single error (correctable) | User/Privilege | ESM | 1.28 |
| B1 TCM (odd) ECC double error (non-correctable) | User/Privilege | Abort (CPU), ESM => nERROR | 3.5 |
| B1 TCM (odd) uncorrectable error (for example, redundant address decode) | User/Privilege | ESM => NMI => nERROR | 2.8 |
| B1 TCM (odd) address bus parity error | User/Privilege | ESM => NMI => nERROR | 2.12 |
| **FLASH WITH CPU BASED ECC** | | | |
| FMC correctable error - Bus1 and Bus2 interfaces (does not include accesses to Bank 7) | User/Privilege | ESM | 1.6 |
| FMC uncorrectable error - Bus1 and Bus2 accesses (does not include address parity error) | User/Privilege | Abort (CPU), ESM => nERROR | 3.7 |
| FMC uncorrectable error - address parity error on Bus1 accesses | User/Privilege | ESM => NMI => nERROR | 2.4 |
| FMC correctable error - Accesses to Bank 7 | User/Privilege | ESM | 1.35 |
| FMC uncorrectable error - Accesses to Bank 7 | User/Privilege | ESM | 1.36 |
| **DMA TRANSACTIONS** | | | |
| External imprecise error on read (Illegal transaction with ok response) | User/Privilege | ESM | 1.5 |
| External imprecise error on write (Illegal transaction with ok response) | User/Privilege | ESM | 1.13 |
| Memory access permission violation | User/Privilege | ESM | 1.2 |
| Memory parity error | User/Privilege | ESM | 1.3 |
| **High-End Timer Transfer Unit 1 (HTU1)** | | | |
| NCNB (Strongly Ordered) transaction with slave error response | User/Privilege | Interrupt => VIM | n/a |
| External imprecise error (Illegal transaction with ok response) | User/Privilege | Interrupt => VIM | n/a |
| Memory access permission violation | User/Privilege | ESM | 1.9 |
| Memory parity error | User/Privilege | ESM | 1.8 |
| **High-End Timer Transfer Unit 2 (HTU2)** | | | |
| NCNB (Strongly Ordered) transaction with slave error response | User/Privilege | Interrupt => VIM | n/a |
| External imprecise error (Illegal transaction with ok response) | User/Privilege | Interrupt => VIM | n/a |
| Memory access permission violation | User/Privilege | ESM | 1.9 |
| Memory parity error | User/Privilege | ESM | 1.8 |

(1) The Undefined Instruction TRAP is NOT detectable outside the CPU. The trap is taken only if the instruction reaches the execute stage of the CPU.

**Table 6-36. Reset/Abort/Error Sources (continued)**

| ERROR SOURCE | SYSTEM MODE | ERROR RESPONSE | ESM HOOKUP group.channel |
|---|---|---|---|
| **N2HET1** | | | |
| Memory parity error | User/Privilege | ESM | 1.7 |
| **N2HET2** | | | |
| Memory parity error | User/Privilege | ESM | 1.34 |
| **MIBSPI** | | | |
| MibSPI1 memory parity error | User/Privilege | ESM | 1.17 |
| MibSPI3 memory parity error | User/Privilege | ESM | 1.18 |
| MibSPI5 memory parity error | User/Privilege | ESM | 1.24 |
| **MIBADC** | | | |
| MibADC1 Memory parity error | User/Privilege | ESM | 1.19 |
| MibADC2 Memory parity error | User/Privilege | ESM | 1.1 |
| **DCAN** | | | |
| DCAN1 memory parity error | User/Privilege | ESM | 1.21 |
| DCAN2 memory parity error | User/Privilege | ESM | 1.23 |
| DCAN3 memory parity error | User/Privilege | ESM | 1.22 |
| **PLL** | | | |
| PLL slip error | User/Privilege | ESM | 1.10 |
| PLL #2 slip error | User/Privilege | ESM | 1.42 |
| **CLOCK MONITOR** | | | |
| Clock monitor interrupt | User/Privilege | ESM | 1.11 |
| **DCC** | | | |
| DCC1 error | User/Privilege | ESM | 1.30 |
| DCC2 error | User/Privilege | ESM | 1.62 |
| **CCM-R4** | | | |
| Self test failure | User/Privilege | ESM | 1.31 |
| Compare failure | User/Privilege | ESM => NMI => nERROR | 2.2 |
| **VIM** | | | |
| Memory parity error | User/Privilege | ESM | 1.15 |
| **VOLTAGE MONITOR** | | | |
| VMON out of voltage range | n/a | Reset | n/a |
| **CPU SELFTEST (LBIST)** | | | |
| CPU Selftest (LBIST) error | User/Privilege | ESM | 1.27 |
| **PIN MULTIPLEXING CONTROL** | | | |
| Mux configuration error | User/Privilege | ESM | 1.37 |
| **POWER DOMAIN CONTROL** | | | |
| PSCON compare error | User/Privilege | ESM | 1.38 |
| PSCON self-test error | User/Privilege | ESM | 1.39 |
| **eFuse CONTROLLER** | | | |
| eFuse Controller Autoload error | User/Privilege | ESM => nERROR | 3.1 |
| eFuse Controller - Any bit set in the error status register | User/Privilege | ESM | 1.40 |
| eFuse Controller self-test error | User/Privilege | ESM | 1.41 |
| **WINDOWED WATCHDOG** | | | |
| WWD Non-Maskable Interrupt exception | n/a | ESM => NMI => nERROR | 2.24 |
| **ERRORS REFLECTED IN THE SYSESR REGISTER** | | | |
| Power-Up Reset | n/a | Reset | n/a |
| Oscillator fail / PLL slip(2) | n/a | Reset | n/a |

(2) Oscillator fail/PLL slip can be configured in the system register (SYS.PLLCTL1) to generate a reset.

**Table 6-36. Reset/Abort/Error Sources (continued)**

| ERROR SOURCE | SYSTEM MODE | ERROR RESPONSE | ESM HOOKUP group.channel |
|---|---|---|---|
| Watchdog exception | n/a | Reset | n/a |
| CPU Reset (driven by the CPU STC) | n/a | Reset | n/a |
| Software Reset | n/a | Reset | n/a |
| External Reset | n/a | Reset | n/a |

## 6.20 Digital Windowed Watchdog

This device includes a digital windowed watchdog (DWWD) module that protects against runaway code execution.

The DWWD module allows the application to configure the time window within which the DWWD module expects the application to service the watchdog. A watchdog violation occurs if the application services the watchdog outside of this window, or fails to service the watchdog at all. The application can choose to generate a system reset or an ESM group2 error signal in case of a watchdog violation.

The watchdog is disabled by default and must be enabled by the application. Once enabled, the watchdog can only be disabled upon a system reset.

## 6.21 Debug Subsystem

### 6.21.1 Block Diagram

The device contains an ICEPICK module to allow JTAG access to the scan chains.

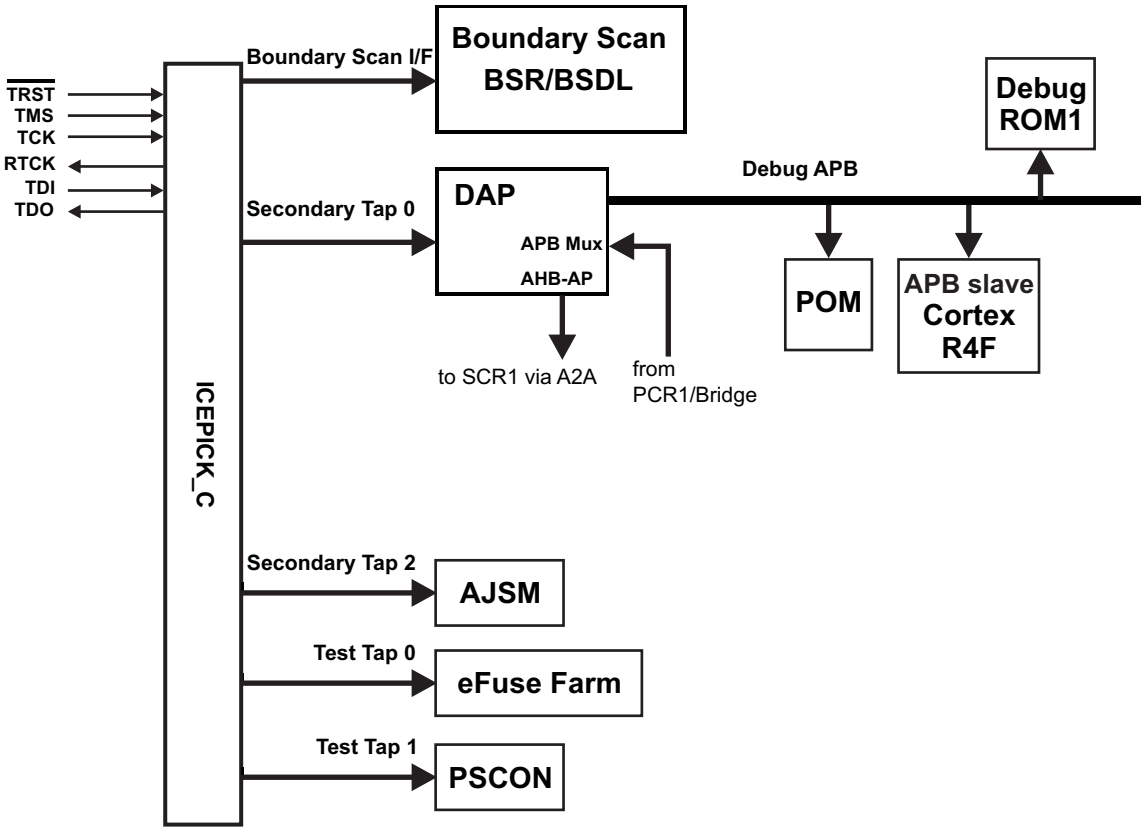



**Figure 6-19. Debug Subsystem Block Diagram**

### 6.21.2 Debug Components Memory Map

**Table 6-37. Debug Components Memory Map**

| MODULE NAME | FRAME CHIP SELECT | FRAME ADDRESS RANGE | | FRAME SIZE | ACTUAL SIZE | RESPNSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME |
|---|---|---|---|---|---|---|
| | | START | END | | | |
| CoreSight Debug ROM | CSCS0 | 0xFFA0_0000 | 0xFFA0_0FFF | 4KB | 4KB | Reads return zeros, writes have no effect |
| Cortex-R4F Debug | CSCS1 | 0xFFA0_1000 | 0xFFA0_1FFF | 4KB | 4KB | Reads return zeros, writes have no effect |

### 6.21.3 JTAG Identification Code

The JTAG ID code for this device is the same as the device ICEPick Identification Code.

**Table 6-38. JTAG ID Code**

| Silicon Revision | ID |
|---|---|
| Rev A | 0x0B95502F |
| Rev B | 0x2B95502F |
| Rev C | 0x3B95502F |

### 6.21.4 Debug ROM

The Debug ROM stores the location of the components on the Debug APB bus:

**Table 6-39. Debug ROM table**

| ADDRESS | DESCRIPTION | VALUE |
|---|---|---|
| 0x000 | pointer to Cortex-R4F | 0x0000 1003 |
| 0x001 | Reserved | 0x0000 2002 |
| 0x002 | Reserved | 0x0000 3002 |
| 0x003 | POM | 0x0000 4003 |
| 0x004 | end of table | 0x0000 0000 |

### 6.21.5 JTAG Scan Interface Timings

**Table 6-40. JTAG Scan Interface Timing (1)**

| No. | Parameter | | Min | MAX | Unit |
|---|---|---|---|---|---|
| | fTCK | TCK frequency (at HCLKmax) | | 12 | MHz |
| | fRTCK | RTCK frequency (at TCKmax and HCLKmax) | 10 | | MHz |
| 1 | td(TCK -RTCK) | Delay time, TCK to RTCK | | 24 | ns |
| 2 | tsu(TDI/TMS - RTCKr) | Setup time, TDI, TMS before RTCK rise (RTCKr) | 26 | | ns |
| 3 | th(RTCKr -TDI/TMS) | Hold time, TDI, TMS after RTCKr | 0 | | ns |
| 4 | th(RTCKr -TDO) | Hold time, TDO after RTCKf | 0 | | ns |
| 5 | td(TCKf -TDO) | Delay time, TDO valid after RTCK fall (RTCKf) | | 12 | ns |

(1) Timings for TDO are specified for a maximum of 50pF load on TDO

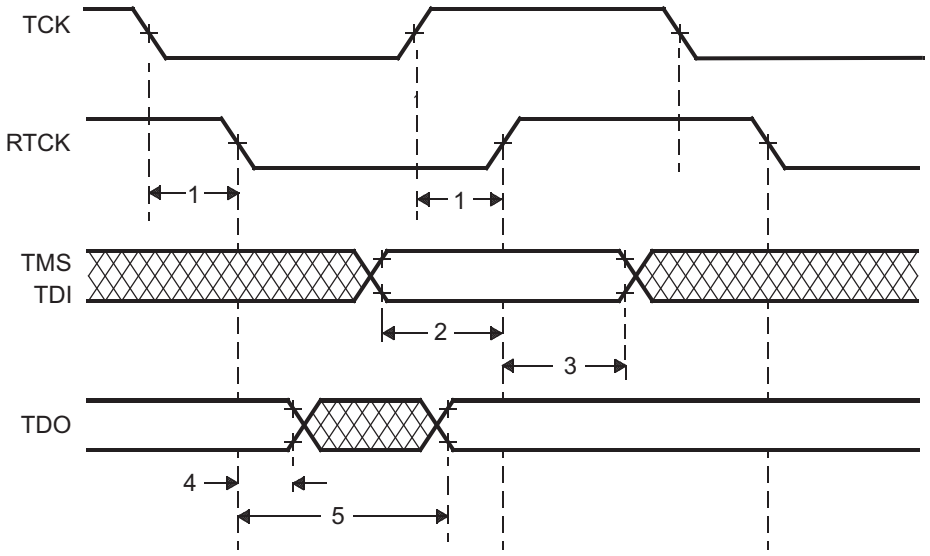



**Figure 6-20. JTAG Timing**

### 6.21.6 Advanced JTAG Security Module

This device includes a an Advanced JTAG Security Module (AJSM). which provides maximum security to the device's memory content by allowing users to secure the device after programming.

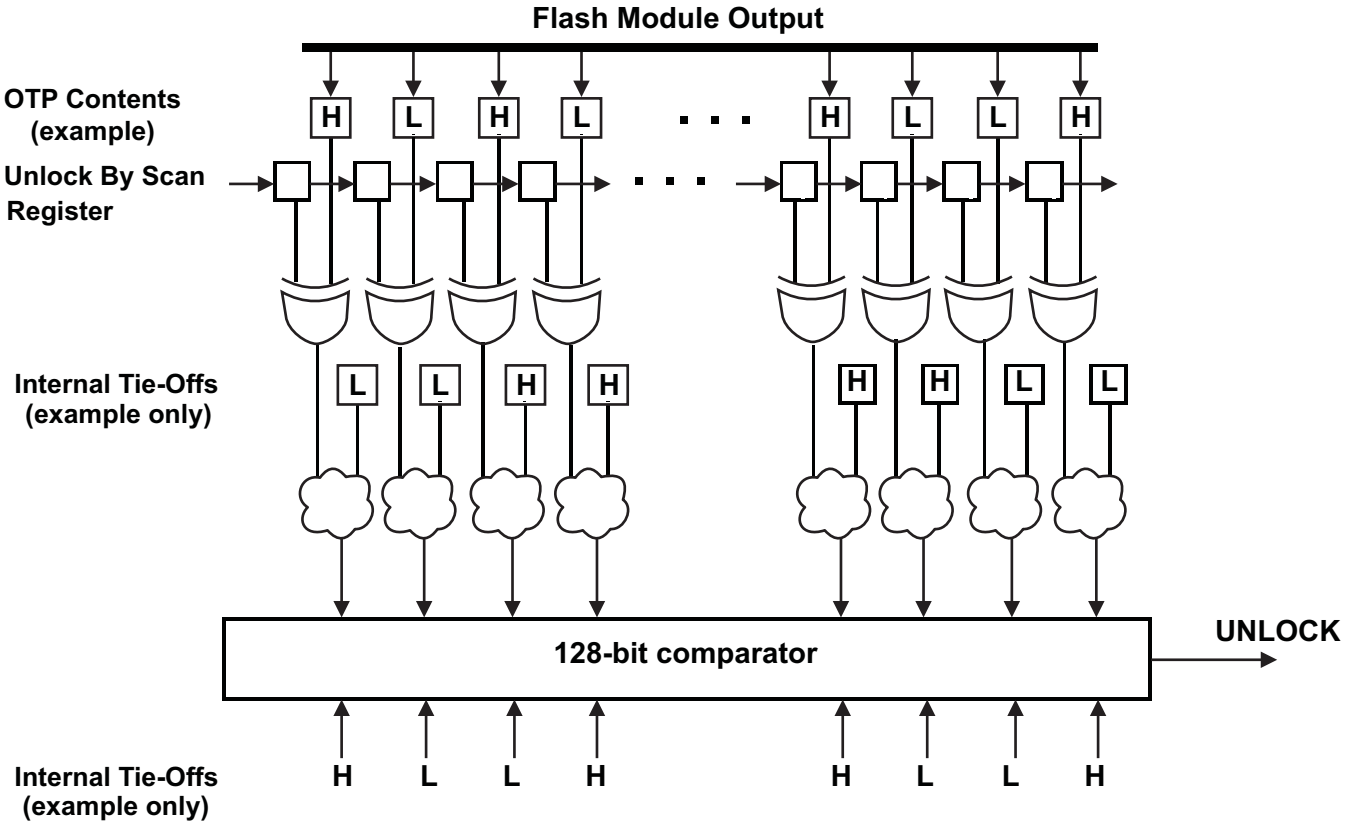



**Figure 6-21. AJSM Unlock**

The device is unsecure by default by virtue of a 128-bit visible unlock code programmed in the OTP address 0xF0000000.The OTP contents are XOR-ed with the "Unlock By Scan" register contents. The outputs of these XOR gates are again combined with a set of secret internal tie-offs. The output of this combinational logic is compared against a secret hard-wired 128-bit value. A match results in the UNLOCK signal being asserted, so that the device is now unsecure.

A user can secure the device by changing at least one bit in the visible unlock code from 1 to 0. Changing a 0 to 1 is not possible since the visible unlock code is stored in the One Time Programmable (OTP) flash region. Also, changing all the 128 bits to zeros is not a valid condition and will permanently secure the device.

Once secured, a user can unsecure the device by scanning an appropriate value into the "Unlock By Scan" register of the AJSM module. This register is accessible by configuring an IR value of 0b1011 on the AJSM TAP. The value to be scanned is such that the XOR of the OTP contents and the Unlock-By-Scan register contents results in the original visible unlock code.

The Unlock-By-Scan register is reset only upon asserting power-on reset (nPORRST).

A secure device only permits JTAG accesses to the AJSM scan chain through the Secondary Tap # 2 of the ICEPick module. All other secondary taps, test taps and the boundary scan interface are not accessible in this state.

### 6.21.7 Boundary Scan Chain

The device supports BSDL-compliant boundary scan for testing pin-to-pin compatibility. The boundary scan chain is connected to the Boundary Scan Interface of the ICEPICK module.

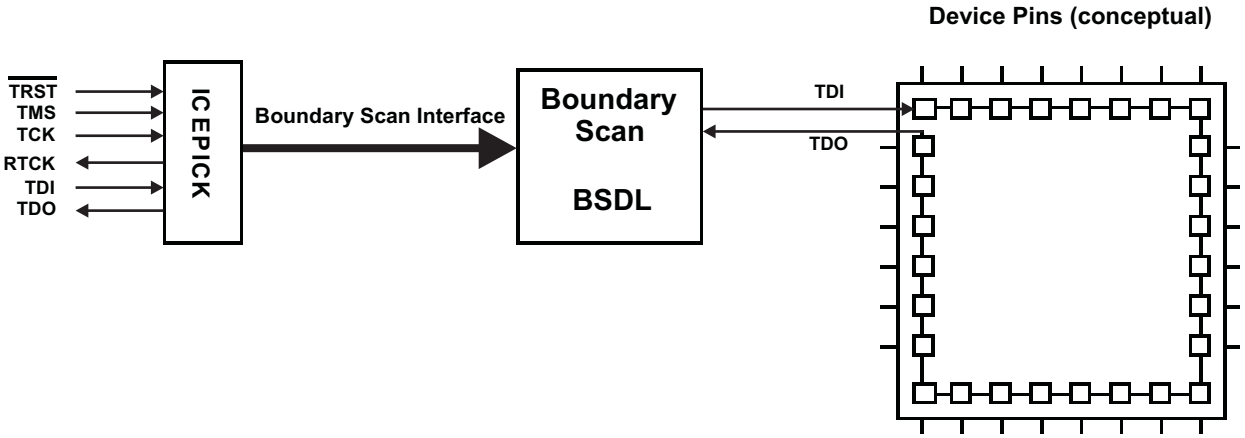



**Figure 6-22. Boundary Scan Implementation (Conceptual Diagram)**

Data is serially shifted into all boundary-scan buffers through TDI, and out through TDO.

# 7 Peripheral Information and Electrical Specifications

## 7.1 Enhanced Translator PWM Modules (ePWM)

Figure 7-1 illustrates the connections between the seven ePWM modules (ePWM1,2,3,4,5,6,7) on the device.

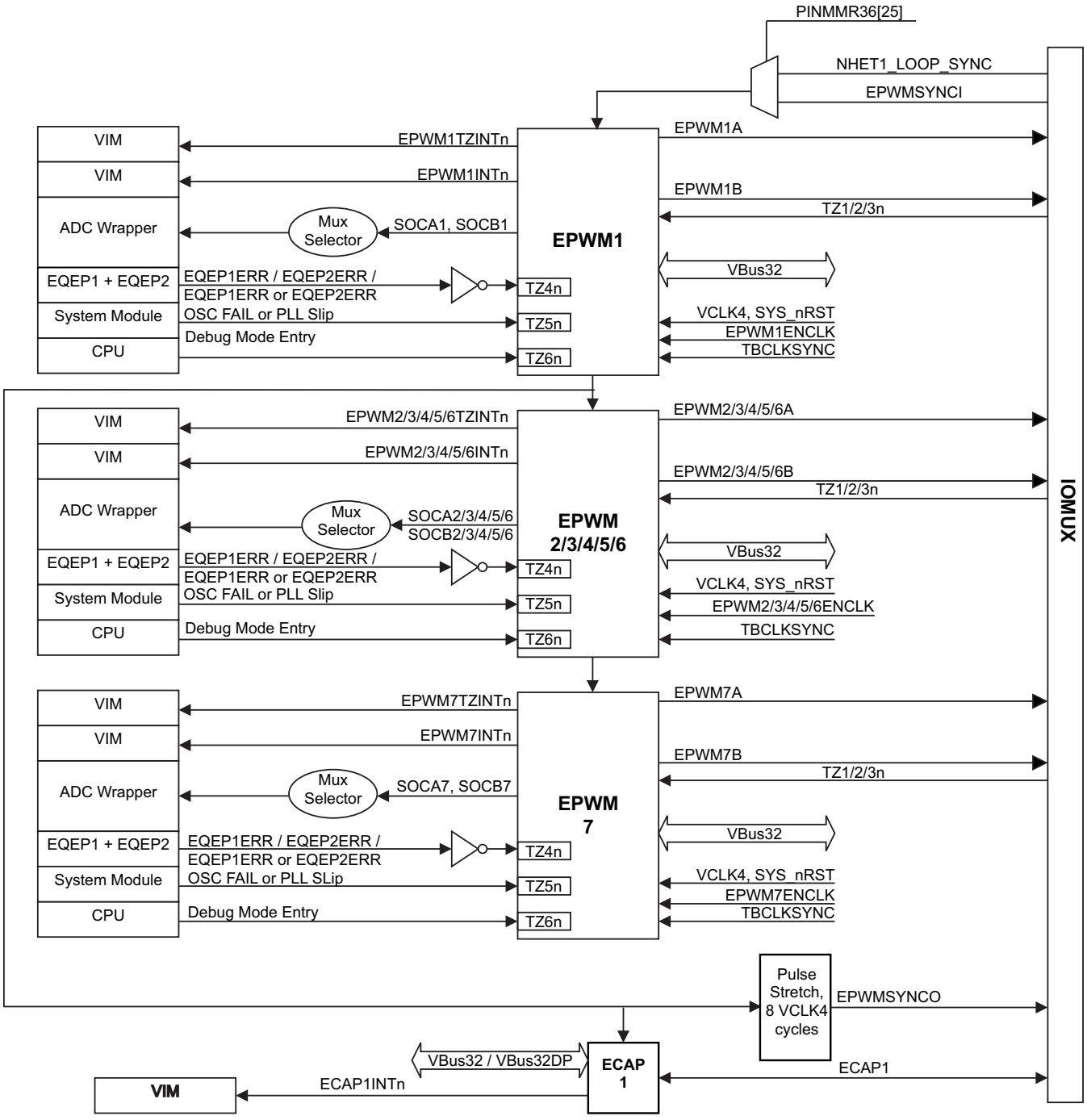



**Figure 7-1. ePWMx Module Interconnections**

### 7.1.1 ePWM Clocking and Reset

Each ePWM module has a clock enable (EPWMxENCLK). When SYS_nRST is active low, the clock enables are ignored and the ePWM logic is clocked so that it can reset to a proper state. When SYS_nRST goes in-active high, the state of clock enable is respected.

**Table 7-1. ePWMx Clock Enable Control**

| ePWM Module Instance | Control Register to Enable Clock | Default Value |
|---|---|---|
| ePWM1 | PINMMR37[8] | 1 |
| ePWM2 | PINMMR37[16] | 1 |
| ePWM3 | PINMMR37[24] | 1 |
| ePWM4 | PINMMR38[0] | 1 |
| ePWM5 | PINMMR38[8] | 1 |
| ePWM6 | PINMMR38[16] | 1 |
| ePWM7 | PINMMR38[24] | 1 |

The default value of the control registers to enable the clocks to the ePWMx modules is 1. This means that the VCLK4 clock connections to the ePWMx modules are enabled by default. The application can choose to gate off the VCLK4 clock to any ePWMx module individually by clearing the respective control register bit.

### 7.1.2 Synchronization of ePWMx Time Base Counters

A time-base synchronization scheme connects all of the ePWM modules on a device. Each ePWM module has a synchronization input (EPWMxSYNCI) and a synchronization output (EPWMxSYNCO). The input synchronization for the first instance (ePWM1) comes from an external pin. Figure 7-1 shows the synchronization connections for all the ePWMx modules. Each ePWM module can be configured to use or ignore the synchronization input. Refer to the ePWM chapter in the TMS570LS12x/11x Technical Reference Manual (SPNU515) for more information.

### 7.1.3 Synchronizing all ePWM Modules to the N2HET1 Module Time Base

The connection between the N2HET1_LOOP_SYNC and SYNCI input of ePWM1 module is implemented as shown in Figure 7-2.

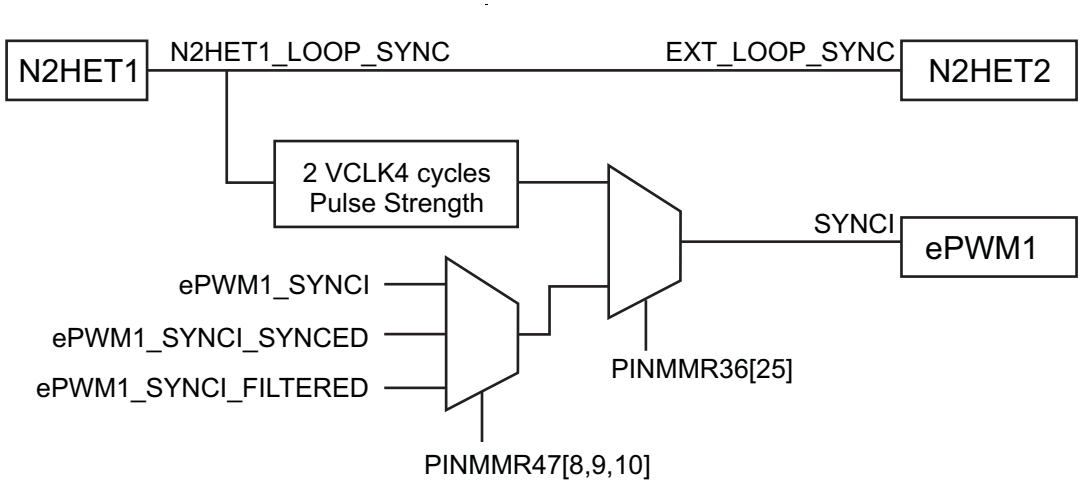



**Figure 7-2. Synchronizing Time Bases Between N2HET1, N2HET2 and ePWMx Modules**

### 7.1.4 Phase-Locking the Time-Base Clocks of Multiple ePWM Modules

The TBCLKSYNC bit can be used to globally synchronize the time-base clocks of all enabled ePWM modules on a device. This bit is implemented as PINMMR37 register bit 1.

When TBCLKSYNC = 0, the time-base clock of all ePWM modules is stopped. This is the default condition.

When TBCLKSYNC = 1, all ePWM time-base clocks are started with the rising edge of TBCLK aligned.

For perfectly synchronized TBCLKs, the prescaler bits in the TBCTL register of each ePWM module must be set identically. The proper procedure for enabling the ePWM clocks is as follows:

1. Enable the individual ePWM module clocks (if disable) using the control registers shown in Table 7-1.
2. Configure TBCLKSYNC = 0. This will stop the time-base clock within any enabled ePWM module.
3. Configure the prescaler values and desired ePWM modes.
4. Configure TBCLKSYNC = 1.

### 7.1.5 ePWM Synchronization with External Devices

The output sync from EPWM1 Module is also exported to a device output terminal so that multiple devices can be synchronized together. The signal pulse is stretched by eight VCLK4 cycles before being exported on the terminal as the EPWM1SYNCO signal.

### 7.1.6 ePWM Trip Zones

The ePWMx modules have six trip zone inputs each. These are active-low signals. The application can control the ePWMx module response to each of the trip zone input separately. The timing requirements from the assertion of the trip zone inputs to the actual response are specified in Section 7.1.8.

#### 7.1.6.1 Trip Zones TZ1n, TZ2n, TZ3n

These three trip zone inputs are driven by external circuits and are connected to device-level inputs. These signals are either connected asynchronously to the ePWMx trip zone inputs, or double-synchronized with VCLK4, or double-synchronized and then filtered with a 6-cycle VCLK4-based counter before connecting to the ePWMx. By default, the trip zone inputs are asynchronously connected to the ePWMx modules.

**Table 7-2. Connection to ePWMx Modules for Device-Level Trip Zone Inputs**

| Trip Zone Input | Control for Asynchronous Connection to ePWMx | Control for Double-Synchronized Connection to ePWMx | Control for Double-Synchronized and Filtered Connection to ePWMx |
|---|---|---|---|
| TZ1n | PINMMR46[16] = 1 | PINMMR46[16] = 0 AND PINMMR46[17] = 1 | PINMMR46[16] = 0 AND PINMMR46[17] = 0 AND PINMMR46[18] = 1 |
| TZ2n | PINMMR46[24] = 1 | PINMMR46[24] = 0 AND PINMMR46[25] = 1 | PINMMR46[24] = 0 AND PINMMR46[25] = 0 AND PINMMR46[26] = 1 |
| TZ3n | PINMMR47[0] = 1 | PINMMR47[0] = 0 AND PINMMR47[1] = 1 | PINMMR47[0] = 0 AND PINMMR47[1] = 0 AND PINMMR47[2] = 1 |

#### 7.1.6.2 Trip Zone TZ4n

This trip zone input is dedicated to eQEPx error indications. There are two eQEP modules on this device. Each eQEP module indicates a phase error by driving its EQEPxERR output High. The following control registers allow the application to configure the trip zone input (TZ4n) to each ePWMx module based on the application's requirements.

**Table 7-3. TZ4n Connections for ePWMx Modules**

| ePWMx | Control for TZ4n = not(EQEP1ERR OR EQEP2ERR) | Control for TZ4n = not(EQEP1ERR) | Control for TZ4n = not(EQEP2ERR) |
|---|---|---|---|
| ePWM1 | PINMMR41[0] = 1 | PINMMR41[0] = 0 AND PINMMR41[1] = 1 | PINMMR41[0] = 1 AND PINMMR41[1] = 0 AND PINMMR41[2] = 1 |
| ePWM2 | PINMMR41[8] | PINMMR41[8] = 0 AND PINMMR41[9] = 1 | PINMMR41[8] = 1 AND PINMMR41[9] = 0 AND PINMMR41[10] = 1 |
| ePWM3 | PINMMR41[16] | PINMMR41[16] = 0 AND PINMMR41[17] = 1 | PINMMR41[16] = 1 AND PINMMR41[17] = 0 AND PINMMR41[18] = 1 |
| ePWM4 | PINMMR41[24] | PINMMR41[24] = 0 AND PINMMR41[25] = 1 | PINMMR41[24] = 1 AND PINMMR41[25] = 0 AND PINMMR41[26] = 1 |
| ePWM5 | PINMMR42[0] | PINMMR42[0] = 0 AND PINMMR42[1] = 1 | PINMMR42[0] = 1 AND PINMMR42[1] = 0 AND PINMMR42[2] = 1 |
| ePWM6 | PINMMR42[8] | PINMMR42[8] = 0 AND PINMMR42[9] = 1 | PINMMR42[8] = 1 AND PINMMR42[9] = 0 AND PINMMR42[10] = 1 |
| ePWM7 | PINMMR42[16] | PINMMR42[16] = 0 AND PINMMR42[17] = 1 | PINMMR42[16] = 1 AND PINMMR42[17] = 0 AND PINMMR42[18] = 1 |

#### 7.1.6.3 Trip Zone TZ5n

This trip zone input is dedicated to a clock failure on the device. That is, this trip zone input is asserted whenever an oscillator failure or a PLL slip is detected on the device. The application can use this trip zone input for each ePWMx module in order to prevent the external system from going out of control when the device clocks are not within expected range (system running at limp clock).

The oscillator failure and PLL slip signals used for this trip zone input are taken from the status flags in the system module. These are level signals are set until cleared by the application.

#### 7.1.6.4 Trip Zone TZ6n

This trip zone input to the ePWMx modules is dedicated to a debug mode entry of the CPU. If enabled, the user can force the PWM outputs to a known state when the emulator stops the CPU. This prevents the external system from going out of control when the CPU is stopped.

### *7.1.7 Triggering of ADC Start of Conversion Using ePWMx SOCA and SOCB Outputs*

A special scheme is implemented in order to select the actual signal used for triggering the start of conversion on the two ADCs on this device. This scheme is defined in Section 7.4.2.3.

### *7.1.8 Enhanced Translator-Pulse Width Modulator (ePWMx) Timings*

**Table 7-4. ePWMx Timing Requirements**

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(SYNCIN)}$ | Synchronization input pulse width | Asynchronous | 2 $t_{c(VCLK4)}$ | | cycles |
| | | Synchronous | 2 $t_{c(VCLK4)}$ | | cycles |
| | | Synchronous, with input filter | 2 $t_{c(VCLK4)}$ + filter width | | cycles |

**Table 7-5. ePWMx Switching Characteristics**

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(PWM)}$ | Pulse duration, ePWMx output high or low | | 33.33 | | ns |
| $t_{w(SYNCOUT)}$ | Synchronization Output Pulse Width | | 8 $t_{c(VCLK4)}$ | | cycles |
| $t_{d(PWM)tza}$ | Delay time, trip input active to PWM forced high, OR Delay time, trip input active to PWM forced low | no pin load | | 25 | ns |

**Table 7-5. ePWMx Switching Characteristics (continued)**

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{d(TZ-PWM)HZ}$ | Delay time, trip input active to PWM Hi-Z | | | 20 | ns |

**Table 7-6. ePWMx Trip-Zone Timing Requirements**

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(TZ)}$ | Pulse duration, TZn input low | Asynchronous | 2 * HSPCLKDIV * CLKDIV * $t_{c(VCLK4)}$ (1) | | ns |
| | | Synchronous | 2 $t_{c(VCLK4)}$ | | ns |
| | | Synchronous, with input filter | 8 $t_{c(VCLK4)}$ | | ns |

(1) Refer to the ePWM chapter of the TMS570LS12x/11x Technical Reference Manual (SPNU515) for more information on the clock divider fields HSPCLKDIV and CLKDIV.

## 7.2 Enhanced Capture Modules (eCAP)

Figure 7-3 shows how the eCAP modules are interconnected on this microcontroller.

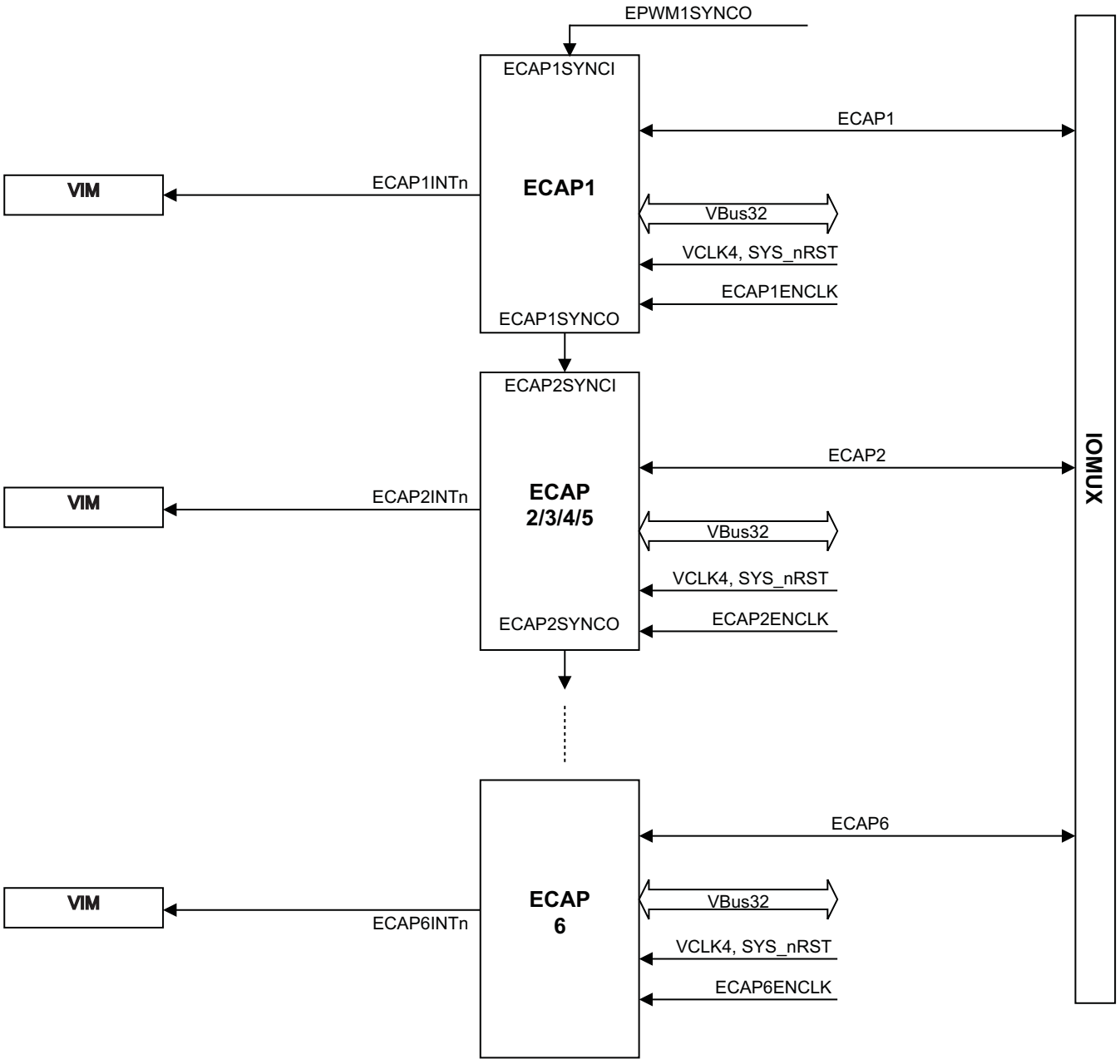



**Figure 7-3. eCAP Module Connections**

### *7.2.1 Clock Enable Control for eCAPx Modules*

Each of the ECAPx modules have a clock enable (ECAPxENCLK). These signals need to be generated from a device-level control register. When SYS_nRST is active low, the clock enables are ignored and the ECAPx logic is clocked so that it can reset to a proper state. When SYS_nRST goes in-active high, the state of clock enable is respected.

**Table 7-7. eCAPx Clock Enable Control**

| ePWM Module Instance | Control Register to Enable Clock | Default Value |
|---|---|---|
| eCAP1 | PINMMR39[0] | 1 |
| eCAP2 | PINMMR39[8] | 1 |
| eCAP3 | PINMMR39[16] | 1 |
| eCAP4 | PINMMR39[24] | 1 |
| eCAP5 | PINMMR40[0] | 1 |
| eCAP6 | PINMMR40[8] | 1 |

The default value of the control registers to enable the clocks to the eCAPx modules is 1. This means that the VCLK4 clock connections to the eCAPx modules are enabled by default. The application can choose to gate off the VCLK4 clock to any eCAPx module individually by clearing the respective control register bit.

### 7.2.2 PWM Output Capability of eCAPx

When not used in capture mode, each of the eCAPx modules can be used as a single-channel PWM output. This is called the auxiliary PWM (APWM) mode of operation of the eCAP modules. Refer to the eCAP chapter of the TMS570LS12x/11x Technical Reference Manual (SPNU515) for more information.

### 7.2.3 Input Connection to eCAPx Modules

The input connection to each of the eCAP modules can be selected between a double-VCLK4-synchronized input or a double-VCLK4-synchronized and filtered input, as shown in Table 7-8.

**Table 7-8. Device-Level Input Connection to eCAPx Modules**

| Input Signal | Control for Double-Synchronized Connection to eCAPx | Control for Double-Synchronized and Filtered Connection to eCAPx |
|---|---|---|
| eCAP1 | PINMMR43[0] = 1 | PINMMR43[0] = 0 AND PINMMR43[1] = 1 |
| eCAP2 | PINMMR43[8] = 1 | PINMMR43[8] = 0 AND PINMMR43[9] = 1 |
| eCAP3 | PINMMR43[16] = 1 | PINMMR43[16] = 0 AND PINMMR43[17] = 1 |
| eCAP4 | PINMMR43[24] = 1 | PINMMR43[24] = 0 AND PINMMR43[25] = 1 |
| eCAP5 | PINMMR44[0] = 1 | PINMMR44[0] = 0 AND PINMMR44[1] = 1 |
| eCAP6 | PINMMR44[8] = 1 | PINMMR44[8] = 0 AND PINMMR44[9] = 1 |

### 7.2.4 Enhanced Capture Module (eCAP) Timings

**Table 7-9. eCAPx Timing Requirements**

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(CAP)}$ | Capture input pulse width | Synchronous | 2 $t_{c(VCLK4)}$ | | cycles |
| | | Synchronous, with input filter | 2 $t_{c(VCLK4)}$ + filter width | | cycles |

**Table 7-10. eCAPx Switching Characteristics**

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(APWM)}$ | Pulse duration, APWMx output high or low | | 20 | | ns |

## 7.3 Enhanced Quadrature Encoder (eQEP)

Figure 7-4 shows the eQEP module interconnections on the device.

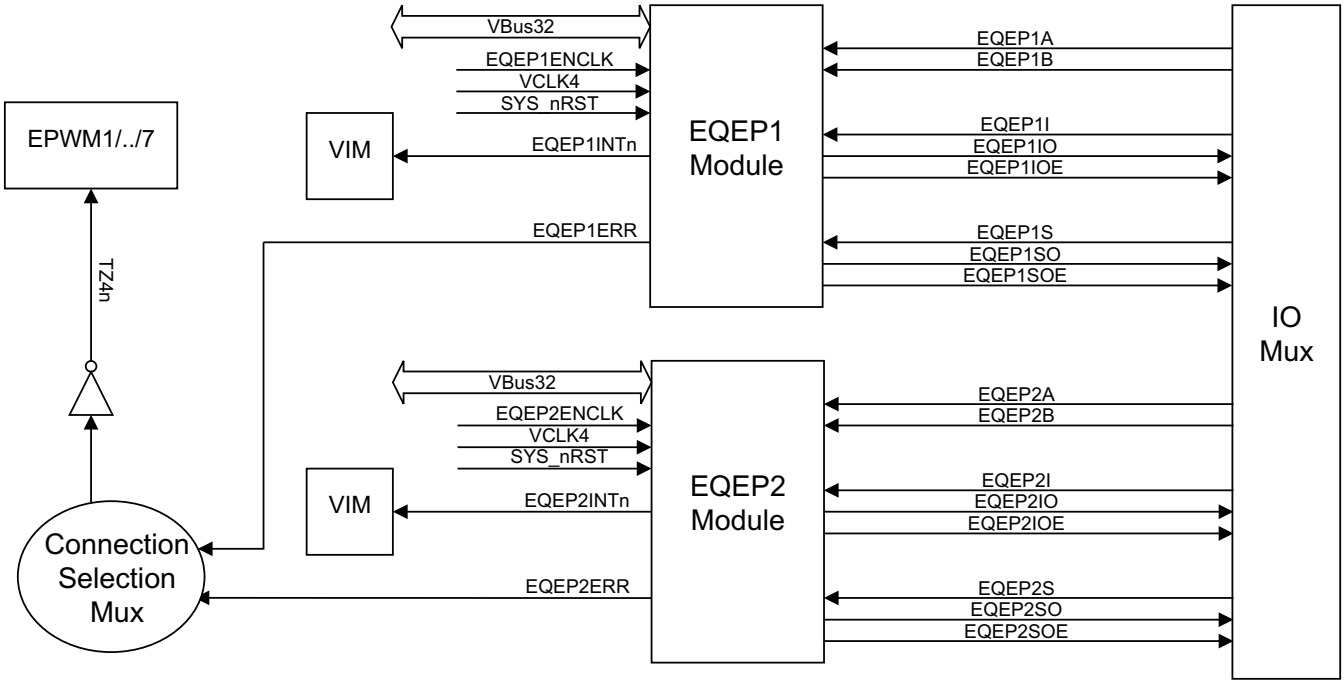



**Figure 7-4. eQEP Module Interconnections**

### 7.3.1 Clock Enable Control for eQEPx Modules

Device-level control registers are implemented to generate the EQEPxENCLK signals. When SYS_nRST is active low, the clock enables are ignored and the eQEPx logic is clocked so that it can reset to a proper state. When SYS_nRST goes in-active high, the state of clock enable is respected.

**Table 7-11. eQEPx Clock Enable Control**

| ePWM Module Instance | Control Register to Enable Clock | Default Value |
|---|---|---|
| eQEP1 | PINMMR40[16] | 1 |
| eQEP2 | PINMMR40[24] | 1 |

The default value of the control registers to enable the clocks to the eQEPx modules is 1. This means that the VCLK4 clock connections to the eQEPx modules are enabled by default. The application can choose to gate off the VCLK4 clock to any eQEPx module individually by clearing the respective control register bit.

### 7.3.2 Using eQEPx Phase Error to Trip ePWMx Outputs

The eQEP module sets the EQEPERR signal output whenever a phase error is detected in its inputs EQEPxA and EQEPxB. This error signal from both the eQEP modules is input to the connection selection multiplexor. This multiplexor is defined in Table 7-3. As shown in Figure 7-1, the output of this selection multiplexor is inverted and connected to the TZ4n trip-zone input of all EPWMx modules. This connection allows the application to define the response of each ePWMx module on a phase error indicated by the eQEP modules.

### 7.3.3 Input Connections to eQEPx Modules

The input connections to each of the eQEP modules can be selected between a double-VCLK4-synchronized input or a double-VCLK4-synchronized and filtered input, as shown in Table 7-12.

**Table 7-12. Device-Level Input Connection to eCAPx Modules**

| Input Signal | Control for Double-Synchronized Connection to eQEPx | Control for Double-Synchronized and Filtered Connection to eQEPx |
|---|---|---|
| eQEP1A | PINMMR44[16] = 1 | PINMMR44[16] = 0 and PINMMR44[17] = 1 |
| eQEP1B | PINMMR44[24] = 1 | PINMMR44[24] = 0 and PINMMR44[25] = 1 |
| eQEP1I | PINMMR45[0] = 1 | PINMMR45[0] = 0 and PINMMR45[1] = 1 |
| eQEP1S | PINMMR45[8] = 1 | PINMMR45[8] = 0 and PINMMR45[9] = 1 |
| eQEP2A | PINMMR45[16] = 1 | PINMMR45[16] = 0 and PINMMR45[17] = 1 |
| eQEP2B | PINMMR45[24] = 1 | PINMMR45[24] = 0 and PINMMR45[25] = 1 |
| eQEP2I | PINMMR46[0] = 1 | PINMMR46[0] = 0 and PINMMR46[1] = 1 |
| eQEP2S | PINMMR46[8] = 1 | PINMMR46[8] = 0 and PINMMR46[9] = 1 |

### 7.3.4 Enhanced Quadrature Encoder Pulse (eQEPx) Timing

**Table 7-13. eQEPx Timing Requirements**

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(QEPP)}$ | QEP input period | Synchronous | 2 $t_{c(VCLK4)}$ | | cycles |
| | | Synchronous, with input filter | 2 $t_{c(VCLK4)}$ + filter width | | cycles |
| $t_{w(INDEXH)}$ | QEP Index Input High Time | Synchronous | 2 $t_{c(VCLK4)}$ | | cycles |
| | | Synchronous, with input filter | 2 $t_{c(VCLK4)}$ + filter width | | cycles |
| $t_{w(INDEXL)}$ | QEP Index Input Low Time | Synchronous | 2 $t_{c(VCLK4)}$ | | cycles |
| | | Synchronous, with input filter | 2 $t_{c(VCLK4)}$ + filter width | | cycles |
| $t_{w(STROBH)}$ | QEP Strobe Input High Time | Synchronous | 2 $t_{c(VCLK4)}$ | | cycles |
| | | Synchronous, with input filter | 2 $t_{c(VCLK4)}$ + filter width | | cycles |
| $t_{w(STROBL)}$ | QEP Strobe Input Low Time | Synchronous | 2 $t_{c(VCLK4)}$ | | cycles |
| | | Synchronous, with input filter | 2 $t_{c(VCLK4)}$ + filter width | | cycles |

**Table 7-14. eQEPx Switching Characteristics**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{d(CNTR)xin}$ | Delay time, external clock to counter increment | | 4 $t_{c(VCLK4)}$ | cycles |
| $t_{d(PCS-OUT)QEP}$ | Delay time, QEP input edge to position compare sync output | | 6 $t_{c(VCLK4)}$ | cycles |

## 7.4 Multibuffered 12bit Analog-to-Digital Converter

The multibuffered A-to-D converter (MibADC) has a separate power bus for its analog circuitry that enhances the A-to-D performance by preventing digital switching noise on the logic circuitry which could be present on $V_{SS}$ and $V_{CC}$ from coupling into the A-to-D analog stage. All A-to-D specifications are given with respect to $AD_{REFLO}$ unless otherwise noted.

**Table 7-15. MibADC Overview**

| Description | Value |
|---|---|
| Resolution | 12 bits |
| Monotonic | Assured |
| Output conversion code | 00h to 3FFh [00 for $V_{AI} \le AD_{REFLO}$; 3FFh for $V_{AI} \ge AD_{REFHI}$] |

### 7.4.1 Features

- 12-bit resolution
- $AD_{REFHI}$ and $AD_{REFLO}$ pins (high and low reference voltages)
- Total Sample/Hold/Convert time: 600ns Minimum at 30MHz ADCLK
- One memory region per conversion group is available (event, group 1, group 2)
- Allocation of channels to conversion groups is completely programmable
- Supports flexible channel conversion order
- Memory regions are serviced either by interrupt or by DMA
- Programmable interrupt threshold counter is available for each group
- Programmable magnitude threshold interrupt for each group for any one channel
- Option to read either 8-bit, 10-bit or 12-bit values from memory regions
- Single or continuous conversion modes
- Embedded self-test
- Embedded calibration logic
- Enhanced power-down mode
  - Optional feature to automatically power down ADC core when no conversion is in progress
- External event pin (ADxEVT) programmable as general-purpose I/O

### 7.4.2 Event Trigger Options

The ADC module supports 3 conversion groups: Event Group, Group1 and Group2. Each of these 3 groups can be configured to be hardware event-triggered. In that case, the application can select from among 8 event sources to be the trigger for a group's conversions.

#### 7.4.2.1 MIBADC1 Event Trigger Hookup

**Table 7-16. MIBADC1 Event Trigger Hookup**

| Group Source Select, G1SRC, G2SRC or EVSRC | Event # | Trigger Event Signal | | | | |
|---|---|---|---|---|---|---|
| | | PINMMR30[0] = 1 (default) | PINMMR30[0] = 0 and PINMMR30[1] = 1 | | | |
| | | | Option A | Control for Option A | Option B | Control for Option B |
| 000 | 1 | AD1EVT | AD1EVT | — | AD1EVT | — |
| 001 | 2 | N2HET1[8] | N2HET2[5] | PINMMR30[8] = 1 | ePWM_B | PINMMR30[8] = 0 and PINMMR30[9] = 1 |
| 010 | 3 | N2HET1[10] | N2HET1[27] | — | N2HET1[27] | — |
| 011 | 4 | RTI Compare 0 Interrupt | RTI Compare 0 Interrupt | PINMMR30[16] = 1 | ePWM_A1 | PINMMR30[16] = 0 and PINMMR30[17] = 1 |
| 100 | 5 | N2HET1[12] | N2HET1[17] | — | N2HET1[17] | — |
| 101 | 6 | N2HET1[14] | N2HET1[19] | PINMMR30[24] = 1 | N2HET2[1] | PINMMR30[24] = 0 and PINMMR30[25] = 1 |
| 110 | 7 | GIOB[0] | N2HET1[11] | PINMMR31[0] = 1 | ePWM_A2 | PINMMR31[0] = 0 and PINMMR31[1] = 1 |
| 111 | 8 | GIOB[1] | N2HET2[13] | PINMMR32[16] = 1 | ePWM_AB | PINMMR31[8] = 0 and PINMMR31[9] = 1 |

**NOTE**

If ADEVT, N2HET1 or GIOB is used as a trigger source, the connection to the MibADC1 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by configuring the function as output onto the pad (through the mux control), or by driving the function from an external trigger source as input. If the mux control module is used to select different functionality instead of the ADEVT, N2HET1[x] or GIOB[x] signals, then care must be taken to disable these signals from triggering conversions; there is no multiplexing on the input connections.

If ePWM_B, ePWM_S2, ePWM_AB, N2HET2[1], N2HET2[5], N2HET2[13], N2HET1[11], N2HET1[17] or N2HET1[19] is used to trigger the ADC the connection to the ADC is made directly from the N2HET or ePWM module outputs. As a result, the ADC can be triggered without having to enable the signal from being output on a device terminal.

**NOTE**

For the RTI compare 0 interrupt source, the connection is made directly from the output of the RTI module. That is, the interrupt condition can be used as a trigger source even if the actual interrupt is not signaled to the CPU.

### 7.4.2.2 MIBADC2 Event Trigger Hookup

**Table 7-17. MIBADC2 Event Trigger Hookup**

| Group Source Select, G1SRC, G2SRC or EVSRC | Event # | Trigger Event Signal | | | | |
|---|---|---|---|---|---|---|
| | | PINMMR30[0] = 1 (default) | PINMMR30[0] = 0 and PINMMR30[1] = 1 | | | |
| | | | Option A | Control for Option A | Option B | Control for Option B |
| 000 | 1 | AD2EVT | AD2EVT | — | AD2EVT | — |
| 001 | 2 | N2HET1[8] | N2HET2[5] | PINMMR31[16] = 1 | ePWM_B | PINMMR31[16] = 0 and PINMMR31[17] = 1 |
| 010 | 3 | N2HET1[10] | N2HET1[27] | — | N2HET1[27] | — |
| 011 | 4 | RTI Compare 0 Interrupt | RTI Compare 0 Interrupt | PINMMR31[24] = 1 | ePWM_A1 | PINMMR31[24] = 0 and PINMMR31[25] = 1 |
| 100 | 5 | N2HET1[12] | N2HET1[17] | — | N2HET1[17] | — |
| 101 | 6 | N2HET1[14] | N2HET1[19] | PINMMR32[0] = 1 | N2HET2[1] | PINMMR32[0] = 0 and PINMMR32[1] = 1 |
| 110 | 7 | GIOB[0] | N2HET1[11] | PINMMR32[8] = 1 | ePWM_A2 | PINMMR32[8] = 0 and PINMMR32[9] = 1 |
| 111 | 8 | GIOB[1] | N2HET2[13] | PINMMR32[16] = 1 | ePWM_AB | PINMMR32[16] = 0 and PINMMR32[17] = 1 |

**NOTE**

If AD2EVT, N2HET1 or GIOB is used as a trigger source, the connection to the MibADC2 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by configuring the function as output onto the pad (through the mux control), or by driving the function from an external trigger source as input. If the mux control module is used to select different functionality instead of the AD2EVT, N2HET1[x] or GIOB[x] signals, then care must be taken to disable these signals from triggering conversions; there is no multiplexing on the input connections.

If ePWM_B, ePWM_S2, ePWM_AB, N2HET2[5], N2HET2[1], N2HET2[13], N2HET1[11], N2HET1[17] or N2HET1[19] is used to trigger the ADC the connection to the ADC is made directly from the N2HET or ePWM module outputs. As a result, the ADC can be triggered without having to enable the signal from being output on a device terminal.

**NOTE**

For the RTI compare 0 interrupt source, the connection is made directly from the output of the RTI module. That is, the interrupt condition can be used as a trigger source even if the actual interrupt is not signaled to the CPU.

#### 7.4.2.3 Controlling ADC1 and ADC2 Event Trigger Options Using SOC Output from ePWM Modules

As shown in Figure 7-5, the ePWMxSOCA and ePWMxSOCB outputs from each ePWM module are used to generate 4 signals – ePWM_B, ePWM_A1, ePWM_A2 and ePWM_AB, that are available to trigger the ADC based on the application requirement.

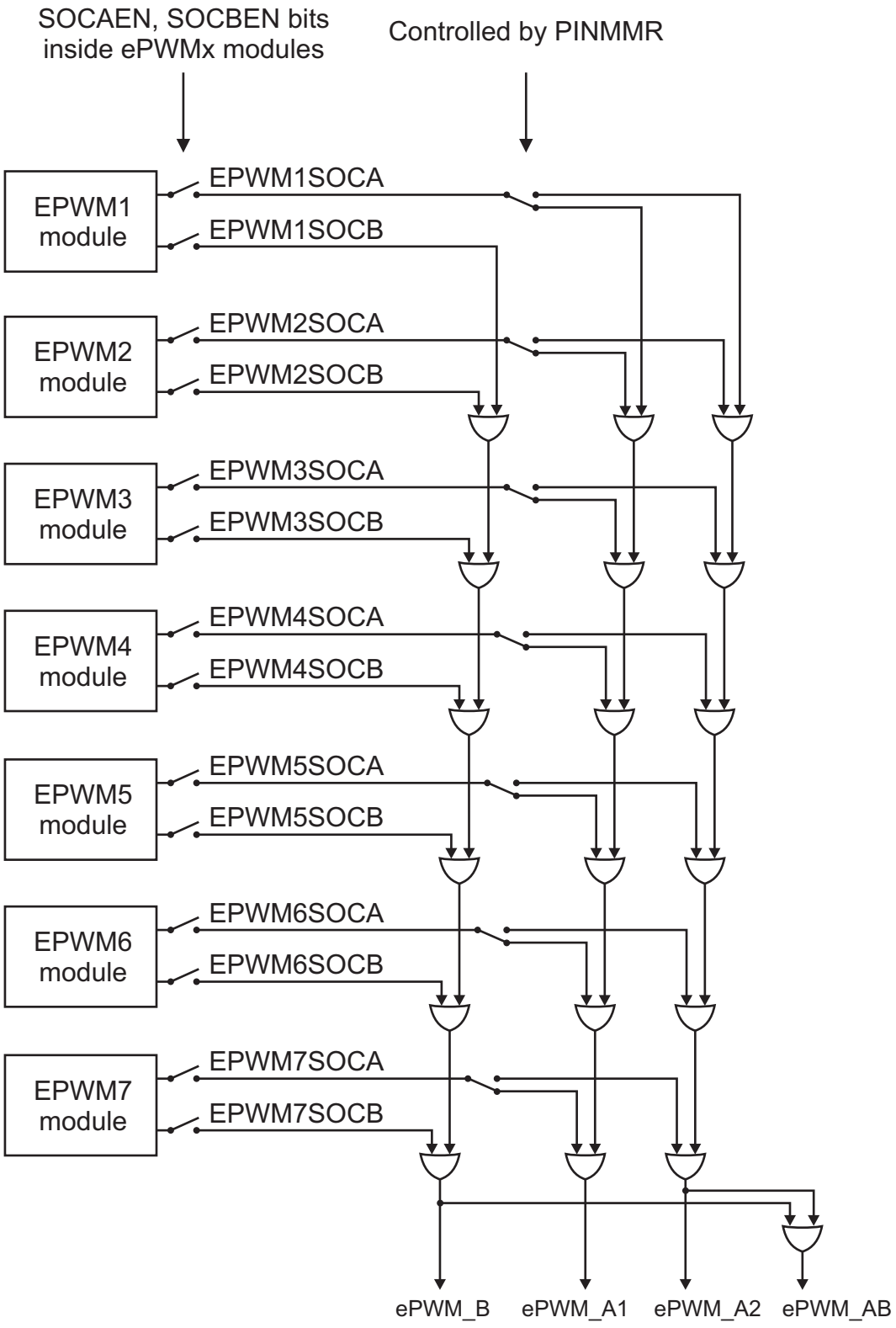



**Figure 7-5. ADC Trigger Source Generation from ePWMx**

**Table 7-18. Control Bit to SOC Output**

| Control Bit | SOC Output |
|---|---|
| PINMMR35[0] | SOC1A_SEL |
| PINMMR35[8] | SOC2A_SEL |
| PINMMR35[16] | SOC3A_SEL |
| PINMMR35[24] | SOC4A_SEL |
| PINMMR36[0] | SOC5A_SEL |
| PINMMR36[8] | SOC6A_SEL |
| PINMMR36[16] | SOC7A_SEL |

The SOCA output from each ePWM module is connected to a "switch" shown in Figure 7-5.

The logic equations for the 4 outputs from the combinational logic shown in Figure 7-5 are:

ePWM_B = SOC1B or SOC2B or SOC3B or SOC4B or SOC5B or SOC6B or SOC7B

ePWM_A1 = [ SOC1A and not(SOC1A_SEL) ] or [ SOC2A and not(SOC2A_SEL) ] or [ SOC3A and not(SOC3A_SEL) ] or [ SOC4A and not(SOC4A_SEL) ] or [ SOC5A and not(SOC5A_SEL) ] or [ SOC6A and not(SOC6A_SEL) ] or [ SOC7A and not(SOC7A_SEL) ]

ePWM_A2 = [ SOC1A and SOC1A_SEL ] or [ SOC2A and SOC2A_SEL ] or [ SOC3A and SOC3A_SEL ] or [ SOC4A and SOC4A_SEL ] or [ SOC5A and SOC5A_SEL ] or [ SOC6A and SOC6A_SEL ] or [ SOC7A and SOC7A_SEL ]

ePWM_AB = ePWM_B or ePWM_A2

### 7.4.3 ADC Electrical and Timing Specifications

**Table 7-19. MibADC Recommended Operating Conditions**

| Parameter | | MIN | MAX | Unit |
|---|---|---|---|---|
| $AD_{REFHI}$ | A-to-D high-voltage reference source | $AD_{REFLO}$ | $V_{CCAD}$ (1) | V |
| $AD_{REFLO}$ | A-to-D low-voltage reference source | $V_{SSAD}$ (1) | $AD_{REFHI}$ | V |
| $V_{AI}$ | Analog input voltage | $AD_{REFLO}$ | $AD_{REFHI}$ | V |
| $I_{AIK}$ | Analog input clamp current (2) ($V_{AI} < V_{SSAD} - 0.3$ or $V_{AI} > V_{CCAD} + 0.3$) | - 2 | 2 | mA |

(1) For $V_{CCAD}$ and $V_{SSAD}$ recommended operating conditions, see Section 5.4.
(2) Input currents into any ADC input channel outside the specified limits could affect conversion results of other channels.

**Table 7-20. MibADC Electrical Characteristics Over Full Ranges of Recommended Operating Conditions**

| Parameter | | Description/Conditions | | MIN | Nom | MAX | Unit |
|---|---|---|---|---|---|---|---|
| $R_{mux}$ | Analog input mux on-resistance | See Figure 7-6 | | | | 250 | Ω |
| $R_{samp}$ | ADC sample switch on-resistance | See Figure 7-6 | | | | 250 | Ω |
| $C_{mux}$ | Input mux capacitance | See Figure 7-6 | | | | 16 | pF |
| $C_{samp}$ | ADC sample capacitance | See Figure 7-6 | | | | 13 | pF |
| $I_{AIL}$ | Analog off-state input leakage current | $V_{CCAD}$ = 3.6V maximum | $V_{SSAD} \le V_{IN} < V_{SSAD}$ + 100mV | -300 | | 200 | nA |
| | | | $V_{SSAD}$ + 100mV ≤ $V_{IN} \le V_{CCAD}$ - 200mV | -200 | | 200 | nA |
| | | | $V_{CCAD}$ - 200mV < $V_{IN} \le V_{CCAD}$ | -200 | | 500 | nA |
| $I_{AIL}$ | Analog off-state input leakage current | $V_{CCAD}$ = 5.5V maximum | $V_{SSAD} \le V_{IN} < V_{SSAD}$ + 300mV | -1000 | | 250 | nA |
| | | | $V_{SSAD}$ + 300mV ≤ $V_{IN} \le V_{CCAD}$ - 300mV | -250 | | 250 | nA |
| | | | $V_{CCAD}$ - 300mV < $V_{IN} \le V_{CCAD}$ | -250 | | 1000 | nA |
| $I_{AOSB1}$ (1) | ADC1 Analog on-state input bias current | $V_{CCAD}$ = 3.6V maximum | $V_{SSAD} \le V_{IN} < V_{SSAD}$ + 100mV | -8 | | 2 | µA |
| | | | $V_{SSAD}$ + 100mV < $V_{IN} < V_{CCAD}$ - 200mV | -4 | | 2 | µA |
| | | | $V_{CCAD}$ - 200mV < $V_{IN} < V_{CCAD}$ | -4 | | 12 | µA |
| $I_{AOSB2}$ (1) | ADC2 Analog on-state input bias current | $V_{CCAD}$ = 3.6V maximum | $V_{SSAD} \le V_{IN} < V_{SSAD}$ + 100mV | -7 | | 2 | µA |
| | | | $V_{SSAD}$ + 100mV ≤ $V_{IN} \le V_{CCAD}$ - 200mV | -4 | | 2 | µA |
| | | | $V_{CCAD}$ - 200mV < $V_{IN} \le V_{CCAD}$ | -4 | | 10 | µA |
| $I_{AOSB1}$ (1) | ADC1 Analog on-state input bias current | $V_{CCAD}$ = 5.5V maximum | $V_{SSAD} \le V_{IN} < V_{SSAD}$ + 300mV | -10 | | 3 | µA |
| | | | $V_{SSAD}$ + 300mV ≤ $V_{IN} \le V_{CCAD}$ - 300mV | -5 | | 3 | µA |
| | | | $V_{CCAD}$ - 300mV < $V_{IN} \le V_{CCAD}$ | -5 | | 14 | µA |
| $I_{AOSB2}$ (1) | ADC2 Analog on-state input bias current | $V_{CCAD}$ = 5.5V maximum | $V_{SSAD} \le V_{IN} < V_{SSAD}$ + 300mV | -8 | | 3 | µA |
| | | | $V_{SSAD}$ + 300mV ≤ $V_{IN} \le V_{CCAD}$ - 300mV | -5 | | 3 | µA |
| | | | $V_{CCAD}$ - 300mV < $V_{IN} \le V_{CCAD}$ | -5 | | 12 | µA |
| $I_{ADREFHI}$ | $AD_{REFHI}$ input current | $AD_{REFHI} = V_{CCAD}$, $AD_{REFLO} = V_{SSAD}$ | | | | 3 | mA |
| $I_{CCAD}$ | Static supply current | Normal operating mode | | | | 15 | mA |
| | | ADC core in power down mode | | | | 5 | µA |

(1) If a shared channel is being converted by both ADC converters at the same time, the on-state leakage is equal to $I_{AOSB1} + I_{AOSB2}$

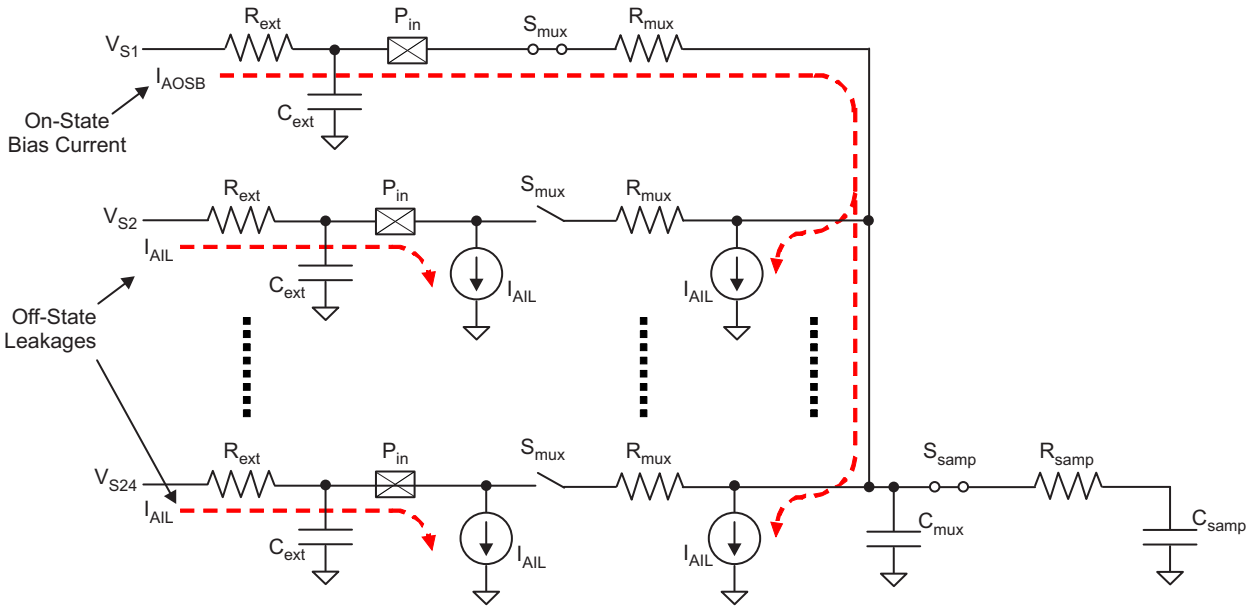



**Figure 7-6. MibADC Input Equivalent Circuit**

**Table 7-21. MibADC Timing Specifications**

| Parameter | | MIN | NOM | MAX | Unit |
|---|---|---|---|---|---|
| $t_{c(ADCLK)}$ (1) | Cycle time, MibADC clock | 0.033 | | | µs |
| $t_{d(SH)}$ (2) | Delay time, sample and hold time | 0.2 | | | µs |
| $t_{d(PU-ADV)}$ | Delay time from ADC power on until first input can be sampled | 1 | | | µs |
| **12-bit mode** | | | | | |
| $t_{d©)}$ | Delay time, conversion time | 0.4 | | | µs |
| $t_{d(SHC)}$ (3) | Delay time, total sample/hold and conversion time | 0.6 | | | µs |
| **10-bit mode** | | | | | |
| $t_{d©)}$ | Delay time, conversion time | 0.33 | | | µs |
| $t_{d(SHC)}$ (3) | Delay time, total sample/hold and conversion time | 0.53 | | | µs |

(1) The MibADC clock is the ADCLK, generated by dividing down the VCLK by a prescale factor defined by the ADCLOCKCR register bits 4:0.
(2) The sample and hold time for the ADC conversions is defined by the ADCLK frequency and the AD<GP>SAMP register for each conversion group. The sample time needs to be determined by accounting for the external impedance connected to the input channel as well as the ADC's internal impedance.
(3) This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors, for example, the prescale settings.

**Table 7-22. MibADC Operating Characteristics Over Full Ranges of Recommended Operating Conditions(1)(2)**

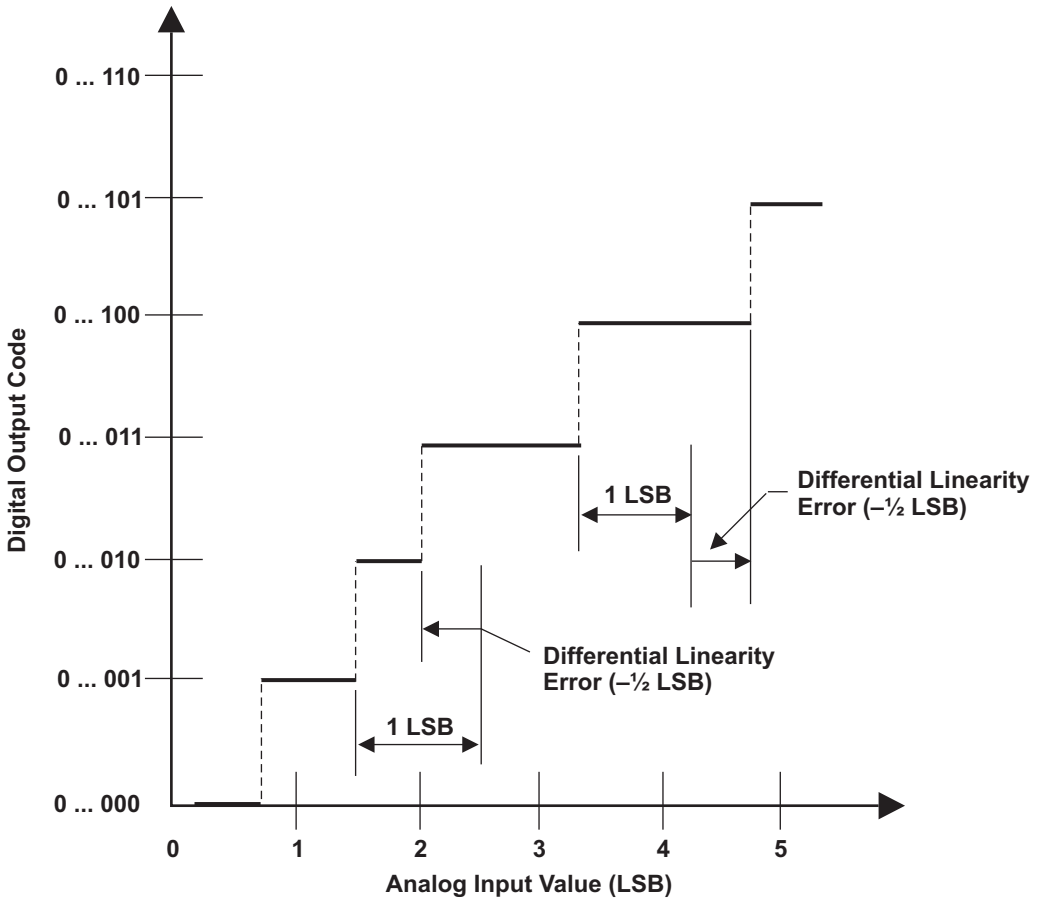
| Parameter | | Description/Conditions | | MIN | Type | MAX | Unit |
|---|---|---|---|---|---|---|---|
| CR | Conversion range over which specified accuracy is maintained | $AD_{REFHI}$ - $AD_{REFLO}$ | | 3 | | 5.5 | V |
| $Z_{SET}$ | Zero Scale Offset | Difference between the first ideal transition (from code 000h to 001h) and the actual transition | 10-bit mode | | | 1 | LSB |
| | | | 12-bit mode | | | 2 | LSB |
| $F_{SET}$ | Full Scale Offset | Difference between the range of the measured code transitions (from first to last) and the range of the ideal code transitions | 10-bit mode | | | 2 | LSB |
| | | | 12-bit mode | | | 3 | LSB |
| $E_{DNL}$ | Differential nonlinearity error | Difference between the actual step width and the ideal value. (See Figure 7-7) | 10-bit mode | | | ± 1.5 | LSB |
| | | | 12-bit mode | | | ± 2 | LSB |
| $E_{INL}$ | Integral nonlinearity error | Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error. | 10-bit mode | | | ± 2 | LSB |
| | | | 12-bit mode | | | ± 2 | LSB |
| $E_{TOT}$ | Total unadjusted error | Maximum value of the difference between an analog value and the ideal midstep value. | 10-bit mode | | | ± 2 | LSB |
| | | | 12-bit mode | | | ± 4 | LSB |

(1) 1 LSB = $(AD_{REFHI} – AD_{REFLO})/ 2^{12}$ for 12-bit mode
(2) 1 LSB = $(AD_{REFHI} – AD_{REFLO})/ 2^{10}$ for 10-bit mode

### 7.4.4 Performance (Accuracy) Specifications

#### 7.4.4.1 MibADC Nonlinearity Errors

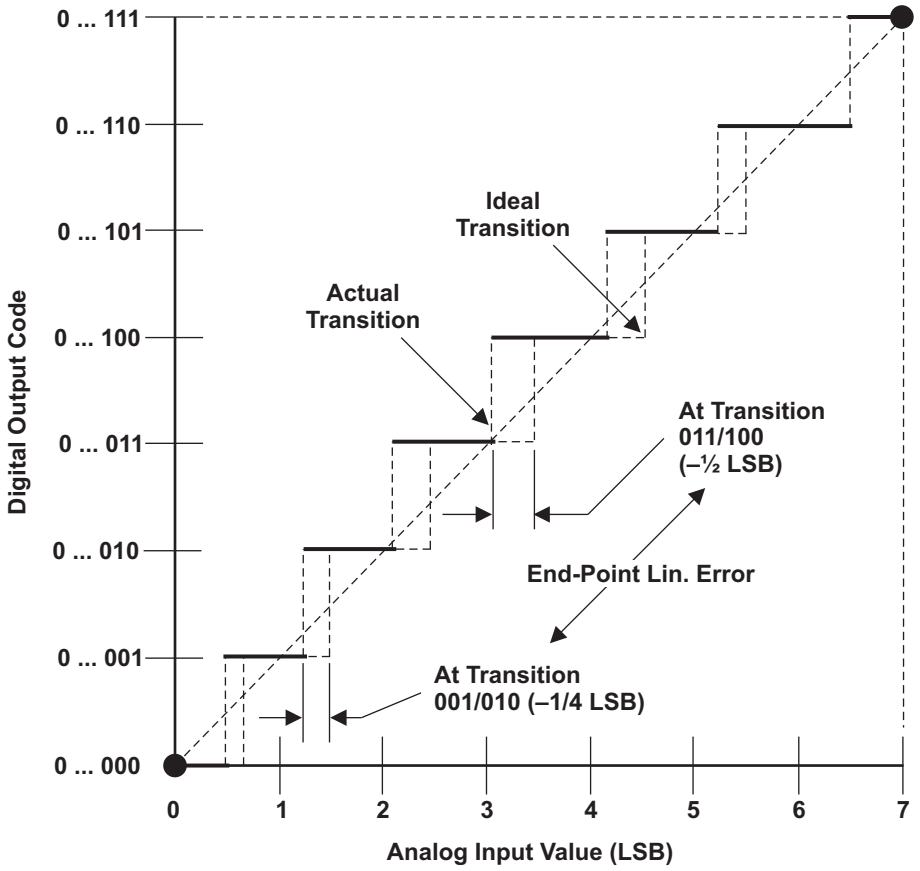
The differential nonlinearity error shown in Figure 7-7 (sometimes referred to as differential linearity) is the difference between an actual step width and the ideal value of 1 LSB.




NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{12}$

**Figure 7-7. Differential Nonlinearity (DNL) Error**

The integral nonlinearity error shown in Figure 7-8 (sometimes referred to as linearity error) is the deviation of the values on the actual transfer function from a straight line.

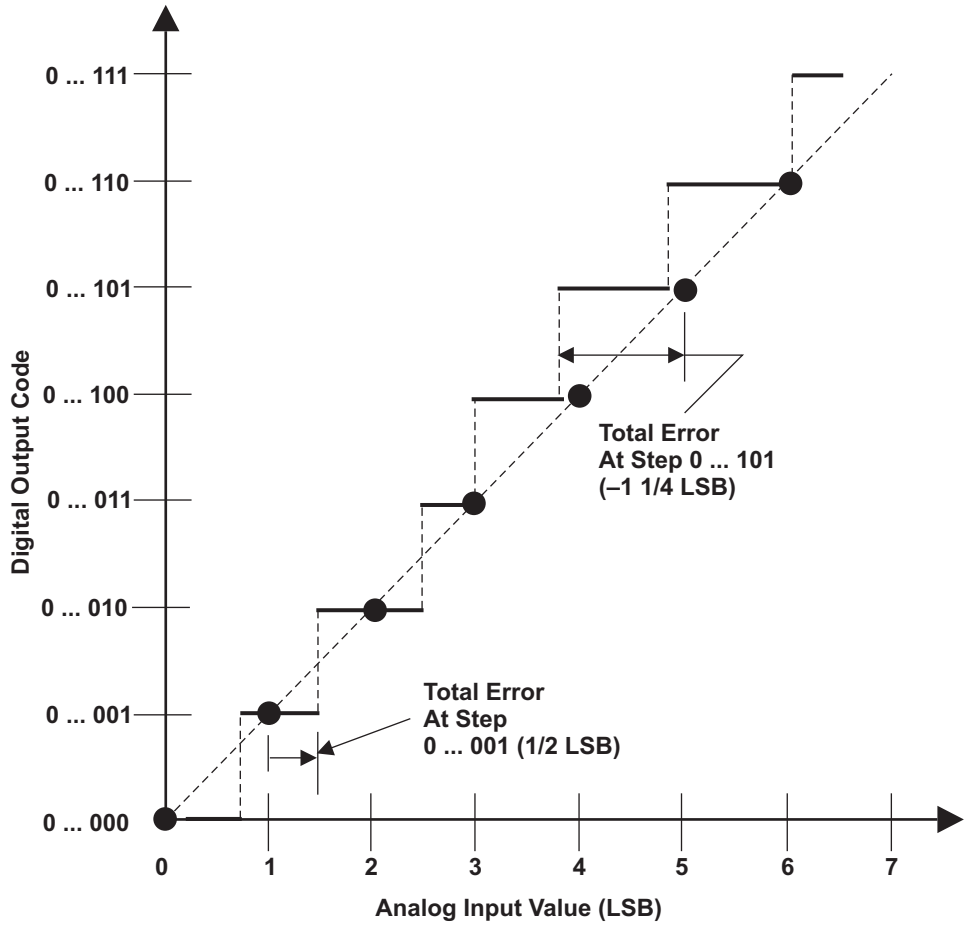



NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{12}$

**Figure 7-8. Integral Nonlinearity (INL) Error**

### 7.4.4.2 MibADC Total Error

The absolute accuracy or total error of an MibADC as shown in Figure 7-9 is the maximum value of the difference between an analog value and the ideal midstep value.




NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{12}$

**Figure 7-9. Absolute Accuracy (Total) Error**

## 7.5 General-Purpose Input/Output

The GPIO module on this device supports two ports, GIOA and GIOB. The I/O pins are bidirectional and bit-programmable. Both GIOA and GIOB support external interrupt capability.

### *7.5.1 Features*

The GPIO module has the following features:

- Each IO pin can be configured as:
  - Input
  - Output
  - Open Drain
- The interrupts have the following characteristics:
  - Programmable interrupt detection either on both edges or on a single edge (set in GIOINTDET)
  - Programmable edge-detection polarity, either rising or falling edge (set in GIOPOL register)
  - Individual interrupt flags (set in GIOFLG register)
  - Individual interrupt enables, set and cleared through GIOENASET and GIOENACLR registers respectively
  - Programmable interrupt priority, set through GIOLVLSET and GIOLVLCLR registers
- Internal pullup/pulldown allows unused I/O pins to be left unconnected

For information on input and output timings see Section 5.11 and Section 5.12

## 7.6 Enhanced High-End Timer (N2HET)

The N2HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The N2HET can be used for pulse width modulated outputs, capture or compare inputs, or general-purpose I/O. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses.

### *7.6.1 Features*

The N2HET module has the following features:

- Programmable timer for input and output timing functions
- Reduced instruction set (30 instructions) for dedicated time and angle functions
- 160 words of instruction RAM protected by parity
- User defined number of 25-bit virtual counters for timer, event counters and angle counters
- 7-bit hardware counters for each pin allow up to 32-bit resolution in conjunction with the 25-bit virtual counters
- Up to 32 pins usable for input signal measurements or output signal generation
- Programmable suppression filter for each input pin with adjustable limiting frequency
- Low CPU overhead and interrupt load
- Efficient data transfer to or from the CPU memory with dedicated High-End-Timer Transfer Unit (HTU) or DMA
- Diagnostic capabilities with different loopback mechanisms and pin status read back functionality

### *7.6.2 N2HET RAM Organization*

The timer RAM uses 4 RAM banks, where each bank has two port access capability. This means that one RAM address may be written while another address is read. The RAM words are 96-bits wide, which are split into three 32-bit fields (program, control, and data).

### 7.6.3 Input Timing Specifications

All of the N2HET channels have an enhanced pulse capture circuit. The N2HET instructions PCNT and WCAP use this circuit to achieve the input timing requirements shown in Figure 7-10 and Table 7-23 below.

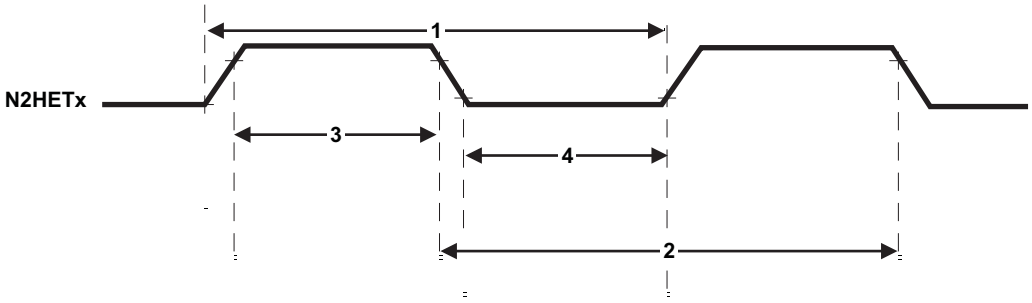



**Figure 7-10. N2HET Input Capture Timings**

**Table 7-23. Input Timing Requirements for N2HET Channels with Enhanced Pulse Capture**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1, 2 | Input signal period, PCNT or WCAP | (HRP) (LRP) $tc_{(VCLK2)}$ + 2 | $2^{25}$ (HRP) (LRP) $tc_{(VCLK2)}$ - 2 | ns |
| 3 | Input signal high phase, PCNT or WCAP | 2 (HRP) $tc_{(VCLK2)}$ + 2 | $2^{25}$ (HRP) (LRP) $tc_{(VCLK2)}$ - 2 | ns |
| 4 | Input signal low phase, PCNT or WCAP | 2 (HRP) $tc_{(VCLK2)}$ + 2 | $2^{25}$ (HRP) (LRP) $tc_{(VCLK2)}$ - 2 | ns |

### 7.6.4 N2HET1-N2HET2 Synchronization

In some applications the N2HET resolutions must be synchronized. Some other applications require a single time base to be used for all PWM outputs and input timing captures.

The N2HET provides such a synchronization mechanism. The Clk_master/slave (HETGCR.16) configures the N2HET in master or slave mode (default is slave mode). A N2HET in master mode provides a signal to synchronize the prescalers of the slave N2HET. The slave N2HET synchronizes its loop resolution to the loop resolution signal sent by the master. The slave does not require this signal after it receives the first synchronization signal. However, anytime the slave receives the re-synchronization signal from the master, the slave must synchronize itself again..

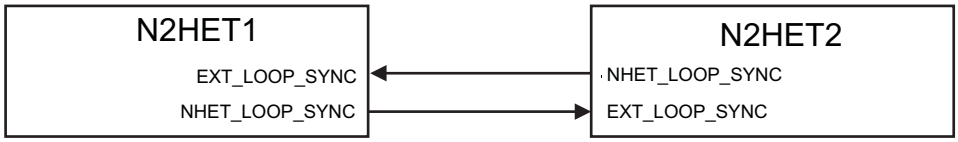



**Figure 7-11. N2HET1 – N2HET2 Synchronization Hookup**

### 7.6.5 N2HET Checking

#### 7.6.5.1 Internal Monitoring

To assure correctness of the high-end timer operation and output signals, the two N2HET modules can be used to monitor each other's signals as shown in Figure 7-12. The direction of the monitoring is controlled by the I/O multiplexing control module.

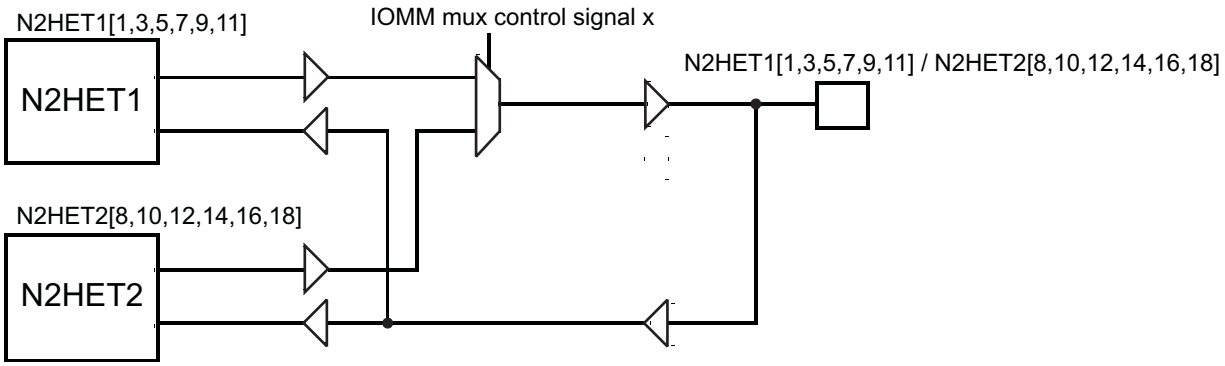



**Figure 7-12. N2HET Monitoring**

#### 7.6.5.2 Output Monitoring using Dual Clock Comparator (DCC)

N2HET1[31] is connected as a clock source for counter 1 in DCC1. This allows the application to measure the frequency of the pulse-width modulated (PWM) signal on N2HET1[31].

Similarly, N2HET2[0] is connected as a clock source for counter 1 in DCC2. This allows the application to measure the frequency of the pulse-width modulated (PWM) signal on N2HET2[0].

Both N2HET1[31] and N2HET2[0] can be configured to be internal-only channels. That is, the connection to the DCC module is made directly from the output of the N2HETx module (from the input of the output buffer).

For more information on DCC see Section 6.7.3.

### *7.6.6 Disabling N2HET Outputs*

Some applications require the N2HET outputs to be disabled under some fault condition. The N2HET module provides this capability through the "Pin Disable" input signal. This signal, when driven low, causes the N2HET outputs identified by a programmable register (HETPINDIS) to be tri-stated. For more details on the "N2HET Pin Disable" feature, see the device-specific Terminal Reference Manual.

GIOA[5] is connected to the "Pin Disable" input for N2HET1, and GIOB[2] is connected to the "Pin Disable" input for N2HET2.

### 7.6.7 High-End Timer Transfer Unit (HTU)

A High End Timer Transfer Unit (HTU) can perform DMA type transactions to transfer N2HET data to or from main memory. A Memory Protection Unit (MPU) is built into the HTU.

#### 7.6.7.1 Features

- CPU and DMA independent
- Master Port to access system memory
- 8 control packets supporting dual buffer configuration
- Control packet information is stored in RAM protected by parity
- Event synchronization (HET transfer requests)
- Supports 32 or 64 bit transactions
- Addressing modes for HET address (8 byte or 16 byte) and system memory address (fixed, 32 bit or 64bit)
- One shot, circular and auto switch buffer transfer modes
- Request lost detection

#### 7.6.7.2 Trigger Connections

**Table 7-24. HTU1 Request Line Connection**

| Modules | Request Source | HTU1 Request |
|---|---|---|
| N2HET1 | HTUREQ[0] | HTU1 DCP[0] |
| N2HET1 | HTUREQ[1] | HTU1 DCP[1] |
| N2HET1 | HTUREQ[2] | HTU1 DCP[2] |
| N2HET1 | HTUREQ[3] | HTU1 DCP[3] |
| N2HET1 | HTUREQ[4] | HTU1 DCP[4] |
| N2HET1 | HTUREQ[5] | HTU1 DCP[5] |
| N2HET1 | HTUREQ[6] | HTU1 DCP[6] |
| N2HET1 | HTUREQ[7] | HTU1 DCP[7] |

**Table 7-25. HET TU2 Request Line Connection**

| Modules | Request Source | HET TU2 Request |
|---|---|---|
| N2HET2 | HTUREQ[0] | HTU2 DCP[0] |
| N2HET2 | HTUREQ[1] | HTU2 DCP[1] |
| N2HET2 | HTUREQ[2] | HTU2 DCP[2] |
| N2HET2 | HTUREQ[3] | HTU2 DCP[3] |
| N2HET2 | HTUREQ[4] | HTU2 DCP[4] |
| N2HET2 | HTUREQ[5] | HTU2 DCP[5] |
| N2HET2 | HTUREQ[6] | HTU2 DCP[6] |
| N2HET2 | HTUREQ[7] | HTU2 DCP[7] |

## 7.7 Controller Area Network (DCAN)

The DCAN supports the CAN 2.0B protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 megabit per second (Mbps). The DCAN is ideal for applications operating in noisy and harsh environments (for example, automotive and industrial fields) that require reliable serial communication or multiplexed wiring.

### 7.7.1 Features

Features of the DCAN module include:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 MBit/s
- The CAN kernel can be clocked by the oscillator for baud-rate generation.
- 64 mailboxes on each DCAN
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Message RAM protected by parity
- Direct access to Message RAM during test mode
- CAN Rx / Tx pins configurable as general purpose IO pins
- Message RAM Auto Initialization
- DMA support

For more information on the DCAN see the TMS570LS12x/11x Technical Reference Manual (SPNU515).

### 7.7.2 Electrical and Timing Specifications

**Table 7-26. Dynamic Characteristics for the DCANx TX and RX pins**

| Parameter | | MIN | MAX | Unit |
|---|---|---|---|---|
| $t_{d(CANnTX)}$ | Delay time, transmit shift register to CANnTX pin (1) | | 15 | ns |
| $t_{d(CANnRX)}$ | Delay time, CANnRX pin to receive shift register | | 5 | ns |

(1) These values do not include rise/fall times of the output buffer.

## 7.8 Local Interconnect Network Interface (LIN)

The SCI/LIN module can be programmed to work either as an SCI or as a LIN. The core of the module is an SCI. The SCI's hardware features are augmented to achieve LIN compatibility.

The SCI module is a universal asynchronous receiver-transmitter that implements the standard nonreturn to zero format. The SCI can be used to communicate, for example, through an RS-232 port or over a K-line.

The LIN standard is based on the SCI (UART) serial data link format. The communication concept is single-master/multiple-slave with a message identification for multi-cast transmission between any network nodes.

### *7.8.1 LIN Features*

The following are features of the LIN module:

- Compatible to LIN 1.3, 2.0 and 2.1 protocols
- Multibuffered receive and transmit units DMA capability for minimal CPU intervention
- Identification masks for message filtering
- Automatic Master Header Generation
  - Programmable Synch Break Field
  - Synch Field
  - Identifier Field
- Slave Automatic Synchronization
  - Synch break detection
  - Optional baudrate update
  - Synchronization Validation
- $2^{31}$ programmable transmission rates with 7 fractional bits
- Error detection
- 2 Interrupt lines with priority encoding

## 7.9 Serial Communication Interface (SCI)

### 7.9.1 Features

- Standard universal asynchronous receiver-transmitter (UART) communication
- Supports full- or half-duplex operation
- Standard nonreturn to zero (NRZ) format
- Double-buffered receive and transmit functions
- Configurable frame format of 3 to 13 bits per character based on the following:
  - Data word length programmable from one to eight bits
  - Additional address bit in address-bit mode
  - Parity programmable for zero or one parity bit, odd or even parity
  - Stop programmable for one or two stop bits
- Asynchronous or isosynchronous communication modes
- Two multiprocessor communication formats allow communication between more than two devices.
- Sleep mode is available to free CPU resources during multiprocessor communication.
- The 24-bit programmable baud rate supports $2^{24}$ different baud rates provide high accuracy baud rate selection.
- Four error flags and Five status flags provide detailed information regarding SCI events.
- Capability to use DMA for transmit and receive data.

## 7.10 Inter-Integrated Circuit (I2C)

The inter-integrated circuit (I2C) module is a multi-master communication module providing an interface between the microcontroller and devices compliant with Philips Semiconductor I2C-bus specification version 2.1 and connected by an I2C-bus. This module will support any slave or master I2C compatible device.

### *7.10.1 Features*

The I2C has the following features:

- Compliance to the Philips I2C bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
  - Bit/Byte format transfer
  - 7-bit and 10-bit device addressing modes
  - General call
  - START byte
  - Multi-master transmitter/ slave receiver mode
  - Multi-master receiver/ slave transmitter mode
  - Combined master transmit/receive and receive/transmit mode
  - Transfer rates of 10 kbps up to 400 kbps (Phillips fast-mode rate)
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Seven interrupts that can be used by the CPU
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

**NOTE**

This I2C module does not support:

- High-speed (HS) mode
- C-bus compatibility mode
- The combined format in 10-bit address mode (the I2C sends the slave address second byte every time it sends the slave address first byte)

### 7.10.2 I2C I/O Timing Specifications

**Table 7-27. I2C Signals (SDA and SCL) Switching Characteristics(1)**

| Parameter | | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $t_{c(I2CCLK)}$ | Cycle time, Internal Module clock for I2C, prescaled from VCLK | 75.2 | 149 | 75.2 | 149 | ns |
| $f_{(SCL)}$ | SCL Clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | µs |
| $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | µs |
| $t_{h(SCLL-SDAL)}$ | Hold time, SCL low after SDA low (for a repeated START condition) | 4 | | 0.6 | | µs |
| $t_{w(SCLL)}$ | Pulse duration, SCL low | 4.7 | | 1.3 | | µs |
| $t_{w(SCLH)}$ | Pulse duration, SCL high | 4 | | 0.6 | | µs |
| $t_{su(SDA-SCLH)}$ | Setup time, SDA valid before SCL high | 250 | | 100 | | ns |
| $t_{h(SDA-SCLL)}$ | Hold time, SDA valid after SCL low (for I2C bus devices) | 0 | 3.45(2) | 0 | 0.9 | µs |
| $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | µs |
| $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for STOP condition) | 4.0 | | 0.6 | | µs |
| $t_{w(SP)}$ | Pulse duration, spike (must be suppressed) | | | 0 | 50 | ns |
| $C_b$(3) | Capacitive load for each bus line | | 400 | | 400 | pF |

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) The maximum $t_{h(SDA-SCLL)}$ for I2C bus devices has only to be met if the device does not stretch the low period ($t_{w(SCLL)}$) of the SCL signal.
(3) $C_b$ = The total capacitance of one bus line in pF.

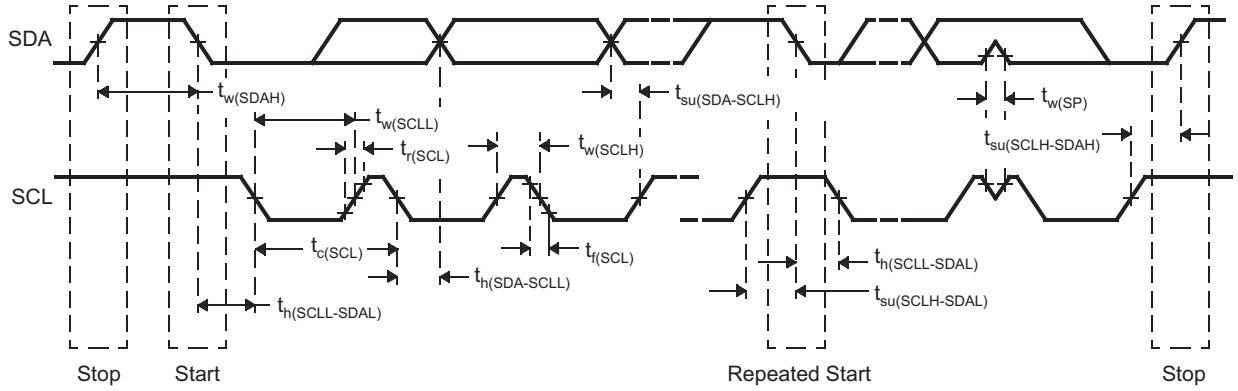



**Figure 7-13. I2C Timings**

**NOTE**

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the LOW period ($t_{w(SCLL)}$) of the SCL signal.
- A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{su(SDA-SCLH)}$.
- $C_b$ = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

## 7.11 Multibuffered / Standard Serial Peripheral Interface

The MibSPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted in and out of the device at a programmed bit-transfer rate. Typical applications for the SPI include interfacing to external peripherals, such as I/Os, memories, display drivers, and analog-to-digital converters.

### *7.11.1 Features*

Both Standard and MibSPI modules have the following features:

- 16-bit shift register
- Receive buffer register
- 8-bit baud clock generator
- SPICLK can be internally-generated (master mode) or received from an external clock source (slave mode)
- Each word transferred can have a unique format
- SPI I/Os not used in the communication can be used as digital input/output signals

**Table 7-28. MibSPI/SPI Configurations PGE Package**

| MibSPIx/SPIx | I/Os |
|---|---|
| MibSPI1 | MIBSPI1SIMO[1:0], MIBSPI1SOMI[1:0], MIBSPI1CLK, MIBSPI1nCS[5:4,2:0], MIBSPI1nENA |
| MibSPI3 | MIBSPI3SIMO[0], MIBSPI3SOMI[0], MIBSPI3CLK, MIBSPI3nCS[5:0], MIBSPI3nENA |
| MibSPI5 | MIBSPI5SIMO[0], MIBSPI5SOMI[2:0], MIBSPI5CLK, MIBSPI5nCS[0], MIBSPI5nENA |
| SPI4 | SPI4SIMO[0], SPI4SOMI[0], SPI4CLK, SPI4nCS[0], SPI4nENA |

**Table 7-29. MibSPI/SPI Configurations ZWT Package**

| MibSPIx/SPIx | I/Os |
|---|---|
| MibSPI1 | MIBSPI1SIMO[1:0], MIBSPI1SOMI[1:0], MIBSPI1CLK, MIBSPI1nCS[5:0], MIBSPI1nENA |
| MibSPI3 | MIBSPI3SIMO[0], MIBSPI3SOMI[0], MIBSPI3CLK, MIBSPI3nCS[5:0], MIBSPI3nENA |
| MibSPI5 | MIBSPI5SIMO[3:0], MIBSPI5SOMI[3:0], MIBSPI5CLK, MIBSPI5nCS[3:0], MIBSPI5nENA |
| SPI2 | SPI2SIMO[0], SPI2SOMI[0], SPI2CLK, SPI2nCS[1:0], SPI2nENA |
| SPI4 | SPI4SIMO[0], SPI4SOMI[0], SPI4CLK, SPI4nCS[0], SPI4nENA |

### *7.11.2 MibSPI Transmit and Receive RAM Organization*

The Multibuffer RAM is comprised of 128 buffers. Each entry in the Multibuffer RAM consists of 4 parts: a 16-bit transmit field, a 16-bit receive field, a 16-bit control field and a 16-bit status field. The Multibuffer RAM can be partitioned into multiple transfer group with variable number of buffers each. Each MibSPIx module supports 8 transfer groups.

### *7.11.3 MibSPI Transmit Trigger Events*

Each of the transfer groups can be configured individually. For each of the transfer groups a trigger event and a trigger source can be chosen. A trigger event can be for example a rising edge or a permanent low level at a selectable trigger source. For example, up to 15 trigger sources are available for use by each transfer group.

#### 7.11.3.1 MIBSPI1 Event Trigger Hookup

**Table 7-30. MIBSPI1 Event Trigger Hookup**

| Event # | TGxCTRL TRIGSRC[3:0] | Trigger |
|---|---|---|
| Disabled | 0000 | No trigger source |
| EVENT0 | 0001 | GIOA[0] |
| EVENT1 | 0010 | GIOA[1] |
| EVENT2 | 0011 | GIOA[2] |
| EVENT3 | 0100 | GIOA[3] |
| EVENT4 | 0101 | GIOA[4] |
| EVENT5 | 0110 | GIOA[5] |
| EVENT6 | 0111 | GIOA[6] |
| EVENT7 | 1000 | GIOA[7] |
| EVENT8 | 1001 | N2HET1[8] |
| EVENT9 | 1010 | N2HET1[10] |
| EVENT10 | 1011 | N2HET1[12] |
| EVENT11 | 1100 | N2HET1[14] |
| EVENT12 | 1101 | N2HET1[16] |
| EVENT13 | 1110 | N2HET1[18] |
| EVENT14 | 1111 | Internal Tick counter |

**NOTE**

For N2HET1 trigger sources, the connection to the MibSPI1 module trigger input is made from the input side of the output buffer (at the N2HET1 module boundary). This way, a trigger condition can be generated even if the N2HET1 signal is not selected to be output on the pad.

**NOTE**

For GIOx trigger sources, the connection to the MibSPI1 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by selecting the GIOx pin as an output pin and selecting the pin to be a GIOx pin, or by driving the GIOx pin from an external trigger source. If the mux control module is used to select different functionality instead of the GIOx signal, then care must be taken to disable GIOx from triggering MibSPI1 transfers; there is no multiplexing on the input connections.

#### 7.11.3.2 MIBSPI3 Event Trigger Hookup

**Table 7-31. MIBSPI3 Event Trigger Hookup**

| Event # | TGxCTRL TRIGSRC[3:0] | Trigger |
|---|---|---|
| Disabled | 0000 | No trigger source |
| EVENT0 | 0001 | GIOA[0] |
| EVENT1 | 0010 | GIOA[1] |
| EVENT2 | 0011 | GIOA[2] |
| EVENT3 | 0100 | GIOA[3] |
| EVENT4 | 0101 | GIOA[4] |
| EVENT5 | 0110 | GIOA[5] |
| EVENT6 | 0111 | GIOA[6] |
| EVENT7 | 1000 | GIOA[7] |
| EVENT8 | 1001 | N2HET1[8] |

**Table 7-31. MIBSPI3 Event Trigger Hookup (continued)**

| Event # | TGxCTRL TRIGSRC[3:0] | Trigger |
|---|---|---|
| EVENT9 | 1010 | N2HET1[10] |
| EVENT10 | 1011 | N2HET1[12] |
| EVENT11 | 1100 | N2HET1[14] |
| EVENT12 | 1101 | N2HET1[16] |
| EVENT13 | 1110 | N2HET1[18] |
| EVENT14 | 1111 | Internal Tick counter |

**NOTE**

For N2HET1 trigger sources, the connection to the MibSPI3 module trigger input is made from the input side of the output buffer (at the N2HET1 module boundary). This way, a trigger condition can be generated even if the N2HET1 signal is not selected to be output on the pad.

**NOTE**

For GIOx trigger sources, the connection to the MibSPI3 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by selecting the GIOx pin as an output pin and selecting the pin to be a GIOx pin, or by driving the GIOx pin from an external trigger source. If the mux control module is used to select different functionality instead of the GIOx signal, then care must be taken to disable GIOx from triggering MibSPI3 transfers; there is no multiplexing on the input connections.

### 7.11.3.3 MIBSPI5 Event Trigger Hookup

**Table 7-32. MIBSPI5 Event Trigger Hookup**

| Event # | TGxCTRL TRIGSRC[3:0] | Trigger |
|---|---|---|
| Disabled | 0000 | No trigger source |
| EVENT0 | 0001 | GIOA[0] |
| EVENT1 | 0010 | GIOA[1] |
| EVENT2 | 0011 | GIOA[2] |
| EVENT3 | 0100 | GIOA[3] |
| EVENT4 | 0101 | GIOA[4] |
| EVENT5 | 0110 | GIOA[5] |
| EVENT6 | 0111 | GIOA[6] |
| EVENT7 | 1000 | GIOA[7] |
| EVENT8 | 1001 | N2HET1[8] |
| EVENT9 | 1010 | N2HET1[10] |
| EVENT10 | 1011 | N2HET1[12] |
| EVENT11 | 1100 | N2HET1[14] |
| EVENT12 | 1101 | N2HET1[16] |
| EVENT13 | 1110 | N2HET1[18] |
| EVENT14 | 1111 | Internal Tick counter |

**NOTE**

For N2HET1 trigger sources, the connection to the MibSPI5 module trigger input is made from the input side of the output buffer (at the N2HET1 module boundary). This way, a trigger condition can be generated even if the N2HET1 signal is not selected to be output on the pad.

**NOTE**

For GIOx trigger sources, the connection to the MibSPI5 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by selecting the GIOx pin as an output pin and selecting the pin to be a GIOx pin, or by driving the GIOx pin from an external trigger source. If the mux control module is used to select different functionality instead of the GIOx signal, then care must be taken to disable GIOx from triggering MibSPI5 transfers; there is no multiplexing on the input connections.

### 7.11.4 MibSPI/SPI Master Mode I/O Timing Specifications

**Table 7-33. SPI Master Mode External Timing Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)**

| NO. | Parameter | | | MIN | MAX | Unit |
|---|---|---|---|---|---|---|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK(4) | | 40 | $256t_{c(VCLK)}$ | ns |
| 2(5) | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 0) | | $0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 1) | | $0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | |
| 3(5) | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 0) | | $0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 1) | | $0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | |
| 4(5) | $t_{d(SPCH-SIMO)M}$ | Delay time, SPISIMO valid before SPICLK low (clock polarity = 0) | | $0.5t_{c(SPC)M} - 6$ | | ns |
| | $t_{d(SPCL-SIMO)M}$ | Delay time, SPISIMO valid before SPICLK high (clock polarity = 1) | | $0.5t_{c(SPC)M} - 6$ | | |
| 5(5) | $t_{v(SPCL-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0) | | $0.5t_{c(SPC)M} - t_{f(SPC)} - 4$ | | ns |
| | $t_{v(SPCH-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1) | | $0.5t_{c(SPC)M} - t_{r(SPC)} - 4$ | | |
| 6(5) | $t_{su(SOMI-SPCL)M}$ | Setup time, SPISOMI before SPICLK low (clock polarity = 0) | | $t_{f(SPC)} + 2.2$ | | ns |
| | $t_{su(SOMI-SPCH)M}$ | Setup time, SPISOMI before SPICLK high (clock polarity = 1) | | $t_{r(SPC)} + 2.2$ | | |
| 7(5) | $t_{h(SPCL-SOMI)M}$ | Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0) | | 10 | | ns |
| | $t_{h(SPCH-SOMI)M}$ | Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1) | | 10 | | |
| 8(6) | $t_{C2TDELAY}$ | Setup time CS active until SPICLK high (clock polarity = 0) | CSHOLD = 0 | $C2TDELAY*t_{c(VCLK)} + 2*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 7$ | $(C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$ | ns |
| | | | CSHOLD = 1 | $C2TDELAY*t_{c(VCLK)} + 3*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 7$ | $(C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$ | |
| | | Setup time CS active until SPICLK low (clock polarity = 1) | CSHOLD = 0 | $C2TDELAY*t_{c(VCLK)} + 2*t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 7$ | $(C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 5.5$ | ns |
| | | | CSHOLD = 1 | $C2TDELAY*t_{c(VCLK)} + 3*t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 7$ | $(C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 5.5$ | |
| 9(6) | $t_{T2CDELAY}$ | Hold time SPICLK low until CS inactive (clock polarity = 0) | | $0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} - 7$ | $0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} + 11$ | ns |
| | | Hold time SPICLK high until CS inactive (clock polarity = 1) | | $0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + tr(SPICS) - 7$ | $0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} + 11$ | ns |
| 10 | $t_{SPIENA}$ | SPIENAn Sample point | | $(C2TDELAY+1) * t_{c(VCLK)} - t_{f(SPICS)} - 29$ | $(C2TDELAY+1)*t_{c(VCLK)}$ | ns |
| 11 | $t_{SPIENAW}$ | SPIENAn Sample point from write to buffer | | | $(C2TDELAY+2)*t_{c(VCLK)}$ | ns |

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is cleared.
(2) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$
(3) For rise and fall timings, see Table 5-7.
(4) When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS+1)t_{c(VCLK)} \geq 40$ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(VCLK)} \geq 40$ns.
The external load on the SPICLK pin must be less than 60pF.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(6) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

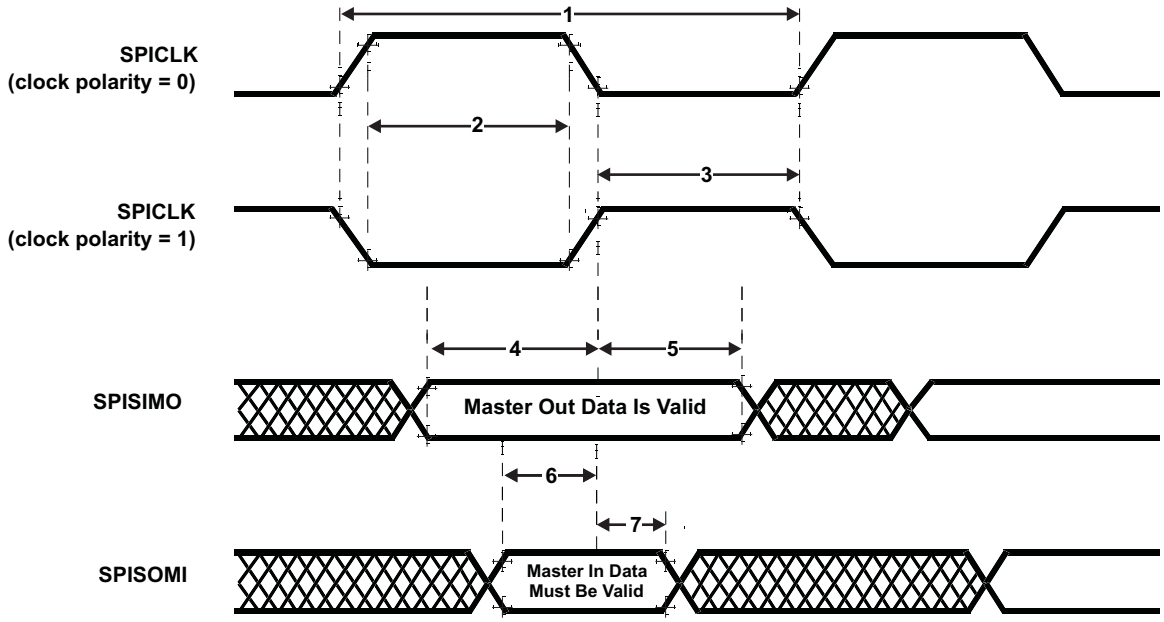



**Figure 7-14. SPI Master Mode External Timing (CLOCK PHASE = 0)**

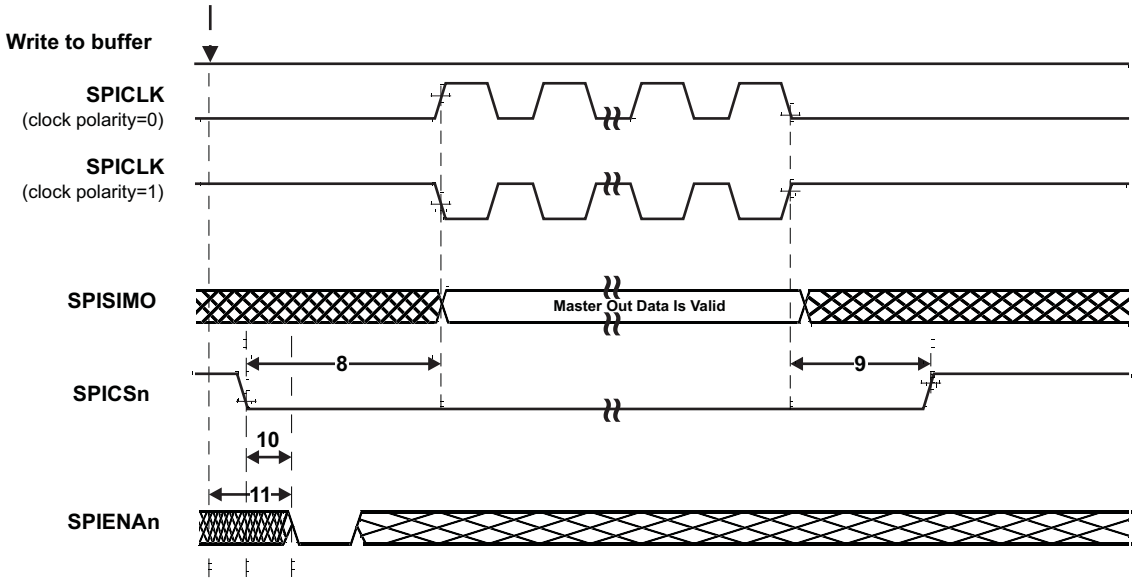



**Figure 7-15. SPI Master Mode Chip Select Timing (CLOCK PHASE = 0)**

**Table 7-34. SPI Master Mode External Timing Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)**

| NO. | Parameter | | | MIN | MAX | Unit |
|---|---|---|---|---|---|---|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK (4) | | 40 | $256t_{c(VCLK)}$ | ns |
| 2(5) | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 0) | | $0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 1) | | $0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | |
| 3(5) | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 0) | | $0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 1) | | $0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | |
| 4(5) | $t_{v(SIMO-SPCH)M}$ | Valid time, SPICLK high after SPISIMO data valid (clock polarity = 0) | | $0.5t_{c(SPC)M} - 6$ | | ns |
| | $t_{v(SIMO-SPCL)M}$ | Valid time, SPICLK low after SPISIMO data valid (clock polarity = 1) | | $0.5t_{c(SPC)M} - 6$ | | |
| 5(5) | $t_{v(SPCH-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0) | | $0.5t_{c(SPC)M} - t_{r(SPC)} - 4$ | | ns |
| | $t_{v(SPCL-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1) | | $0.5t_{c(SPC)M} - t_{f(SPC)} - 4$ | | |
| 6(5) | $t_{su(SOMI-SPCH)M}$ | Setup time, SPISOMI before SPICLK high (clock polarity = 0) | | $t_{r(SPC)} + 2.2$ | | ns |
| | $t_{su(SOMI-SPCL)M}$ | Setup time, SPISOMI before SPICLK low (clock polarity = 1) | | $t_{f(SPC)} + 2.2$ | | |
| 7(5) | $t_{v(SPCH-SOMI)M}$ | Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0) | | 10 | | ns |
| | $t_{v(SPCL-SOMI)M}$ | Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1) | | 10 | | |
| 8(6) | $t_{C2TDELAY}$ | Setup time CS active until SPICLK high (clock polarity = 0) | CSHOLD = 0 | $0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 7$ | $0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$ | ns |
| | | | CSHOLD = 1 | $0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 7$ | $0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$ | |
| | | Setup time CS active until SPICLK low (clock polarity = 1) | CSHOLD = 0 | $0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 7$ | $0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 5.5$ | ns |
| | | | CSHOLD = 1 | $0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 7$ | $0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 5.5$ | |
| 9(6) | $t_{T2CDELAY}$ | Hold time SPICLK low until CS inactive (clock polarity = 0) | | $T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} - 7$ | $T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} + 11$ | ns |
| | | Hold time SPICLK high until CS inactive (clock polarity = 1) | | $T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} - 7$ | $T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} + 11$ | ns |
| 10 | $t_{SPIENA}$ | SPIENAn Sample Point | | $(C2TDELAY+1)* t_{c(VCLK)} - t_{f(SPICS)} - 29$ | $(C2TDELAY+1)*t_{c(VCLK)}$ | ns |
| 11 | $t_{SPIENAW}$ | SPIENAn Sample point from write to buffer | | | $(C2TDELAY+2)*t_{c(VCLK)}$ | ns |

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.
(2) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$
(3) For rise and fall timings, see the Table 5-7.
(4) When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS +1)t_{c(VCLK)} \geq 40ns$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(VCLK)} \geq 40ns$.
The external load on the SPICLK pin must be less than 60pF.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(6) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

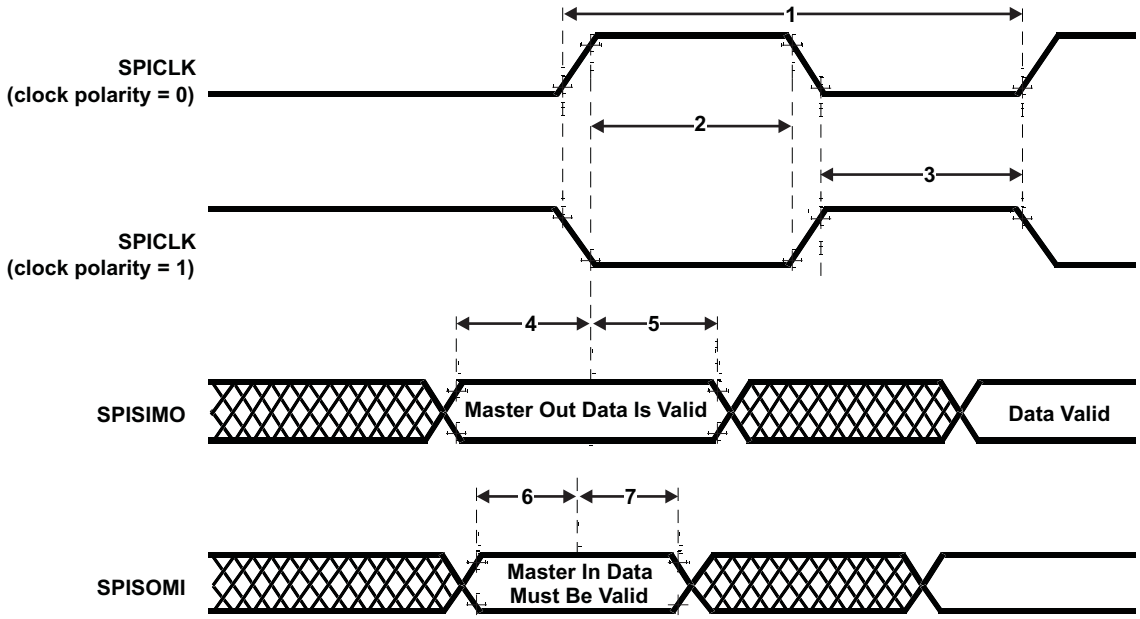



**Figure 7-16. SPI Master Mode External Timing (CLOCK PHASE = 1)**

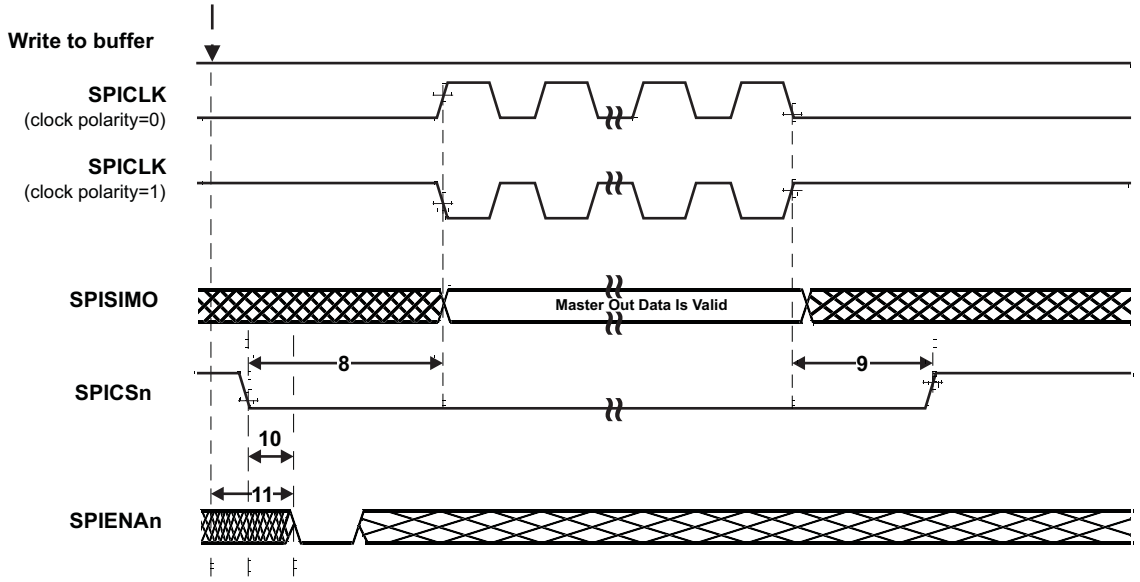



**Figure 7-17. SPI Master Mode Chip Select Timing (CLOCK PHASE = 1)**

### 7.11.5 SPI Slave Mode I/O Timings

**Table 7-35. SPI Slave Mode External Timing Parameters (CLOCK PHASE = 0, SPICLK = input, SPISIMO = input, and SPISOMI = output)(1)(2)(3)(4)**

| NO. | Parameter | | MIN | MAX | Unit |
|---|---|---|---|---|---|
| 1 | $t_{c(SPC)S}$ | Cycle time, SPICLK(5) | 40 | | ns |
| 2(6) | $t_{w(SPCH)S}$ | Pulse duration, SPICLK high (clock polarity = 0) | 14 | | ns |
| | $t_{w(SPCL)S}$ | Pulse duration, SPICLK low (clock polarity = 1) | 14 | | |
| 3(6) | $t_{w(SPCL)S}$ | Pulse duration, SPICLK low (clock polarity = 0) | 14 | | ns |
| | $t_{w(SPCH)S}$ | Pulse duration, SPICLK high (clock polarity = 1) | 14 | | |
| 4(6) | $t_{d(SPCH-SOMI)S}$ | Delay time, SPISOMI valid after SPICLK high (clock polarity = 0) | | $t_{rf(SOMI)}$ + 20 | ns |
| | $t_{d(SPCL-SOMI)S}$ | Delay time, SPISOMI valid after SPICLK low (clock polarity = 1) | | $t_{rf(SOMI)}$ + 20 | |
| 5(6) | $t_{h(SPCH-SOMI)S}$ | Hold time, SPISOMI data valid after SPICLK high (clock polarity =0) | 2 | | ns |
| | $t_{h(SPCL-SOMI)S}$ | Hold time, SPISOMI data valid after SPICLK low (clock polarity =1) | 2 | | |
| 6(6) | $t_{su(SIMO-SPCL)S}$ | Setup time, SPISIMO before SPICLK low (clock polarity = 0) | 4 | | ns |
| | $t_{su(SIMO-SPCH)S}$ | Setup time, SPISIMO before SPICLK high (clock polarity = 1) | 4 | | |
| 7(6) | $t_{h(SPCL-SIMO)S}$ | Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0) | 2 | | ns |
| | $t_{h(SPCH-SIMO)S}$ | Hold time, SPISIMO data valid after S PICLK high (clock polarity = 1) | 2 | | |
| 8 | $t_{d(SPCL-SENAH)S}$ | Delay time, SPIENAn high after last SPICLK low (clock polarity = 0) | $1.5t_{c(VCLK)}$ | $2.5t_{c(VCLK)}+t_{r(ENAn)}+22$ | ns |
| | $t_{d(SPCH-SENAH)S}$ | Delay time, SPIENAn high after last SPICLK high (clock polarity = 1) | $1.5t_{c(VCLK)}$ | $2.5t_{c(VCLK)}+t_{r(ENAn)}+22$ | |
| 9 | $t_{d(SCSL-SENAL)S}$ | Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer) | $t_{f(ENAn)}$ | $t_{c(VCLK)}+t_{f(ENAn)}+27$ | ns |

(1) The MASTER bit (SPIGCR1.0) is cleared and the CLOCK PHASE bit (SPIFMTx.16) is cleared.
(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(VCLK)}$, where PS = prescale value set in SPIFMTx.[15:8].
(3) For rise and fall timings, see Table 5-7.
(4) $t_{c(VCLK)}$ = interface clock cycle time = $1 / f_{(VCLK)}$
(5) When the SPI is in Slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(VCLK)} \geq 40$ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(VCLK)} \geq 40$ns.
(6) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

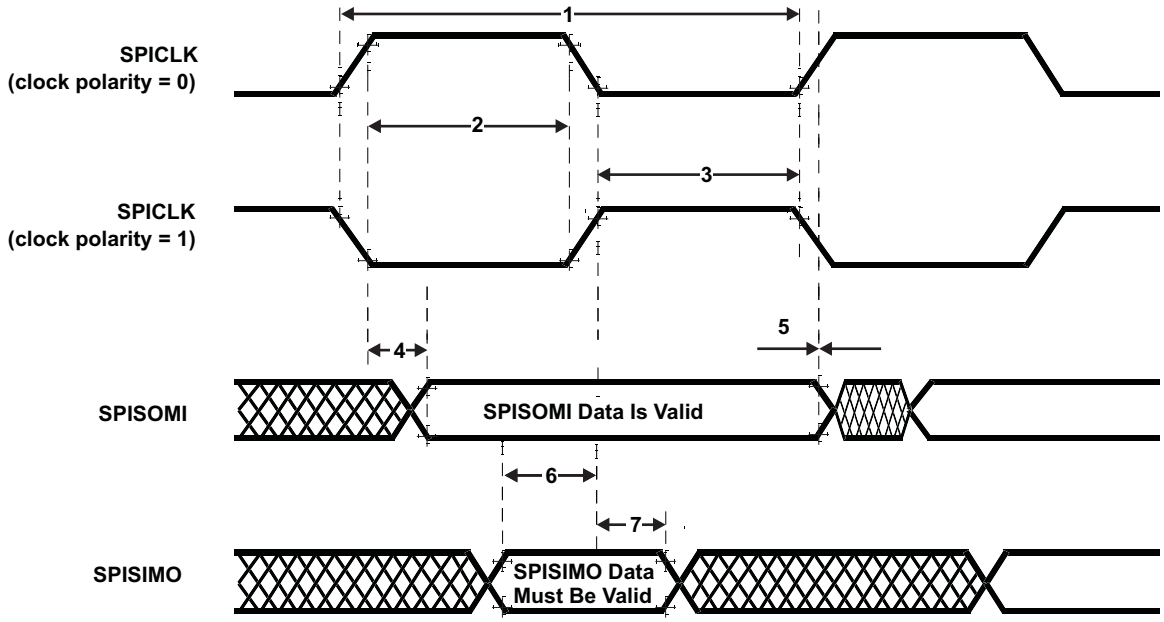



**Figure 7-18. SPI Slave Mode External Timing (CLOCK PHASE = 0)**

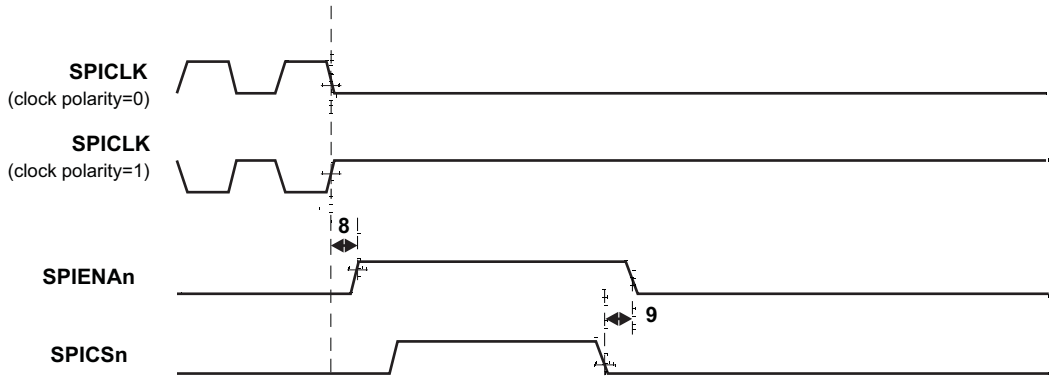



**Figure 7-19. SPI Slave Mode Enable Timing (CLOCK PHASE = 0)**

**Table 7-36. SPI Slave Mode External Timing Parameters (CLOCK PHASE = 1, SPICLK = input, SPISIMO = input, and SPISOMI = output)(1)(2)(3)(4)**

| NO. | Parameter | | MIN | MAX | Unit |
|---|---|---|---|---|---|
| 1 | $t_{c(SPC)S}$ | Cycle time, SPICLK(5) | 40 | | ns |
| 2(6) | $t_{w(SPCH)S}$ | Pulse duration, SPICLK high (clock polarity = 0) | 14 | | ns |
| | $t_{w(SPCL)S}$ | Pulse duration, SPICLK low (clock polarity = 1) | 14 | | |
| 3(6) | $t_{w(SPCL)S}$ | Pulse duration, SPICLK low (clock polarity = 0) | 14 | | ns |
| | $t_{w(SPCH)S}$ | Pulse duration, SPICLK high (clock polarity = 1) | 14 | | |
| 4(6) | $t_{d(SOMI-SPCL)S}$ | Delay time, SPISOMI data valid after SPICLK low (clock polarity = 0) | | $t_{rf(SOMI)}$ + 20 | ns |
| | $t_{d(SOMI-SPCH)S}$ | Delay time, SPISOMI data valid after SPICLK high (clock polarity = 1) | | $t_{rf(SOMI)}$ + 20 | |
| 5(6) | $t_{h(SPCL-SOMI)S}$ | Hold time, SPISOMI data valid after SPICLK high (clock polarity =0) | 2 | | ns |
| | $t_{h(SPCH-SOMI)S}$ | Hold time, SPISOMI data valid after SPICLK low (clock polarity =1) | 2 | | |
| 6(6) | $t_{su(SIMO-SPCH)S}$ | Setup time, SPISIMO before SPICLK high (clock polarity = 0) | 4 | | ns |
| | $t_{su(SIMO-SPCL)S}$ | Setup time, SPISIMO before SPICLK low (clock polarity = 1) | 4 | | |
| 7(6) | $t_{v(SPCH-SIMO)S}$ | High time, SPISIMO data valid after SPICLK high (clock polarity = 0) | 2 | | ns |
| | $t_{v(SPCL-SIMO)S}$ | High time, SPISIMO data valid after SPICLK low (clock polarity = 1) | 2 | | |
| 8 | $t_{d(SPCH-SENAH)S}$ | Delay time, SPIENAn high after last SPICLK high (clock polarity = 0) | $1.5t_{c(VCLK)}$ | $2.5t_{c(VCLK)}+t_{r(ENAn)}$ + 22 | ns |
| | $t_{d(SPCL-SENAH)S}$ | Delay time, SPIENAn high after last SPICLK low (clock polarity = 1) | $1.5t_{c(VCLK)}$ | $2.5t_{c(VCLK)}+t_{r(ENAn)}$ + 22 | |
| 9 | $t_{d(SCSL-SENAL)S}$ | Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer) | $t_{f(ENAn)}$ | $t_{c(VCLK)}+t_{f(ENAn)}$+ 27 | ns |
| 10 | $t_{d(SCSL-SOMI)S}$ | Delay time, SOMI valid after SPICSn low (if new data has been written to the SPI buffer) | $t_{c(VCLK)}$ | $2t_{c(VCLK)}+t_{rf(SOMI)}$+ 28 | ns |

(1) The MASTER bit (SPIGCR1.0) is cleared and the CLOCK PHASE bit (SPIFMTx.16) is set.
(2) If the SPI is in slave mode, the following must be true: tc(SPC)S ≤ (PS + 1) tc(VCLK), where PS = prescale value set in SPIFMTx.[15:8].
(3) For rise and fall timings, see Table 5-7.
(4) $t_{c(VCLK)}$ = interface clock cycle time = 1 /$f_{(VCLK)}$
(5) When the SPI is in Slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS+1)t_{c(VCLK)} \geq 40$ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(VCLK)} \geq 40$ns.
(6) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

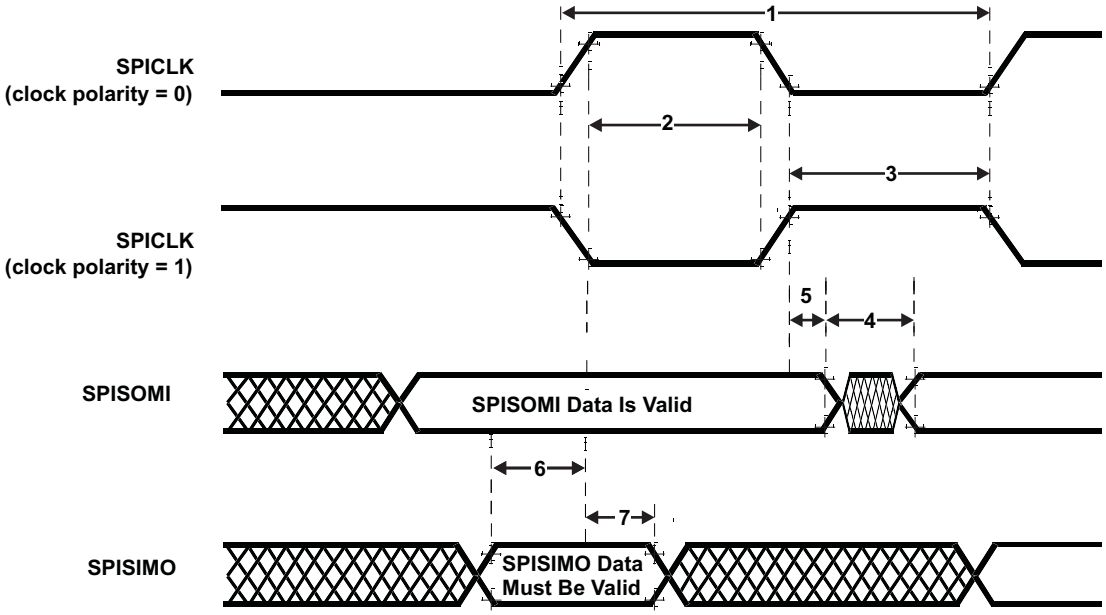



**Figure 7-20. SPI Slave Mode External Timing (CLOCK PHASE = 1)**

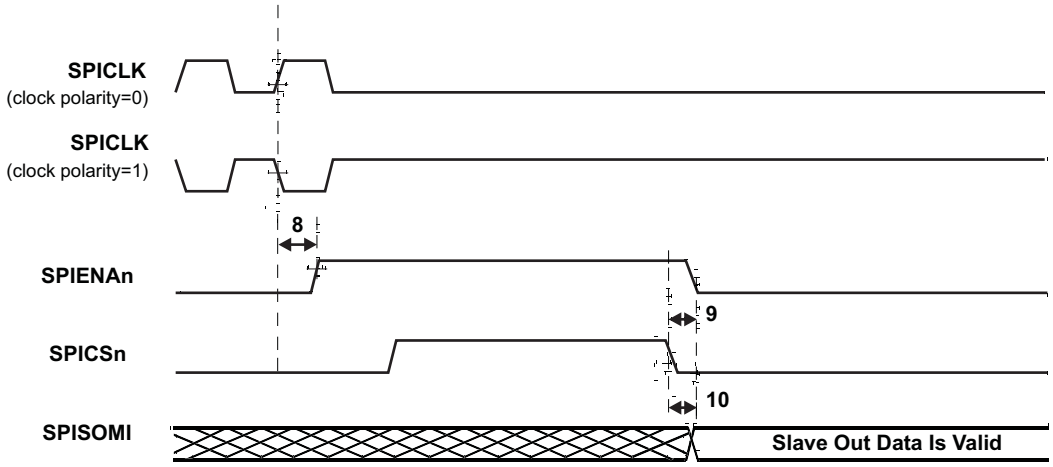



**Figure 7-21. SPI Slave Mode Enable Timing (CLOCK PHASE = 1)**

# 8 Device and Documentation Support

## 8.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all devices and support tools. Each commercial family member has one of three prefixes: TMX, TMP, or TMS (for example,TMS570LS1224). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

**TMX** Experimental device that is not necessarily representative of the final device's electrical specifications.

**TMP** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

**TMS** Fully-qualified production device.

TMX and TMP devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

The figure below illustrates the numbering and symbol nomenclature for the TMS570LS1224 .

| Full Part # | TMS | 570 | LS | 12 | 2 | 4 | B | ZWT | Q | Q1 | R |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Orderable Part # | TMX | 570 | | 12 | 2 | 4 | B | ZWT | Q | Q1 | R |

**Prefix: TM**
TMS = Fully Qualified
TMP = Prototype
TMX = Samples

**Core Technology:**
570 = Cortex R4F

**Architecture:**
LS = Dual CPUs in Lockstep
(not included in orderable part #)

**Flash Memory Size:**
12 = 1.25MB

**RAM MemorySize:**
2 = 192kB

**Peripheral Set:**
4 = no FlexRay, no Ethernet

**Die Revision:**
A = Die Revision A
B = Die Revision B

**Package Type:**
ZWT = 337-Pin Plastic BGA with pb-free solder ball
PGE = 144 Pin Plastic Quad Flatpack

**Temperature Range:**
Q = -40...+125°C

**Quality Designator:**
Q1 = Automotive

**Shipping Options:**
R = Tape and Reel

**Figure 8-1. TMS570LS1224 Device Numbering Conventions**

## 8.2 Documentation Support

### 8.2.1 Related Documentation from Texas Instruments

The following documents describe the *TMS570LS11x/12x* microcontroller..

**SPNU515** ***TMS570LS12x/11x 16/32-Bit RISC Flash Microcontroller Technical Reference Manual*** details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the device.

**SPNZ199** ***TMS570LS12x/11x Microcontroller, Silicon Revision B, Silicon Errata*** describes the usage notes and known exceptions to the functional specifications for the device silicon revision B.

**SPNZ218** ***TMS570LS12x/11x Microcontroller, Silicon Revision C, Silicon Errata*** describes the usage notes and known exceptions to the functional specifications for the device silicon revision C.

### 8.2.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**TI Embedded Processors Wiki** ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 8.3 Trademarks

E2E is a trademark of Texas Instruments.
CoreSight is a trademark of ARM Limited.
ARM, Cortex are registered trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere.


## 8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 8.6 Device Identification

### 8.6.1 Device Identification Code Register

The device identification code register identifies several aspects of the device including the silicon version. The details of the device identification code register are shown in Table 8-1. The device identification code register value for this device is:

- Rev A = 0x8046AD05
- Rev B = 0x8046AD15
- Rev C = 0x8046AD1D

**Figure 8-2. Device ID Bit Allocation Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CP-15 | UNIQUE ID | | | | | | | | | | | | | | TECH |
| R-1 | R-00000000100011 | | | | | | | | | | | | | | R-0 |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TECH | | | I/O VOLTAGE | PERIPH PARITY | FLASH ECC | | RAM ECC | VERSION | | | | | 1 | 0 | 1 |
| R-101 | | | R-0 | R-1 | R-10 | | R-1 | R-00011 | | | | | R-1 | R-0 | R-1 |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Table 8-1. Device ID Bit Allocation Register Field Descriptions**

| Bit | Field | Value | Description |
|---|---|---|---|
| 31 | CP15 | | Indicates the presence of coprocessor 15 |
| | | 1 | CP15 present |
| 30-17 | UNIQUE ID | 100011 | Unique device identification number<br>This bitfield holds a unique number for a dedicated device configuration (die). |
| 16-13 | TECH | | Process technology on which the device is manufactured. |
| | | 0101 | F021 |
| 12 | I/O VOLTAGE | | I/O voltage of the device. |
| | | 0 | I/O are 3.3v |
| 11 | PERIPHERAL PARITY | 1 | Peripheral Parity<br>Parity on peripheral memories |
| 10-9 | FLASH ECC | | Flash ECC |
| | | 10 | Program memory with ECC |
| 8 | RAM ECC | | Indicates if RAM memory ECC is present. |
| | | 1 | ECC implemented |
| 7-3 | REVISION | | Revision of the Device. |
| 2-0 | 101 | | The platform family ID is always 0b101 |

### 8.6.2 Die Identification Registers

The two die ID registers at addresses 0xFFFFFF7C and 0xFFFFFF80 form a 64-bit dieid with the information as shown in Table 8-2.

**Table 8-2. Die-ID Registers**

| Item | # of Bits | Bit Location |
|---|---|---|
| X Coordinate on Wafer | 12 | 0xFFFFFF7C[11:0] |
| Y Coordinate on Wafer | 12 | 0xFFFFFF7C[23:12] |
| Wafer # | 8 | 0xFFFFFF7C[31:24] |
| Lot # | 24 | 0xFFFFFF80[23:0] |

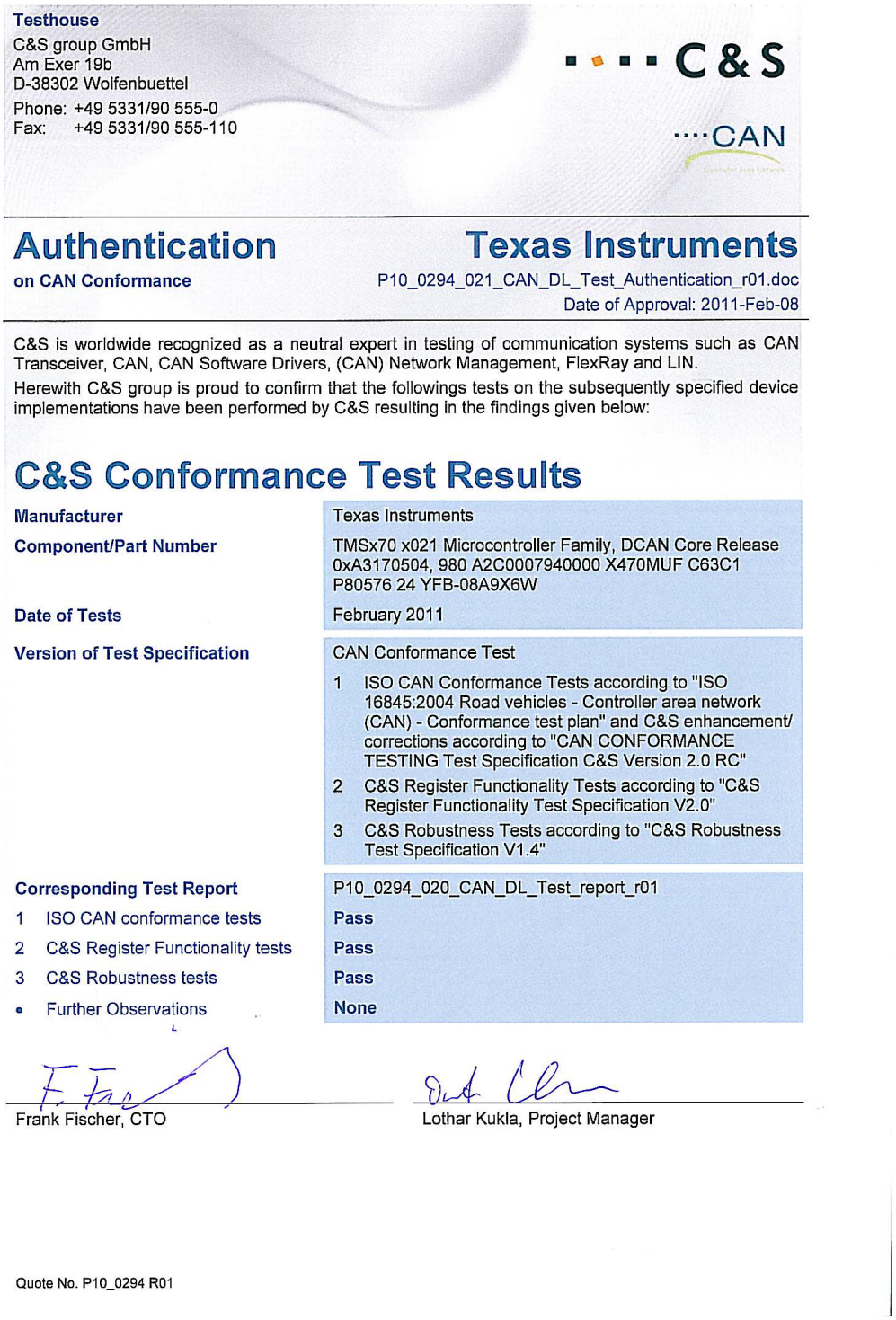
**Table 8-2. Die-ID Registers (continued)**

| Item | # of Bits | Bit Location |
|---|---|---|
| Reserved | 8 | 0xFFFFFF80[31:24] |

## 8.7 Module Certifications

The following communications modules have received certification of adherence to a standard.

### 8.7.1 DCAN Certification



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C&S
CAN

**Authentication**
on CAN Conformance

**Texas Instruments**
P10_0294_021_CAN_DL_Test_Authentication_r01.doc
Date of Approval: 2011-Feb-08

C&S is worldwide recognized as a neutral expert in testing of communication systems such as CAN Transceiver, CAN, CAN Software Drivers, (CAN) Network Management, FlexRay and LIN.

Herewith C&S group is proud to confirm that the followings tests on the subsequently specified device implementations have been performed by C&S resulting in the findings given below:

## C&S Conformance Test Results

| | |
|---|---|
| **Manufacturer** | Texas Instruments |
| **Component/Part Number** | TMSx70 x021 Microcontroller Family, DCAN Core Release 0xA3170504, 980 A2C0007940000 X470MUF C63C1 P80576 24 YFB-08A9X6W |
| **Date of Tests** | February 2011 |
| **Version of Test Specification** | CAN Conformance Test<br>1 ISO CAN Conformance Tests according to "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan" and C&S enhancement/ corrections according to "CAN CONFORMANCE TESTING Test Specification C&S Version 2.0 RC"<br>2 C&S Register Functionality Tests according to "C&S Register Functionality Test Specification V2.0"<br>3 C&S Robustness Tests according to "C&S Robustness Test Specification V1.4" |
| **Corresponding Test Report** | P10_0294_020_CAN_DL_Test_report_r01 |
| 1 ISO CAN conformance tests | **Pass** |
| 2 C&S Register Functionality tests | **Pass** |
| 3 C&S Robustness tests | **Pass** |
| • Further Observations | **None** |

Frank Fischer, CTO

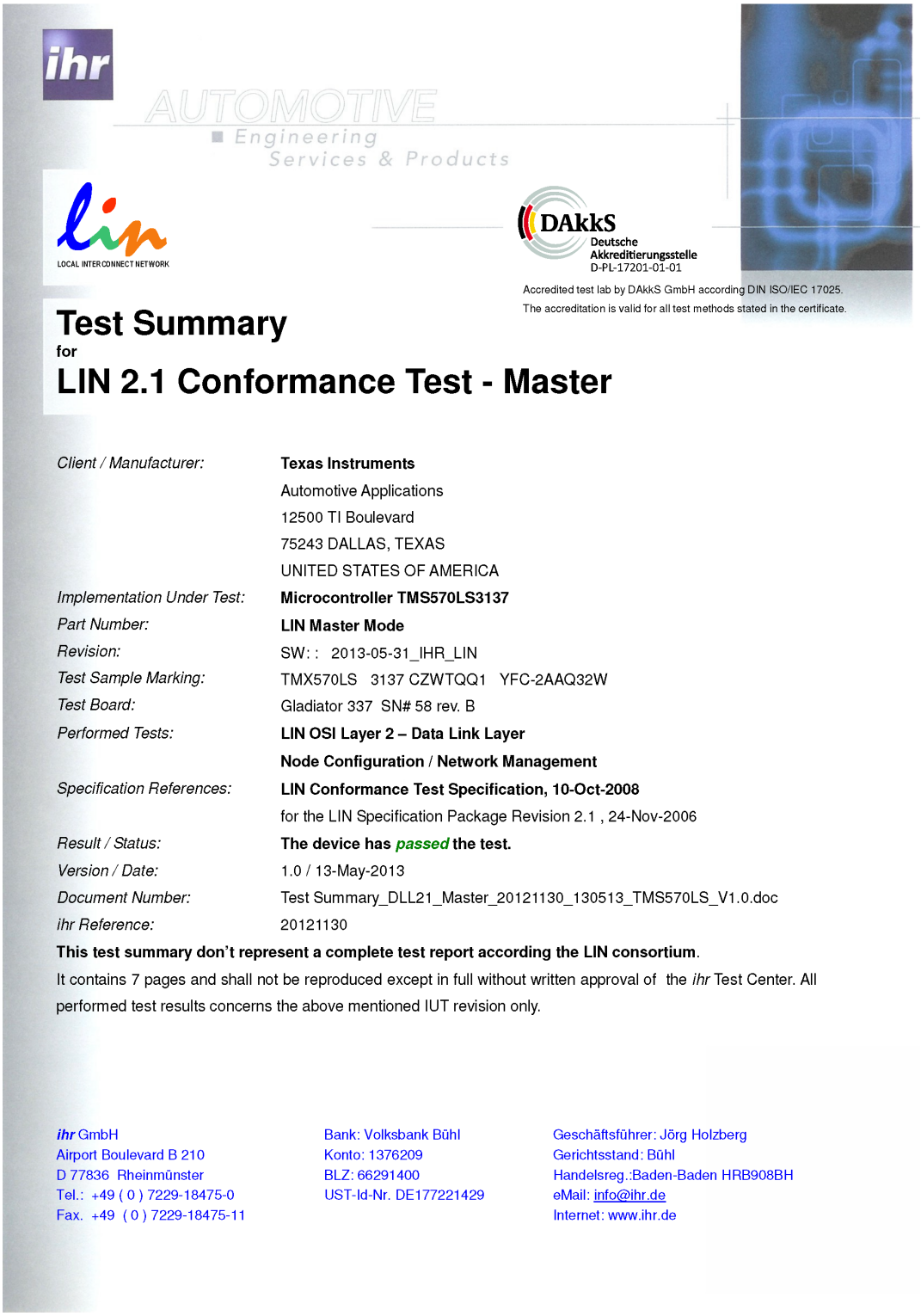
Lothar Kukla, Project Manager

Quote No. P10_0294 R01

**Figure 8-3. DCAN Certification**

### 8.7.2 LIN Certification

#### 8.7.2.1 LIN Master Mode



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**Test Summary**
for
**LIN 2.1 Conformance Test - Master**

| | |
|---|---|
| *Client / Manufacturer:* | **Texas Instruments** |
| | Automotive Applications |
| | 12500 TI Boulevard |
| | 75243 DALLAS, TEXAS |
| | UNITED STATES OF AMERICA |
| *Implementation Under Test:* | **Microcontroller TMS570LS3137** |
| *Part Number:* | **LIN Master Mode** |
| *Revision:* | SW: : 2013-05-31_IHR_LIN |
| *Test Sample Marking:* | TMX570LS 3137 CZWTQQ1 YFC-2AAQ32W |
| *Test Board:* | Gladiator 337 SN# 58 rev. B |
| *Performed Tests:* | **LIN OSI Layer 2 – Data Link Layer** |
| | **Node Configuration / Network Management** |
| *Specification References:* | **LIN Conformance Test Specification, 10-Oct-2008** |
| | for the LIN Specification Package Revision 2.1 , 24-Nov-2006 |
| *Result / Status:* | **The device has *passed* the test.** |
| *Version / Date:* | 1.0 / 13-May-2013 |
| *Document Number:* | Test Summary_DLL21_Master_20121130_130513_TMS570LS_V1.0.doc |
| *ihr Reference:* | 20121130 |

**This test summary don't represent a complete test report according the LIN consortium**.
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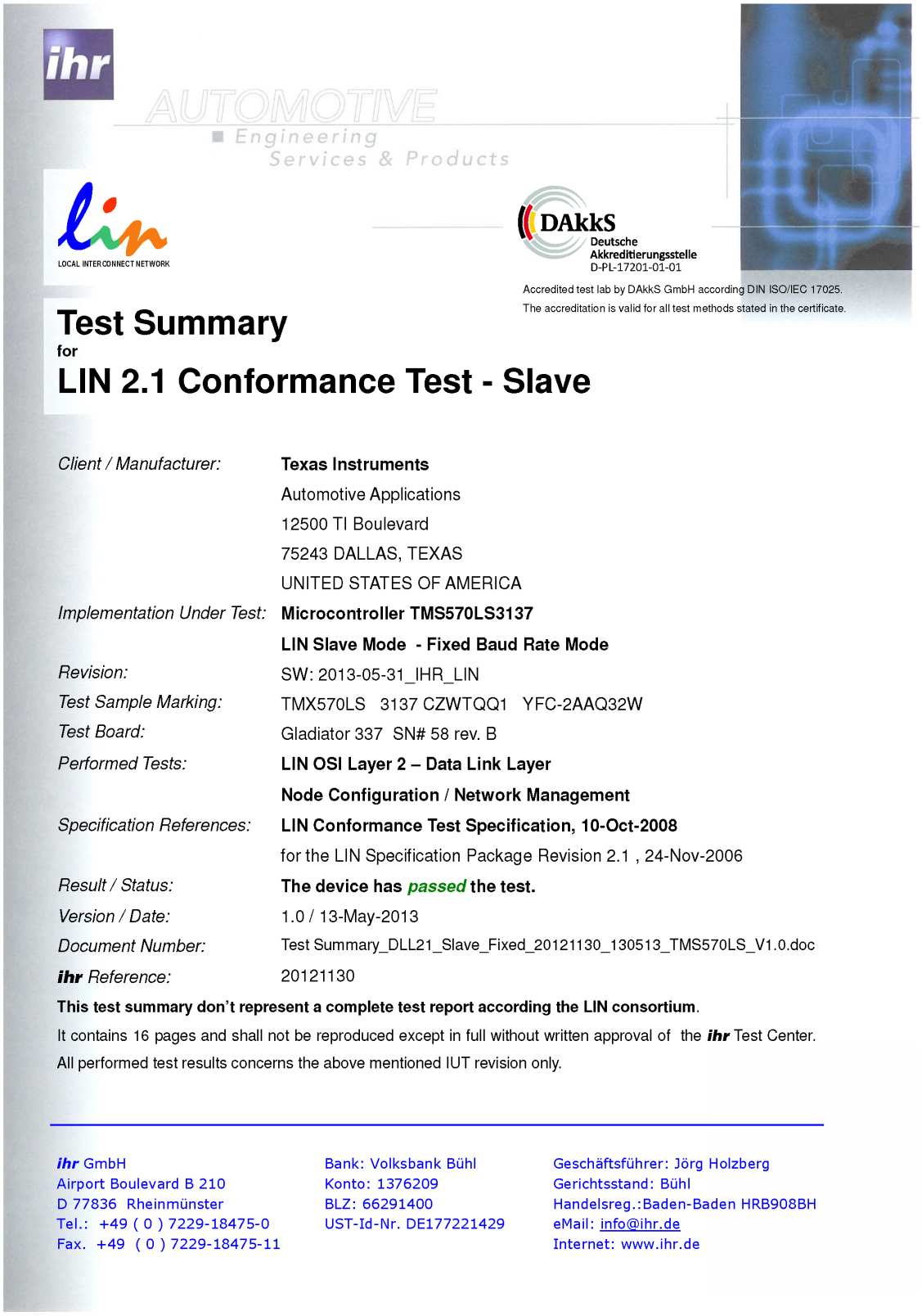
**Figure 8-4. LIN Certification - Master Mode**

### 8.7.2.2 LIN Slave Mode - Fixed Baud Rate



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# Test Summary
for
# LIN 2.1 Conformance Test - Slave

| | |
|---|---|
| *Client / Manufacturer:* | **Texas Instruments** |
| | Automotive Applications |
| | 12500 TI Boulevard |
| | 75243 DALLAS, TEXAS |
| | UNITED STATES OF AMERICA |
| *Implementation Under Test:* | **Microcontroller TMS570LS3137** |
| | **LIN Slave Mode - Fixed Baud Rate Mode** |
| *Revision:* | SW: 2013-05-31_IHR_LIN |
| *Test Sample Marking:* | TMX570LS 3137 CZWTQQ1 YFC-2AAQ32W |
| *Test Board:* | Gladiator 337 SN# 58 rev. B |
| *Performed Tests:* | **LIN OSI Layer 2 – Data Link Layer** |
| | **Node Configuration / Network Management** |
| *Specification References:* | **LIN Conformance Test Specification, 10-Oct-2008** |
| | for the LIN Specification Package Revision 2.1 , 24-Nov-2006 |
| *Result / Status:* | **The device has *passed* the test.** |
| *Version / Date:* | 1.0 / 13-May-2013 |
| *Document Number:* | Test Summary_DLL21_Slave_Fixed_20121130_130513_TMS570LS_V1.0.doc |
| ***ihr** Reference:* | 20121130 |

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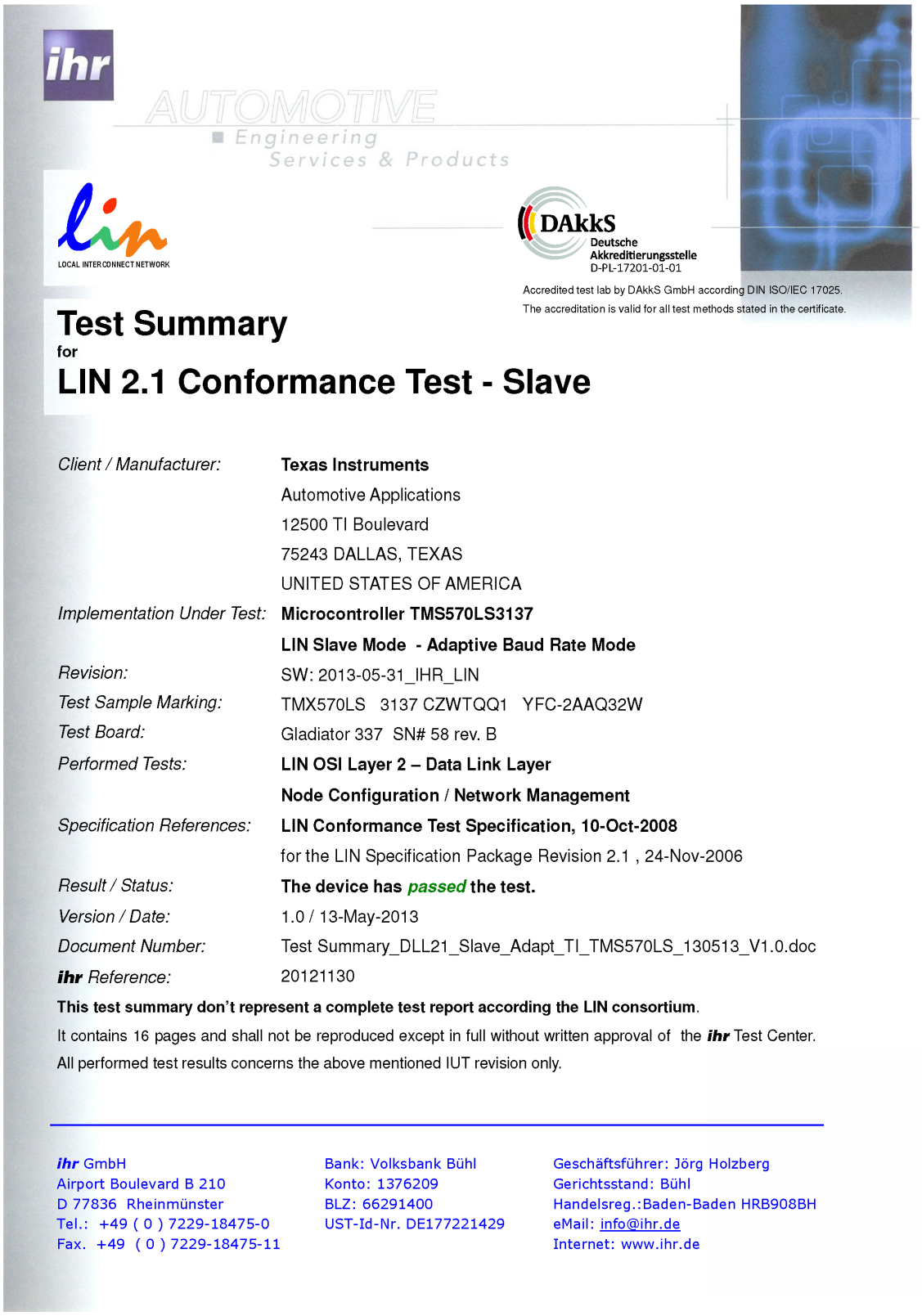
eMail: info@ihr.de
Internet: www.ihr.de

**Figure 8-5. LIN Certification - Slave Mode - Fixed Baud Rate**

### 8.7.2.3 LIN Slave Mode - Adaptive Baud Rate



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# Test Summary
for
# LIN 2.1 Conformance Test - Slave

| | |
|---|---|
| *Client / Manufacturer:* | **Texas Instruments** |
| | Automotive Applications |
| | 12500 TI Boulevard |
| | 75243 DALLAS, TEXAS |
| | UNITED STATES OF AMERICA |
| *Implementation Under Test:* | **Microcontroller TMS570LS3137** |
| | **LIN Slave Mode - Adaptive Baud Rate Mode** |
| *Revision:* | SW: 2013-05-31_IHR_LIN |
| *Test Sample Marking:* | TMX570LS 3137 CZWTQQ1 YFC-2AAQ32W |
| *Test Board:* | Gladiator 337 SN# 58 rev. B |
| *Performed Tests:* | **LIN OSI Layer 2 – Data Link Layer** |
| | **Node Configuration / Network Management** |
| *Specification References:* | **LIN Conformance Test Specification, 10-Oct-2008** |
| | for the LIN Specification Package Revision 2.1 , 24-Nov-2006 |
| *Result / Status:* | **The device has *passed* the test.** |
| *Version / Date:* | 1.0 / 13-May-2013 |
| *Document Number:* | Test Summary_DLL21_Slave_Adapt_TI_TMS570LS_130513_V1.0.doc |
| ***ihr** Reference:* | 20121130 |

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**Figure 8-6. LIN Certification - Slave Mode - Adaptive Baud Rate**

# 9 Mechanical Packaging and Orderable Information

## 9.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMS5701224CPGEQQ1 | ACTIVE | LQFP | PGE | 144 | 60 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 125 | TMS570LS 1224CPGEQQ1 | Samples |
| TMS5701224CZWTQQ1 | ACTIVE | NFBGA | ZWT | 337 | 90 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 125 | TMS570LS 1224CZWTQQ1 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

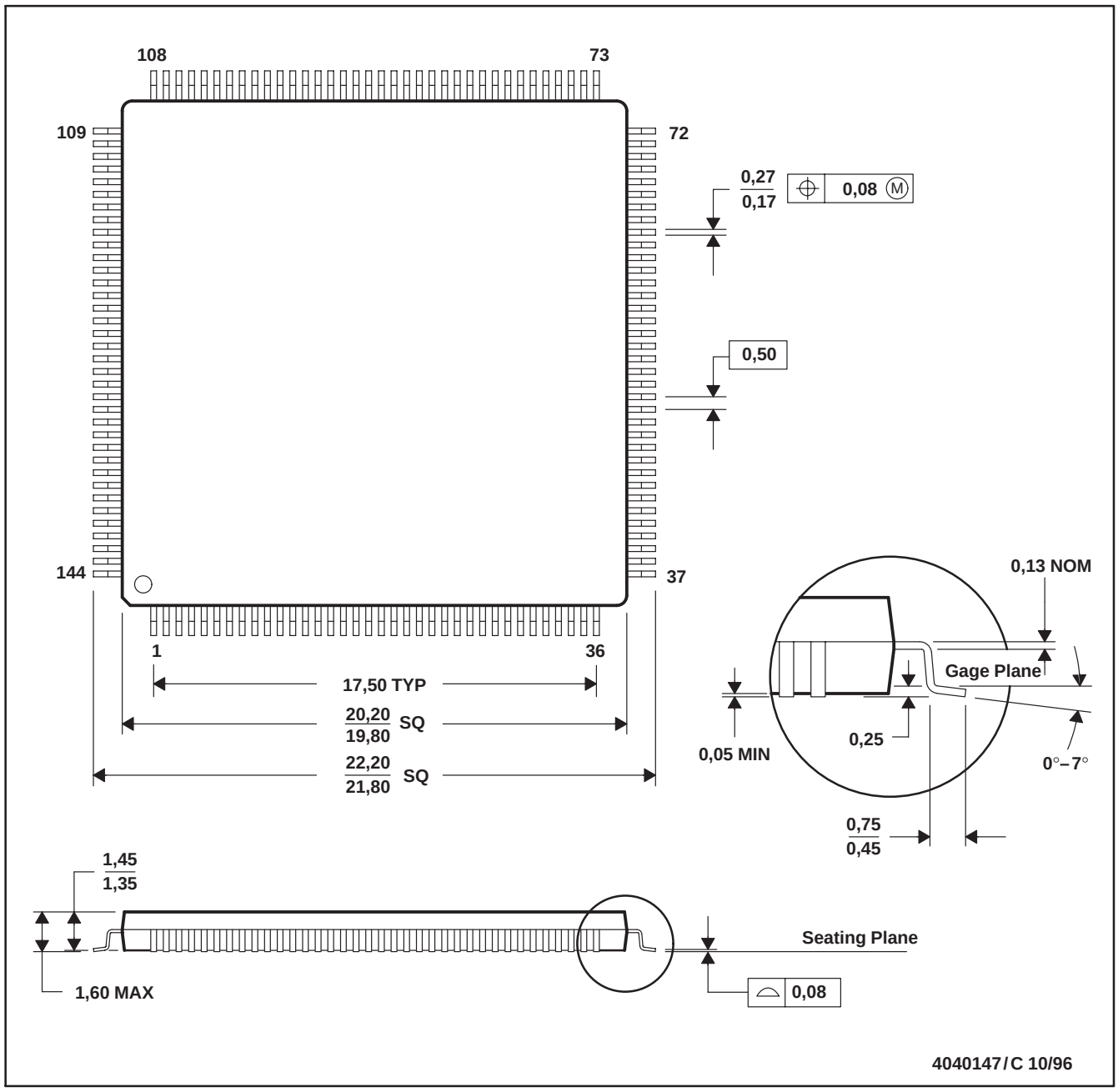
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

MTQF017A – OCTOBER 1994 – REVISED DECEMBER 1996

**PGE (S-PQFP-G144)** **PLASTIC QUAD FLATPACK**



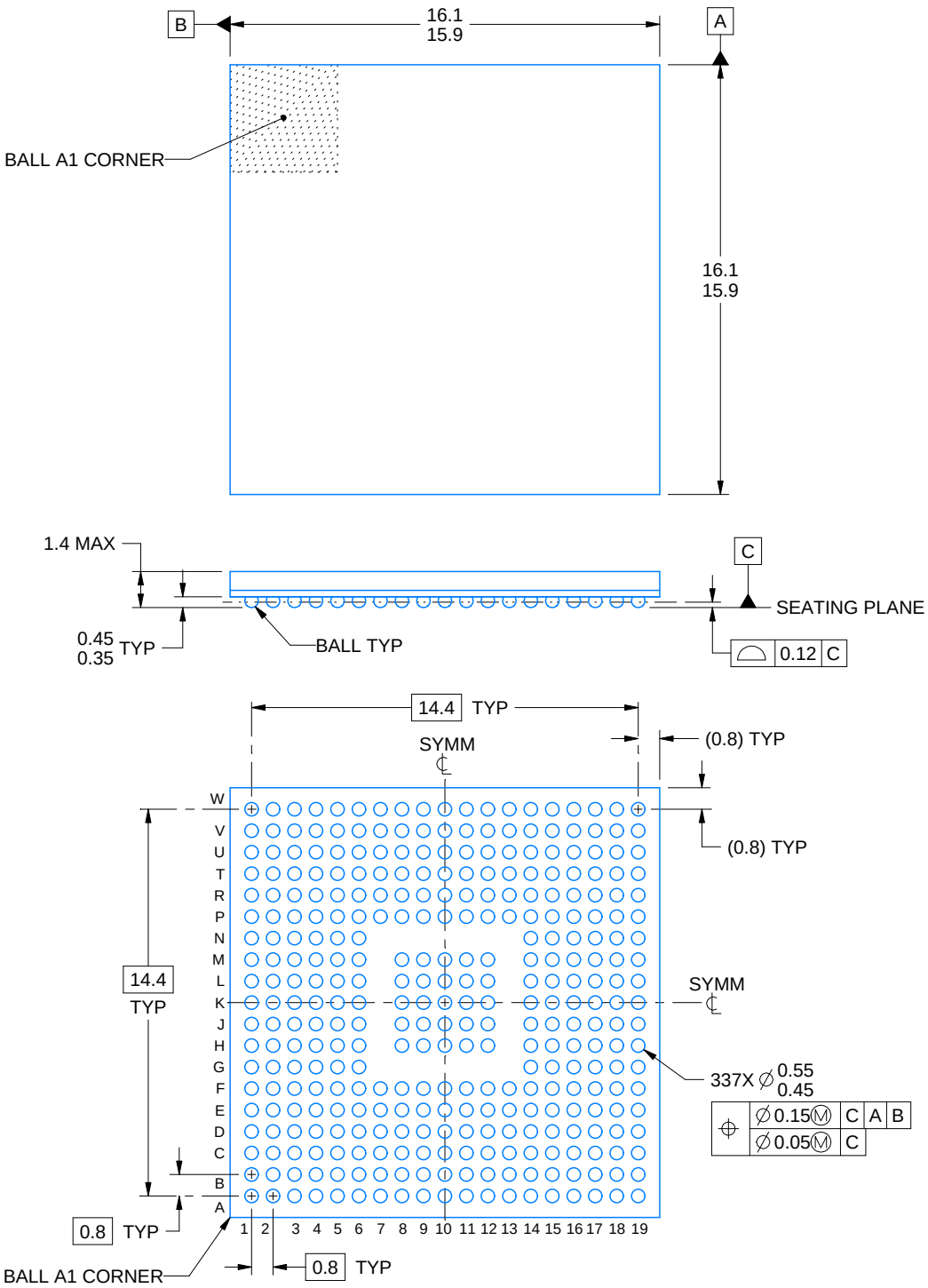

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

# PACKAGE OUTLINE

## ZWT0337A

## NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY




NOTES:

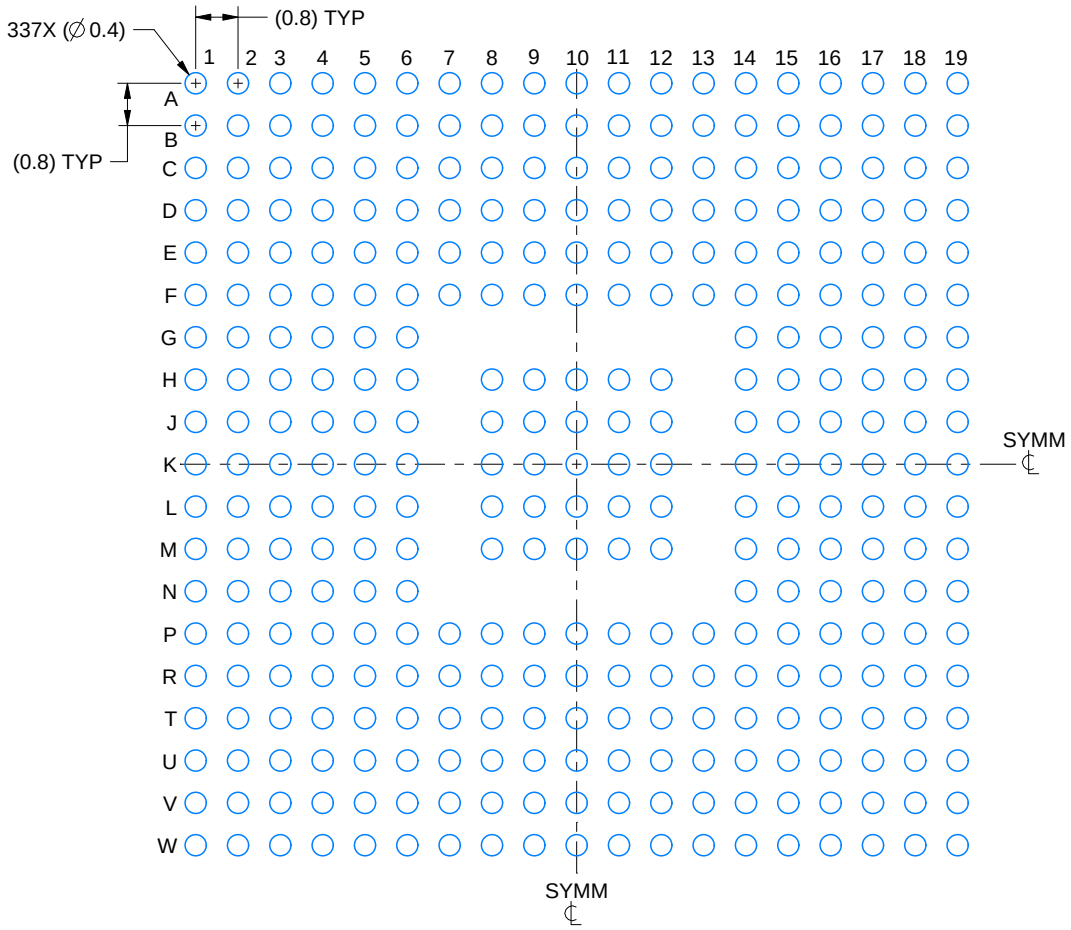
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

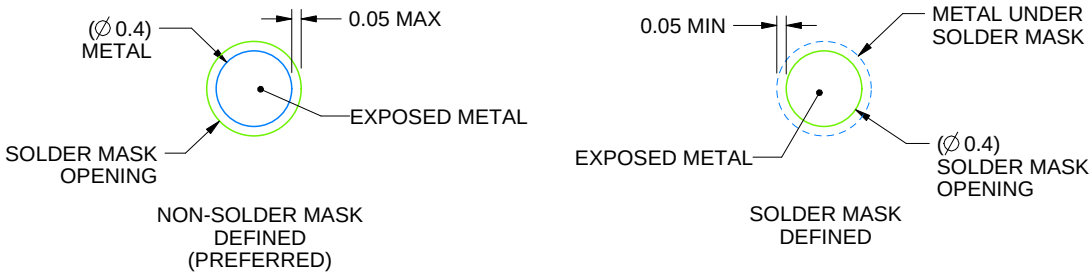
## ZWT0337A

## NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:7X

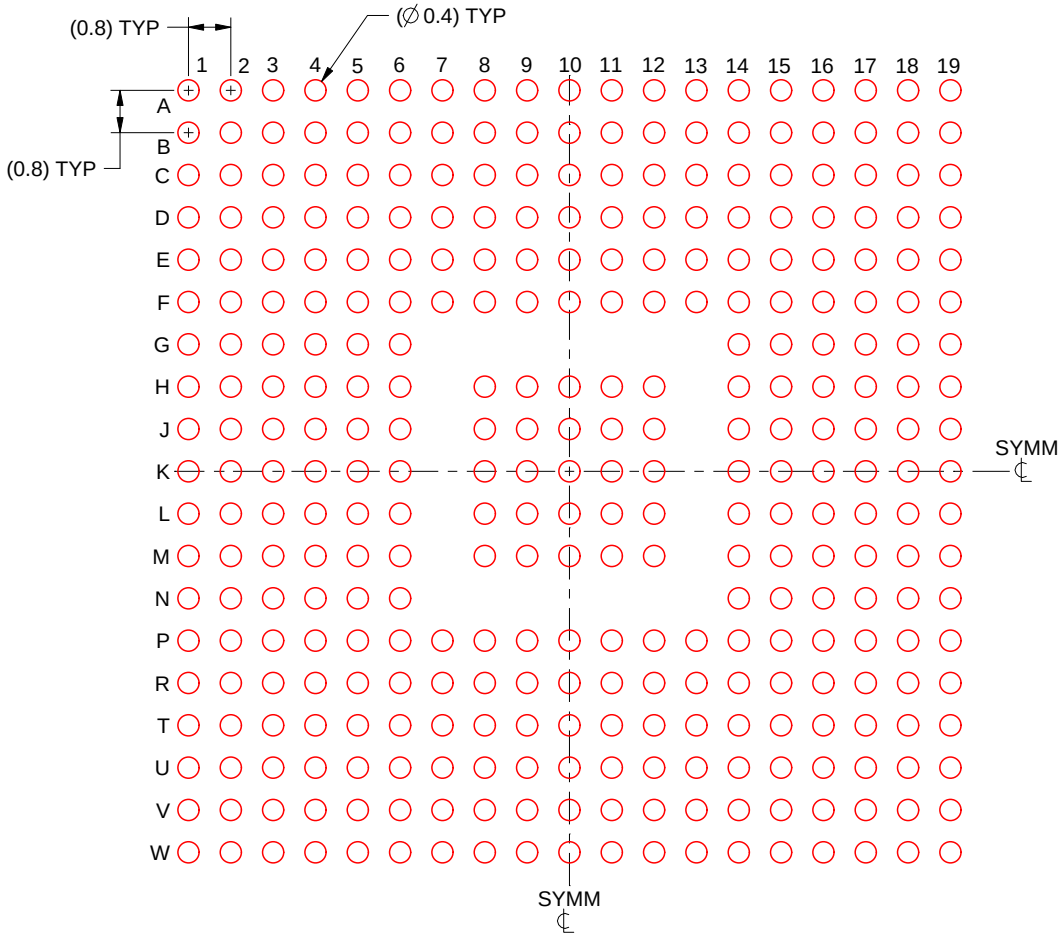



SOLDER MASK DETAILS
NOT TO SCALE

4223381/A 02/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).




SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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