

LT3090
**–36V, 600mA Negative Linear Regulator
with Programmable Current Limit**
DESCRIPTION

Demonstration circuit 1948A is a 600mA low dropout negative linear regulator featuring the LT[®]3090. This device is designed for applications requiring negative output voltage, high current with no heat sink, output adjustability to zero and low dropout voltage.

The LT3090 features fast transient response, high PSRR and low output noise. The LT3090 supplies 600mA at a typical dropout voltage of 300mV. Operating quiescent current is nominally 1mA and drops to $\ll 1\mu\text{A}$ in shutdown. A single resistor adjusts the LT3090's precision programmable current limit. The LT3090's positive or negative current monitor either sources a current (0.5mA/A) or

sinks a current (1mA/A) proportional to output current. Built-in protection includes reverse output protection, internal current limit with foldback and thermal shutdown with hysteresis.

The LT3090 is offered in a 10 pin DFN package and a 16-lead MSOP package.

The LT3090 data sheet gives a complete description of the device, operation and application information. The data sheet should be read in conjunction with this quick start guide for working on or modifying the demo circuit 1948A.

Design files for this circuit board are available at
<http://www.linear.com/demo/DC1948A>

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PERFORMANCE SUMMARY Specifications are at $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Range	$V_{OUT} = 1.2\text{V}$, $I_{OUT1} = 1\text{mA}$	–36		–1.5	V
V_{OUT}	Output Voltage	Shunt at 1, 2 for JP1	–1.286	–1.25	–1.213	V
		Shunt at 3, 4 for JP1	–2.575	–2.5	–2.425	V
		Shunt at 5, 6 for JP1	–5.15	–5	–4.85	V
		Shunt at 7, 8 for JP1	–12.36	–12	–11.64	V
		Shunt at 9, 10 for JP1	–15.45	–15	–14.55	V
		Shunt at 11, 12 for JP1 and R10 Stuffed as 357k Ω	–18.54	–18	–17.46	V
I_{OUT}	Output Current	R1 = 10k, (Note 1)	600			mA

Note 1. This is for the typical condition when $V_{IN} - V_{OUT} < 5\text{V}$. Current limit varies with different values of $V_{IN} - V_{OUT}$. Refer to the LT3090 data sheet for details.

QUICK START PROCEDURE

Demonstration circuit 1948A is easy to set up to evaluate the performance of the LT3090. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

NOTE. When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the input or output voltage ripple by touching the probe tip directly across the terminals of the input or output capacitors. See Figure 2 for proper scope probe technique.

1. Use JP2 to set the desired output voltage.
2. Put JP4 on ON position.
3. With power off, connect the input power supply to VIN and GND.

4. Turn on the power at the VIN.

NOTE. Make sure that the VIN voltage does not exceed -36V.

5. Check for the proper output voltages:

NOTE. If there is no output, temporarily disconnect the load to make sure that the load is not set too high or is shorted.

6. Once the proper output voltages are established, adjust the loads within the operating range and observe the output voltage regulation, efficiency and other parameters.

NOTE. Make sure that the power dissipation is limited below the thermal limit.

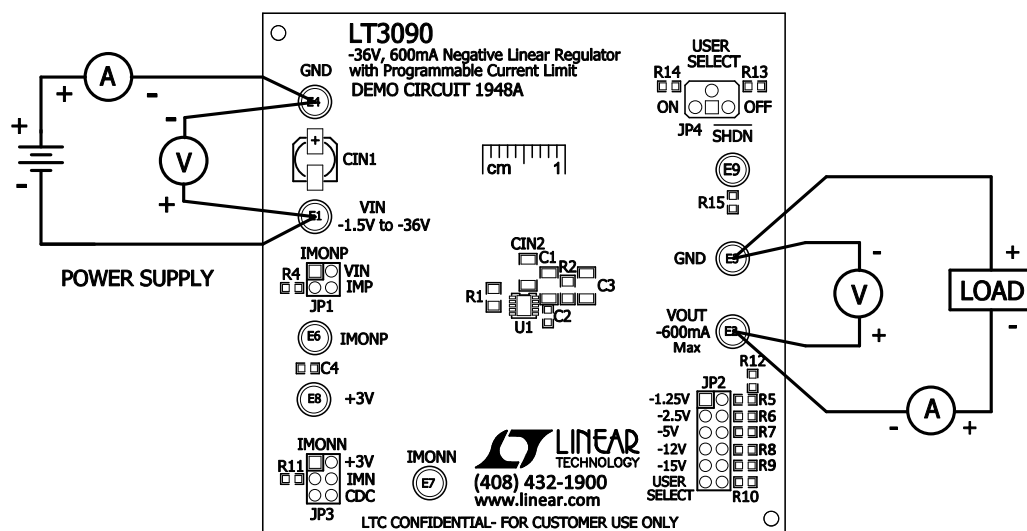


Figure 1. DC1948A Proper Equipment Setup

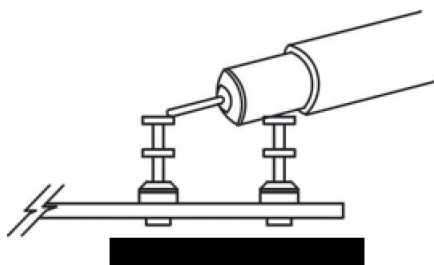


Figure 2. Measuring Input or Output Ripple

POSITIVE OR NEGATIVE CURRENT MONITOR CONFIGURATION

There are both positive and negative current monitors on the LT3090. The configurations for these two monitors are different. When the positive current monitor is in use, JP1 needs to be configured on IMP position and JP3 needs to be configured on +3V position. Meantime a +3V external power supply needs to be connected to +3V turret. Figure 3 shows this configuration.

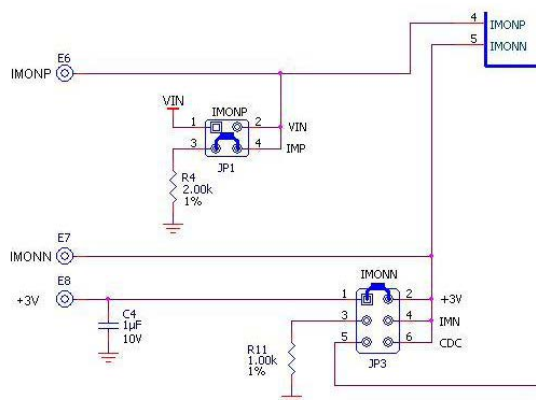


Figure 3. Positive Current Monitor Configuration

When the negative current monitor is in use, JP1 needs to be configured on VIN position and JP3 needs to be configured on IMN position. There is no external power supply needed. Figure 4 shows this configuration.

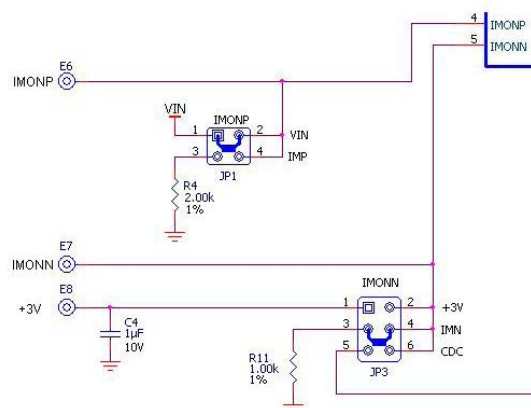


Figure 4. Negative Current Monitor Configuration

CABLE DROP COMPENSATION CONFIGURATION

Demo Circuit 1948A can be configured to evaluate the cable drop compensation on the LT3090. Note that cable drop compensation is only using negative current monitor configuration. JP1, JP3 and R12 shall be configured. JP1 needs to be configured on VIN position. JP3 needs to be

configured on CDC position. R12 needs to be replaced by a calculated value which has the following relationship with the total output cable impedance (R_{CBL}) below. R12 and R_{CBL} are both in $k\Omega$:

$$R12 = R_{CBL} \cdot 1k$$

THERMAL IMAGE

An example thermal image shows the temperature distribution on board. The test is complete in still air at room temperature with 2.1W power dissipation in the LT3090. This gives the IC case-to-ambient thermal resistance of about $\theta_{JA} = 24^{\circ}\text{C/W}$ on the demo board.

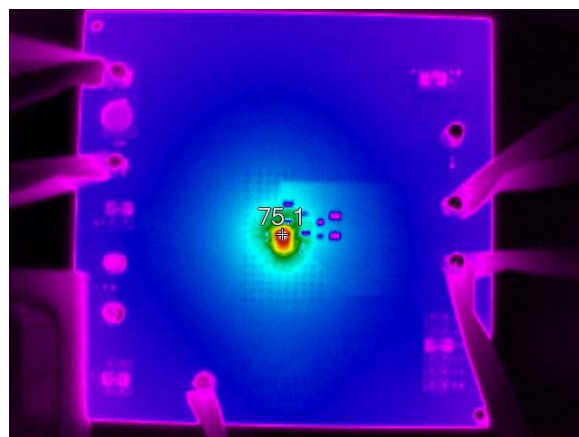


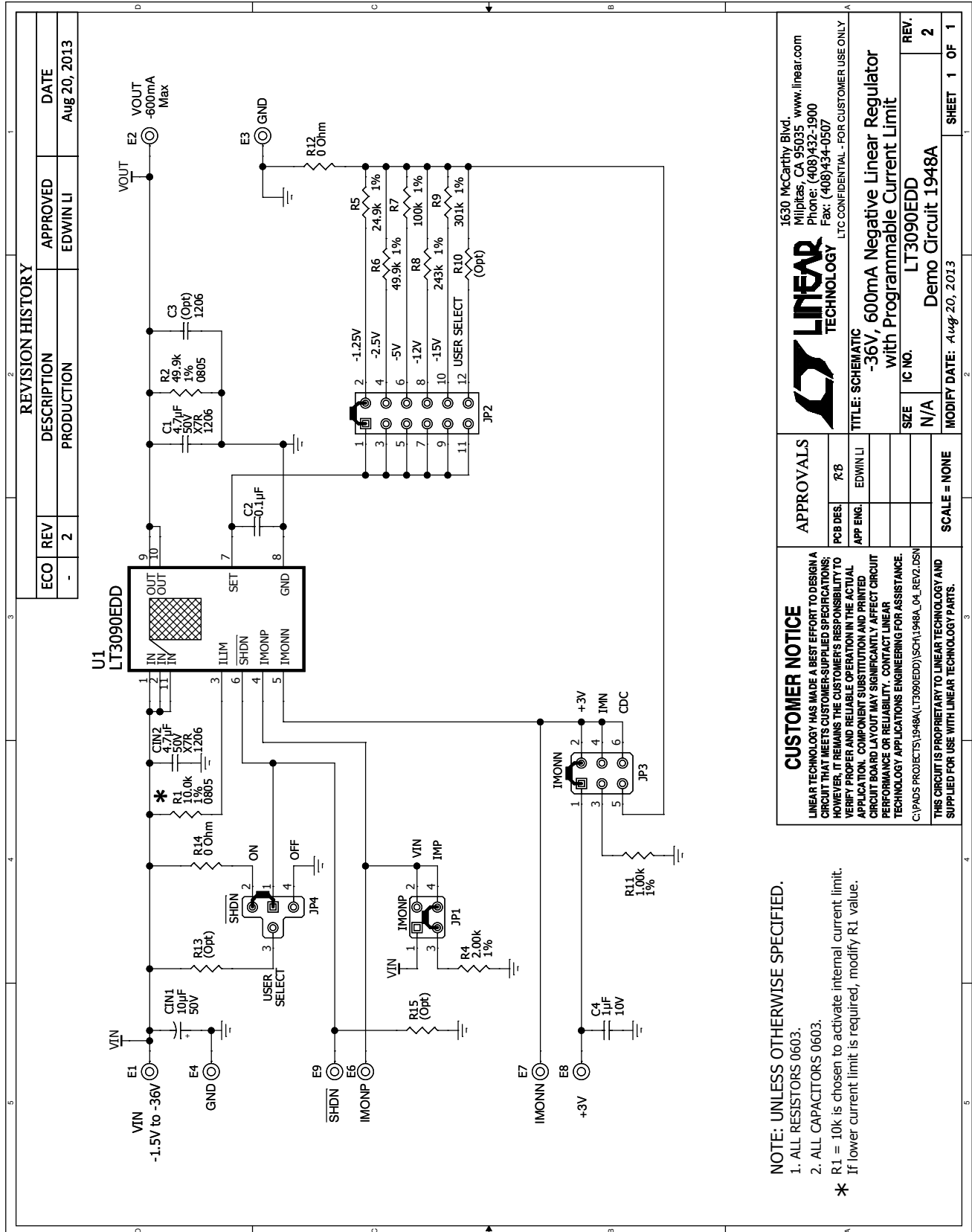
Figure 5. Temperature Rise at 2.1W Dissipation

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PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	2	C1, CIN2	CAP, X7R 4.7 μ F 50V 10% 1206	TDK C3216X7R1H475KT
2	1	C2	CAP, X7R 0.1 μ F 16V 10% 0603	AVX 0603YC104KAT2A
3	1	C4	CAP, X7R 1 μ F 10V 10% 0603	TAIYO YUDEN LMK107BJ105KA
4	1	R1	RES, CHIP 10k 0.1W 1% 0805	VISHAY CRCW080510K0FKTA
5	1	R2	RES, CHIP 49.9k 0.1W 1% 0805	VISHAY CRCW080549K9FKTA
6	1	R4	RES, CHIP 2k 0.06W 1% 0603	VISHAY CRCW06032K00FKEA
7	1	R5	RES, CHIP 24.9k 0.06W 1% 0603	VISHAY CRCW060324K9FKEA
8	1	R6	RES, CHIP 49.9k 0.06W 1% 0603	VISHAY CRCW060349K9FKEA
9	1	R7	RES, CHIP 100k 0.06W 1% 0603	VISHAY CRCW0603100KFKEA
10	1	R8	RES, CHIP 243k 0.06W 1% 0603	VISHAY CRCW0603243KFKEA
11	1	R9	RES, CHIP 301k 0.06W 1% 0603	VISHAY CRCW0603301KFKEA
12	1	R11	RES, CHIP 1k 0.06W 1% 0603	VISHAY CRCW06031K00FKEA
13	1	R12, R14	RES, CHIP 0 Ω 0.25W 5A 0603	VISHAY CRCW06030000Z0EA
14	1	U1	IC, NEGATIVE LINEAR REG DFN(10) (DD) 3mm $\times$ 3mm	LINEAR TECHNOLOGY CORPORATION LT3090EDD
Additional Demo Board Circuit Components				
1	1	CIN1	CAP, ALUM 10 μ F 50V 10%	SUNCON 50CE10BSS
2	0	C3 (OPT)	CAP, 1206	
3	0	R10, R13, R15 (OPT)	RES, 0603	
Hardware: For Demo Board Only				
1	8	E1, E2, E3, E4, E6, E7, E8, E9	TURRET, TESTPOINT	MILL MAX 2501-2-00-80-00-00-07-0
2	1	JP1	HEADERS, DBL ROW 2 $\times$ 2 2mm CTRS	SAMTEC TMM-102-02-L-D
3	1	JP2	HEADERS, DBL ROW 2 $\times$ 6 2mm CTRS	SAMTEC TMM-106-02-L-D
4	1	JP3	HEADERS, DBL ROW 2 $\times$ 3 2mm CTRS	SAMTEC TMM-103-02-L-D
5	1	JP4	HEADERS, 2mm CTRS	SAMTEC ASP-157349-01
6	4	XJP1, XJP2, XJP3, XJP4	SHUNT, 2mm CTRS	SAMTEC 2SN-BK-G

SCHEMATIC DIAGRAM



NOTE: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTORS 0603.
2. ALL CAPACITORS 0603.

* R1 = 10k is chosen to activate internal current limit.
If lower current limit is required, modify R1 value.

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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