5-V Dual Differential PECL Buffer-to-TTL Translator

FEATURES

- **Dual 5-V Differential PECL-to-TTL Buffer**
- **24-mA TTL Ouputs**
- **Operating Range**
  - **PECL V_{CC} = 4.75 V to 5.25 V with GND = 0 V**
- **Support for Clock Frequencies of 250 MHz (TYP)**
- **3.5-ns Typical Propagation Delay**
- **Output Default Low with Inputs Left Open or <1.3 V**
- **Internal Input 50-kΩ Pull-Down Resistor**
- **Built-In Temperature Compensation**
- **Drop-In Compatible to the MC100ELT23**

APPLICATIONS

- **Data and Clock Transmission Over Backplane**
- **Signaling Level Conversion for Clock or Data**

DESCRIPTION

The SN65ELT23 is a low power dual PECL-to-TTL translator device. The device includes circuitry to maintain a known logic low level when inputs are in an open condition. The SN65ELT23 is housed in an industry standard SOIC-8 package and is also available in an optional TSSOP-8 package.

PIN ASSIGNMENT

D or DGK PACKAGE
(TOP VIEW)

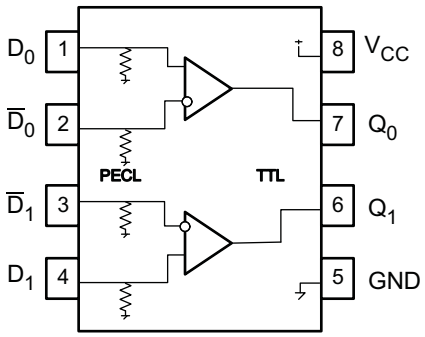


Table 1. Pin Descriptions

PIN	FUNCTION
D_0, $\overline{D}_0$, D_1, $\overline{D}_1$	PECL inputs
Q_0, Q_1	TTL outputs
V_{CC}	Positive supply
GND	Ground

ORDERING INFORMATION(1)(2)

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65ELT23D	ELT23	SOIC	NiPdAu
SN65ELT23DGK	SIKI	MSOP	NiPdAu

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Leaded device options are not initially available; contact a sales representative for further details.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER	CONDITIONS	VALUE	UNIT
Absolute supply voltage, V_{CC}		6	V
Absolute input voltage, V_I	GND = 0 and $V_I \le V_{CC}$	0 to 6	V
Output current	Continuous	50	mA
	Surge	100	
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING T_A < 25°C (mW)	THERMAL RESISTANCE, JUNCTION-TO-AMBIENT NO AIRFLOW	DERATING FACTOR T_A > 25°C (mW/°C)	POWER RATING T_A = 85°C (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
MSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
θ_{JB}	Junction-to-board thermal resistance	SOIC		79		°C/W
		MSOP		120		
θ_{JC}	Junction-to-case thermal resistance	SOIC		98		°C/W
		MSOP		74		

KEY ATTRIBUTES

CHARACTERISTICS	PARAMETER	VALUE
Moisture sensitivity level		Level 1
Flammability rating (oxygen index: 28 to 34)		UL 94 V-0 at 0.125 in
Internal pull down resistor		50 KΩ
Electrostatic discharge	Human body model	2 KV
	Charged-device model	1.5 KV
	Machine model	200 V
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test		

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PECL INPUT DC CHARACTERISTICS

At V_{CC} = 5.0 V, GND = 0.0 V (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	T_A = –40°C			T_A = 25°C			T_A = 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage, single-ended	See (3)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Low-level input voltage, single-ended		3190	2280	3525	3190	2280	3525	3190	2280	3525	mV
V_{IHCMR}	High-level input voltage common-mode range, differential	See (4)	2.2		5.0	2.2		5.0	2.2		5.0	V
I_{IH}	High-level input current				255			175			175	µA
I_{IL}	Low-level input current		0.5			0.5			0.5			µA

(1) The device meets the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Input and output parameters vary 1:1 with V_{CC}. V_{CC} can vary ±0.25 V.
(3) TTL output R_L = 500 Ω to GND
(4) $V_{IHCMR(min)}$ varies 1:1 with GND, $V_{IHCMR(max)}$ varies 1:1 with V_{CC}.

TTL OUTPUT DC CHARACTERISTICS

At V_{CC} = 4.75 V to 5.25 V, T_A = –40°C to 85°C (unles otherwiase noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	Power supply current			20	25	mA
I_{CCL}	Power supply current			21	27	mA
I_{OS}	Output short circuit current		–150		–50	mA
V_{OH}	High-level output voltage (2)	I_{OH} = –3.0 mA	2.4		V_{CC} – 0.7V	V
V_{OL}	Low-level output voltage	I_{OL} = 24 mA			0.5	V

(1) The device meets the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Max level is assured by design

AC CHARACTERISTICS

At V_{CC} = 5.0 V, GND = 0.0 V (unless otherwise noted)(1)(2)(3)

PARAMETER		TEST CONDITIONS	T_A = –40°C			T_A = 25°C			T_A = 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Max switching frequency	at Vol < 0.5V and Voh > 2.4V (see Figure 5)		250			250			250		MHz
t_{PLH}/t_{PHL}	Propagation delay times to output	At 1.5 V	2.0	3.5	5.0	2.0	3.7	5.0	2.0	3.9	5.0	ns
t_{JITTER}	Random clock jitter (RMS)			4.1	10		3.7	10		3.7	10	ps
V_{PP}	Input voltage swing (4)		200		1000	200		1000	200		1000	mV
t_r/t_f	Output rise times (10%–90%)		1.0	1.7	3.0	1.0	1.8	3.0	1.0	1.9	3.0	ns
	Output fall times (10%–90%)		0.5	1.0	1.6	0.5	1.1	1.6	0.5	1.3	1.6	

(1) The device meets the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) V_{CC} can vary ±0.25 V.
(3) TTL output R_L = 500 Ω to GND and C_L = 20 pF to GND, see Figure 1.
(4) $V_{PP(min)}$ is the minimum input swing for which AC parameters are assured.

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Typical Output Loading Used for Device Evaluation

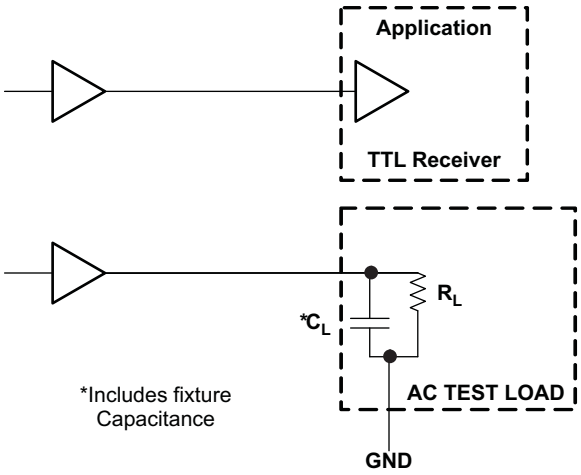


Figure 1. TTL Output Loading Used for Device Evaluation

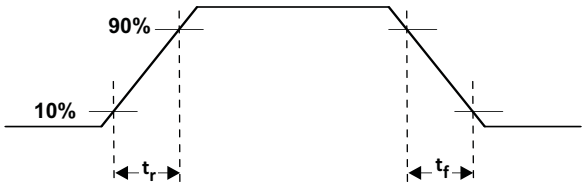


Figure 2. Output Rise and Fall Times

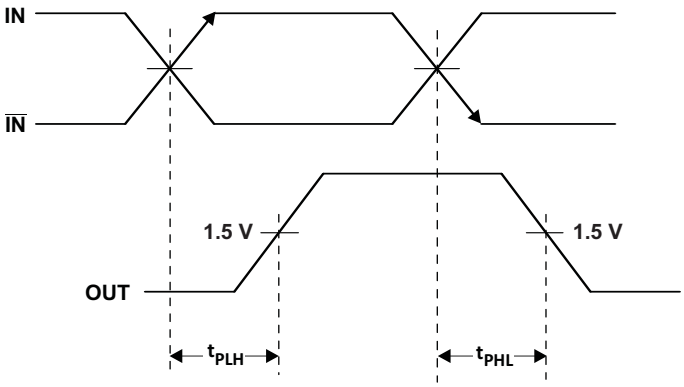


Figure 3. Output Propagation Delay

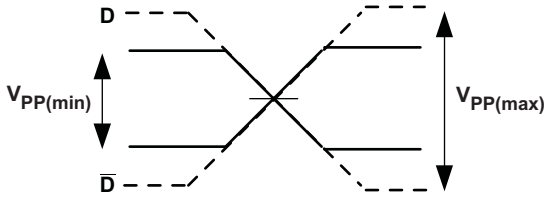


Figure 4. Input Voltage Swing

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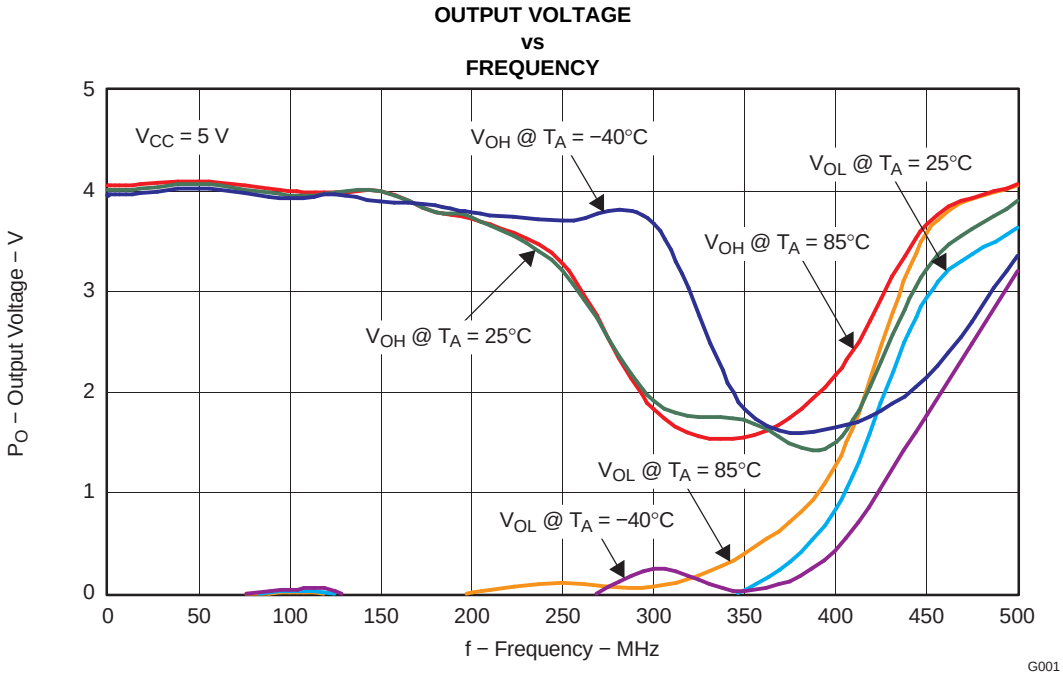

OUTPUT VOLTAGE
vs
FREQUENCY
V_{CC} = 5 V
V_{OH} @ T_A = −40°C
V_{OL} @ T_A = 25°C
V_{OH} @ T_A = 85°C
V_{OH} @ T_A = 25°C
V_{OL} @ T_A = 85°C
V_{OL} @ T_A = −40°C
P_O – Output Voltage – V
f – Frequency – MHz
0
1
2
3
4
5
0
50
100
150
200
250
300
350
400
450
500
G001

Figure 5.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65ELT23D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT23	Samples
SN65ELT23DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIKI	Samples
SN65ELT23DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIKI	Samples
SN65ELT23DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT23	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

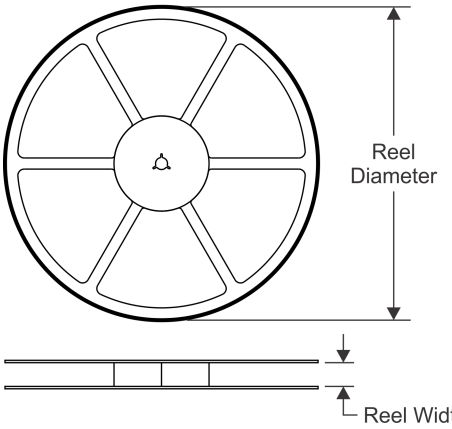
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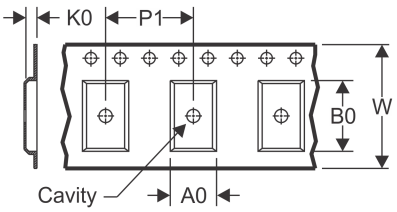
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

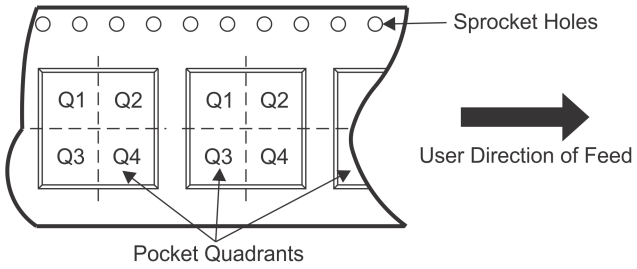


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

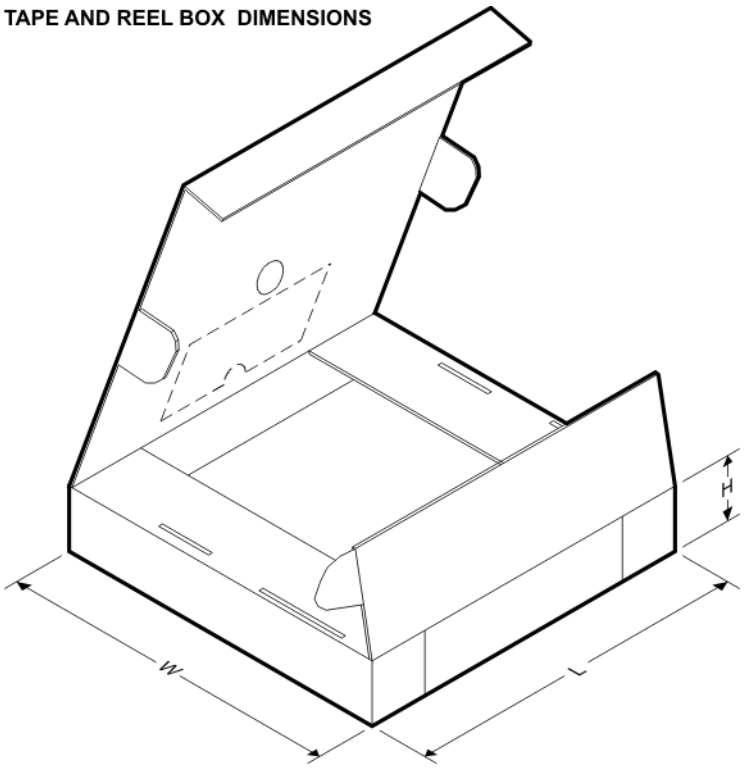
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

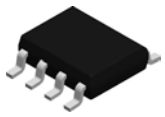
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ELT23DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65ELT23DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ELT23DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
SN65ELT23DR	SOIC	D	8	2500	367.0	367.0	35.0

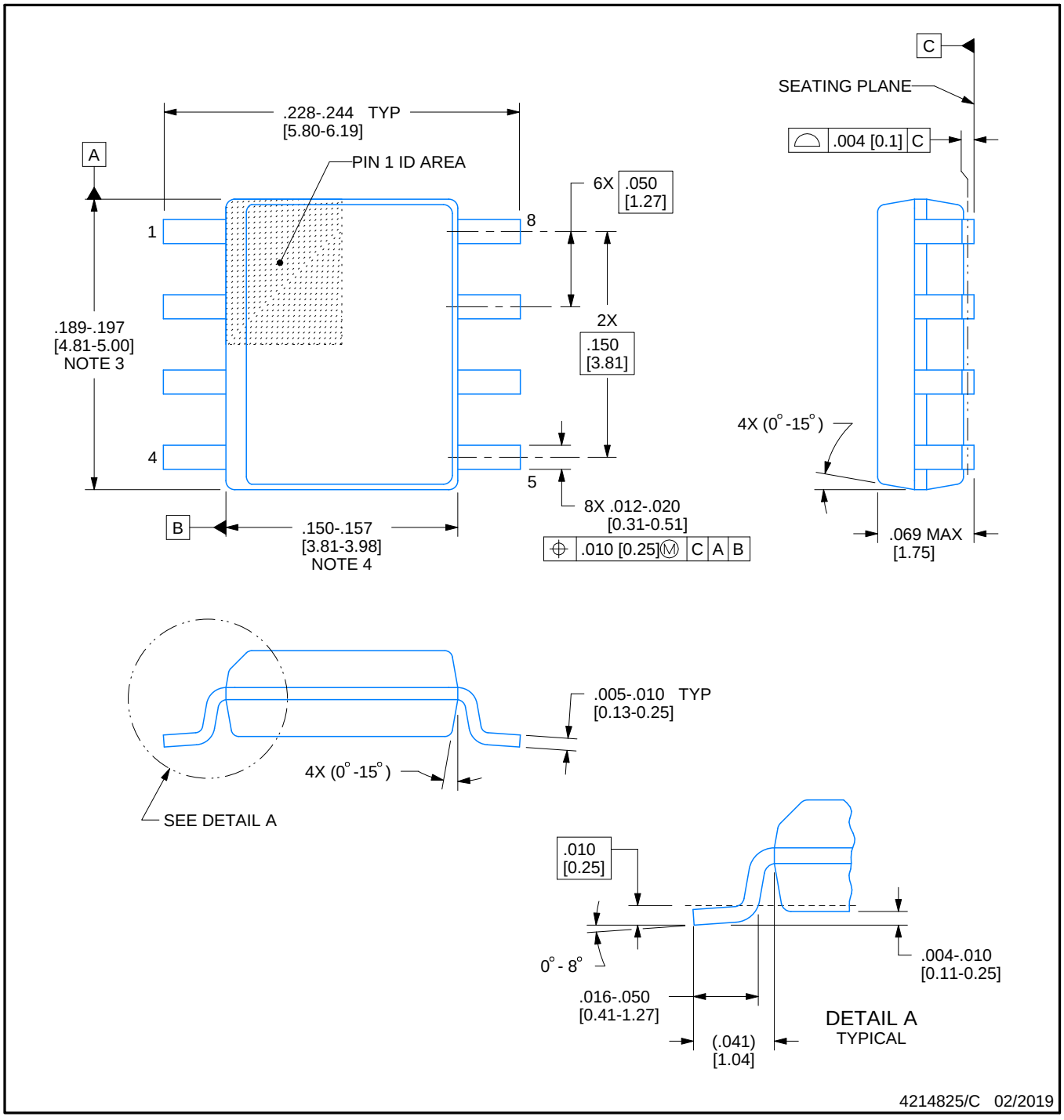


PACKAGE OUTLINE

D0008A

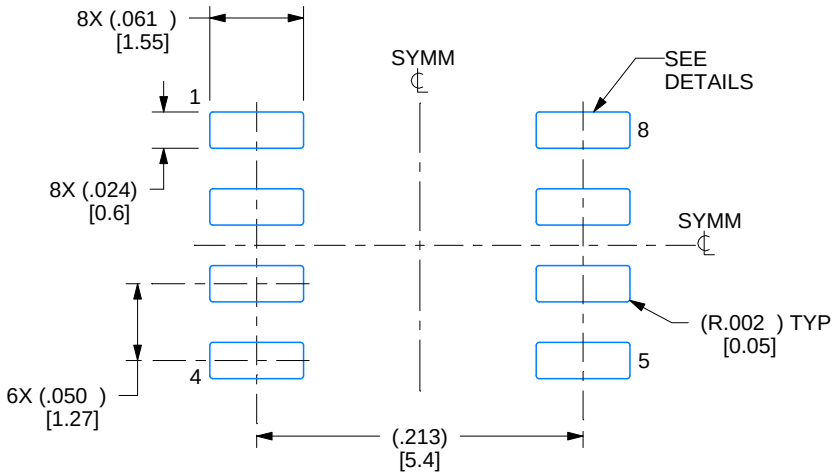
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

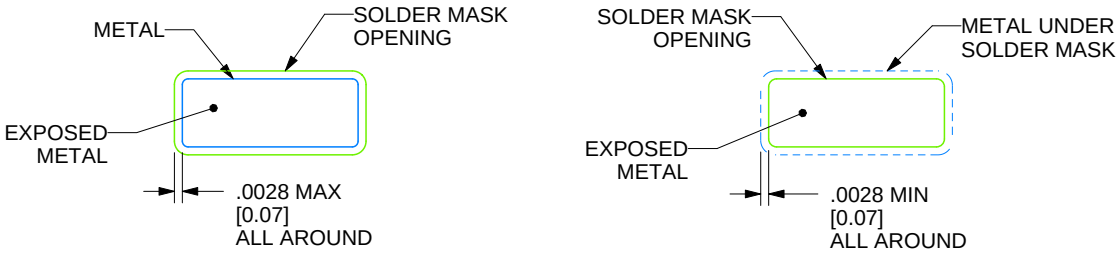


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

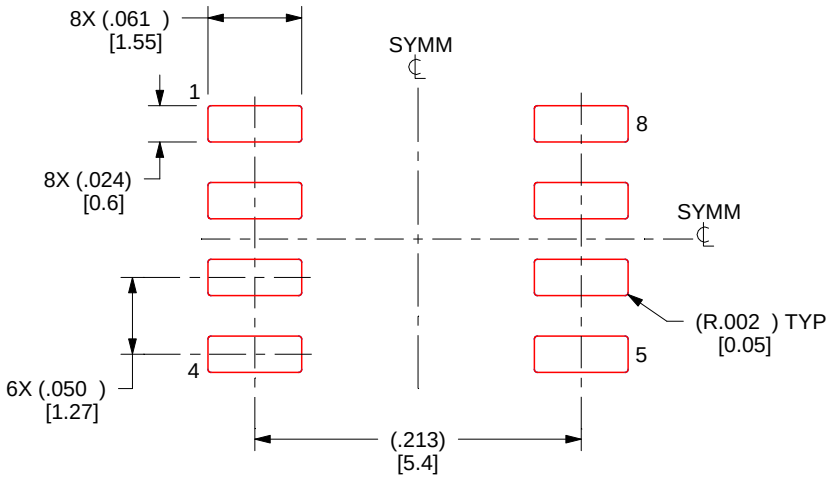
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



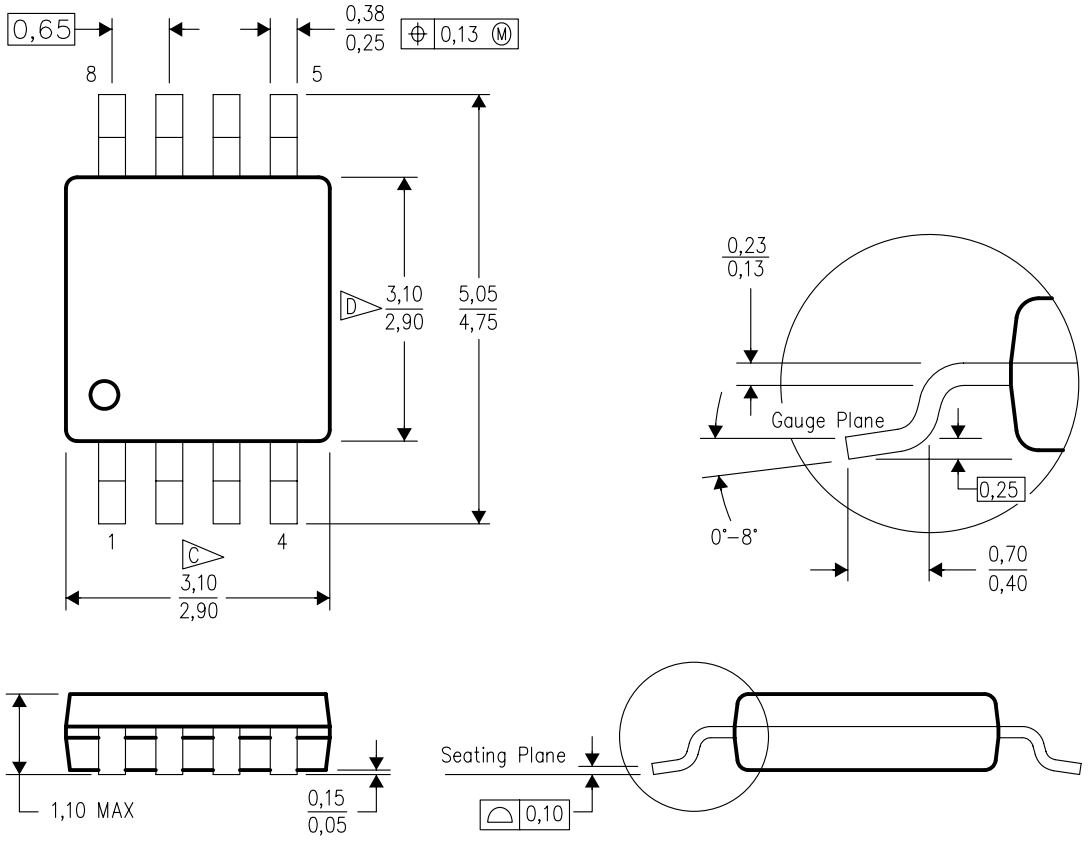
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

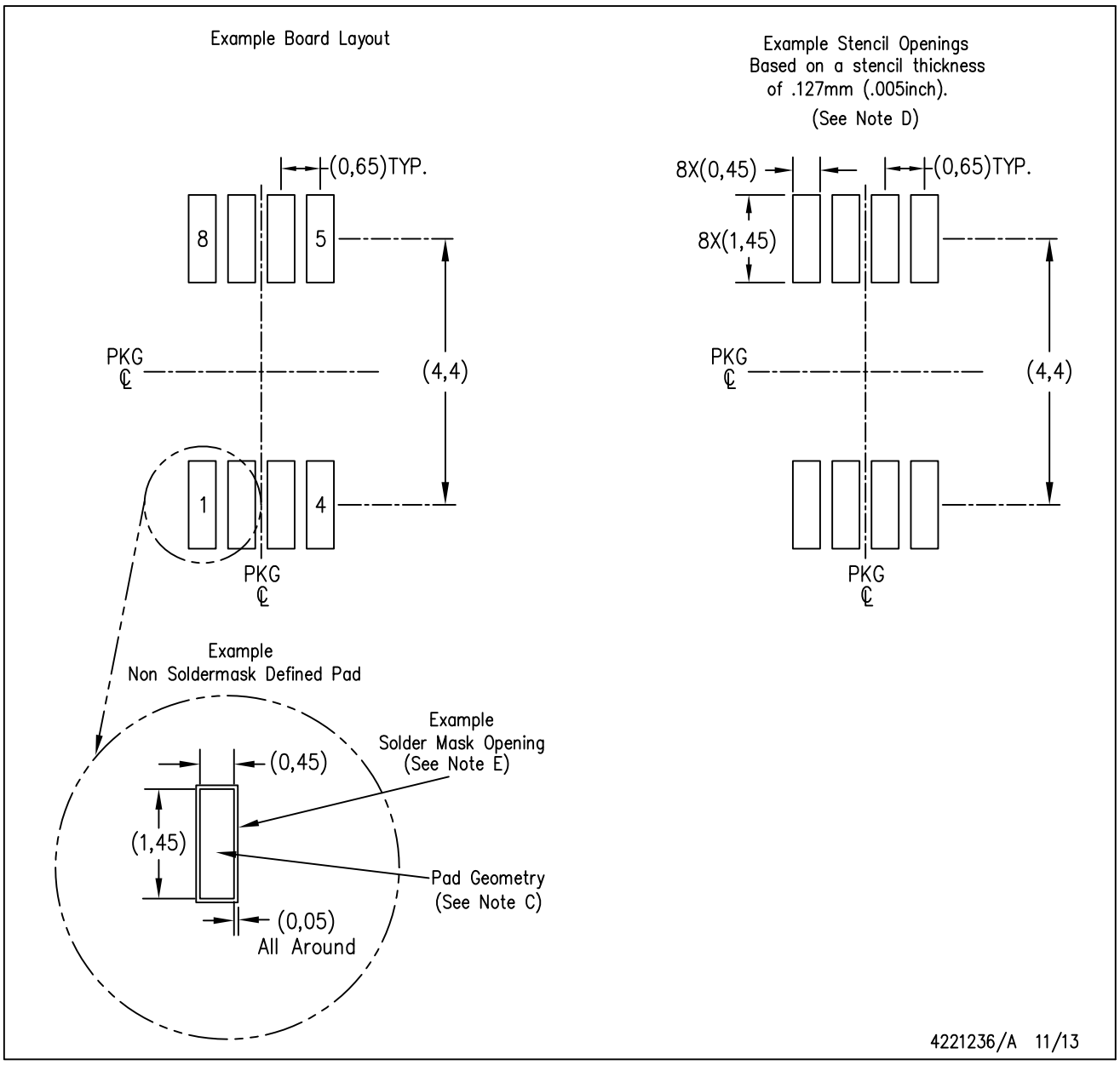
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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