THS413x High-Speed, Low-Noise, Fully-Differential I/O Amplifiers

1 Features

- High Performance
  - 150 MHz, –3 dB Bandwidth (V_{CC} = ±15 V)
  - 51 V/µs Slew Rate
  - –100 dB Third Harmonic Distortion at 250 kHz
- Low Noise
  - 1.3 nV/√Hz Input-Referred Noise
- Differential-Input/Differential-Output
  - Balanced Outputs Reject Common-Mode Noise
  - Reduced Second-Harmonic Distortion Due to Differential Output
- Wide Power-Supply Range
  - V_{CC} = 5 V Single Supply to ±15 V Dual Supply
- $I_{CC(SD)}$ = 860 µA in Shutdown Mode (THS4130)

2 Applications

- Single-Ended To Differential Conversion
- Differential ADC Driver
- Differential Antialiasing
- Differential Transmitter And Receiver
- Output Level Shifter

3 Description

The THS413x device is one in a family of fully-differential input/differential output devices fabricated using Texas Instruments' state-of-the-art BiComI complementary bipolar process.

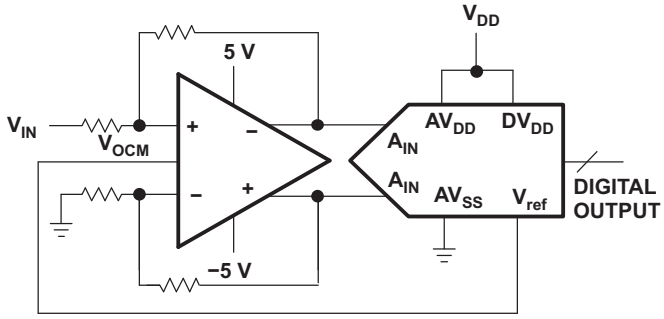
The THS413x is made of a true fully-differential signal path from input to output. This design leads to an excellent common-mode noise rejection and improved total harmonic distortion.

Device Information(1)

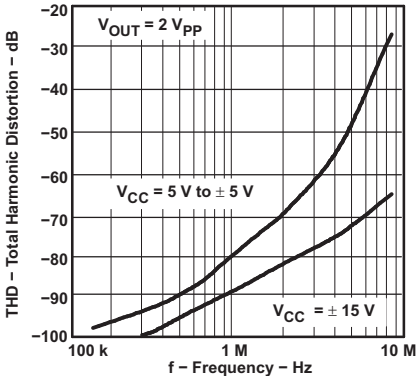
PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS4130	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm
	HVSSOP (8)	3.00 mm x 3.00 mm
THS4131	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm
	HVSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical A/D Application Circuit



Total Harmonic Distortion vs Frequency



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (May 2011) to Revision I — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision G (January 2010) to Revision H — **Page**

- Changed footnote A in Figure 45. ... 25

Changes from Revision F (January 2006) to Revision G — **Page**

- Changed DGK package specifications in the *Dissipation Rating* table ... 7

5 Device Comparison Tables

Table 1. Available Device Packages

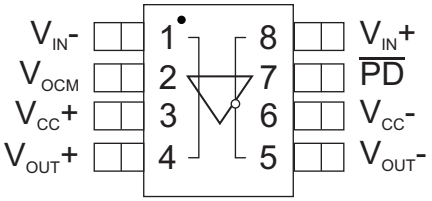
PACKAGED DEVICES						
T_A	SMALL OUTLINE (D)	MSOP PowerPAD™ (DGN)	SYMBOL	MSOP (DGK)	SYMBOL	EVALUATION MODULES
0°C to +70°C	THS4130CD	THS4130CDGN	AOB	THS4130CDGK	ATP	THS4130EVM
	THS4131CD	THS4131CDGN	AOD	THS4131CDGK	ATQ	THS4131EVM
–40°C to +85°C	THS4130ID	THS4130IDGN	AOC	THS4130IDGK	ASO	—
	THS4131ID	THS4131IDGN	AOE	THS4131IDGK	ASP	—

Table 2. Device Description Table

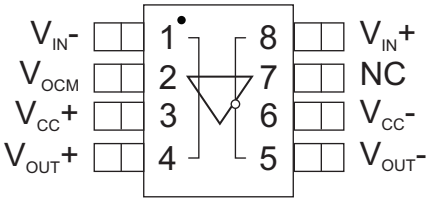
DEVICE	DESCRIPTION
THS412x	100 MHz, 43 V/µs, 3.7 nV/√Hz
THS414x	160 MHz, 450 V/µs, 6.5 nV/√Hz
THS415x	180 MHz, 850 V/µs, 9 nV/√Hz

6 Pin Configuration and Functions

D, DGN, or DGK Package
8-Pin SOIC, VSSOP, or HVSSOP
THS4130 Top View



D, DGN, or DGK Package
8-Pin SOIC, VSSOP, or HVSSOP
THS4131 Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	THS4130	THS4131		
NC	—	7	—	No connect
$\overline{PD}$	7	—	I	Active low powerdown pin
V_{CC+}	3	3	I/O	Positive supply voltage pin
$V_{CC–}$	6	6	I/O	Negative supply voltage pin
$V_{IN–}$	1	1	I	Negative input pin
V_{OCM}	2	2	I	Common mode input pin
V_{OUT+}	4	4	O	Positive output pin
$V_{OUT–}$	5	5	O	Negative output pin
V_{IN+}	8	8	I	Positive input pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage		$-V_{CC}$	$+V_{CC}$	V
V_{CC-} to V_{CC+}	Supply voltage		–33	33	V
I_O(2)	Output current			150	mA
V_{ID}	Differential input voltage		–6	6	V
	Continuous total power dissipation		See *Dissipation Ratings*		
T_J(3)	Maximum junction temperature			150	°C
T_J(4)	Maximum junction temperature, continuous operation, long-term reliability			125	°C
T_A	Operating free-air temperature	C-suffix	0	70	°C
		I-suffix	–40	85	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The THS413x may incorporate a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical briefs SLMA002 and SLMA004 for more information about using the PowerPAD thermally-enhanced package.
(3) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.
(4) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

7.2 ESD Ratings

			VALUE	UNIT
THS4130: D, DGN, OR DGK PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(1)	±1500	
THS4131: D, DGN, OR DGK PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{cc+} to V_{cc-}	Dual supply	±2.5		±15	V
	Single supply	5		30	
T_A	C-suffix	0		70	°C
	I-suffix	–40		85	

7.4 Thermal Information

THERMAL METRIC[1]		THS413x			UNIT
		D (SOIC)	DGN (VSSOP)	DGK (HVSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.5	55.8	182.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.3	61.6	72.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.8	34.5	103.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14	13.8	11.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.3	34.4	101.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics[1]

V_{CC}= ±5 V, R_L = 800Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small-signal bandwidth (–3 dB), single-ended input, differential output, V_I = 63 mV_{PP}	V_{CC} = 5	Gain = 1, R_f = 390 Ω		125		MHz
		V_{CC} = ±5	Gain = 1, R_f = 390 Ω		135		
		V_{CC} = ±15	Gain = 1, R_f = 390 Ω		150		
	Small-signal bandwidth (–3 dB), single-ended input, differential output, V_I = 63 mV_{PP}	V_{CC} = 5	Gain = 2, R_f = 750 Ω		80		
		V_{CC} = ±5	Gain = 2, R_f = 750 Ω		85		
		V_{CC} = ±15	Gain = 2, R_f = 750 Ω		90		
SR	Slew rate[2]	Gain = 1			52		V/µs
t_s	Settling time to 0.1%	Step voltage = 2 V, gain = 1			78		ns
	Settling time to 0.01%	Step voltage = 2 V, gain = 1			213		
DISTORTION PERFORMANCE							
THD	Total harmonic distortion, differential input, differential output, gain = 1, R_f = 390 Ω, R_L = 800 Ω, V_O= 2 V_{PP}	V_{CC} = 5	f = 250 kHz		–95		dBc
			f = 1 MHz		–81		
		V_{CC} = ±5	f = 250 kHz		–96		
			f = 1 MHz		–80		
		V_{CC} = ±15	f = 250 kHz		–97		
			f = 1 MHz		–80		
	V_O = 4 V_{PP}	V_{CC} = ±5	f = 250 kHz		–91		
			f = 1 MHz		–75		
		V_{CC} = ±15	f = 250 kHz		–91		
			f = 1 MHz		–75		
SFDR	Spurious-free dynamic range, differential input, differential output, gain = 1, R_f = 390 Ω, R_L = 800 Ω, f = 250 kHz	V_O= 2 V_{PP}	V_{CC} = ±2.5		97		dB
			V_{CC} = ±5		98		
			V_{CC} = ±15		99		
		V_O = 4 V_{PP}	V_{CC} = ±5		93		
			V_{CC} = ±15		95		

(1) The full range temperature is 0°C to +70°C for the C-suffix, and –40°C to +85°C for the I-suffix.
(2) Slew rate is measured from an output level range of 25% to 75%.

Electrical Characteristics(1) (continued)

V_{CC}= ±5 V, R_L = 800Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Third intermodulation distortion		$V_{I(PP)}$ = 4 V, G = 1, F1 = 3 MHz, F2 = 3.5 MHz			–53		dBc
Third-order intercept		$V_{I(PP)}$ = 4 V, G = 1, F1 = 3 MHz, F2 = 3.5 MHz			41.5		dB
NOISE PERFORMANCE							
V_n	Input voltage noise	f = 10 kHz			1.3		nV/√Hz
I_n	Input current noise	f = 10 kHz			1		pA/√Hz
DC PERFORMANCE							
	Open-loop gain	T_A = +25°C		71	78		dB
		T_A = full range		69			
$V_{(OS)}$	Input offset voltage	T_A = +25°C			0.2	2	mV
		T_A = full range				3	
	Common-mode input offset voltage, referred to V_{OCM}	T_A = +25°C			0.2	3.5	
	Input offset voltage drift	T_A = full range			4.5		µV/°C
I_{IB}	Input bias current	T_A = full range			2	6	µA
I_{OS}	Input offset current	T_A = full range			100	500	nA
	Offset drift				2		nA/°C
INPUT CHARACTERISTICS							
CMRR	Common-mode rejection ratio	T_A = full range		80	95		dB
V_{ICR}	Common-mode input voltage range			–3.7 7 to 4.3	–4 to 4.5		V
R_I	Input resistance	Measured into each input terminal			34		MΩ
C_I	Input capacitance, closed loop				4		pF
r_o	Output resistance	Open loop			41		Ω
OUTPUT CHARACTERISTICS							
	Output voltage swing	V_{CC} = 5 V	T_A = +25°C	1.2 to 3.8	0.9 to 4.1		V
			T_A = full range	1.3 to 3.7	±4		
		V_{CC} = ±5 V	T_A = +25°C	±3.7			
			T_A = full range	±3.6			
		V_{CC} = ±15 V	T_A = +25°C	±10.5	±12.4		
			T_A = full range	±10.2			

Electrical Characteristics(1) (continued)

V_{CC}= ±5 V, R_L = 800Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_O	Output current	V_{CC} = 5 V, R_L = 7 Ω	T_A = +25°C	25	45		mA
			T_A = full range	20			
		V_{CC} = ±5 V, R_L = 7 Ω	T_A = +25°C	30	55		
			T_A = full range	28			
		V_{CC} = ±15 V, R_L = 7 Ω	T_A = +25°C	60	85		
			T_A = full range	65			
POWER SUPPLY							
V_{CC}	Supply voltage range	Single supply		4		33	V
		Split supply		±2		±16.5	
I_{CC}	Quiescent current	V_{CC} = ±5 V	T_A = +25°C		12.3	15	mA
			T_A = full range			16	
		V_{CC} = ±15 V	T_A = +25°C		14		
$I_{CC(SD)}$	Quiescent current (shutdown) (THS4130 only)(3)	V = –5 V	T_A = +25°C		0.86	1.4	mA
			T_A = full range			1.5	
PSRR	Power-supply rejection ratio (dc)		T_A = +25°C	73	98		dB
			T_A = full range	70			

(3) For detailed information on the behavior of the power-down circuit, see the *Power-Down Mode* section.

7.6 Dissipation Ratings

PACKAGE	θ_{JA}(1) (°C/W)	θ_{JC} (°C/W)	POWER RATING(2)	
			T_A= +25°C	T_A = +85°C
D	97.5	38.3	1.02 W	410 mW
DGN	58.4	4.7	1.71 W	685 mW
DGK	134	72	750 mW	300 mW

(1) This data was taken using the JEDEC standard High-K test PCB.
(2) Power rating is determined with a junction temperature of +125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below +125°C for best performance and long-term reliability.

7.7 Typical Characteristics

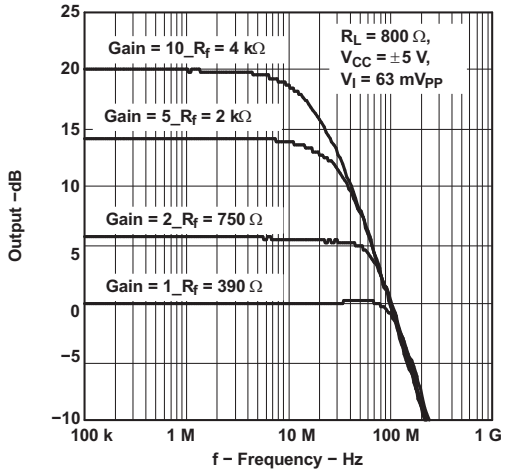


Figure 1. Small-Signal Frequency Response

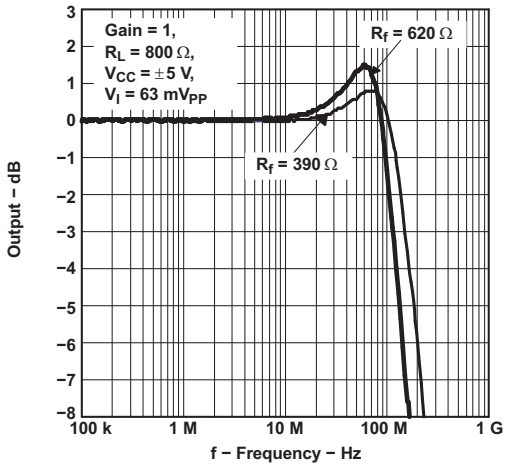


Figure 2. Small-Signal Frequency Response

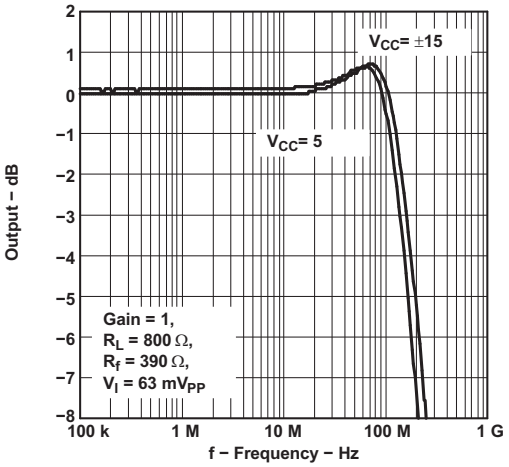


Figure 3. Small-Signal Frequency Response (Various Supplies)

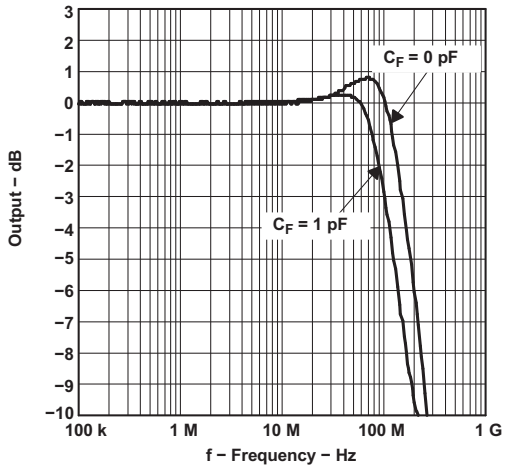


Figure 4. Small-Signal Frequency Response (Various C_F)

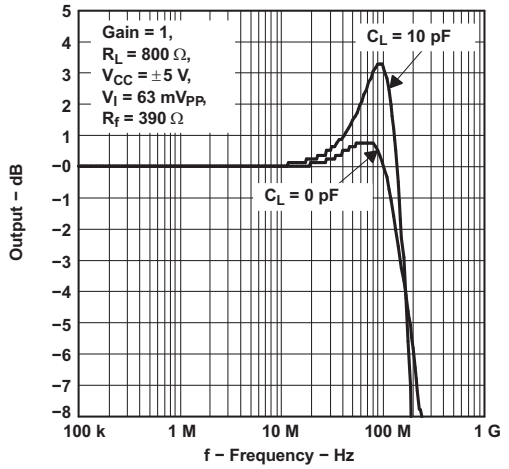


Figure 5. Small-Signal Frequency Response (Various C_L)

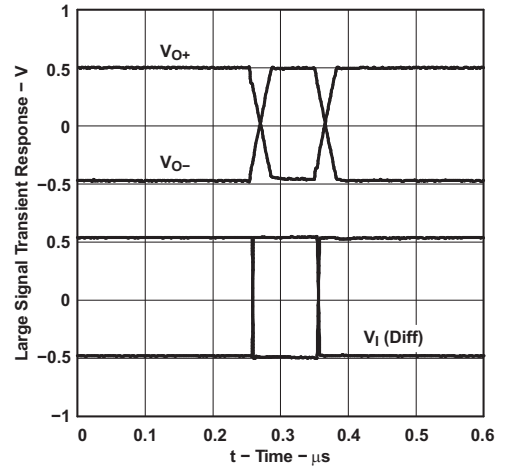


Figure 6. Large-Signal Transient Response (Differential In/Single Out)

Typical Characteristics (continued)

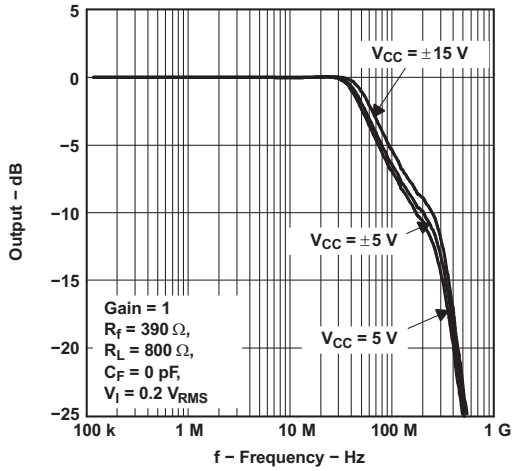


Figure 7. Large-Signal Frequency Response

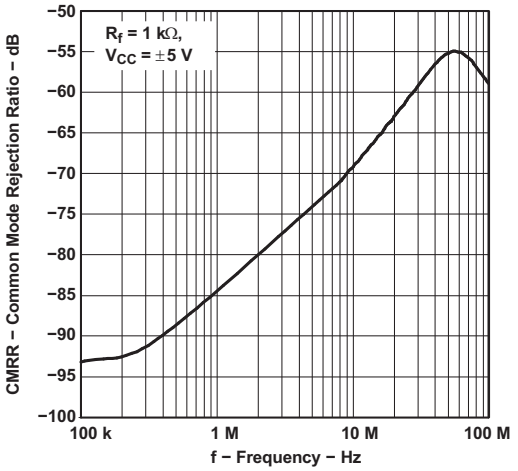


Figure 8. Common-Mode Rejection Ratio vs Frequency

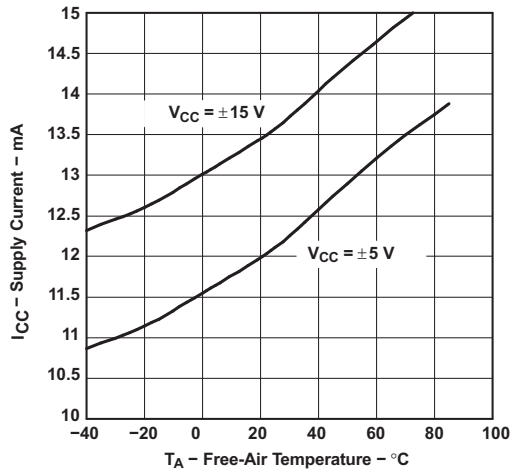


Figure 9. Supply Current vs Free-Air Temperature

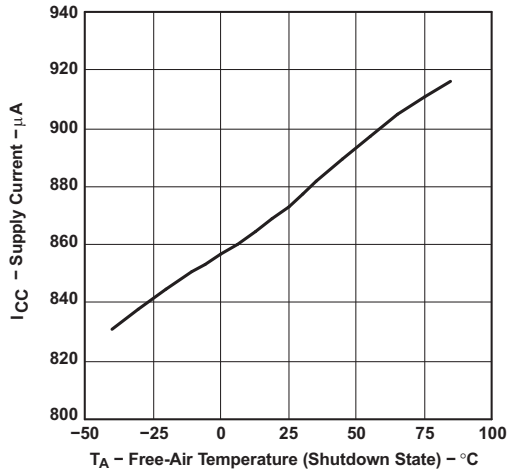


Figure 10. Supply Current vs Free-Air Temperature (Shutdown State)

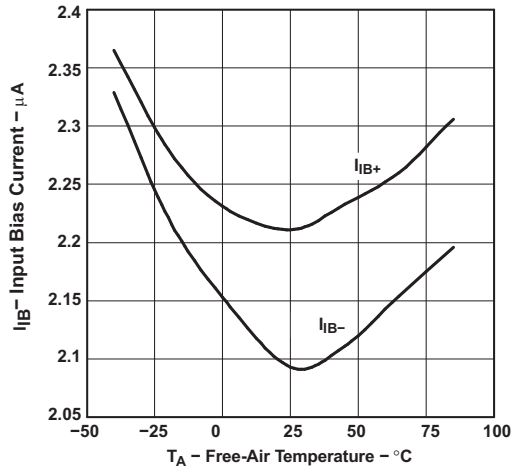


Figure 11. Input Bias Current vs Free-Air Temperature

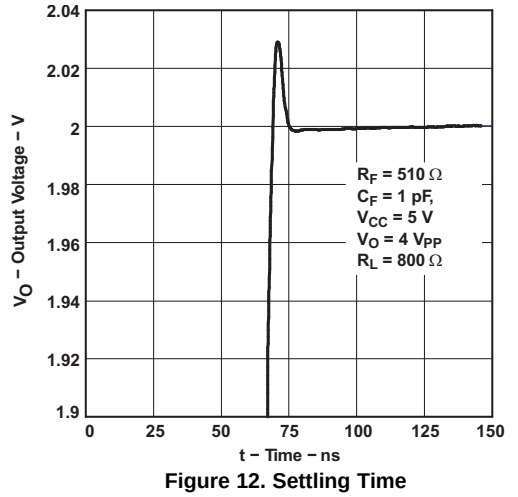


Figure 12. Settling Time

Typical Characteristics (continued)

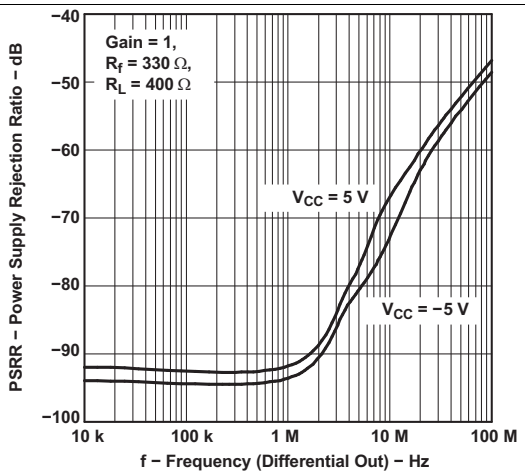


Figure 13. Power-Supply Rejection Ratio vs Frequency (Differential Out)

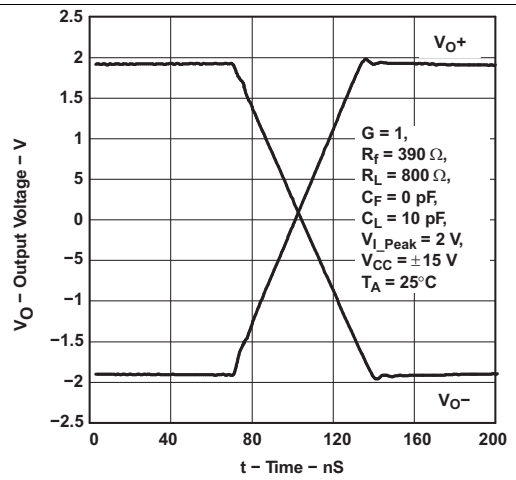


Figure 14. Large-Signal Transient Response

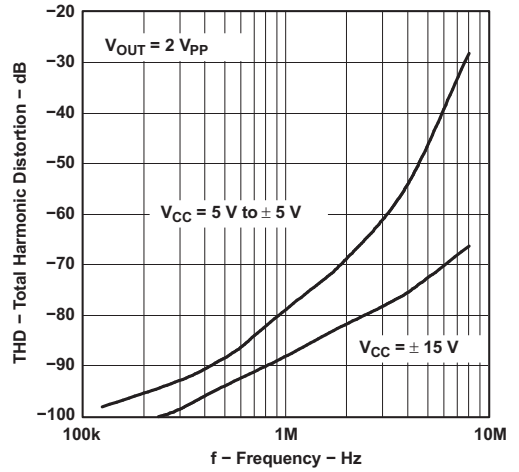


Figure 15. Total Harmonic Distortion vs Frequency

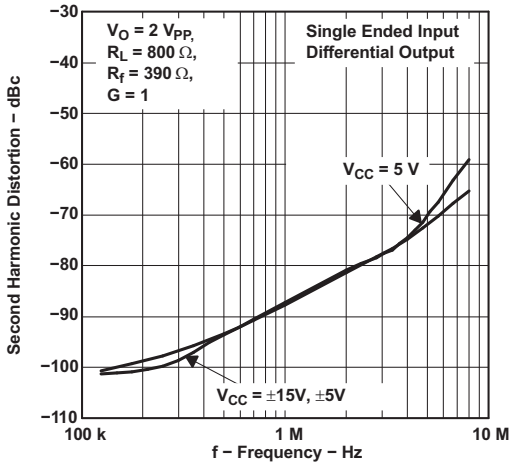


Figure 16. Second-Harmonic Distortion vs Frequency

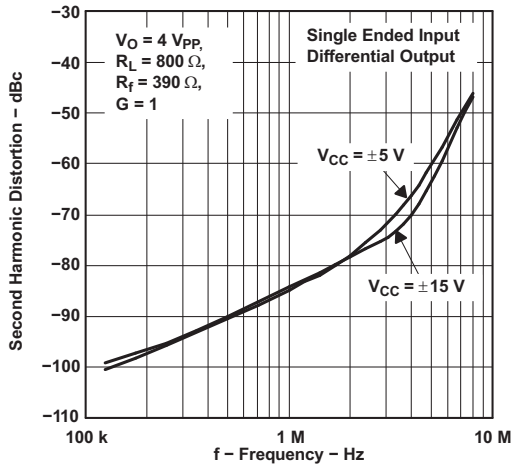


Figure 17. Second-Harmonic Distortion vs Frequency

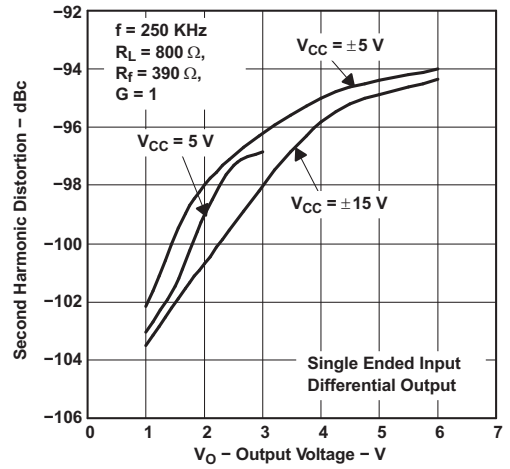


Figure 18. Second-Harmonic Distortion vs Output Voltage

Typical Characteristics (continued)

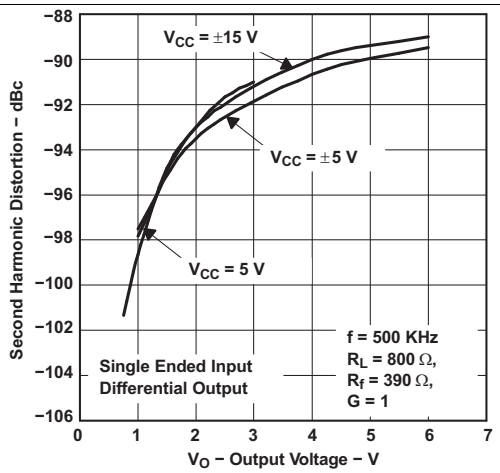


Figure 19. Second-Harmonic Distortion vs Output Voltage

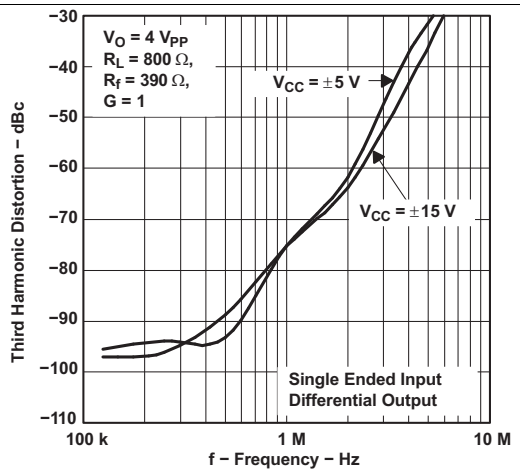


Figure 20. Third-Harmonic Distortion vs Frequency

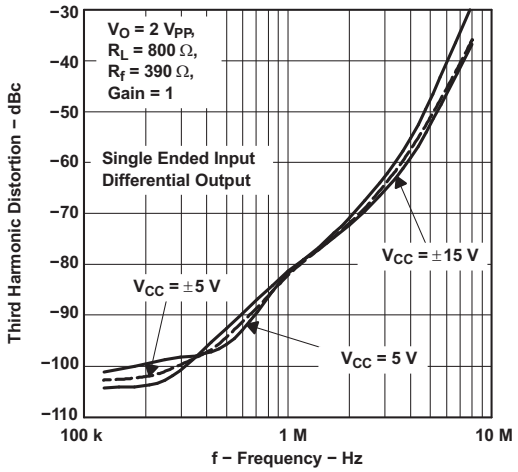


Figure 21. Third-Harmonic Distortion vs Frequency

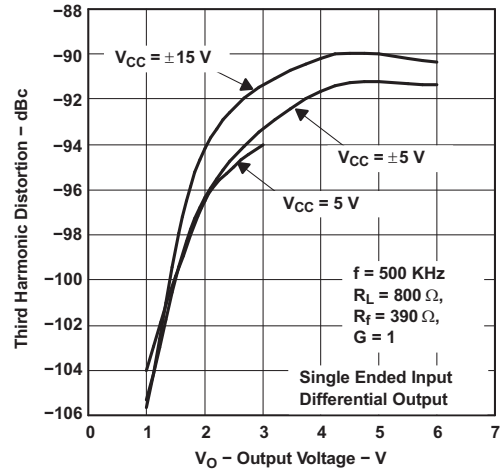


Figure 22. Third-Harmonic Distortion vs Output Voltage

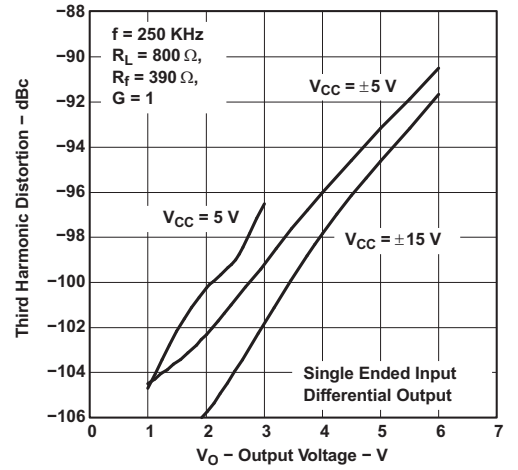


Figure 23. Third-Harmonic Distortion vs Output Voltage

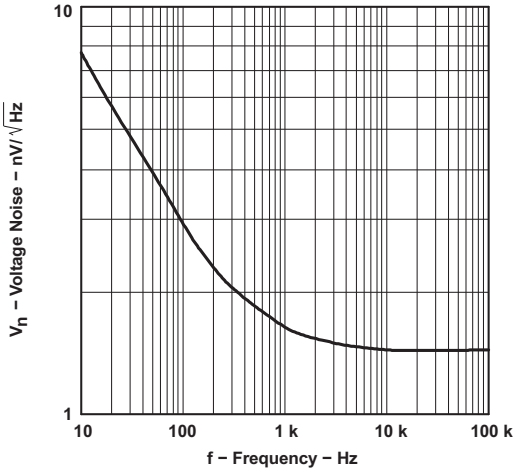


Figure 24. Voltage Noise vs Frequency

Typical Characteristics (continued)

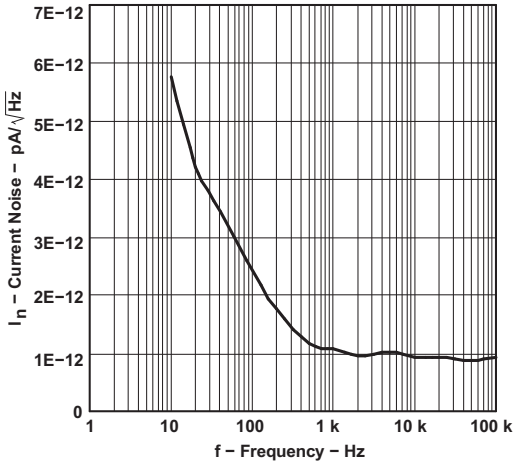


Figure 25. Current Noise vs Frequency

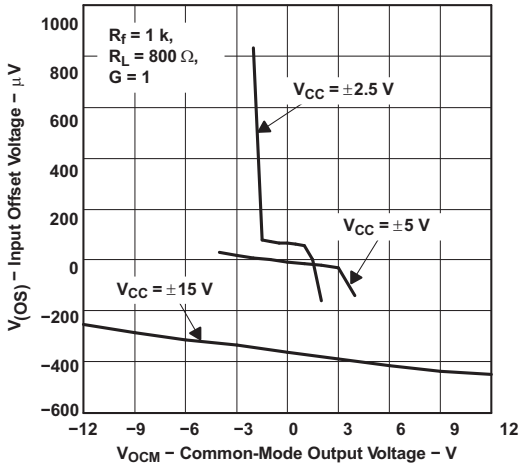


Figure 26. Input Offset Voltage vs Common-Mode Output Voltage

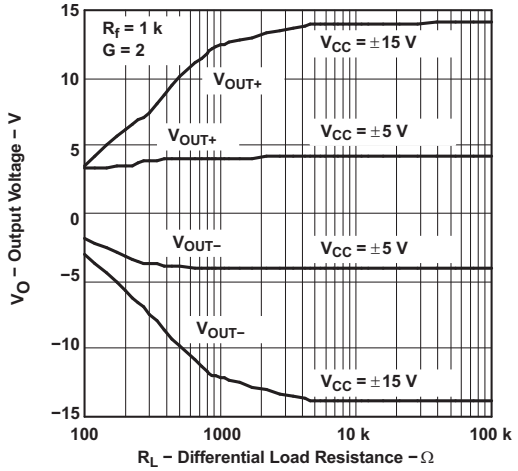


Figure 27. Output Voltage vs Differential Load Resistance

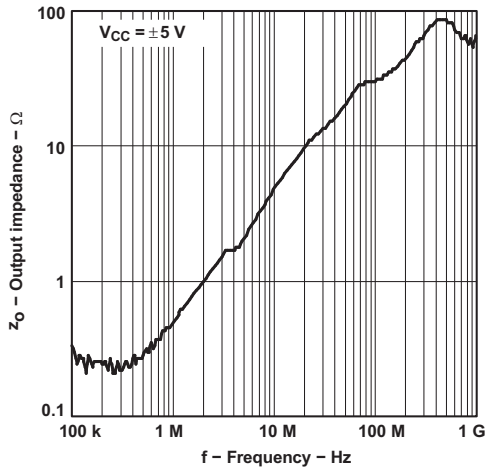


Figure 28. Output Impedance vs Frequency

8 Detailed Description

8.1 Overview

The THS413x is a fully-differential amplifier. Differential amplifiers are typically *differential in/single out*, whereas fully-differential amplifiers are *differential in/differential out*.

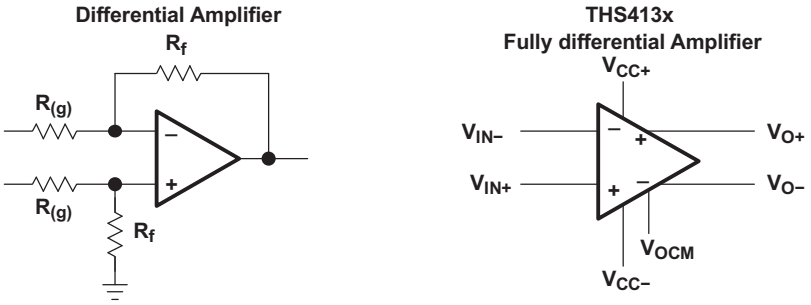


Figure 29. Differential Amplifier Versus a Fully-Differential Amplifier

To understand the THS413x fully-differential amplifiers, the definition for the pin outs of the amplifier are provided.

$$\text{Input voltage definition } V_{ID} = (V_{I+}) - (V_{I-})\ V_{IC} = \frac{(V_{I+}) + (V_{I-})}{2} \tag{1}$$

$$\text{Output voltage definition } V_{OD} = (V_{O+}) - (V_{O-})\ \ V_{OC} = \frac{(V_{O+}) + (V_{O-})}{2} \tag{2}$$

$$\text{Transfer function } \ V_{OD} = V_{ID} \times A_{(f)} \tag{3}$$

$$\text{Output common mode voltage } \ V_{OC} = V_{OCM} \tag{4}$$

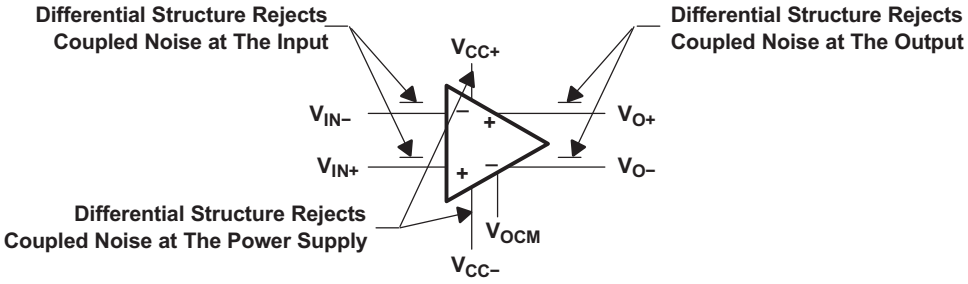


Figure 30. Definition of the Fully-Differential Amplifier

If each output is measured independently, each output is one-half of the input signal when gain is 1. The following equations express the transfer function for each output:

$$V_O = \frac{1}{2} V_I \tag{5}$$

The second output is equal and opposite in sign:

$$V_O = -\frac{1}{2} V_I \tag{6}$$

Fully-differential amplifiers may be viewed as two inverting amplifiers. In this case, the equation of an inverting amplifier holds true for gain calculations. One advantage of fully-differential amplifiers is that they offer twice as much dynamic range compared to single-ended amplifiers. For example, a 1-V_{PP} ADC can only support an input signal of 1 V_{PP}. If the output of the amplifier is 2 V_{PP}, then it is not as practical to feed a 2-V_{PP} signal into the targeted ADC. Using a fully-differential amplifier enables the user to break down the output into two 1-V_{PP} signals with opposite signs and feed them into the differential input nodes of the ADC. In practice, the designer has been

Overview (continued)

able to feed a 2-V peak-to-peak signal into a 1-V differential ADC with the help of a fully-differential amplifier. The final result indicates twice as much dynamic range. Figure 31 illustrates the increase in dynamic range. The gain factor should be considered in this scenario. The THS413x fully-differential amplifier offers an improved CMRR and PSRR due to its symmetrical input and output. Furthermore, second-harmonic distortion is improved. Second harmonics tend to cancel because of the symmetrical output.

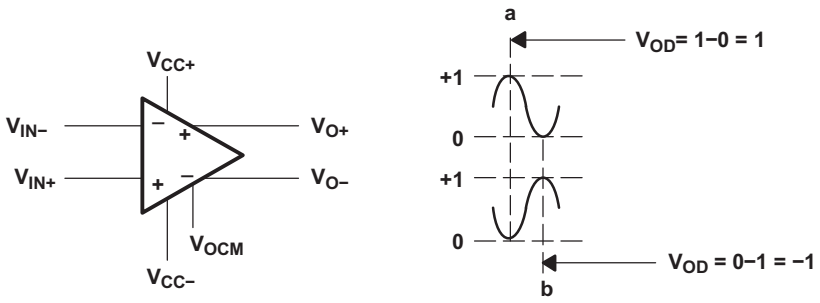


Figure 31. Fully-Differential Amplifier With Two 1-V_{PP} Signals

Similar to the standard inverting amplifier configuration, input impedance of a fully-differential amplifier is selected by the input resistor, $R_{(g)}$. If input impedance is a constraint in design, the designer may choose to implement the differential amplifier as an instrumentation amplifier. This configuration improves the input impedance of the fully-differential amplifier. Figure 32 depicts the general format of instrumentation amplifiers.

The general transfer function for this circuit is:

$$\frac{V_{OD}}{V_{IN1} - V_{IN2}} = \frac{R_f}{R_{(g)}}\left(1 + \frac{2R2}{R1}\right) \quad (7)$$

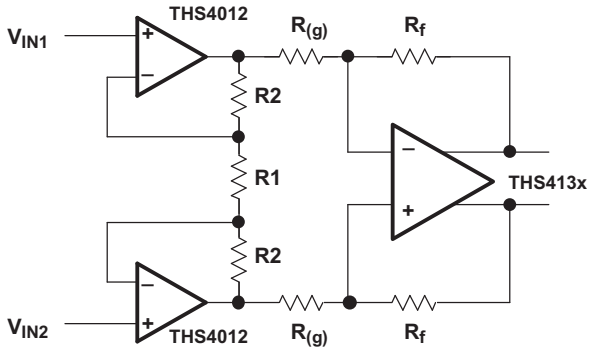
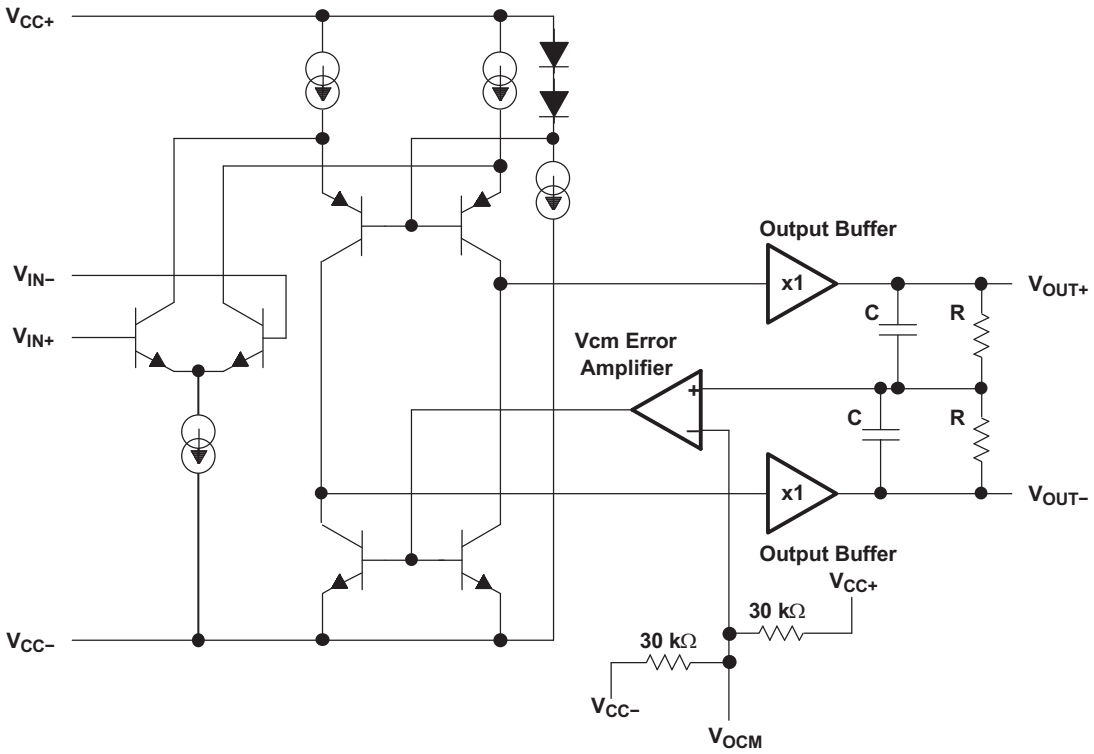


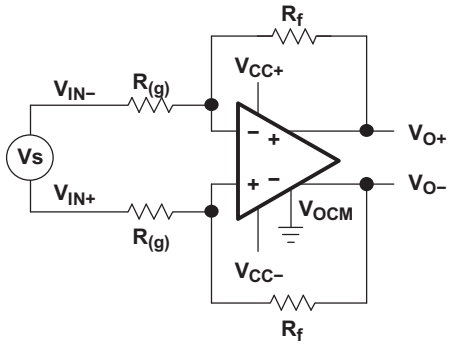
Figure 32. Instrumentation Amplifier

8.2 Functional Block Diagram



8.3 Feature Description

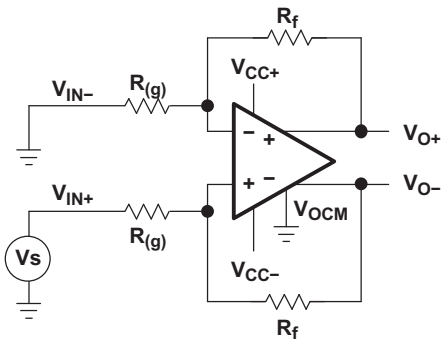
Figure 33 and Figure 34 depict the differences between the operation of the THS413x fully-differential amplifier in two different modes. Fully-differential amplifiers can work with differential input or can be implemented as single in/differential out.



Note: For proper operation, maintain symmetry by setting $R_f1 = R_f2 = R_f$ and $R_{(g)}1 = R_{(g)}2 = R_{(g)} \Rightarrow A = R_f/R_{(g)}$

Figure 33. Amplifying Differential Signals

Feature Description (continued)



RECOMMENDED RESISTOR VALUES

GAIN	$R_{(g)}$ Ω	R_f Ω
1	390	390
2	374	750
5	402	2010
10	402	4020

Figure 34. Single In With Differential Out

8.4 Device Functional Modes

8.4.1 Power-Down Mode

The power-down mode is used when power saving is required. The power-down terminal ($\overline{PD}$) found on the THS413x is an active low terminal. If it is left as a no-connect terminal, the device always stays on due to an internal 50 kΩ resistor to V_{CC}. The threshold voltage for this terminal is approximately 1.4 V above $V_{CC–}$. This means that if the $\overline{PD}$ terminal is 1.4 V above $V_{CC–}$, the device is active. If the $\overline{PD}$ terminal is less than 1.4 V above $V_{CC–}$, the device is off. For example, if $V_{CC–}$ = –5 V, then the device is on when PD reaches –3.6 V, (–5 V + 1.4 V = –3.6 V). By the same calculation, the device is off below –3.6 V. It is recommended to pull the terminal to $V_{CC–}$ in order to turn the device off. Figure 35 shows the simplified version of the power-down circuit. While in the power-down state, the amplifier goes into a high-impedance state. The amplifier output impedance is typically greater than 1 MΩ in the power-down state.

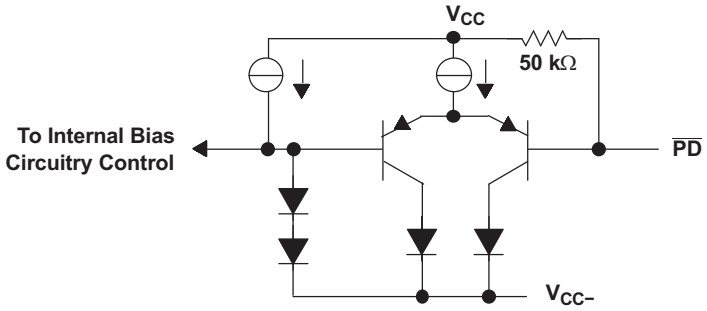


Figure 35. Simplified Power-Down Circuit

Due to the similarity of the standard inverting amplifier configuration, the output impedance appears to be very low while in the power-down state. This is because the feedback resistor (R_f) and the gain resistor ($R_{(g)}$) are still connected to the circuit. Therefore, a current path is allowed between the input of the amplifier and the output of the amplifier. An example of the closed loop output impedance is shown in Figure 36.

Device Functional Modes (continued)

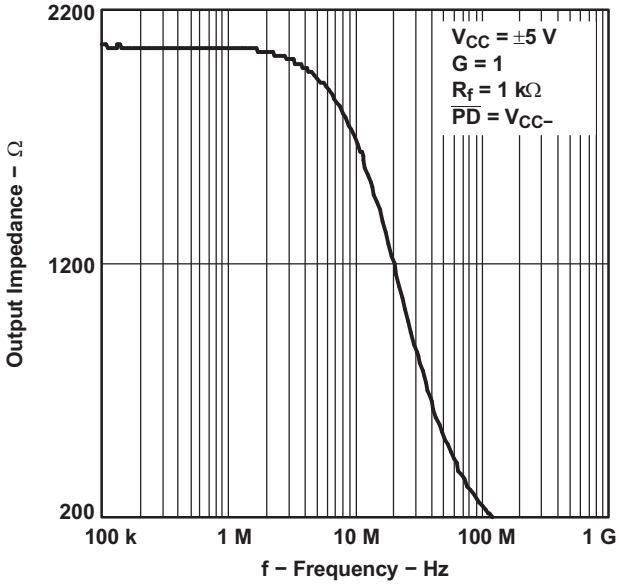


Figure 36. Output Impedance (in Power-Down) vs Frequency

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Resistor Matching

Resistor matching is important in fully-differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistor. CMRR, PSRR, and cancellation of the second-harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized.

V_{OCM} sets the dc level of the output signals. If no voltage is applied to the V_{OCM}pin, it is set to the midrail voltage internally defined as:

$$\frac{(V_{CC+})+(V_{CC-})}{2} \tag{8}$$

In the differential mode, the V_{OCM} on the two outputs cancel each other. Therefore, the output in the differential mode is the same as the input in the gain of 1. V_{OCM} has a high bandwidth capability up to the typical operation range of the amplifier. For the prevention of noise going through the device, use a 0.1 µF capacitor on the V_{OCM} pin as a bypass capacitor. The *Functional Block Diagram* shows the simplified diagram of the THS413x.

9.1.2 Driving a Capacitive Load

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS413x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the device phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 37. A minimum value of 20 Ω should work well for most applications. For example, in 50-Ω transmission systems, setting the series resistor value to 50 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

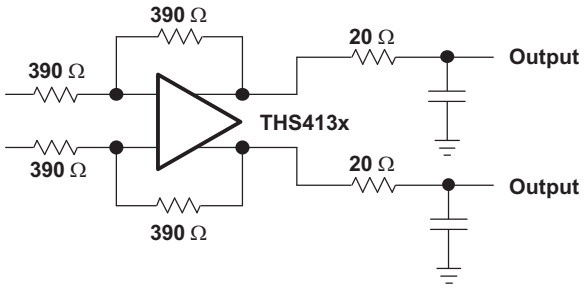


Figure 37. Driving a Capacitive Load

9.1.3 Data Converters

Data converters are one of the most popular applications for the fully-differential amplifiers. Figure 38 shows a typical configuration of a fully-differential amplifier attached to a differential analog-to-digital converter (ADC).

Application Information (continued)

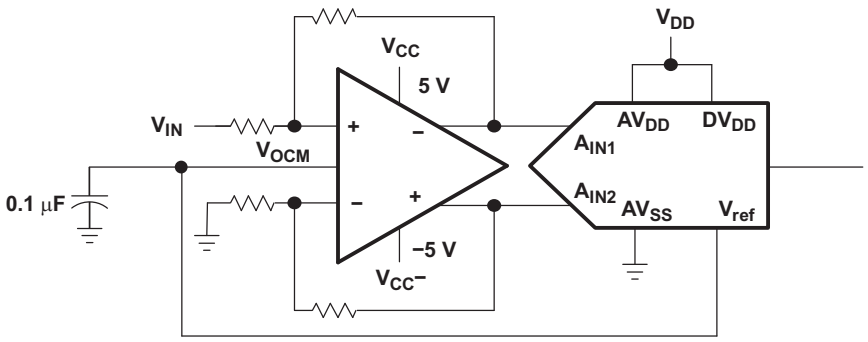


Figure 38. Fully-Differential Amplifier Attached to a Differential ADC

Fully-differential amplifiers can operate with a single supply. V_{OCM} defaults to the midrail voltage, $V_{CC}/2$. The differential output may be fed into a data converter. This method eliminates the use of a transformer in the circuit. If the ADC has a reference voltage output (V_{ref}), then it is recommended to connect it directly to the V_{OCM} of the amplifier using a bypass capacitor for stability. For proper operation, the input common-mode voltage to the input terminal of the amplifier should not exceed the common-mode input voltage range.

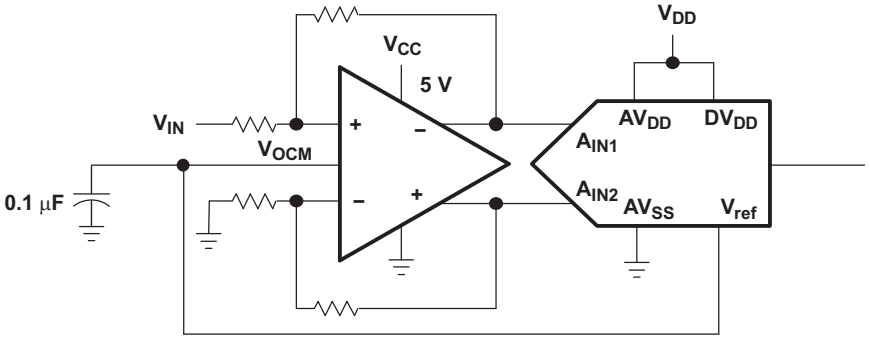


Figure 39. Fully-Differential Amplifier Using a Single Supply

9.1.4 Single-Supply Applications

Some single-supply applications may require the input voltage to exceed the common-mode input voltage range. In such cases, the circuit configuration of Figure 40 is suggested to bring the common-mode input voltage within the specifications of the amplifier.

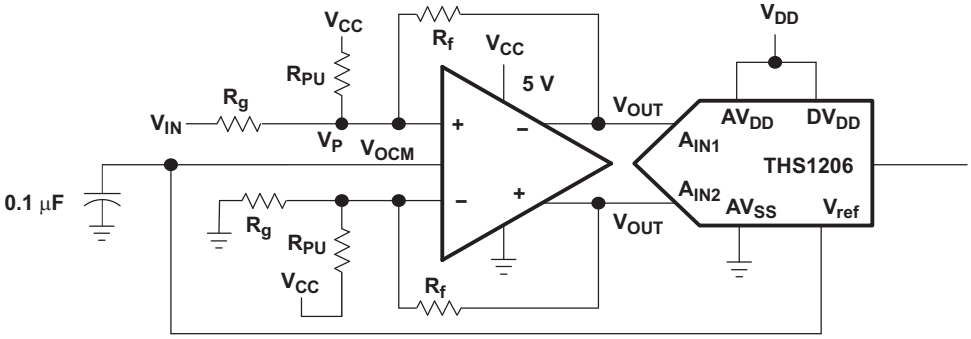


Figure 40. Circuit With Improved Common-Mode Input Voltage

Equation 9 is used to calculate R_{PU}:

Application Information (continued)

$$R_{PU} = \frac{V_P - V_{CC}}{(V_{IN} - V_P)\frac{1}{RG} + (V_{OUT} - V_P)\frac{1}{RF}} \quad (9)$$

9.2 Typical Application

For signal conditioning in ADC applications, it is important to limit the input frequency to the ADC. Low-pass filters can prevent the aliasing of the high-frequency noise with the frequency of operation. Figure 41 presents a method by which the noise may be filtered in the THS413x.

Figure 41 shows a typical application design example for the THS413x device in active low-pass filter topology driving and ADC.

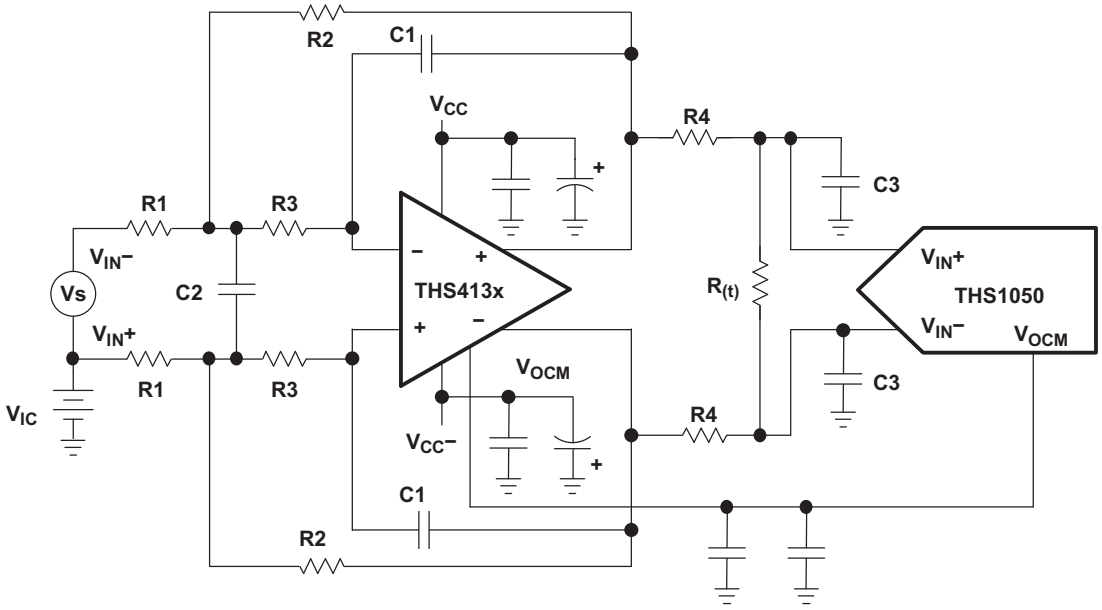


Figure 41. Antialias Filtering

9.2.1 Design Requirements

Table 3 shows example design parameters and values for the typical application design example in Figure 41.

Table 3. Design Parameters

DESIGN PARAMETERS	VALUE
Supply voltage	±2.5 V to ±15 V
Amplifier topology	Voltage feedback
Output control	DC coupled with output common mode control capability
Filter requirement	500 kHz, Multiple feedback low pass filter

9.2.2 Detailed Design Procedure

9.2.2.1 Active Antialias Filtering

Figure 41 shows a multiple-feedback (MFB) lowpass filter. The transfer function for this filter circuit is:

$$H_d(f) = \left(\frac{K}{-\left(\frac{f}{FSF \times fc}\right)^2 + \frac{1}{Q}\frac{jf}{FSF \times fc} + 1} \right) \times \left(\frac{\frac{Rt}{2R4 + Rt}}{1 + \frac{j2\pi fR4RtC3}{2R4 + Rt}} \right) \text{ Where } K = \frac{R2}{R1} \quad (10)$$

$$FSF \times fc = \frac{1}{2\pi\sqrt{2 \times R2R3C1C2}} \text{ and } Q = \frac{\sqrt{2 \times R2R3C1C2}}{R3C1 + R2C1 + KR3C1} \quad (11)$$

K sets the pass band gain, fc is the cutoff frequency for the filter, FSF is a frequency scaling factor, and Q is the quality factor.

$$FSF = \sqrt{Re^2 + |Im|^2} \text{ and } Q = \frac{\sqrt{Re^2 + |Im|^2}}{2Re} \quad (12)$$

where Re is the real part, and Im is the imaginary part of the complex pole pair. Setting R2 = R, R3 = mR, C1 = C, and C2 = nC results in:

$$FSF \times fc = \frac{1}{2\pi RC\sqrt{2 \times mn}} \text{ and } Q = \frac{\sqrt{2 \times mn}}{1 + m(1 + K)} \quad (13)$$

Start by determining the ratios, m and n, required for the gain and Q of the filter type being designed, then select C and calculate R for the desired fc.

9.2.3 Application Curve

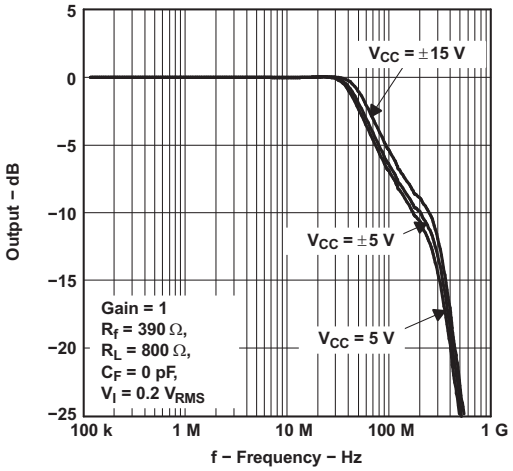


Figure 42. Large-Signal Frequency Response

10 Power Supply Recommendations

The THS413x device was designed to be operated on power supplies ranging from 2.5V to 15V. Single power supplies ranging from 5V to 30V can also be used. TI recommends using power-supply accuracy of 5%, or better. When operated on a board with high-speed digital signals, it is important to provide isolation between digital signal noise and the analog input pins. The THS413x is connected to power supplies through pin 3 (V_{CC+}) and pin 6 (V_{CC-}). Each supply pin should be decoupled to GND as close to the device as possible with a low-inductance, surface-mount ceramic capacitor of approximately 10 nF. When vias are used to connect the bypass capacitors to a ground plane the vias should be configured for minimal parasitic inductance. One method of reducing via inductance is to use multiple vias. For broadband systems, two capacitors per supply pin are advised.

To avoid undesirable signal transients, the THS413x device should not be powered on with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs when an ADC is used in the application.

11 Layout

11.1 Layout Guidelines

To achieve the levels of high-frequency performance of the THS413x device, follow proper printed-circuit board (PCB) high-frequency design techniques. A general set of guidelines is given below. In addition, a THS413x device evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power-supply decoupling—Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board are the best implementation.
- Short trace runs/compact part placements—Optimum high-frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high-frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

11.2 Layout Example

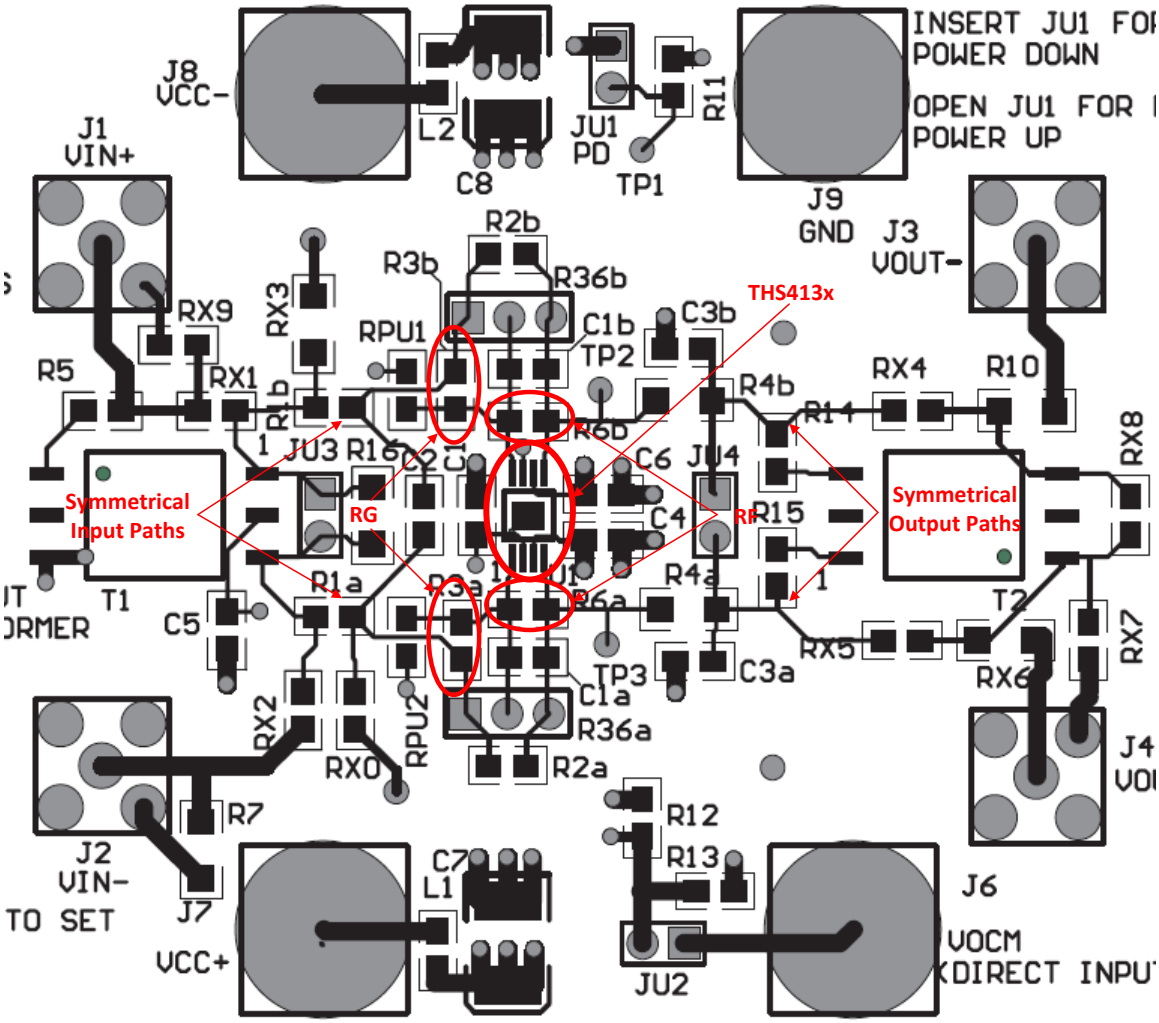


Figure 43. THS413x EVM Top Layer

Layout Example (continued)

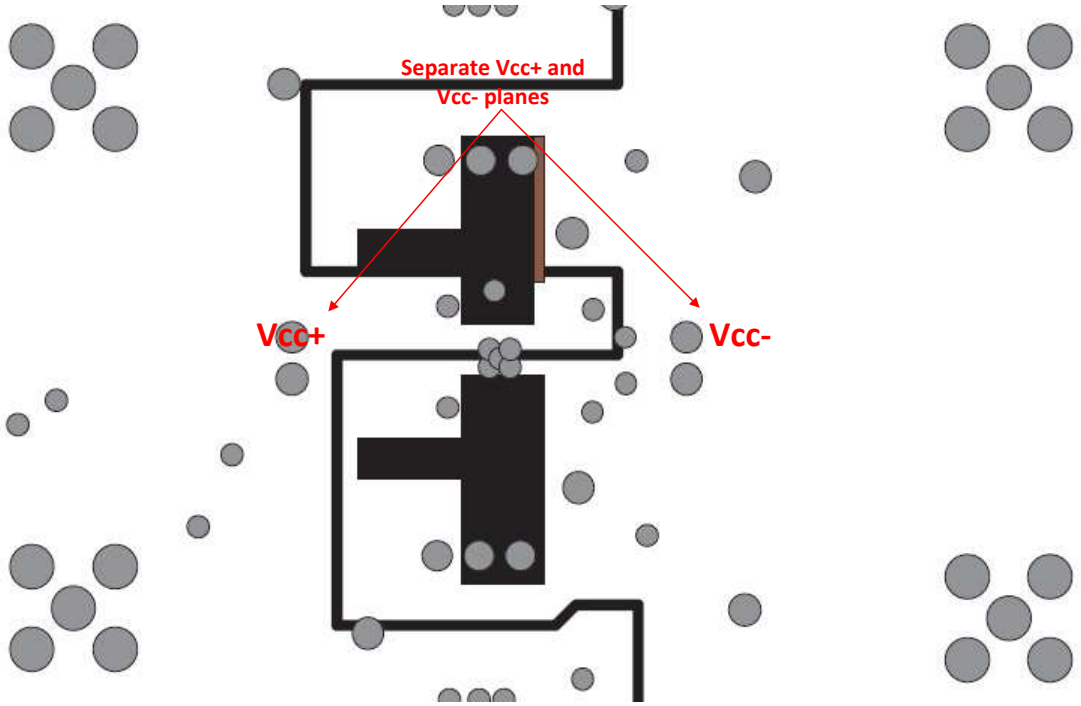


Figure 44. THS413x EVM Layer 3

11.3 General PowerPAD Design Considerations

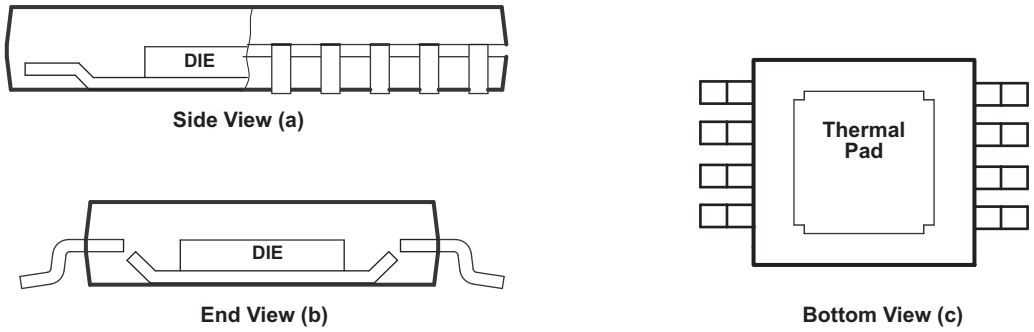
The THS413x is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted (see Figure 45**a** and Figure 45**b**). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see Figure 45**c**). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the previously awkward mechanical methods of heatsinking.

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, (*PowerPAD Thermally-Enhanced Package*, SLMA002). This document can be found on the TI website (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to SLMA002 when ordering.

General PowerPAD Design Considerations (continued)



A. The thermal pad (PowerPAD) is electrically isolated from all other pins and can be connected to any potential from V_{CC-} to V_{CC+}. Typically, the thermal pad is connected to the ground plane because this plane tends to physically be the largest and is able to dissipate the most amount of heat.

Figure 45. Views of Thermally-Enhanced DGN Package

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

EVM User's Guide for High-Speed Fully-Differential Amplifier, SLOU101

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
THS4130	Click here	Click here	Click here	Click here	Click here
THS4131	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4130CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	4130C	Samples
THS4130CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	4130C	Samples
THS4130CDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	Call TI | NIPDAU	Level-1-260C-UNLIM	0 to 70	ATP	Samples
THS4130CDGN	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOB	Samples
THS4130CDGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOB	Samples
THS4130CDGNRG4	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOB	Samples
THS4130ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I	Samples
THS4130IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	Call TI | NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASO	Samples
THS4130IDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 85	ASO	Samples
THS4130IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	Call TI | NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASO	Samples
THS4130IDGN	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOC	Samples
THS4130IDGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOC	Samples
THS4130IDGNRG4	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOC	Samples
THS4130IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I	Samples
THS4130IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I	Samples
THS4131CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	4131C	Samples
THS4131CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	4131C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4131CDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	Call TI | NIPDAU	Level-1-260C-UNLIM	0 to 70	ATQ	Samples
THS4131CDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	0 to 70	ATQ	Samples
THS4131CDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	Call TI | NIPDAU	Level-1-260C-UNLIM	0 to 70	ATQ	Samples
THS4131CDGN	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOD	Samples
THS4131CDGNG4	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOD	Samples
THS4131CDGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOD	Samples
THS4131CDGNRG4	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOD	Samples
THS4131CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	4131C	Samples
THS4131ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I	Samples
THS4131IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I	Samples
THS4131IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	Call TI | NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASP	Samples
THS4131IDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 85	ASP	Samples
THS4131IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASP	Samples
THS4131IDGN	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOE	Samples
THS4131IDGNG4	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOE	Samples
THS4131IDGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOE	Samples
THS4131IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

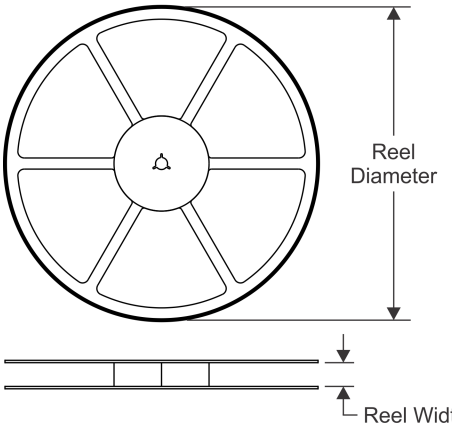
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

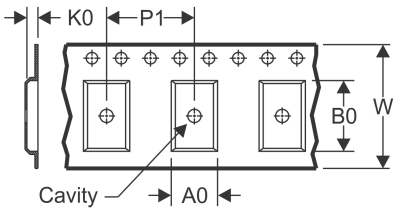
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

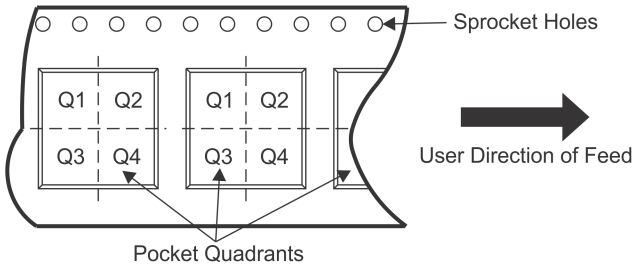


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

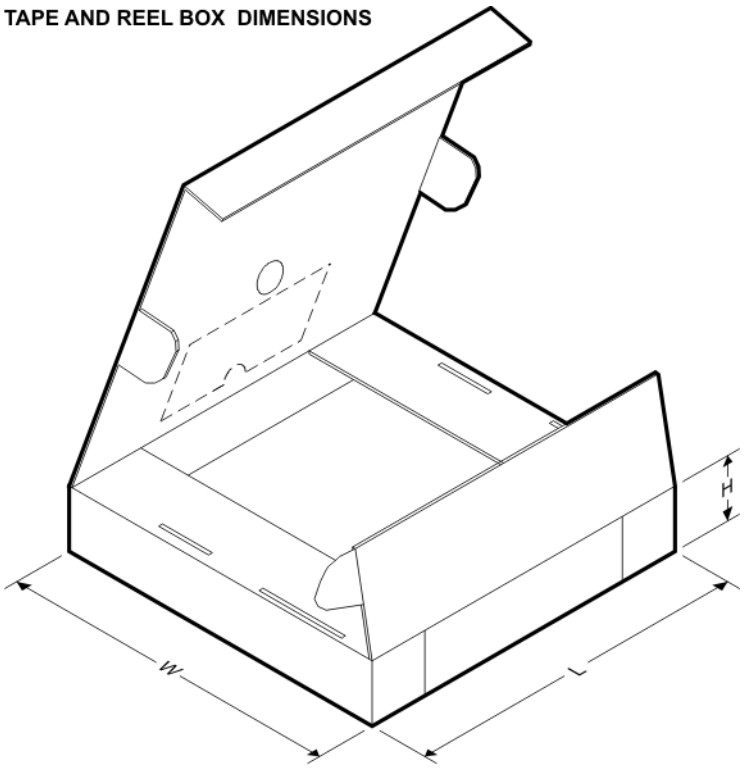
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4130CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4131CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4131IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

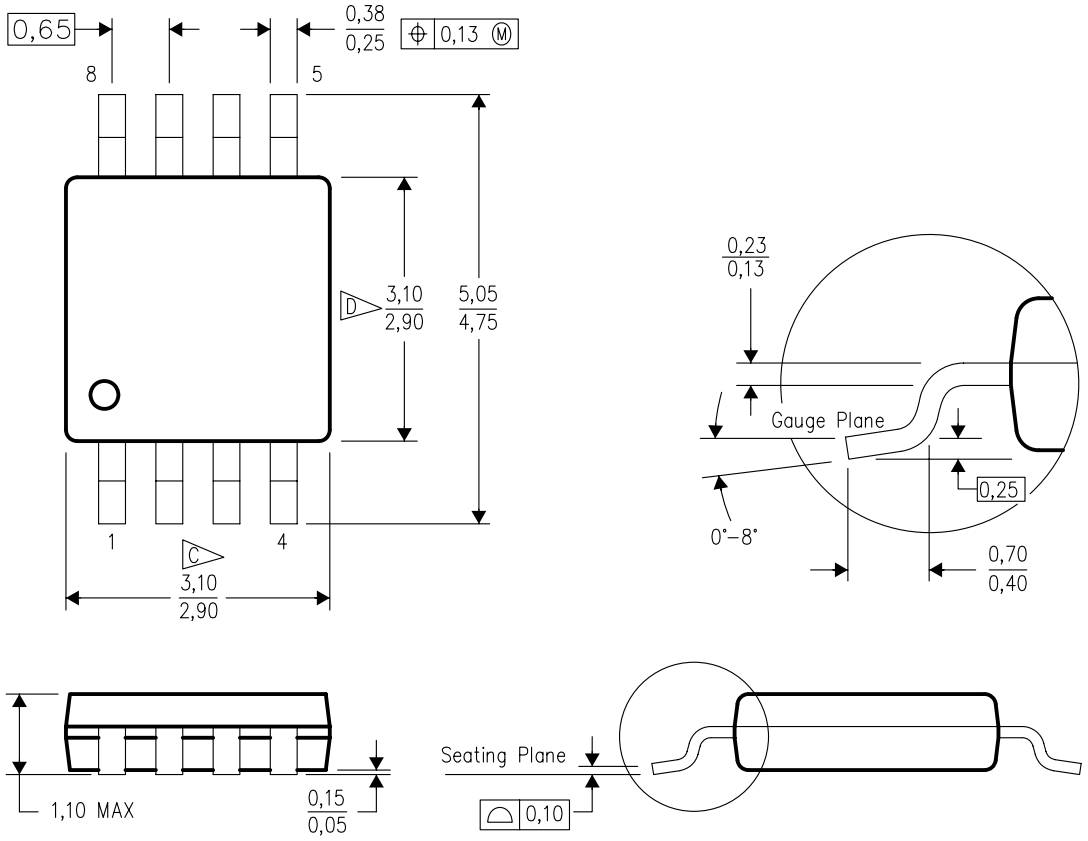
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4130CDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
THS4130IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4130IDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
THS4130IDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4131CDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4131CDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
THS4131CDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4131IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4131IDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
THS4131IDR	SOIC	D	8	2500	350.0	350.0	43.0

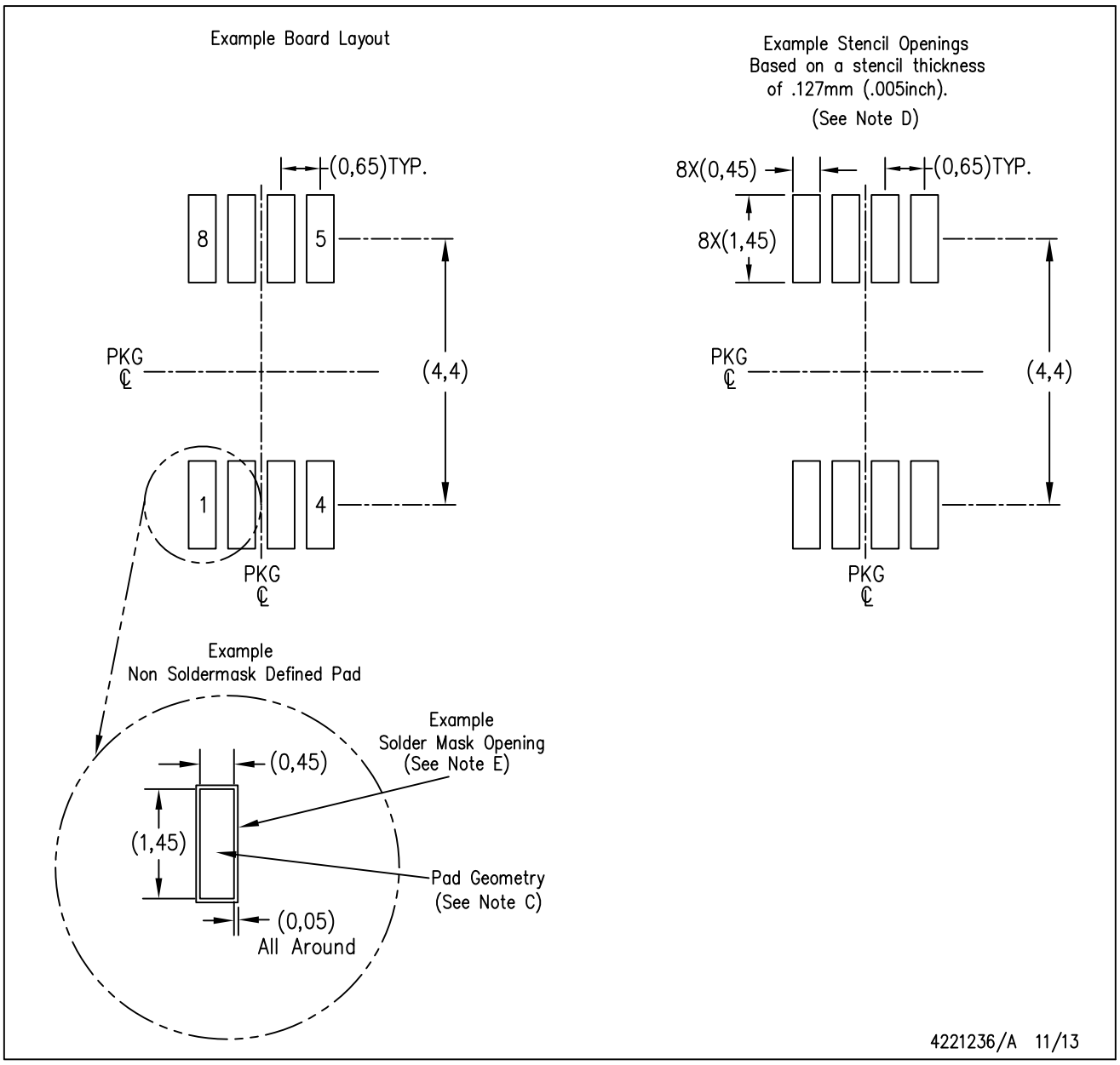
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

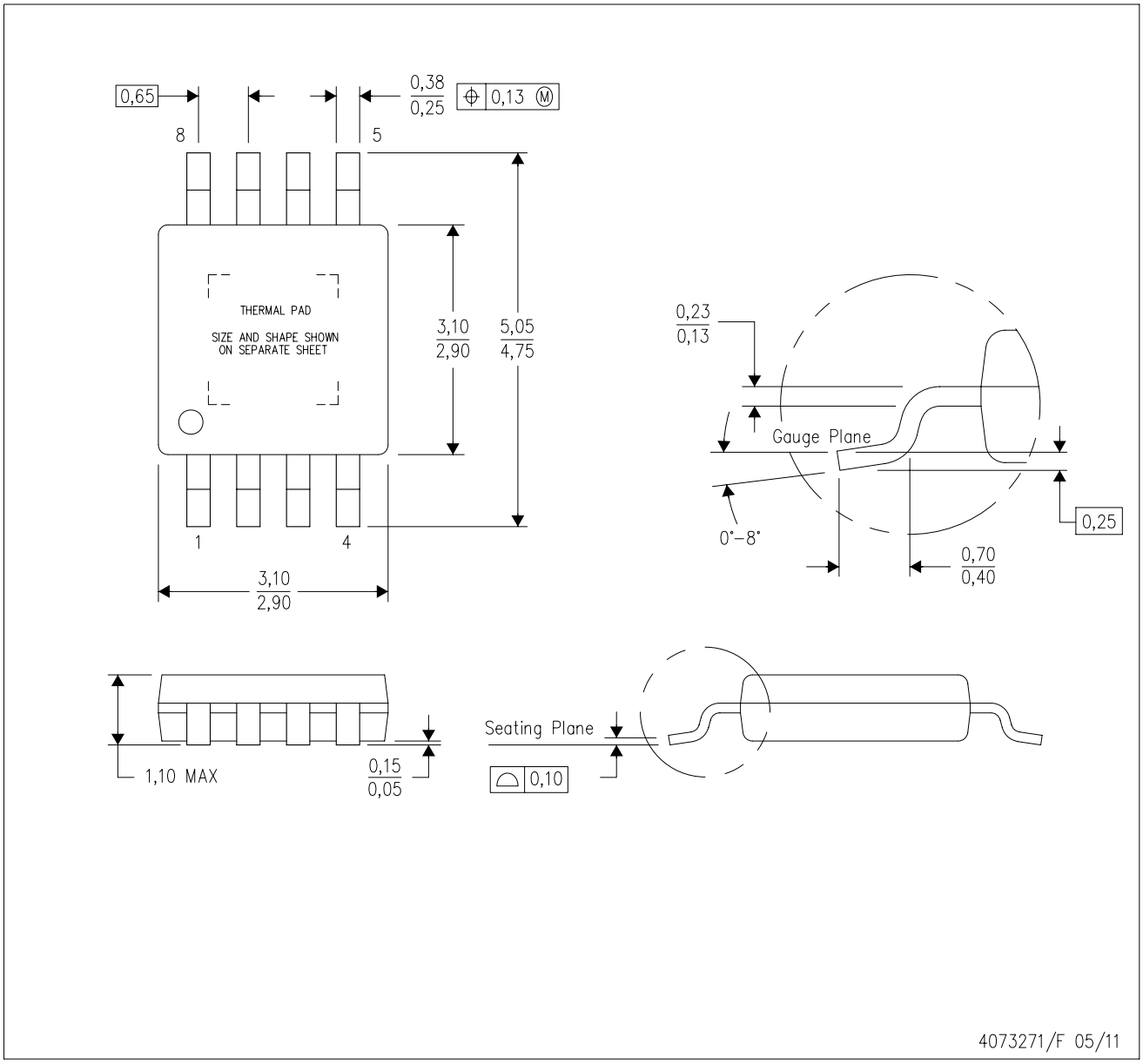
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

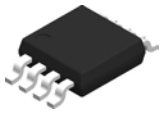


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

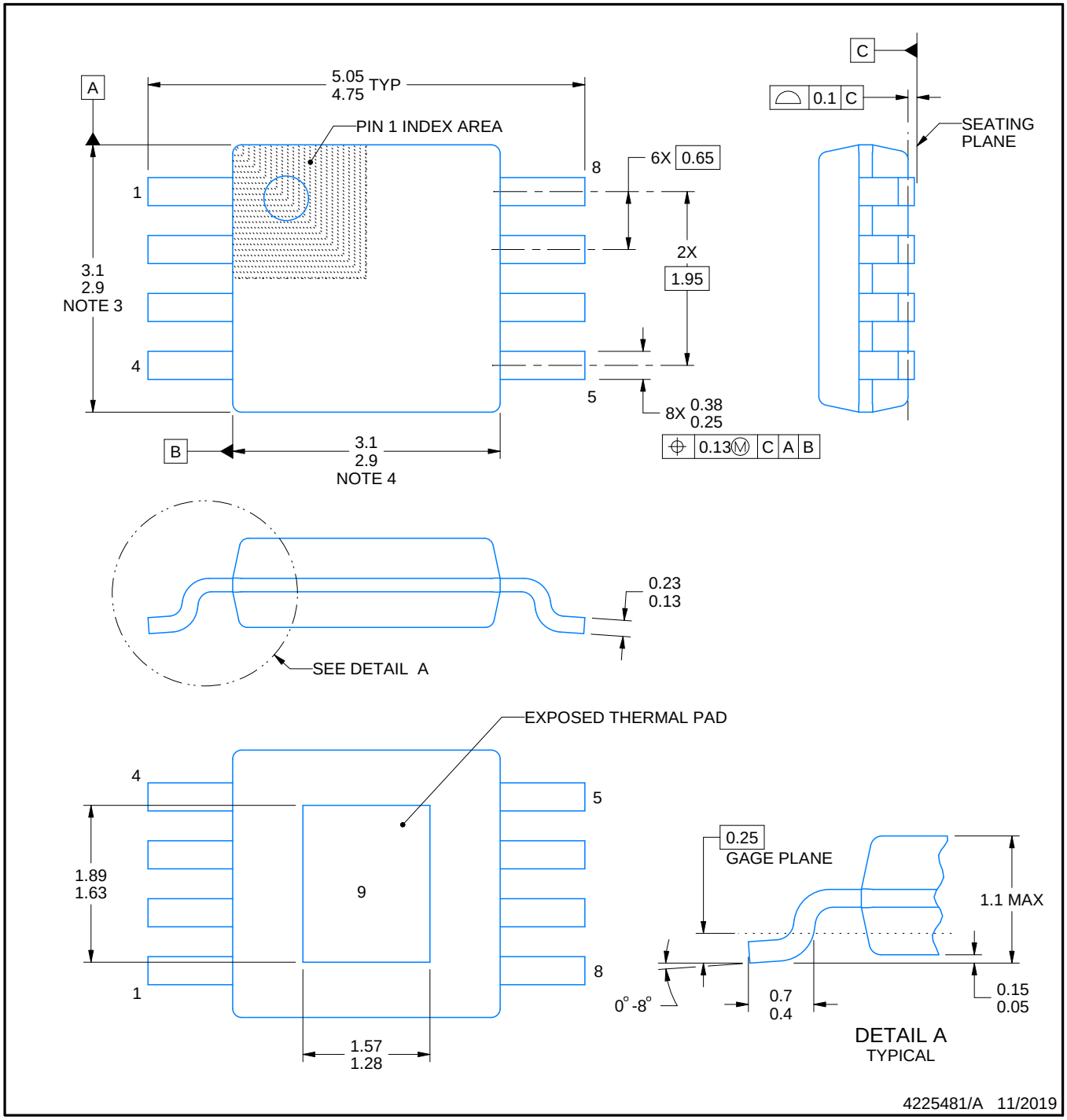
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

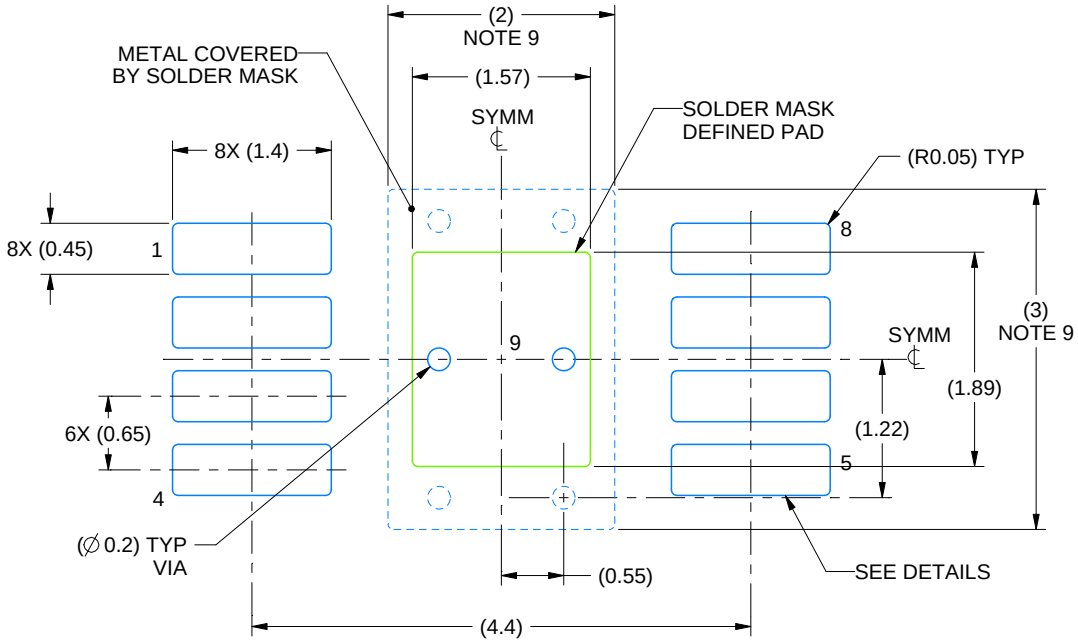
SMALL OUTLINE PACKAGE



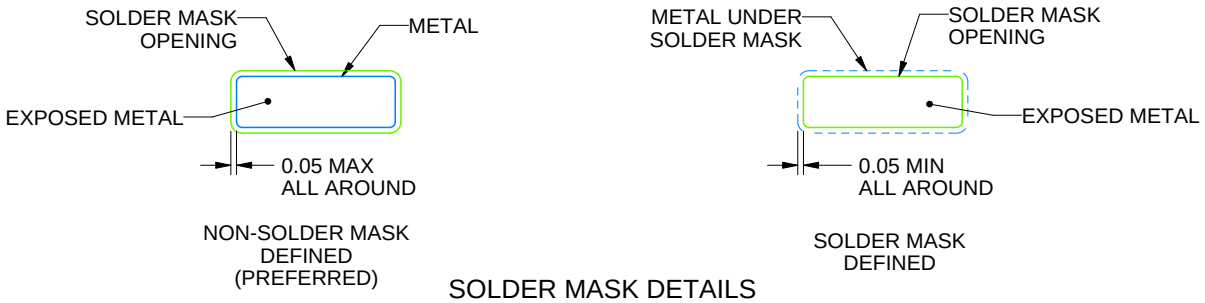
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

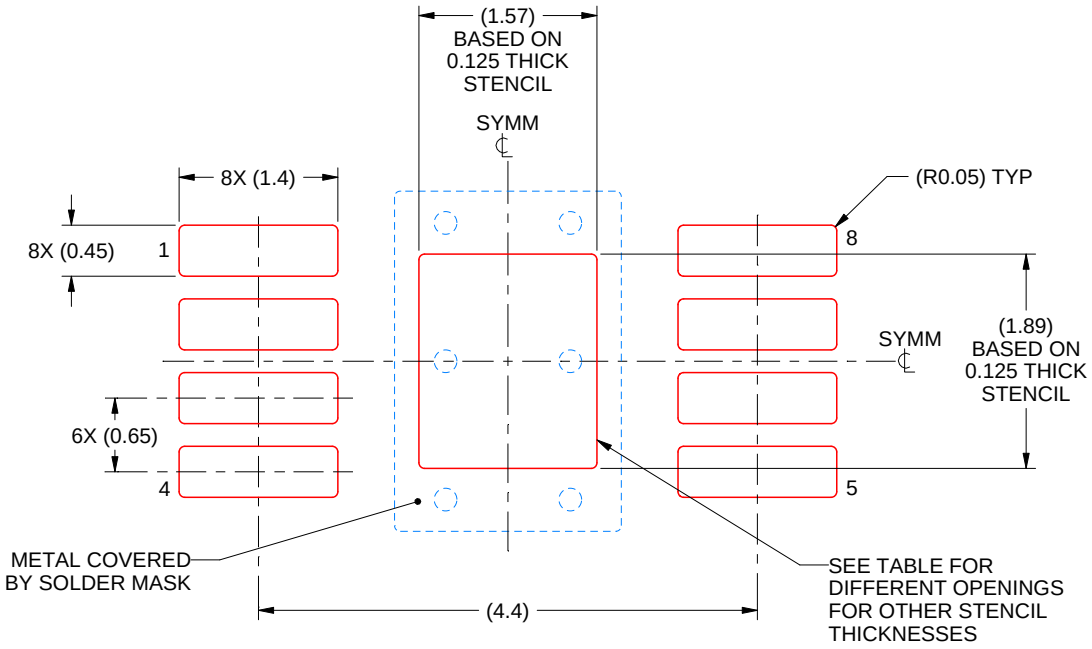


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

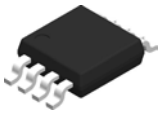
4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

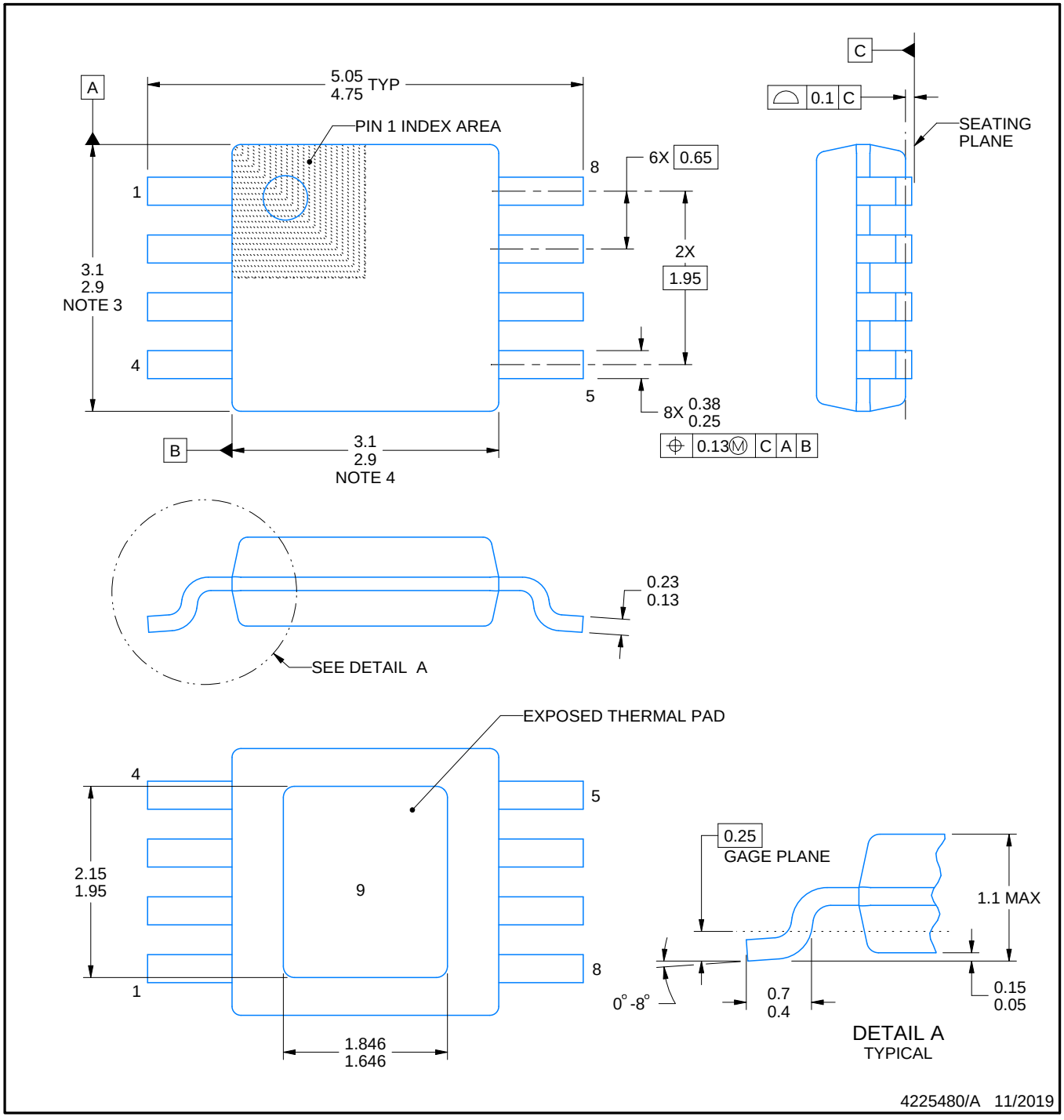
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

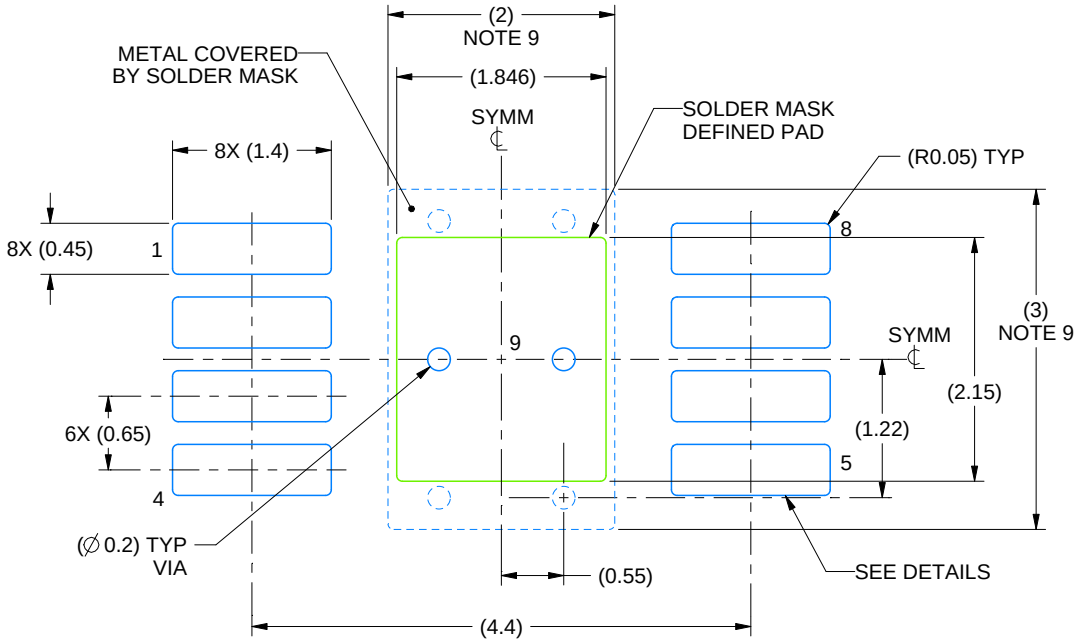
SMALL OUTLINE PACKAGE



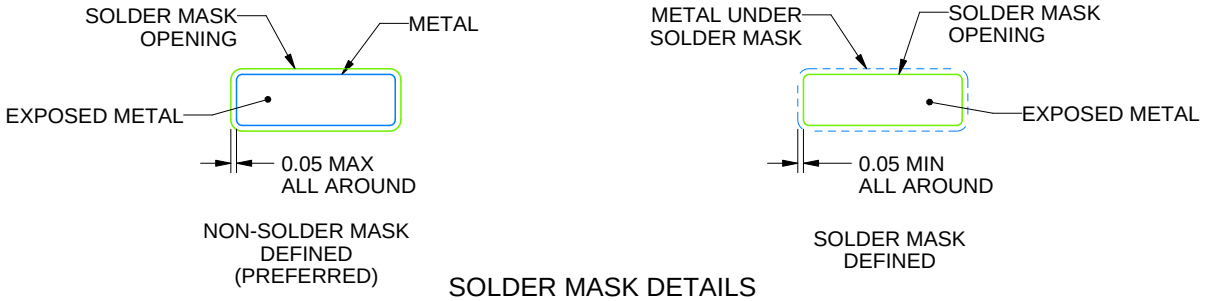
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

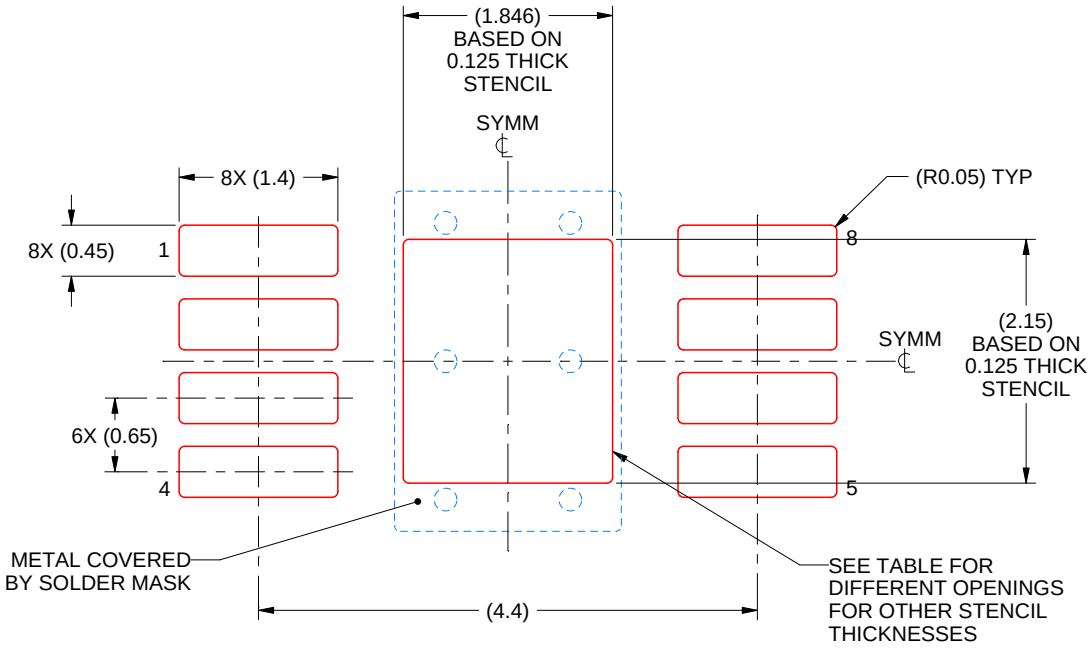


SOLDER MASK DETAILS

4225480/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



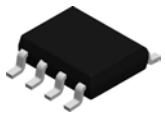
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.06 X 2.40
0.125	1.846 X 2.15 (SHOWN)
0.15	1.69 X 1.96
0.175	1.56 X 1.82

4225480/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

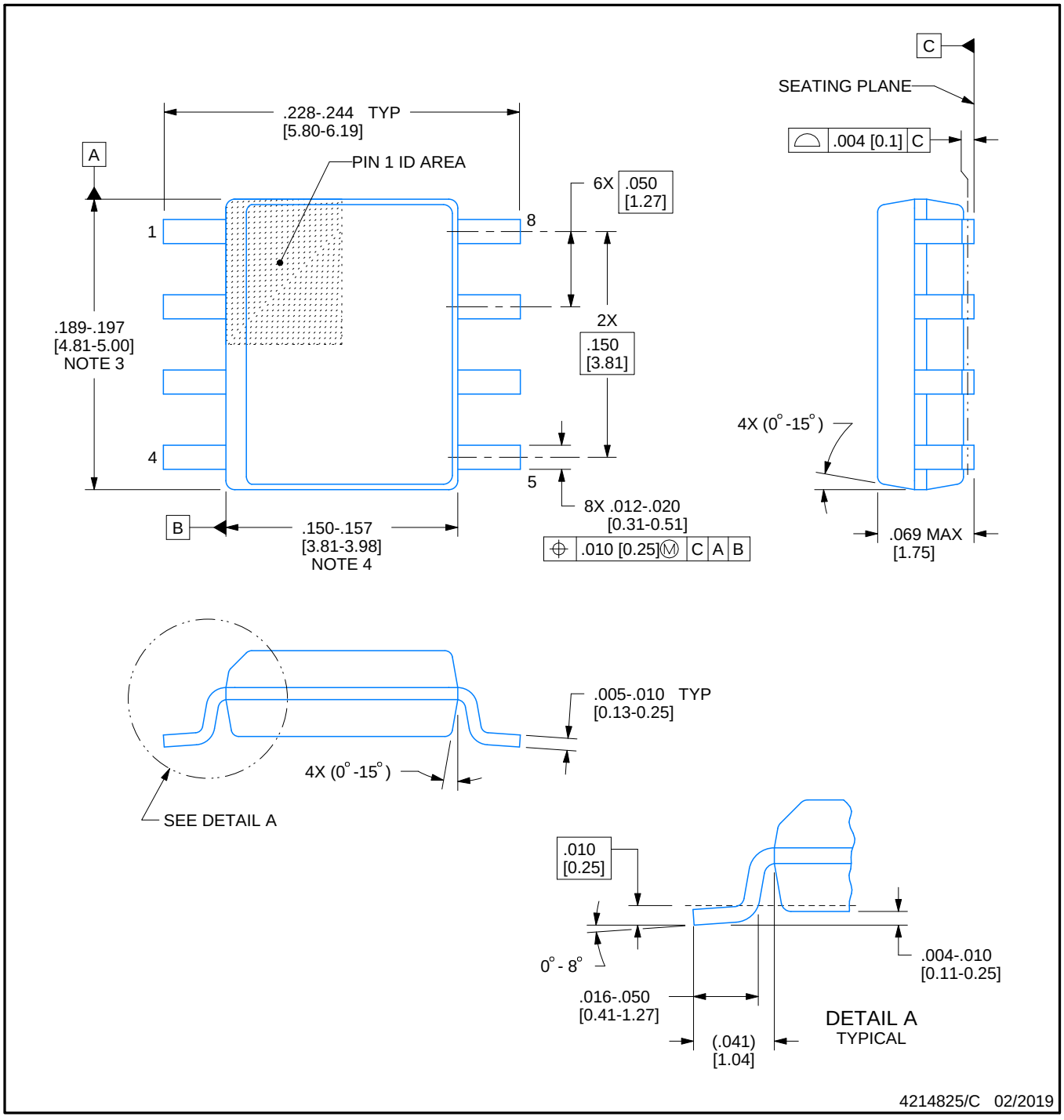


PACKAGE OUTLINE

D0008A

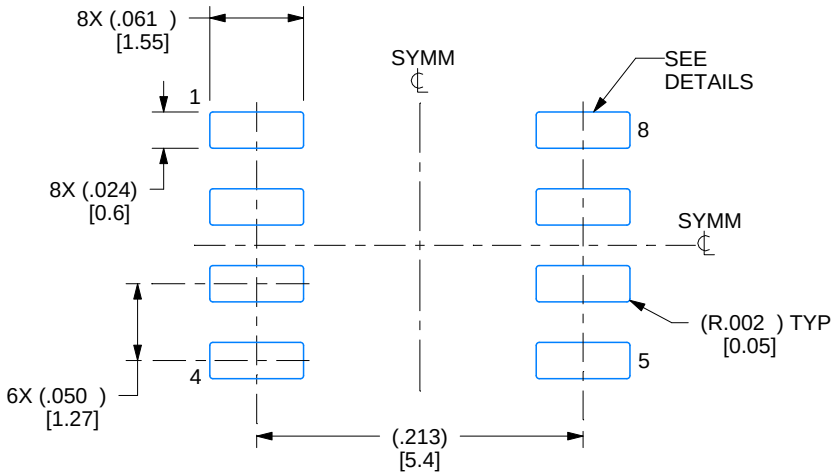
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

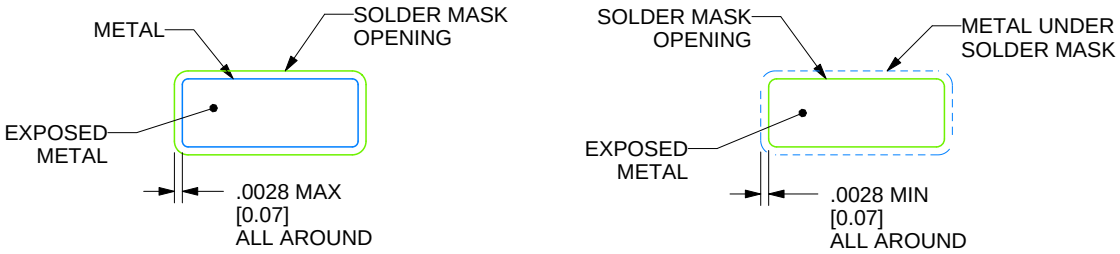


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

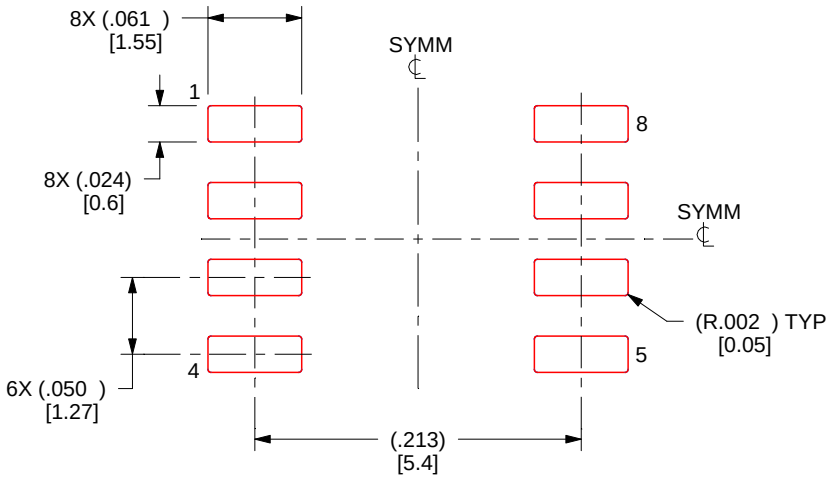
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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