STM32L5 Nucleo-144 board (MB1361)

Introduction

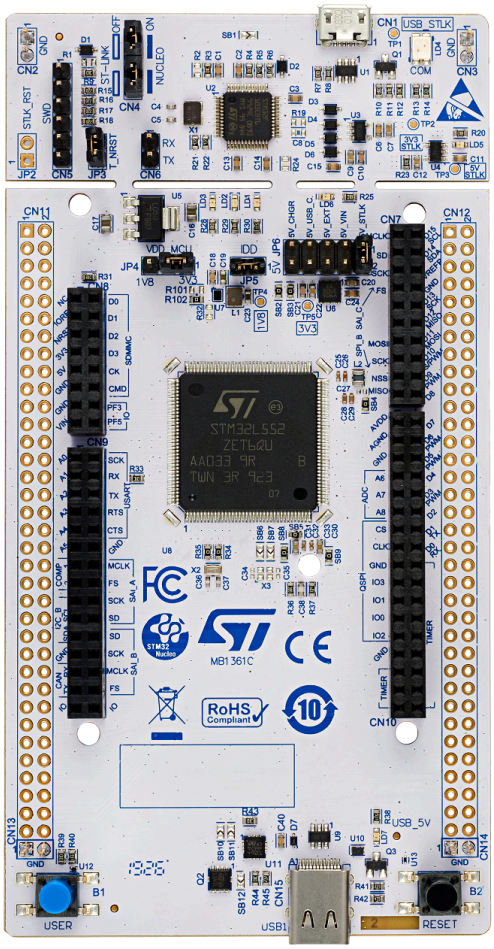
The STM32L5 Nucleo-144 board based on the MB1361 reference board (NUCLEO-L552ZE-Q) provides an affordable and flexible way for users to try out new concepts and build prototypes by choosing from the various combinations of performance and power consumption features, provided by the STM32L5 microcontroller.

The ST Zio connector, which extends the ARDUINO® Uno V3 connectivity, and the ST morpho headers provide easy expansion of the functionality of the STM32 Nucleo open development platform with a wide choice of specialized shields.

The STM32L5 Nucleo-144 board does not require any separate probe as it integrates the ST-LINK/V2-1 debugger/programmer.

The STM32L5 Nucleo-144 board comes with the STM32 comprehensive free software libraries and examples available with the STM32CubeL5 MCU Package.

Figure 1. STM32L5 Nucleo-144 board



Picture is not contractual.

1 Features

- STM32L552ZET6QU microcontroller (Arm® Cortex®-M33 at 110 MHz) in LQFP144 package, featuring 512 Kbytes of Flash memory and 256 Kbytes of SRAM
- Internal SMPS to generate V_{core} logic supply, identified by '-Q' suffixed boards(1)
- USB FS
- 3 user LEDs
- RESET and USER push-buttons
- 32.768 kHz crystal oscillator
- Board connectors:
  - USB Type-C® connector
  - SWD
  - ARDUINO® Uno V3 expansion connector
  - ST morpho expansion connector
- Flexible power-supply options: ST-LINK, USB V_{BUS} or external sources
- On-board ST-LINK/V2-1 debugger/programmer with USB re-enumeration capability: mass storage, Virtual COM port, and debug port
- Comprehensive free software libraries and examples available with the STM32CubeL5 MCU Package
- Support of a wide choice of Integrated Development Environments (IDEs) including IAR Embedded Workbench®, MDK-ARM, and STM32CubeIDE

1. *SMPS significantly reduces power consumption in Run mode, by generating V_{core} logic supply from an internal DC/DC converter.*

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Ordering information

To order the NUCLEO-L552ZE-Q Nucleo-144 board, refer to Table 1. Additional information is available from the datasheet and reference manual of the target STM32.

Table 1. Ordering information

Order code	Board reference	Target STM32
NUCLEO-L552ZE-Q	MB1361	STM32L552ZET6QU

2.1 Product marking

Evaluation tools marked as “ES” or “E” are not yet qualified and therefore not ready to be used as reference design or in production. Any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering sample tools as reference designs or in production.

“E” or “ES” marking examples of location:

- On the targeted STM32 that is soldered on the board (For an illustration of STM32 marking, refer to the STM32 datasheet “Package information” paragraph at the *www.st.com* website).
- Next to the evaluation tool ordering part number that is stuck or silk-screen printed on the board.

This board features a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a "U" marking option at the end of the standard part number and is not available for sales.

In order to use the same commercial stack in his application, a developer may need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

2.2 Products and codification

The meaning of the codification is explained in Table 2.

Table 2. Codification explanation

NUCLEO-XXYYZE-Q	Description	Example: NUCLEO-L552ZE-Q
XX	MCU series in STM32 Arm Cortex MCUs	STM32L5 Series
YY	MCU product line in the series	STM32L552
Z	STM32 package pin count	144 pins
E	STM32 Flash memory size:	512 Kbytes
-Q	STM32 has internal SMPS function	SMPS

The order code is mentioned on a sticker placed on the top or bottom side of the board.

3 Development environment

3.1 System requirements

- Windows® OS (7, 8 and 10), Linux® 64-bit, or macOS®
- USB Type-A or USB Type-C® to Micro-B cable

Note: macOS® is a trademark of Apple Inc. registered in the U.S. and other countries.
All other trademarks are the property of their respective owners.

3.2 Development toolchains

- IAR Systems - IAR Embedded Workbench®(1)
- Keil® - MDK-ARM(1)
- STMicroelectronics - STM32CubeIDE

1. *On Windows® only.*

3.3 Demonstration software

The demonstration software, included in the STM32Cube MCU Package corresponding to the on-board microcontroller, is preloaded in the STM32 Flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from *www.st.com*.

4 Conventions

Table 3 provides the conventions used for the ON and OFF settings in the present document.

Table 3. ON/OFF convention

Convention	Definition
Jumper JPx ON	Jumper fitted
Jumper JPx OFF	Jumper not fitted
Jumper JPx [1-2]	Jumper fitted between Pin 1 and Pin 2
Solder bridge SBx ON	SBx connections closed by 0 Ω resistor
Solder bridge SBx OFF	SBx connections left open
Resistor Rx ON	Resistor soldered
Resistor Rx OFF	Resistor not soldered

5 Quick start

The STM32L5 Nucleo-144 board is a low-cost and easy-to-use development kit, to quickly evaluate and start development with an STM32L5 Series microcontroller in an LFQFP144-pin package. Before installing and using the product, accept the Evaluation Product License Agreement from the www.st.com/epla webpage. For more information on the STM32L5 Nucleo-144 board and for demonstration software, visit the www.st.com/stm32nucleo webpage.

5.1 Getting started

Follow the sequence below to configure the STM32L5 Nucleo-144 board and launch the demonstration application (refer to Figure 4 for component location):

1. Check the jumper position on the board (refer to Default board configuration).
2. For the correct identification of the device interfaces from the host PC and before connecting the board, install the ST-LINK/V2-1 USB driver available on the *www.st.com* website.
3. Connect the STM32L5 Nucleo-144 board to a PC with a USB cable (Type-A to Micro-B) through the USB connector CN1 to power the board.
4. Then, the green LED LD6 (5V_PWR) lights up, LD4 (COM) and green LED LD1 blink.
5. Press USER button B1 (blue)
6. Observe how the blinking of the LEDs LD1, LD2, and LD3 changes, according to clicks on button B1.
7. Download the demonstration software and several software examples that help to use the STM32 Nucleo features. These are available on the *www.st.com* website.
8. Develop your application using the available examples.

5.2 Default board configuration

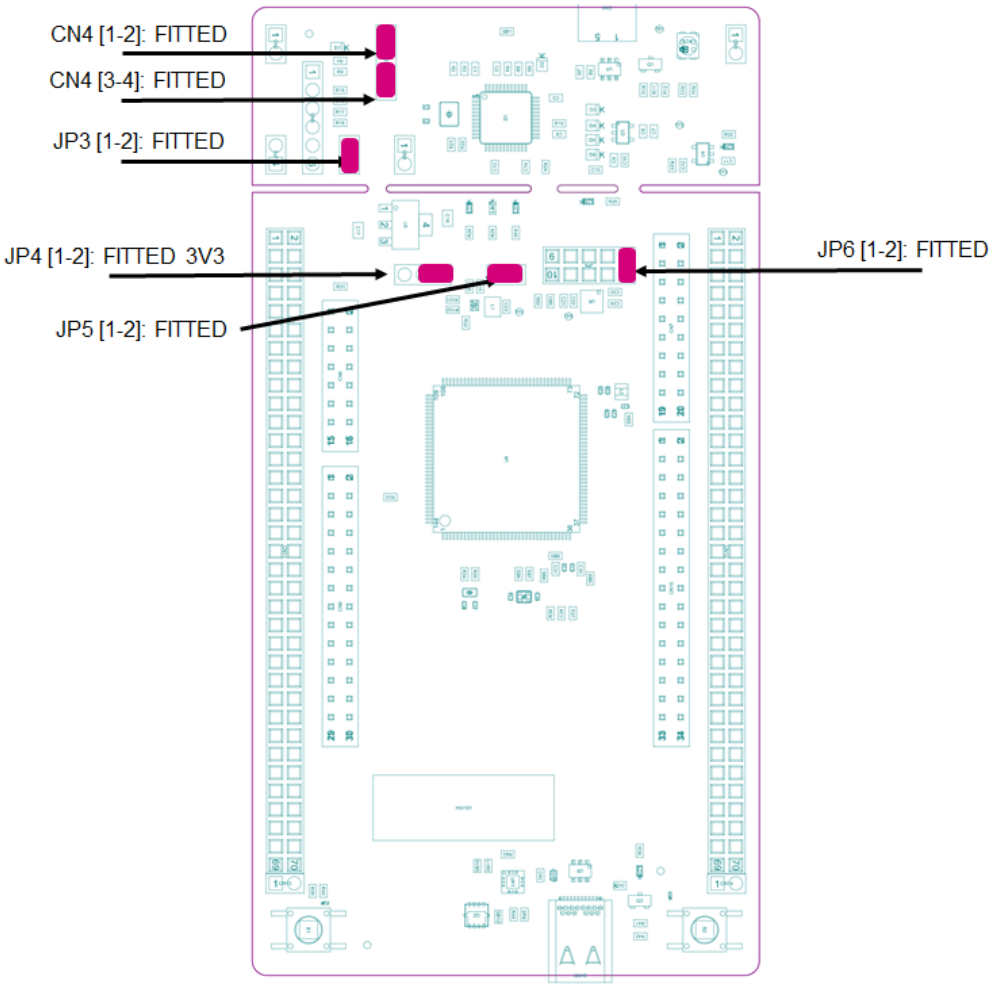
By default, the NUCLEO board is sent with VDD_MCU@3V3. It is possible to set the board for VDD_MCU@1V8. Before switching to 1V8, check that extension module and external shield connected to the NUCLEO board are 1V8 compatible.

The default jumper configuration and voltage setting are shown in Table 4.

Table 4. Default jumper configuration

Jumper	Definition	Default position	Comment
CN4	SWD interface	ON [1-2] ON [3-4]	On-board ST-LINK/V2-1 debugger
JP3	T_NRST	ON	RST connected between MCU target and debugger
JP4	VDD MCU	ON [1-2]	VDD MCU voltage selection 3V3
JP5	IDD measurement	ON	MCU VDD current measurement
JP6	5V power selection	ON [1-2]	5V from ST-LINK

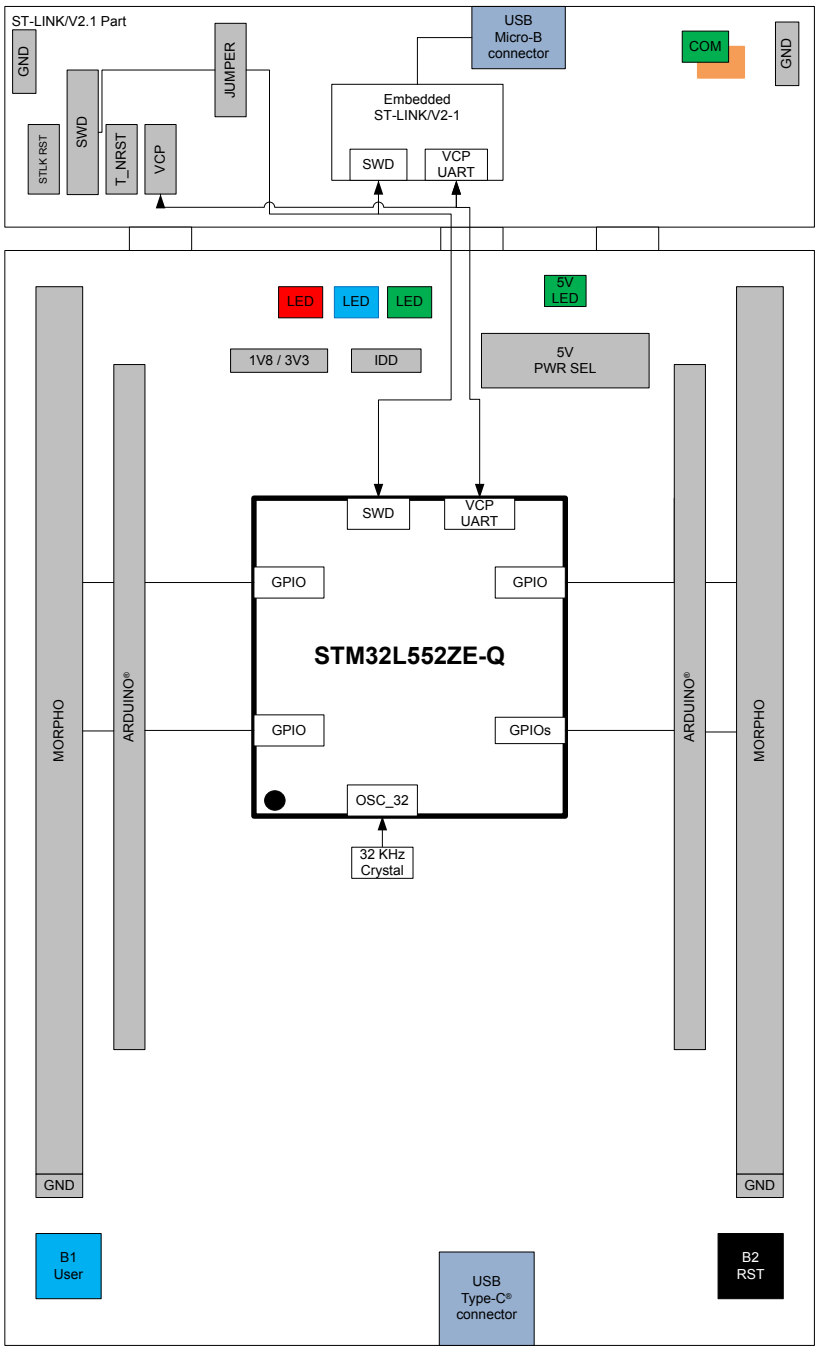
Figure 2. **Default board configuration**



6 Hardware layout and configuration

The STM32L5 Nucleo-144 board is designed around an STM32L552 microcontroller in an LFQFP 144-pin package. Figure 3 shows the connections between the STM32 and its peripherals (ST-LINK/V2-1, push-button, LEDs, USB, ST Zio connectors, and ST morpho headers). Figure 4 and Figure 5 show the location of these features on the STM32L5 Nucleo-144 board. The mechanical dimensions of the board are shown in Figure 6.

Figure 3. Hardware block diagram



6.1 STM32L5 Nucleo-144 board layout

Figure 4. **STM32L5 Nucleo-144 board top layout**

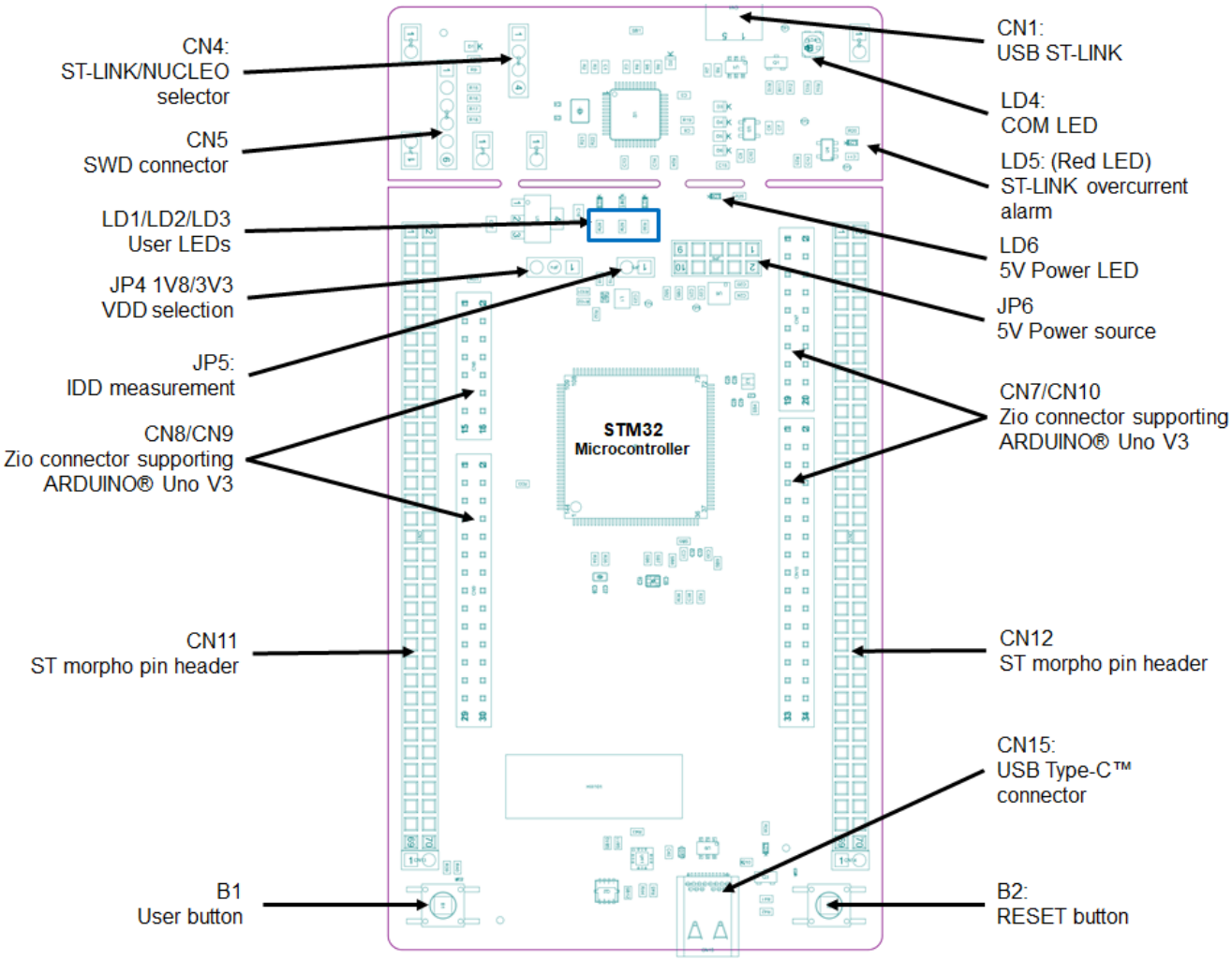
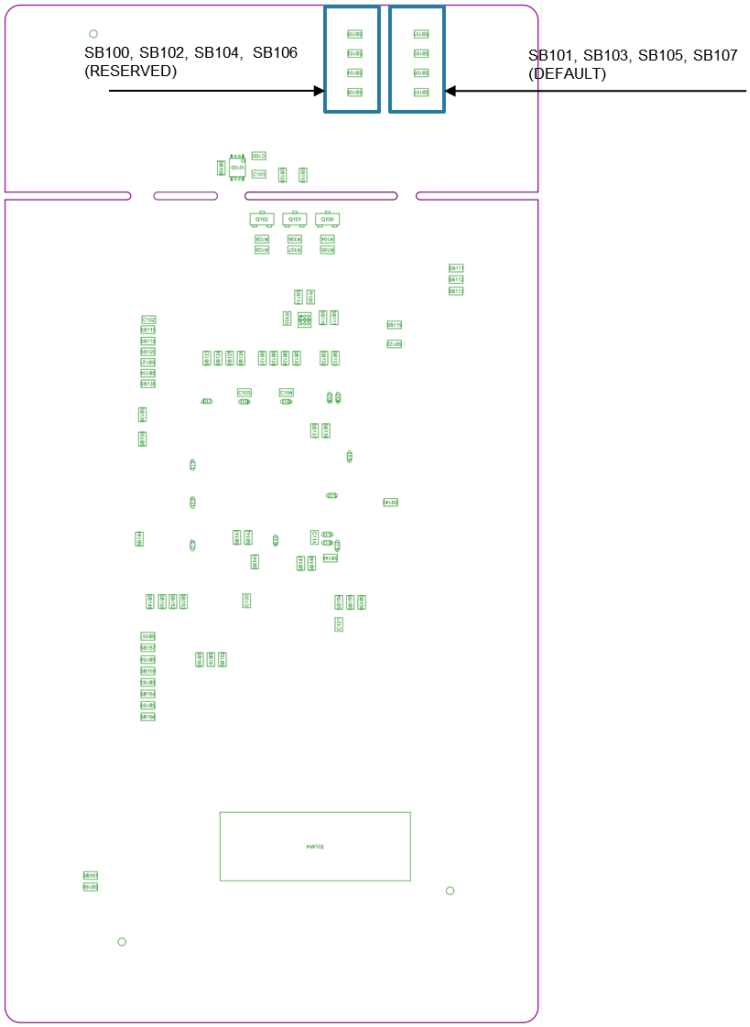
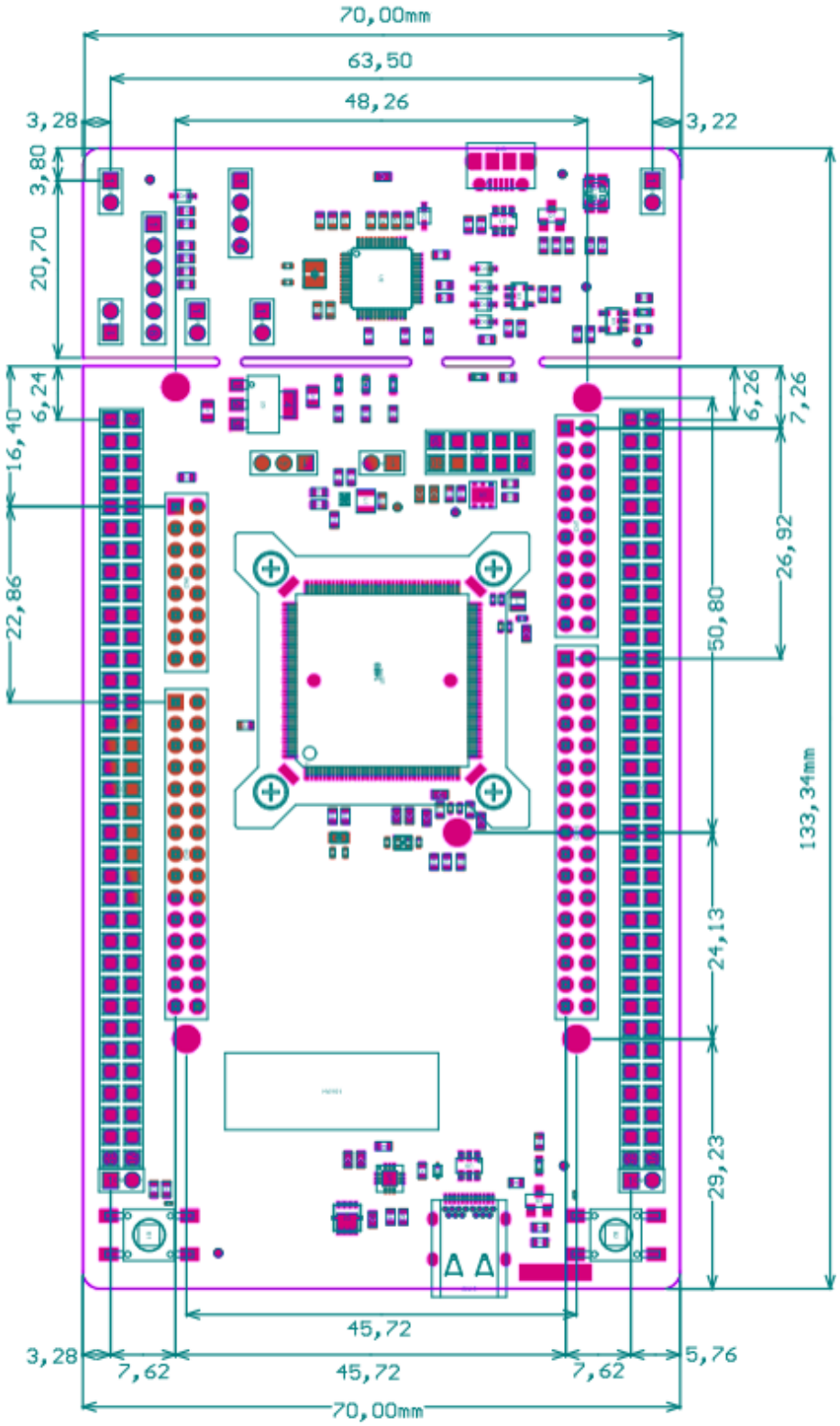


Figure 5. **STM32L5 Nucleo-144 board bottom layout**



6.2 Mechanical drawing

Figure 6. **STM32L5 Nucleo-144 board mechanical drawing (in millimeter)**



6.3 Embedded ST-LINK/V2-1

The ST-LINK/V2-1 programming and debugging tool is integrated into the STM32L5 Nucleo-144 board.

For detailed information about the debugging and programming features of ST-LINK/V2-1, refer to the *ST-LINK/V2 in-circuit debugger/programmer for STM8 and STM32* user manual (UM1075) and *Overview of ST-LINK derivatives* technical note (TN1235).

Features supported by the ST-LINK/V2-1:

- USB software re-enumeration
- Virtual COM port interface on USB
- Mass storage interface on USB
- USB power management request for more than 100 mA power on USB

Features not supported on ST-LINK/V2-1:

- SWIM interface
- Minimum supported application voltage limited to 3.0 V

Known limitation:

- Activating the readout protection on the STM32 target prevents the target application from running afterward. The target readout protection must be kept disabled on ST-LINK/V2-1 boards.

The embedded ST-LINK/V2-1 is directly connected to the SWD port of the target STM32.

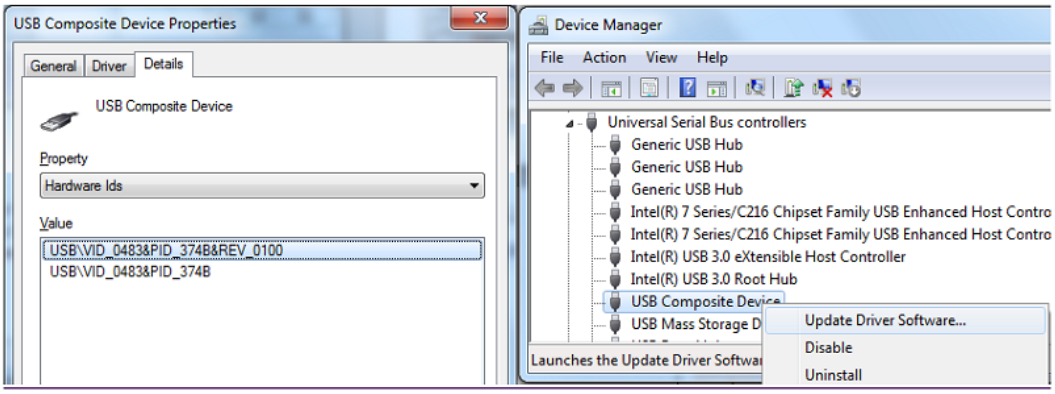
6.3.1 Drivers

The ST-LINK/V2-1 requires a dedicated USB driver, which, for Windows 7®, Windows 8® and Windows 10®, is found at *www.st.com*.

In case the STM32L5 Nucleo-144 board is connected to the PC before the driver is installed, some STM32L5 Nucleo-144 interfaces may be declared as *"Unknown"* in the PC device manager. In this case, the user must install the dedicated driver files, and update the driver of the connected device from the device manager as shown in Figure 7.

Note: Prefer using the USB Composite Device handle for a full recovery.

Figure 7. USB composite device



6.3.2 ST-LINK/V2-1 firmware upgrade

The ST-LINK/V2-1 embeds a firmware mechanism for the in-situ upgrade through the USB port. As the firmware may evolve during the lifetime of the ST-LINK/V2-1 product (for example new functionalities, bug fixes, support for new microcontroller families), it is recommended to visit the *www.st.com* website before starting to use the STM32L5 Nucleo-144 board and periodically, to stay up-to-date with the latest firmware version.

6.3.3 NUCLEO ST-LINK/V2-1 hardware configuration

The embedded ST-LINK/V2-1 can be used in two different ways according to the jumper states, refer to Table 5 for setting, depending on the configuration:

- Program/debug the MCU on-board
- Program/debug an MCU in an external application board using a cable connected to SWD connector

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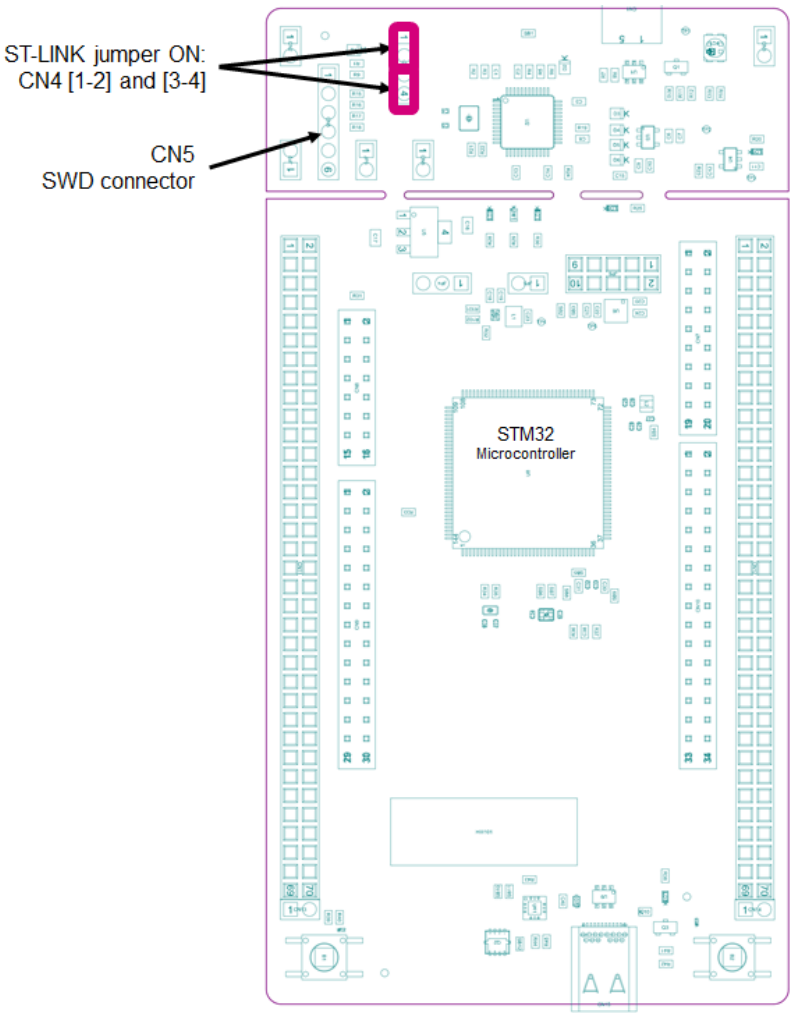
Table 5. ST-LINK jumper configuration

Jumper	Definition	Default position	Comment
CN4	T_SWCLK / T_SWDIO	ON [1-2] ON [3-4]	ST-LINK/V2-1 functions enabled for on-board programming
		OFF [1-2] OFF [3-4]	ST-LINK/V2-1 functions enabled from external connector (SWD supported)

6.3.3.1 *Using the ST-LINK/V2-1 to program and debug the STM32 on-board*

To program the STM32 on-board, plug in the two jumpers on the CN4 connector, as shown in Figure 8. In this case, do not use the CN5 SWD connector as that can disturb communication with the STM32 microcontroller of the Nucleo.

Figure 8. ST-LINK debugger: JP configuration for on-board MCU



6.3.3.2 *Using the ST-LINK/V2-1 to program and debug an external STM32 application*

It is easy to use the ST-LINK/V2-1 to program the STM32 on an external application.

Simply remove the two jumpers from CN4, as shown in Figure 9, and connect your application to the SWD debug connector (CN5) according to Table 6.

Note: JP3 T_NRST (target STM32 reset) must be open when CN5 pin 5 is used with an external application.

Figure 9. ST-LINK debugger: JP configuration for external MCU

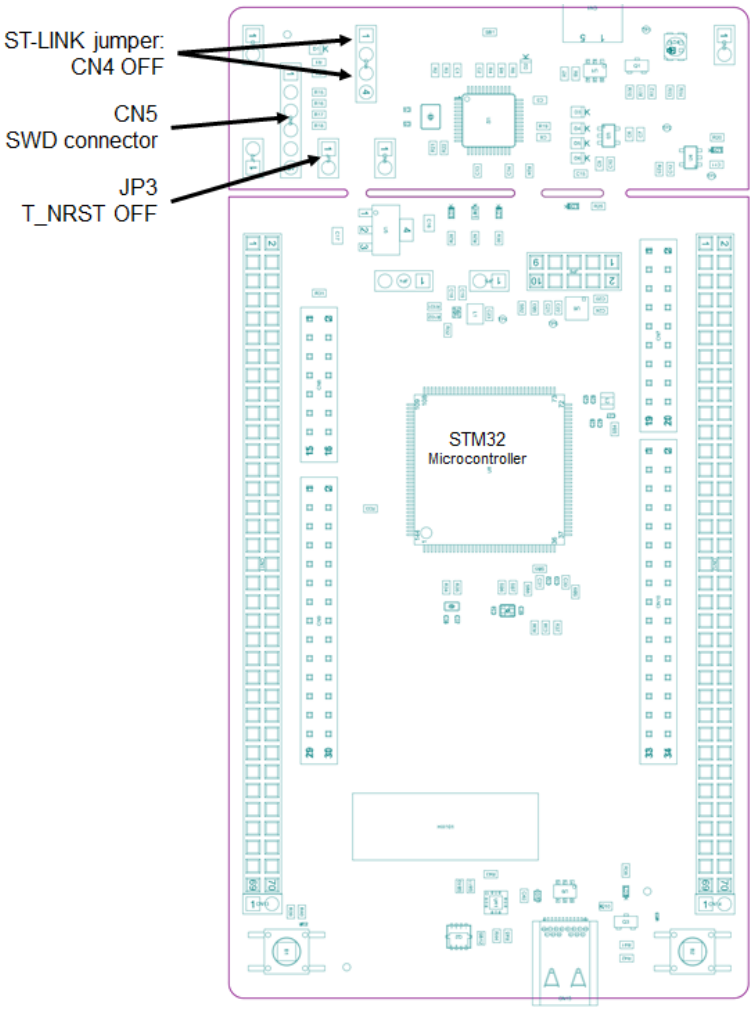


Table 6. Debug connector SWD: pinning

Connector	Pin number	Pin name	Signal name	STM32 pin	Function
SWD CN5	1	1	VDD_TARGET: AIN_1	-	VDD from application
	2	2	T_JTCK	-	SWD clock
	3	3	GND	-	Ground
	4	4	T_JTMS	-	SWD data I/O
	5	5	T_NRST	-	Reset of target MCU
	6	6	T_SWO	-	SWD out (optional)

6.4 Power supply

6.4.1 External power supply input

The Nucleo board is designed to be powered by several DC power supply. It is possible to configure the Nucleo board to use any of the following sources for the power supply:

- 5V_STLK from ST-LINK USB connector CN1
- VIN (7 to 12 V) from ARDUINO®-included Zio connector CN8 or ST morpho connector CN11
- 5V_EXT from ST morpho connector CN11
- 5V_USB_C from USB Type-C® connector CN15
- 5V_CHGR from ST-LINK USB connector CN1
- 3V3 on ARDUINO®-included Zio connector CN8 or ST morpho connector CN11

If VIN, 5V_EXT or 3V3 is used to power a Nucleo-144 board, this power source must comply with the standard EN-60950-1: 2006+A11/2009 and must be Safety Extra Low Voltage (SELV) with limited power capability.

The power supply capabilities are summarized in Table 7.

Table 7. Power sources capability

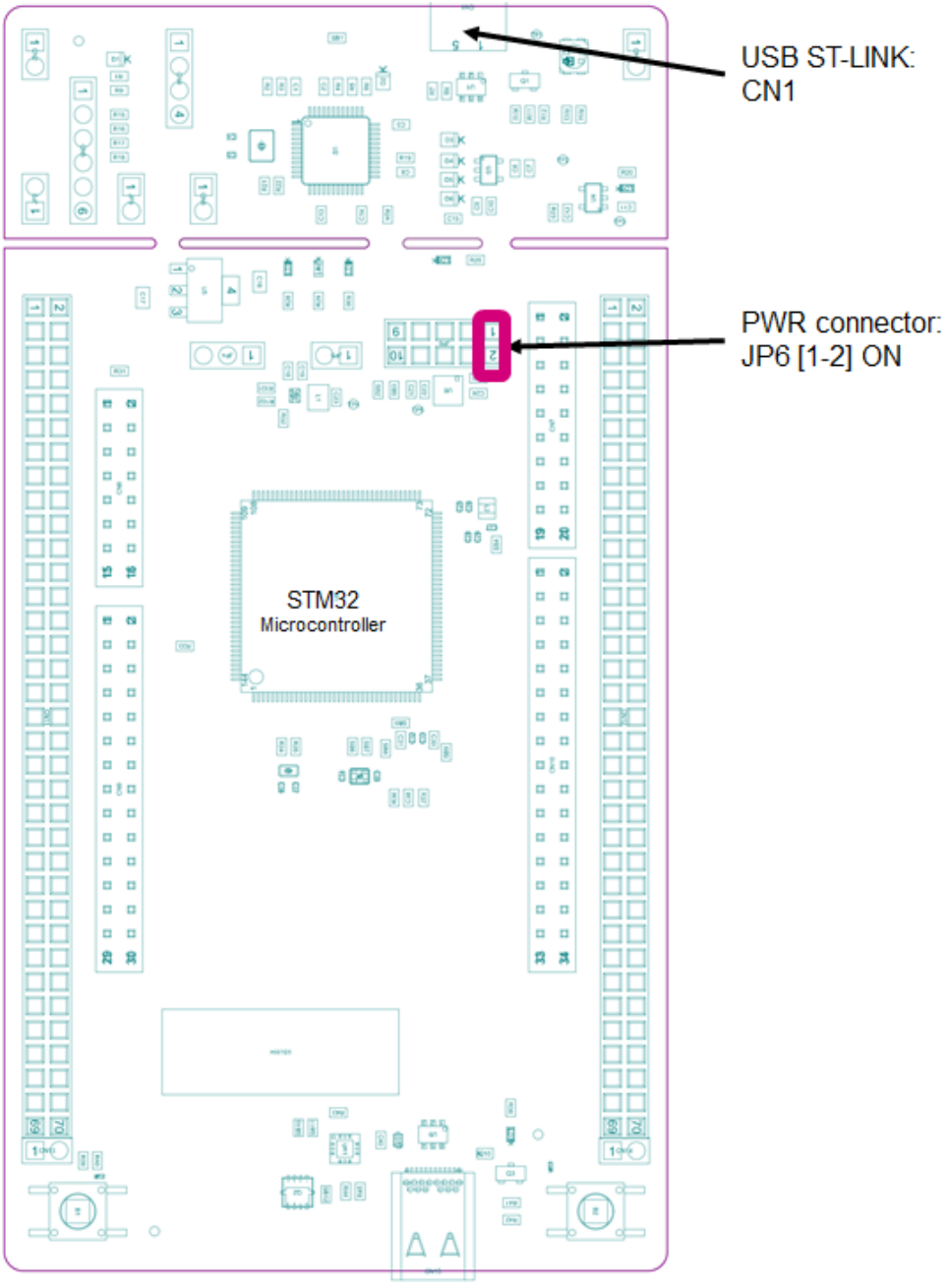
Input Power name	Connector pins	Voltage range	Max. current	Limitation
5V_STLK	CN1 pin 1 JP6 [1-2]	4.75 to 5.25 V	500 mA	Maximum current depending on the presence or absence of USB enumeration: • 100 mA without enumeration • 500 mA with enumeration OK
VIN / 5V_VIN	CN8 pin 15 CN11 pin 24 JP6 [3-4]	7 to 12 V	800 mA	From 7 to 12 V only and input current capability is linked to input voltage: • 800 mA input current when VIN = 7 V • 450 mA input current when 7 V < VIN < 9 V • 250 mA input current when 9 V < VIN < 12 V
5V_EXT	CN11 pin 6 JP6 [5-6]	4.75 to 5.25 V	500 mA	Maximum current depending on the power source
5V_USB_C	CN15 JP6 [7-8]	4.75 to 5.25 V	1 A	Maximum current depending on the USB host used to power the Nucleo
5V_CHGR	CN1 pin 1 JP6 [9-10]	4.75 to 5.25 V	500 mA	Maximum current depending on the USB wall charger used to power the Nucleo
3V3	CN8 pin 7 CN11 pin 16 JP5 pin 2	3.0 to 3.6 V		Used when the ST-LINK part of PCB is not used or removed. SB3 must be OFF to protect LDO U6.

5V_STLK is a DC power with limitation from ST-LINK USB connector (USB Type Micro-B connector of ST-LINK/V2-1). In this case, the JP6 jumper must be on pin [1-2] to select the 5V_STLK power source on the JP6 silkscreen. This is the default setting. If the USB enumeration succeeds, the 5V_STLK power is enabled, by asserting the PWR_ENn signal (from STM32F103CBT6). This pin is connected to a power switch TPS2041C, which powers the board. This power switch also features a 500 mA current limitation, to protect the PC in case of an onboard short-circuit.

Nucleo board with its shield can be powered from ST-LINK USB connector CN1, but only the ST-LINK circuit has the power before USB enumeration because the host PC only provides 100 mA to the board at that time. During the USB enumeration, the Nucleo board asks for the 500mA power to the host PC. If the host can provide the required power, the enumeration finishes by a `SetConfiguration` command and then, the power switch is switched ON, the Green LED LD6 is turned ON, thus Nucleo board and its shield on it can consume 500 mA current, but no more. If the host is not able to provide the requested current, the enumeration fails. Therefore, the power switch remains OFF and the MCU part including the extension board is not powered, and the green LED LD6 remains turned OFF. In this case, it is mandatory to use an external power supply.

5V_STLK configuration: Jumper JP6 [1-2] must be connected as shown in Figure 10.

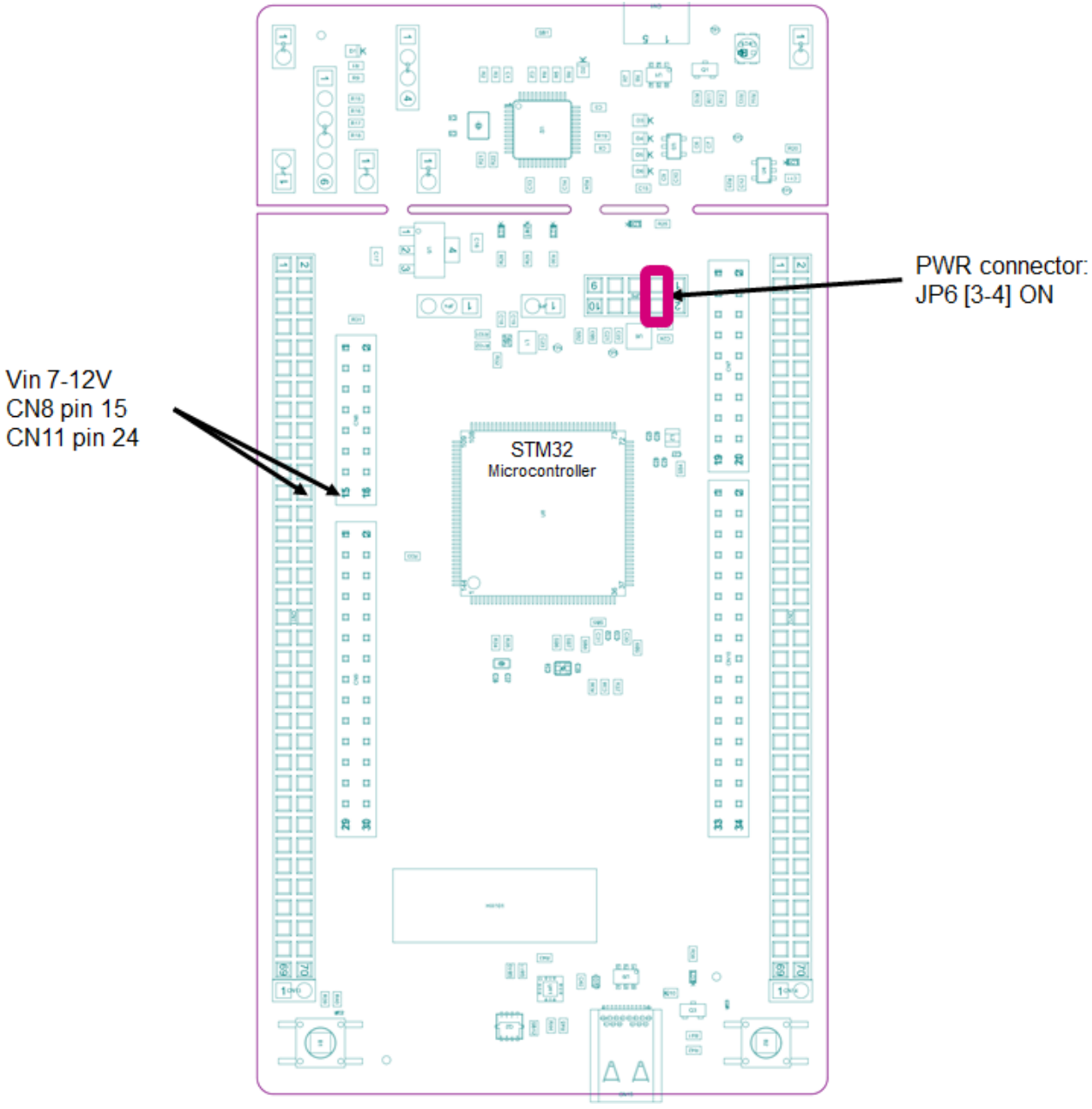
Figure 10. JP6 [1-2]: 5V_STLK Power source



VIN (5V_VIN) is the 7 to 12 V DC power from the ARDUINO®-included Zio connector, CN8 pin 15 named VIN on the connector silkscreen, or from the ST morpho connector CN11 pin 24. In this case, the JP6 jumper must be on pin [3-4] to select the 5V_VIN power source on the JP6 silkscreen. In that case, the DC power comes from the power supply through the ARDUINO® Uno V3 battery shield (compatible with Adafruit PowerBoost 500 shield).

5V_VIN configuration: Jumper JP6 [3-4] must be connected as shown in Figure 11.

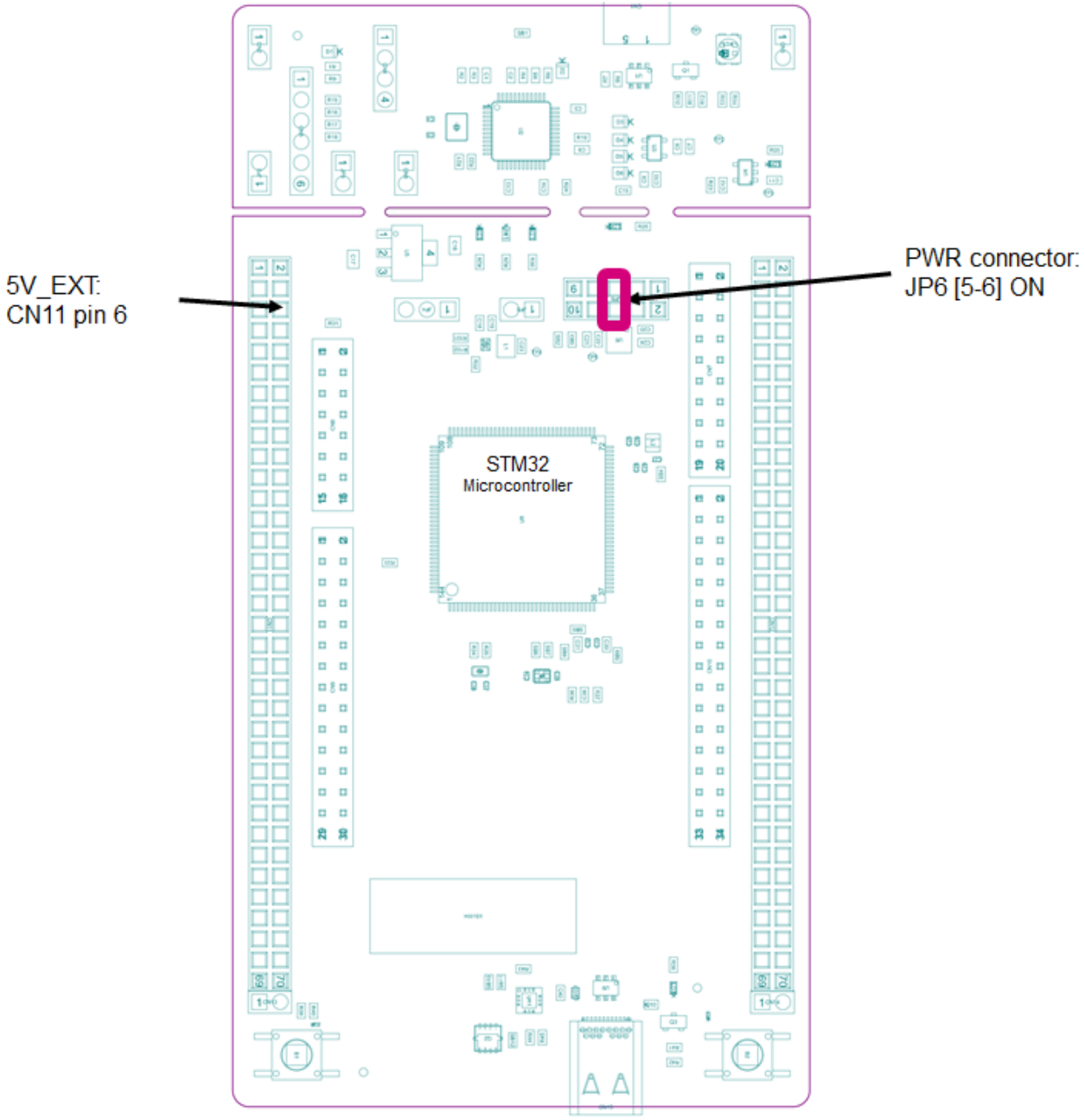
Figure 11. JP6 [3-4]: 5V_VIN Power source



5V_EXT is the DC power coming from external (5V DC power from ST morpho connector CN11 pin 6). In this case, the JP6 jumper must be on pin [5-6] to select the 5V_EXT power source on the JP6 silkscreen.

5V_EXT configuration: Jumper JP6 [5-6] must be connected as shown in Figure 12.

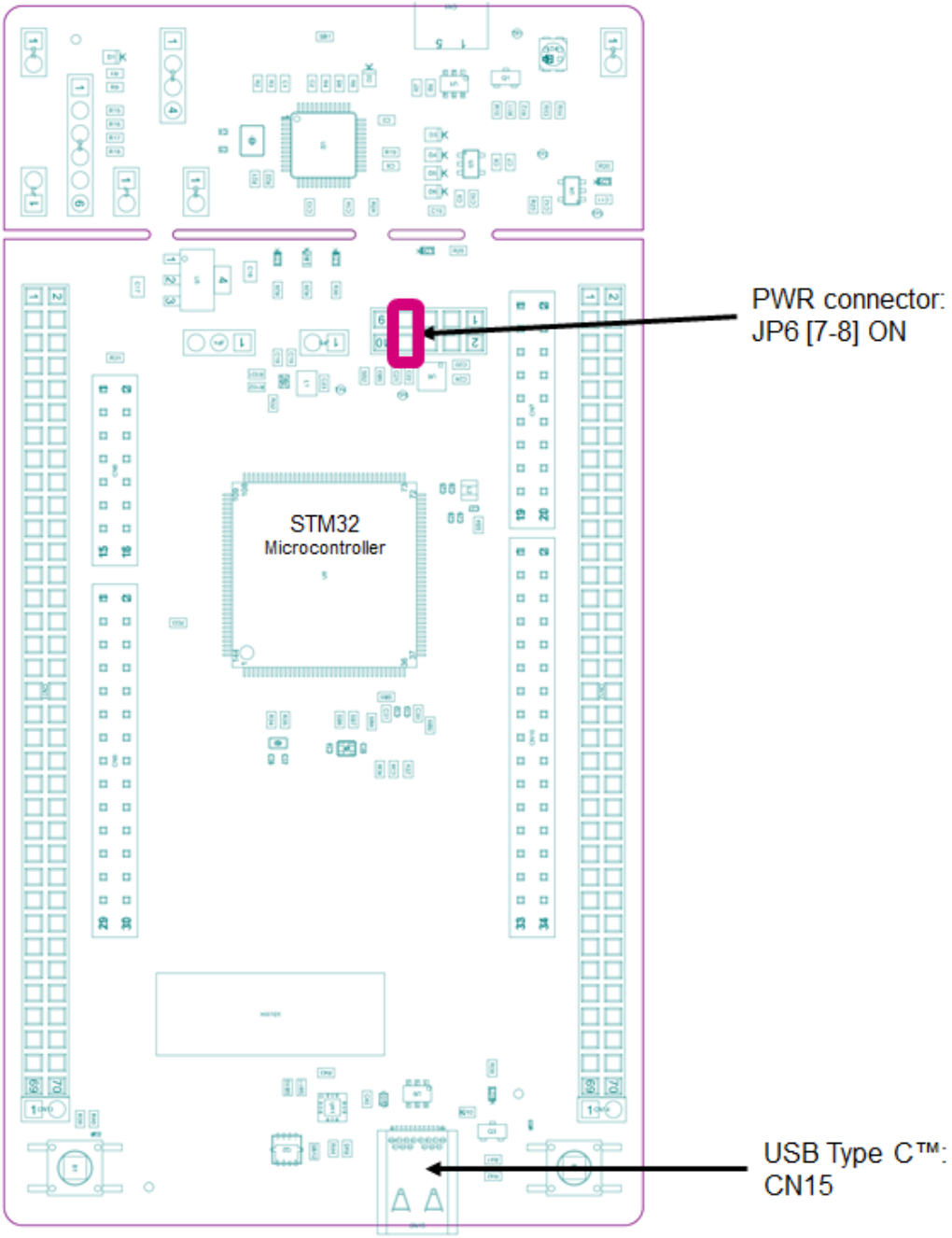
Figure 12. **JP6 [5-6]: 5V_EXT Power source**



5V_USB_C is the DC power supply connected to the user USB Type-C® (CN15). In this case, to select the 5V_USB_TYPE_C power source on the JP6 silkscreen, the jumper must be on pins [7-8].

5V_USB_C configuration: Jumper JP6 [7-8] must be connected as shown in Figure 13.

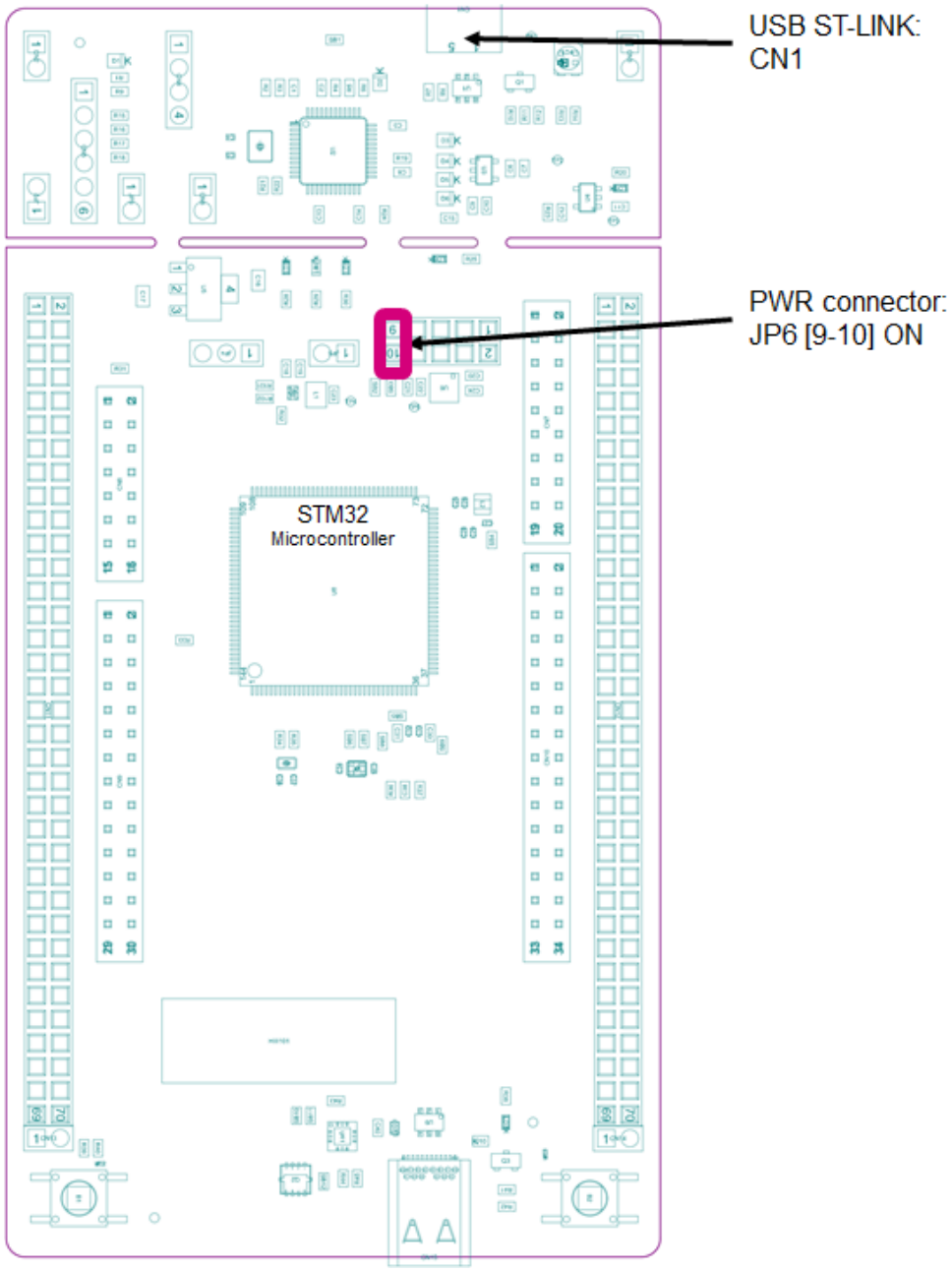
Figure 13. **JP6 [7-8]: 5V_USB_C Power source**



5V_CHGR is the DC power charger connected to USB ST-LINK (CN1). To select the 5V_USB_CHARGER power source on the JP6 silkscreen, the jumper must be on pins [9-10]. In this case, if an external USB charger powers the Nucleo board, then the debug is not available. If a computer is connected instead of the charger, the current limitation is no more effective. In this case, the computer can be damaged and it is recommended to select 5V_STLK mode.

5V_USB_CHG configuration: Jumper JP6 [9-10] must be connected as shown in Figure 14.

Figure 14. **JP6 [9-10]: 5V_CHGR Power source**



Note: With this JP6 configuration (5V_CHGR), the USB_PWR protection is bypassed. Never use this configuration with a computer connected instead of the charger, because as the USB_PWR protection is bypassed, the board eventually requests more than 500 mA and this can damage the computer.

Caution: A solder bridge (SB1) can be used to bypass the USB PWR protection switch. (This is not an ST recommended setting). SB1 can be set only in the case when the PC USB powers the board and maximum current consumption on 5V_STLINK **does not exceed 100 mA** (including an eventual extension board or ARDUINO® shield). In such condition, USB enumeration always succeeds, since no more than 100 mA is requested from the PC. Possible configurations of SB1 are summarized in Table 8.

Table 8. **SB1 bypass USB Power protection**

SB	Default position	Power supply	Limitation
SB1	OFF (not soldered)	USB PWR through CN1	500 mA limited by Power switch
	ON (soldered)		100 mA
	OFF (not soldered)	VIN or 5V_EXT PWR	No current limitation
	ON (soldered)		Forbidden configuration (1)

1. *SB1 must be removed when the board is powered by 5V_EXT (CN11 pin 6) or by VIN (CN8 pin 15 or CN11 pin 24).*

Warning:

In case maximum current consumption of the Nucleo and its extension boards exceeds 500 mA, it is recommended to power the Nucleo using an external power supply connected to 5V_EXT or VIN.

External 3V3 power supply input. In certain situations, it is interesting to use the 3V3 (CN8 pin 7, CN11 pin 16, or JP5 pin 2) directly as power input, for instance in case the 3V3 is provided by an extension board. When Nucleo is powered by 3V3, the ST-LINK is not powered thus programming and debug features are unavailable.

Two different configurations are possible to use 3V3 to power the board:

- When ST-LINK is removed (PCB cut)
- When 3V3 is provided from a shield, on CN8 pin 7, or CN11 pin 16. In this case, it is recommended to removed SB3 (U6 3V3 regulator output protection) to not inject voltage at the output of U6

With external 3V3 ST-LINK part is not supplied, so JP3 (T_NRST) must be removed.

6.4.2 Programing/debugging when the power supply is not from ST-LINK (5V_STLK)

VIN, 5V_EXT or 5V_USB_TYPE_C can be used as an external power supply, in case the current consumption of Nucleo and expansion boards exceeds the allowed current on USB. In such a condition, it is still possible to use USB for communication for programming or debugging only.

In this case, it is mandatory to power the board first using VIN, 5V_EXT or 5V_USB_TYPE_C then connect the USB cable to the PC. Proceeding this way the enumeration succeeds, thanks to the external power source.

The following power sequence procedure must be respected:

1. Connect the JP6 jumper according to the 5V selected external power source.
2. Make sure that SB1 is removed.
3. Connect the external power source according to JP6.
4. Power ON the external power supply.
5. Check that 5V GREEN LED LD6 is turned ON.
6. Connect the PC to the CN1 USB connector.

If this sequence is not respected, the board may be powered by V_{BUS} first from ST-LINK, and the following risk may be encountered:

- If more than 500 mA current is needed by the board, the PC may be damaged or current can be limited by PC. Therefore, the board is not powered correctly.
- 500 mA is requested at enumeration (since SB1 must be OFF) so there is a risk that request is rejected and enumeration does not succeed if PC cannot provide such current. Consequently, the board is not powered (LED LD6 remains OFF).

6.4.3 External power supply output

- 5V: When the Nucleo board is powered by USB, VIN or 5V_EXT, this 5V, present on CN8 pin 9 or CN11 pin 18, can be used as an output power supply for an ARDUINO® shield or an extension board. In this case, the maximum current of the power source specified in Table 7 above needs to be respected.
- 3V3: The internal 3V3, on CN8 pin 7 or CN11 pin 16, can be used also as a power supply output. The current is limited by the maximum current capability of the regulator U6 (LD39050PUR33 from STMicroelectronics: 500 mA max concerning Nucleo board consumption + shield consumption).

6.4.4 Internal power supply

NUCLEO board are designed to support two specific voltage configuration:

- 3V3 MCU configuration to reach NUCLEO low-power mode
- 1V8 MCU configuration to demonstrate MCU low-voltage capability

6.4.4.1 *3V3*

Regardless of the 5V power source, an LDO is used to switch from 5V to the default power source of the VDD_MCU: 3V3. The maximum current capability of this source is 500 mA. To select the 3V3 voltage for the VDD_MCU, connect the Jumper JP4 to pin [1-2].

6.4.4.2 *1V8*

An external SMPS is used for the MCU to work at 1V8. This helps to reduce max power consumption. The external SMPS capability is 400 mA. This power supply must be reserved only for the VDD_MCU. To select the 1V8 voltage for the VDD_MCU, connect the Jumper JP4 to pin [2-3].

6.4.4.3 *Internal V_{core} SMPS Power supply*

Power figures in Run Mode are significantly improved, by generating V_{core} logic supply from the internal DC/DC converter (this function is only available on '-Q' suffixed boards).

For all general information concerning Design recommendations for STM32L5 with INTERNAL SMPS, and design guide for ultra-low-power applications with performance, refer to L5 Hardware Getting started (AN5211) at the *www.st.com* website.

6.5 LEDs

User LD1

A green user LED is connected to the STM32 I/O PA5 (SB120 ON and SB118 OFF, optional configuration corresponding to the ST Zio D13) or PC7 (SB120 OFF and SB118 ON, default configuration). A transistor is used to drive the LED when the I/O voltage is 1V8.

User LD2

A blue user LED is connected to PB7. A transistor is used to drive the LED when the I/O voltage is 1V8.

User LD3

A red user LED is connected to PA9. A transistor is used to drive the LED when the I/O voltage is 1V8.

These user LEDs are ON when the I/O is HIGH value, and are OFF when the I/O is LOW.

LD4 COM

The tricolor LED LD4 (green, orange, and red) provides information about ST-LINK communication status. The LD4 default color is red. LD4 turns to green to indicate that the communication is in progress between the PC and the ST-LINK/V2-1, with the following setup:

- Slow blinking red/off: at power-on before USB initialization
- Fast blinking red/off: after the first correct communication between PC and ST-LINK/V2-1 (enumeration)
- Red LED ON: when the initialization between the PC and ST-LINK/V2-1 is complete
- Green LED ON: after a successful target communication initialization
- Blinking red/green: during communication with the target
- Green ON: communication finished and successful
- Orange ON: communication failure

LD5 ST-LINK USB power switch fault

LD5 indicates that the board power consumption on USB exceeds 500 mA. Consequently, the user must power the board with an external power supply.

LD6 PWR

The green LED indicates that the STM32 part is powered by a 5V source, and this source is available on CN8 pin 9 and CN11 pin 18.

LD7 USB Type-C®

This green LED is driven by the presence of the 5V_USB_TYPEC. Refer to Section 6.13.1 USB FS device for more details.

6.6 Push-buttons

Two buttons are available on the Nucleo board.

B1 USER

The blue button for User and Wake-Up function is connected to the I/O PC13 supported TAMPER function (default) or to I/O PA0 supported Wakeup function (optional) of the STM32 Microcontroller. When the button is pressed the logic state is “1”, otherwise the logic state is “0”.

B2 RESET

The black button connected to NRST is used to reset the STM32 microcontroller. When the button is pressed the logic state is “0”, otherwise the logic state is “1”.

The blue and black plastic hats placed on these push-buttons can be removed if necessary when a shield or an application board is plugged on top of Nucleo. This avoids pressure on the buttons and consequently a possible permanent target MCU reset.

6.7 IDD measurement

The JP5 jumper, labeled **IDD**, allows the consumption of the STM32 microcontroller to be measured by removing the jumper and connecting an ammeter.

- Jumper ON: STM32 Microcontroller is powered (default).
- Jumper OFF: an ammeter or an external 3V3 power source must be connected to power and to measure the STM32 microcontroller’s consumption.

The IDD jumper only performs the current measurement for 3V3 voltage. To measure the STM32 microcontroller consumption in 3V3 and 1V8 modes, it is preferable to use the JP4 jumper as IDD.

6.8 JP4 VDD_MCU voltage selection 1V8 or 3V3

The JP4 jumper selects the VDD_MCU voltage. It can be used as an IDD current measurement point for 3V3 and 1V8 voltages.

- Set JP4 to [1-2] to set VDD_MCU to 3V3 (IDD can be measured by ammeter between pin 1 and 2)
- Set JP4 to [2-3] to set VDD_MCU to 1V8 (IDD can be measured by ammeter between pin 3 and 2)

Consumption on this jumper includes MCU pin connected to VDD and the U100 Level shifter supply pin for 1V8 compatibility. Level Shifter consumption is negligible according to correct SWD settings and according to the correct setting of the I/O, to avoid an I/O floating level.

To correctly supply the MCU, it is mandatory to configure SBs as shown in Table 9. The role of these SBs is to provide input to dedicated MCU part for current measurement and probing purposes.

Table 9. MCU Power supplies

SB configuration	MCU Power supply
JP4 [1-2] / JP4 [2-3]	Jumper selection for VDD_MCU 3V3 or 1V8
SB4 ON	SB for VDDSMPS input voltage
SB5 ON	SB for VREFP input voltage

SB configuration	MCU Power supply
SB132 ON	SB for VDD_USB input voltage
SB133 ON	SB for VDDIO2 PG [2-15] input voltage
SB146 ON	SB for VBAT input voltage
SB149 OFF / SB150 ON	SB for VDDA input voltage
	For more detail about VDDA/VREFP power supply, refer to MCU datasheet

Warning:
The power sequence is not respected when using 1V8 VDD. Refer to the Getting started with STM32L5 Series hardware development application note AN5211, and STM32L5xx products datasheets for power sequencing.

6.9 OSC clock sources

Three clock sources are described below.

- LSE is the 32.768 kHz crystal for the STM32 embedded RTC.
- MCO is the 8 MHz clock from ST-LINK MCU for the STM32 microcontroller.
- HSE is the 16 MHz oscillator for the STM32 microcontroller. This clock is not implemented in a basic configuration.

6.9.1 LSE: OSC 32 KHz clock supply

There are three ways to configure the pins corresponding to the low-speed clock (LSE):

LSE on-board oscillator X2 crystal (Default configuration)

Refer to the AN2867 for oscillator design guide for STM32 microcontrollers, with the following characteristics: 32.768 kHz, 6 pF, 20 ppm. It is recommended to use NX2012SA- 32.768KHZ-EXS00A-MU00527 manufactured by NDK. The following configuration is needed:

- R34 and R35 ON
- SB147 and SB148 OFF

Oscillator from external to PC14 input

From external oscillator through the pin 25 of the CN11 connector. The following configuration is needed:

- R34 and R35 OFF
- SB147 and SB148 ON

LSE not used

PC14 and PC15 are used as GPIOs instead of low-speed clocks. The following configuration is needed:

- R34 and R35 OFF
- SB147 and SB148 ON

6.9.2 OSC clock supply

There are four ways to configure the pins corresponding to the external high-speed clock (HSE):

HSE: on-board oscillator X3 crystal (Default: not connected)

For typical frequencies and its capacitors and resistors, refer to the STM32 microcontroller datasheet. Refer to the AN2867 for oscillator design guide for STM32 microcontrollers. The X3 crystal has the following characteristics: 16 MHz, 8 pF, 20 ppm. It is recommended to use NX2016SA_16MHz_EXS00A-CS07826 manufactured by NDK. The following configuration is needed:

- SB142 and SB145 OFF (PH0/PH1 not connected to CN11 as I/O)
- SB143 (MCO) OFF
- SB6 and SB7 ON (connected to external HSE)

MCO from ST-LINK (Default: not connected):

MCO, the output of ST-LINK MCU, is used as an input clock. This frequency cannot be changed. It is fixed at 8 MHz, and connected to PH0 OSC_IN of STM32 microcontroller. The following configuration is needed:

- SB142 OFF and SB145 ON (Only PH1 connected to CN11 as I/O)
- SB143 ON (MCO connected to PH0)
- SB6 and SB7 OFF (not connected to external HSE)

External oscillator to PH0 input (Default: not connected)

The input clock comes from an external oscillator through pin 29 of the CN11 connector. The following configuration is needed:

- SB142 ON and SB145 ON (PH0/PH1 connected to CN11)
- SB143 OFF: MCO not connected to PH0
- SB6 and SB7 OFF (not connected to external HSE)

HSE not used (Default configuration)

PH0 and PH1 are used as GPIOs instead of clocks. The following configuration is needed:

- SB142 and SB145 ON (PH0/PH1 connected to CN11 as I/O)
- SB143 OFF: MCO not connected to PH0
- SB6 and SB7 OFF (External HSE)

6.10 Reset sources

The reset signal of Nucleo board is active LOW and the reset sources include:

- The RESET button B2
- The embedded ST-LINK/V2-1
- The ARDUINO®-included Zio connector CN8 pin 5
- The ST morpho connector CN11 pin 14

6.11 RSS/bootloader

The bootloader is located in the system memory, programmed by ST during production. It is used to reprogram the Flash memory via USART, I^2C, SPI, CAN FD, or USB FS in device mode through the DFU (device firmware upgrade). The bootloader is available on all devices. Refer to the *STM32 microcontroller system memory boot mode* application note AN2606 for more details.

The Root Secure Services (RSS) are embedded in a Flash area named secure information block, programmed during ST production. For example, it enables Secure Firmware Installation (SFI), thanks to the RSS extension firmware (RSSe SFI). This feature allows customers to protect the confidentiality of the FW to be provisioned into the STM32 when production is sub-contracted to an untrusted third party. The RSS is available on all devices, after enabling the TrustZone® through TZEN option bit.

The bootloader version can be identified by reading the bootloader ID at the address `0x0BF97FFE`.

6.11.1 Limitation

The STM32L5 part soldered on NUCLEO-L552ZE-Q with the Finish Good (FG) NUL552ZEQ$AU1 (sticker available on the top side of the board) embeds bootloader V9.0 affected by the limitations to be worked around, as described hereunder.

The bootloader ID of the bootloader V9.0 is `0x90`.

The following limitations exist in the bootloader V9.0:

Option Byte programming in RDP level 0.5

Issue: The user cannot program non-secure option bytes in RDP level 0.5 through the bootloader.

Workaround: The user can program option bytes, thanks to STM32CubeProgrammer GUI or command-line interfaces through JTAG. To know how to program option bytes through STM32CubeProgrammer, refer to *STM32CubeProgrammer* user manual (UM2237).

Impossible to set TZEN option bit

Issue: The user cannot set the TZEN option bit through Bootloader interfaces.

Workaround: Instead of the bootloader interface, the user can use JTAG to set the TZEN option bit.

Go command on USB-DFU interface

Issue: The user cannot use Go command through the bootloader on the USB-DFU interface.

Workaround: Instead of the USB-DFU interface, the user can use JTAG or any other communication ports supported by Bootloader to run Go command, like USART, I^2C, SPI or CAN FD.

Caution: Only SFI through JTAG is fully supported on bootloader V9.0. SFI through bootloader interfaces is partially supported because some option bytes cannot be managed by the bootloader and they must be set through JTAG.

6.11.2 Boot from RSS

On the NUCLEO-L552ZE-Q, PH3-BOOT0 is fixed to a LOW level allowing the boot from the memory address defined by SECBOOTADD0 option byte. In order to change the boot from RSS, it is necessary to set PH3-BOOT0 to the HIGH level just by applying 3V3 on the PH3-BOOT0 signal. The easiest solution is to make a direct connection between CN11 pin 5 (VDD) and 7 (PH3_BOOT0).

6.12 Virtual COM port: LPUART or USART

An LPUART or a USART interface of STM32 microcontroller on NUCLEO board can be connected to ST-LINK/V2-1 MCU or on shields on ST morpho connectors and ARDUINO® Uno V3 connectors.

The selection between LPUART and USART is performed by setting related solder bridges.

Refer to Table 10 and Table 11 below for the UART or LPUART connection to VCP interfaces or ARDUINO® UART.

Table 10. LPUART1 connection

Solder bridge configuration(1)	Feature
SB127, SB129 ON **SB124, SB126, SB128, SB130 OFF**	**LPUART1 (PG7/PG8) connected to ST-LINK VCP.** **Must be the interface for 1V8 MCU mode because PG [2-15] stay at 3V3 IO interface link to the VDDIO power supply.**
SB128, SB130 ON SB123, SB125, SB127, SB129 OFF	LPUART1 (PG7/PG8) connected to Zio, ARDUINO® D0/D1

1. *The default configuration is in bold.*

Table 11. USART3 connection

Solder bridge configuration(1)	Feature
SB124, SB126 ON SB123, SB125, SB127, SB129 OFF	USART3 (PD8/PD9) connected to ST-LINK VCP Only 3V3 mode supported
SB123, SB125 ON **SB124, SB126, SB128, SB130 OFF**	**USART3 (PD8/PD9) connected to Zio, ARDUINO® D0/D1**

By default:

- Communication between target MCU and ST-LINK MCU is enabled on LPUART1.
- Communication between target MCU, ARDUINO®, and ST morpho connectors, is enabled on USART3, not to interfere with the VCP interface.

The Virtual COM port settings are 115200 bps, 8-bit data, no parity, 1 stop bit, and no flow control.

6.13 USB Type-C® FS

The STM32 Nucleo-144 board supports USB full-speed (FS) communication. The USB connector CN15 is a USB Type-C® connector.

The STM32 Nucleo-144 board supports USB Type-C® SINK mode only.

A green LED LD7 lights up when V_{BUS} is powered by a USB host and the NUCLEO-L552ZE-Q board works as a USB device.

6.13.1 USB FS device

When a USB host connection to the CN15 USB Type-C® connector of STM32 Nucleo-144 is detected, the STM32 Nucleo-144 board starts behaving as a USB device. Depending on the powering capability of the USB host, the board can take power from the V_{BUS} terminal of CN15. In the board schematic diagrams, the corresponding power voltage line is called 5V_USB_C. The STM32 Nucleo-144 board supports USB voltage 5V: 4.75 V to 5.25 V. MCU VDD_USB supports the 3V3 voltage only. Section 6.4 provides information on how to use powering options. The hardware configuration for the USB FS interface is shown in Table 12.

Table 12. HW configuration for the USB interface

IO	HW	Setting	Configuration(1)
PA11	SB137	**OFF**	**PA11 used as USB_FS_N diff pair interface** No other muxing
		ON	PA11 can be used as an I/O on the morpho connector. USB function can be used, but performances are low due to the track length to the Zio connector: impedance mismatch.
PA12	SB138	**OFF**	**PA12 used as USB_FS_P diff pair interface** No other muxing
		ON	PA12 can be used as an I/O on the morpho connector. USB function can be used, but performances are low due to the track length to the Zio connector: impedance mismatch.

1. *The default configuration is shown in bold.*

6.13.2 UCPD

The USB Type-C® introduces the USB Power Delivery feature. The STM32 Nucleo-144 supports the dead battery and the SINK mode.

In addition to the I/O DP/DM directly connected to the USB Type-C® connector, 5 I/Os are also used for UCPD configuration: Configuration Channel (CCx), VBUS-SENSE, UCPD Dead Battery (DBn) and UCPD_FAULT (FLT) feature.

To protect the STM32 Nucleo-144 from USB over-voltage, a USB Type-C® port protection, PPS compliant, is used: TCPP01-M12 IC compliant with IEC6100-4-2 level 4.

- Configuration Channel I/O: UCPD_CCx: These signals are connected to the associated CCx line of the USB Type-C® connector through the STM USB port Protection TCPP01-M12. These lines are used for the configuration channel lines (CCx) to select the USB Type-C® current mode. The STM32 Nucleo-144 supports only SINK current mode.
- Dead Battery I/O: UCPD_DBn: This signal is connected to the associated DBn line of the TCPP01-M12. The STM USB port Protection TCPP01-M12 managed internally the Dead Battery resistors.

- V_{BUS} fault detection: UCPD_FLT: This signal is provided by the *STM USB Type-C® port protection.* It is used as fault reporting to MCU after a bad V_{BUS} level detection. By design, the STM32 Nucleo-144 V_{BUS} protection is set to 6 V max. (R45 is set to 2K7 to select 6 V maximum).

Table 13 describes the HW configuration for the UCPD feature.

Table 13. HW configuration for the UCPD feature

IO	HW	Setting	Configuration(1)
PA15	SB10	**OFF**	**PA15 connected to the USB Type-C®port protection and used as UCPD_CC1**
		ON	PA15 directly connected to USB Type-C® connector. USB Type-C® port protection is bypassed.
PB15	SB11	**OFF**	**PB15 connected to the USB Type-C® port protection and used as UCPD_CC2**
		ON	PB15 directly connected to the USB Type-C® connector. USB Type-C® port protection is bypassed.
PC2	SB8	**ON**	**PC2 used as VBUS_SENSE**
		OFF	PC2 NOT used for UCPD Can be used on Zio connector
PB5	-	-	**IO UCPD_DBn connected to USB Type-C® port protection and used as Dead battery feature**
PB14	-	-	**IO UCPD_FLT connected to USB Type-C® port protection and used as over-voltage fault reporting to MCU**

1. *The default configuration is shown in bold*

6.13.3 USB Type-C® connector

Figure 15 shows the pinout of the USB Type-C® connector CN15.

Figure 15. CN15 USB Type-C® connector pinout

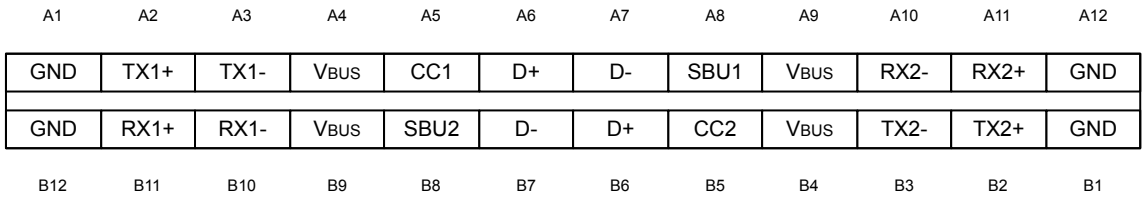


Table 14 describes the pinout of the USB Type-C® connector CN15.

Table 14. CN15 USB Type-C® connector pinout

STM32 pin	Signal name	Pin name	Pin	Pin	Pin name	Signal name	STM32 pin
-	GND	GND	A1	B12	GND	GND	-
-	-	TX1+	A2	B11	RX1+	-	-
-	-	TX1-	A3	B10	RX1-	-	-
-	VBUS_C/ 5V_USB_C	VBUS	A4	B9	VBUS	VBUS_C/ 5V_USB_C	-
A15	UCPD_CC1	CC1	A5	B8	SBU2	-	-

STM32 pin	Signal name	Pin name	Pin	Pin	Pin name	Signal name	STM32 pin
USB_DP2	USB_DP2	D+	A6	B7	D-	USB_DM2	USB_DM2
USB_DM2	USB_DM2	D-	A7	B6	D+	USB_DP2	USB_DP2
-	-	SBU1	A8	B5	CC2	UCPD_CC2	PB15
-	VBUS_C/ 5V_USB_C	VBUS	A9	B4	VBUS	VBUS_C/ 5V_USB_C	-
-	-	RX2-	A10	B3	TX2-	-	-
-	-	RX2+	A11	B2	TX2+	-	-
-	GND	GND	A12	B1	GND	GND	-

6.14 Jumper configuration

The jumper default positions are explained in Table 4. Default jumper configuration, and shown in Figure 2. The Table 15 below explains the other jumper settings and configuration.

Table 15. Jumper configuration

Jumper / CN	Definition	Setting [1]	Comment
CN4	T_SWCLK T_SWDIO	**ON [1-2] ON [3-4]**	**ST-LINK/V2-1 enable for on-board MCU debugger**
		OFF	ST-LINK/V2-1 functions enabled for external CN5 connector
JP2	STLK_RST	ON [1-2]	use to reset ST-LINK MCU
		OFF	**Normal mode**
JP3	T_NRST	**ON**	**ST-LINK able to reset target MCU**
		OFF	ST-LINK not able to reset target MCU configuration to use when CN5 is used with external application
JP4	VDD_MCU voltage selection	**ON [1-2]**	**VDD_MCU voltage selection = 3V3**
		ON [2-3]	VDD_MCU voltage selection = 1V8
		OFF	No VDD_MCU power supply (forbidden)
JP5	IDD measurement	**ON [1-2]**	**VDD =3V3**
		OFF	U6 LDO not used. External 3V3 source can be connected on pin 2 (ULPBench probe as an example)
JP6	5V Power selection	**ON [1-2]**	**5V from ST-LINK**
		ON [3-4]	5V from ARDUINO® VIN 7 to 12 V
		ON [5-6]	5V from 5V_EXT
		ON [7-8]	5V from user USB_UCPD (USB Type-C®)
		ON [9-10]	5V from USB_CHGR
		OFF	No 5V Power source, configuration when external 3V3 is used
CN13 / CN14	GND	NA	GND probe

1. *Default jumper state in bold.*

6.15 Solder bridge configuration

Table 16 details the solder bridges of the STM32L5 Nucleo-144 board.

Table 16. SB configuration

Definition	Bridge	Setting[1][2]	Comment
ST-LINK USB Power bypass mode	SB1	**OFF**	**USB power switch protection enable**
		ON	USB power switch by-passed (not recommended)
3V3_PER	SB2	OFF	3V3 for peripheral not available (not recommended)
		ON	**Used to provide 3V3 to some peripheral without impacting the IDD measurement**
3V3 LDO output	SB3	OFF	U7 LDO output does not provide 3V3. An external 3V3 is needed. LDO protection is active when external 3V3 is used
		ON	**U7 LDO output provides 3V3**
MCU VDDSMPS	SB4	OFF	VDDSMPS input not supplied (not recommended)
		ON	**VDDSMPS input connected to VDD_MCU**
MCU_VREFP	SB5	OFF	VREFP input not supplied (not recommended)
		ON	**VREFP input connected to VDDA**
	SB115	**OFF**	**VREFP not connected to Zio, ARDUINO® pin 6**
		ON	VREFP connected to Zio, ARDUINO® pin 6
HSE CLK selection	SB6/SB7	**OFF/OFF**	**HSE NOT provided by External HSE CLK X3**
		ON/ON	HSE provided by External HSE CLK X3
	SB143	**OFF**	**ST-LINK MCO NOT used for HSE CLK**
		ON	ST-LINK MCO used for HSE CLK
	SB142	OFF	PH0 NOT connected to morpho connector MCO usage
		ON	**PH0 connected to morpho connector**
	SB145	OFF	PH1 NOT connected to morpho connector
		ON	**PH1 connected to morpho connector I/O usage**
USB	SB8	OFF	PC2 not connected to USB Type-C® VBUS_SENSE used as ADC_A7 on Zio connector
		ON	**PC2 connected to USB Type-C® VBUS_SENSE**
	SB144	OFF	PC2 not connected to ADC_A7 on Zio connector used as USB Type-C® VBUS_SENSE
		ON	**PC2 connected to ADC_A7 on Zio connector**
	SB10	**OFF**	**PA15 connected to *STM USB Type-C® port protection* and used as CC1**
		ON	*USB Type-C® port protection* is bypassed (not recommended debug only)
	SB11	**OFF**	**PB15 connected to *STM USB Type-C® port protection* and used as CC2**
		ON	*USB Type-C® port protection* is bypassed (not recommended debug only)
	SB137/SB138	**OFF/OFF**	**PA11/PA12 used as USB_FS_P/N interface**
		ON/ON	PA11/PA12 used as I/O connected to morpho connector CN12

Definition	Bridge	Setting[1][2]	Comment
(Continued) USB	SB135	OFF	PB5 not connected to Zio CN7 for SPI_B interface: Reserved for UCPD_DBn
		ON	**PB5 connected to Zio CN7 for SPI_B interface, can't be used for UCPB_DBn**
AGND	SB9	**ON**	**AGND connected to GND. Reserved, do not modify.**
SWD interface (Reserved)	SB100/SB102/ SB104/SN106	**OFF**	Reserved, do not modify
SWD interface (Default)	SB101/SB103/ SB105/SB107	**ON**	Reserved, do not modify
SWO	SB108	**OFF**	**SWO connected through level shifter to target MCU I/O 1V8 compatibility**
		ON	SWO not connected through the level shifter. Debug mode only compatible with MCU I/O 3V3
	SB140	OFF	PB3 used as I/O on Zio and morpho connector
		ON	**PB3, used as SWO_MCU, connected between STLINK and target MCU**
Level shifter	SB109	OFF	Level shifter not connected to VDD_MCU
		ON	**Level shifter connected to VDD_MCU (SB110 must be disconnected)**
	SB110	**OFF**	**Level shifter not connected to 3V3_PER**
		ON	Level shifter connected to 3V3_PER (SB109 must be disconnected)
IOREF selection	SB111	**OFF**	**IOREF NOT connected to 3V3_PER power supply**
		ON	IOREF connected to 3V3_PER power supply
	SB112	OFF	IOREF NOT connected to VDD_MCU power supply
		ON	**IOREF connected to VDD_MCU power supply**
	SB113	**OFF**	**IOREF NOT connected to 3V3 power supply**
		ON	IOREF connected to 3V3 power supply
SMPS 1V8 power input	SB114	**ON**	**SMPS 1V8 U7/U101 powered by 5V**
		OFF	SMPS 1V8 U7/U101 NOT powered
User LED GREEN	SB118	OFF	Green user LED green not driven by PC7
		ON	**Green user LED driven by PC7**
	SB120	**OFF**	**Green user LED not driven by PA5**
		ON	Green user LED driven by PA5 with ARD_D13
SDMMC I/O	SB119	OFF	PC8 not connected to morpho CN12 pin 2 to avoid stub on Zio CN8 SDMMC_D0
		ON	**PC8 connected to morpho CN12 pin 2 and Zio CN8 pin 2**
	SB122	OFF	PC9 not connected to morpho CN12 pin 1 to avoid stub on Zio CN8 SDMMC_D1
		ON	**PC9 connected to morpho CN12 pin 1 and Zio CN8 pin 4**
Zio SAI_D / SPI_B interface	SB121	OFF	PA4 not connected to Zio CN7 for SAI_D interface
		ON	**PA4 connected to Zio CN7 for SAI_D interface**
	SB136	OFF	PA4 not connected to Zio CN7 for SPI_B interface
		ON	**PA4 connected to Zio CN7 for SPI_B interface**
	SB134	OFF	PB4 not connected to Zio CN7 for SAI_D interface

Definition	Bridge	Setting[1][2]	Comment
(Continued) Zio SAI_D / SPI_B interface	(Continued) SB134	**ON**	**PB4 connected to Zio CN7 for SAI_D interface**
	SB139	OFF	PB4 not connected to Zio CN7 for SPI_B interface
		ON	**PB4 connected to Zio CN7 for SPI_B interface**
	SB135	OFF	PB5 not connected to Zio CN7 for SPI_B interface: Reserved for UCPD_DB1
		ON	**PB5 connected to Zio CN7 for SPI_B interface, shared with for UCPB_DB1**
PD8 USART3_TX	SB123	OFF	PD8 USART3_TX not connected to ARDUINO® D1 TX
		ON	**PD8 USART3_TX connected to ARDUINO® D1 TX**
	SB124	**OFF**	**PD8 USART3_TX not connected to STLK VCP TX**
		ON	PD8 USART3_TX connected to STLK VCP TX
PD9 USART3_RX	SB125	OFF	PD9 USART3_RX not connected to ARDUINO® D0 RX
		ON	**PD9 USART3_RX connected to ARDUINO® D0 RX**
	SB126	**OFF**	**PD9 USART3_RX not connected to STLK VCP RX**
		ON	PD9 USART3_RX connected to STLK VCP RX
PG7 LPUART1_TX	SB127	OFF	PG7 LPUART1_TX not connected to STLK VCP TX
		ON	**PG7 LPUART1_TX connected to STLK VCP TX** **Configuration to support debug with 1V8 mode**
	SB128	**OFF**	**PG7 LPUART1_TX not connected to ARDUINO® D1 TX**
		ON	PG7 LPUART1_TX connected to ARDUINO® D1 TX
	SB168	OFF	PG7 LPUART1_TX not connected to morpho connector CN12
		ON	**PG7 LPUART1_TX connected to morpho connector CN12**
PG8 LPUART1_RX	SB129	OFF	PG8 LPUART1_RX not connected to STLK VCP RX
		ON	**PG8 LPUART1_RX connected to STLK VCP RX** **Configuration to support debug with 1V8 mode**
	SB130	**OFF**	**PG8 LPUART1_RX not connected to ARDUINO® D0 RX**
		ON	PG8 LPUART1_RX connected to ARDUINO® D0 RX
	SB167	OFF	PG8 LPUART1_RX not connected to morpho connector CN12
		ON	**PG8 LPUART1_RX connected to morpho connector CN12**
MCU VDD_USB	SB132	OFF	VDD_USB input not supplied
		ON	**VDD_USB input connected to VDD**
MCU VDDIO	SB133	OFF	VDDIO input not supplied (no PG [2-15] I/O)
		ON	**VDDIO input connected to VDD**
MCU VDD_USB	SB146	OFF	VBAT input not supplied
		ON	**VBAT input connected to VDD_MCU 3V3 or 1V8**
LSE CLK selection	SB147/SB148	**OFF**	**LSE provided by External LSE CLK X2 (R34/R35) PC14 and PC15 not connected to morpho connector**
		ON	PC14 and PC15 connected to morpho connector, LSE NOT provided by External LSE CLK X2
MCU VDDA	SB149	**OFF**	**VDDA input not supplied by VDD**
		ON	VDDA input connected to VDD (SB150 must be not connected)

Definition	Bridge	Setting[1][2]	Comment
(Continued) MCU VDDA	SB150	OFF	VDDA input not supplied by VDD_MCU
		ON	**VDDA input connected to VDD_MCU (SBN149 must be not connected)**
PB10 I/O selection	SB151	OFF	PB10 not used as QSPI_CLK
		ON	**PB10 used as QSPI_CLK**
	SB157	OFF	PB10 not used as TIMER for Motor Control
		ON	**PB10 used as TIMER for Motor Control**
PA2 I/O	SB152	OFF	PA2 not used as QSPI_CS
		ON	**PA2 used as QSPI_CS**
	SB153	OFF	PA2 not used as ARDUINO® A1 ADC
		ON	**PA2 used as ARDUINO® A1 ADC**
User button	SB154	OFF	User button NOT connected to PC13
		ON	**User button connected to PC13**
	SB155	**OFF**	**User button NOT connected to PA0**
		ON	User button connected to PA0
PA0	SB156	OFF	PA0 not used as TIMER for Motor control, reserved for User button
		ON	**PA0 can be used as TIMER for Motor control, can't be used as a user button**
PE15 I/O selection	SB158	OFF	PE15 not used as QSPI_IO3
		ON	**PE15 used as QSPI_IO3**
	SB159	OFF	PE15 not used as TIMER for Motor Control
		ON	**PE15 used as TIMER for Motor Control**
PB0 I/O selection	SB160	OFF	PB0 not used as QSPI_IO1
		ON	**PB0 used as QSPI_IO1**
	SB161	OFF	PB0 not used as ARDUINO® A3 ADC
		ON	**PB0 used as ARDUINO® A3 ADC**
	SB162	OFF	PB0 not connected on morpho CN11 pin to avoid stub on ARDUINO® ADC A3
		ON	**PB0 connected on morpho CN11**
PE12 I/O selection	SB163	OFF	PE12 not used as QSPI_IO0
		ON	**PE12 used as QSPI_IO0**
	SB164	OFF	PE12 not used as TIMER for Motor Control
		ON	**PE12 used as TIMER for Motor Control**
PE14 I/O selection		OFF	PE14 not used as QSPI_IO2
		ON	**PE14 used as QSPI_IO2**
		OFF	PE14 not used as TIMER for Motor Control
		ON	**PE14 used as TIMER for Motor Control**

1. *Default SBx state is shown in bold.*
2. *All NUCLEO products are delivered with solder-bridges configured according to the target MCU supported.*

7 Extension connectors

Six extension connectors are implemented on the STM32L5 Nucleo-144 board:

- CN7, CN8, CN9, and CN10 for Zio connector supporting ARDUINO® Uno V3
- CN11 and CN12 for ST morpho connector

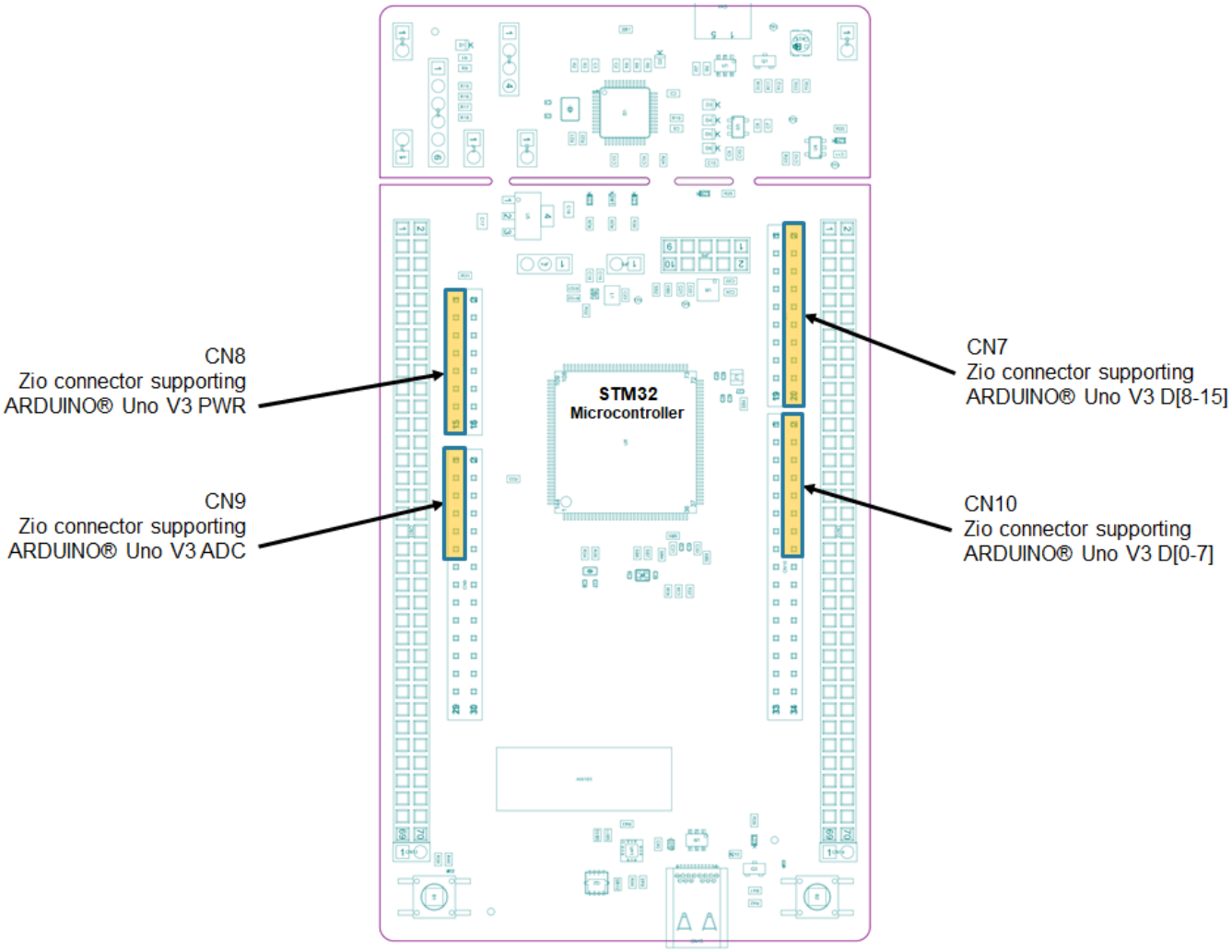
The jumpers for voltage selection and IDD measurements are not described here.

7.1 Zio connectors supporting ARDUINO® Uno V3

The CN7, CN8, CN9 and CN10 Zio connectors are female connectors supporting ARDUINO® standard. Most shields designed for ARDUINO® can fit the Nucleo board.

Caution: The STM32 microcontroller I/Os are 3V3 compatible, while ARDUINO® Uno V3 is 5V compatible.

Figure 16. Zio connectors supporting ARDUINO® Uno V3



The related pinout for the ARDUINO® connector are listed in Table 17, Table 18, Table 19 and Table 20

Table 17. Pinout of ARDUINO®-included Zio connector CN7

Pin	Pin name	Signal name	STM32 pin	MCU function	Pin	Pin name	Signal name	STM32 pin	MCU function
1	D16	SAI_C_MCLK	PC6	SAI2_A	2	D15	I2C_A_SCL	PB8	I2C1
3	D17	SAI_C_SD	PD11	SAI2_A	4	D14	I2C_A_SDA	PB9	I2C1
5	D18	SAI_C_SCK	PB13	SAI2_A	6	VREFP	-	-	-
7	D19	SAI_C_FS	PD12	SAI2_A	8	GND	-	-	-
9	D20	SAI_D_FS	PA4	SAI1_B/ SPI3	10	D13	SPI_A_SCK	PA5	SPI1
11	D21	SAI_D_MCLK	PB4	SAI1_B/ SPI3	12	D12	SPI_A_MISO	PA6	SPI1
13	D22	SAI_D_SD/ SPI_B_MOSI	PB5	SAI1_B/ SPI3	14	D11	SPI_A_MOSI / TIM_E_PWM1	PA7	SPI1
15	D23	SAI_D_SCK/ SPI_B_SCK	PB3	SAI1_B/ SPI3	16	D10	SPI_A_CS / TIM_B_PWM3	PD14	SPI1/ TIM4_CH3
17	D24	SPI_B_NSS	PA4	SAI1/SPI3	18	D9	TIM_B_PWM2	PD15	TIM4_CH4
19	D25	SPI_B_MISO	PB4	SAI1/SPI3	20	D8	IO	PF12	-

Table 18. Pinout of ARDUINO®-included Zio connector CN8

Pin	Pin name	Signal name	STM32 pin	ARD function	Pin	Pin name	Signal name	STM32 pin	MCU function
1	NC	NC	-	ARD RES	2	D43	SDMMC_D0	PC8	SDMMC1
3	IOREF	IOREF	-	ARD IOREF	4	D44	SDMMC_D1	PC9	SDMMC1
5	NRST	NRST	NRST	ARD RESET	6	D45	SDMMC_D2	PC10	SDMMC1
7	3V3	3V3	-	ARD 3V3 I/O	8	D46	SDMMC_D3	PC11	SDMMC1
9	5V	5V	-	ARD 5V Output	10	D47	SDMMC_CK	PC12	SDMMC1
11	GND	GND	-	ARD GND	12	D48	SDMMC_CMD	PD2	SDMMC1
13	GND	GND	-	ARD GND	14	D49	I/O	PF3	-
15	VIN	VIN	-	ARD VIN	16	D50	I/O	PF5	-

Table 19. Pinout of ARDUINO®-included Zio connector CN9

Pin	Pin names	Signal name	STM32 pin	MCU function	Pin	Pin names	Signal name	STM32 pin	MCU function
1	A0	ADC	PA3	ADC12_IN 8	2	D51	USART_B_SCL K	PD7	USART2
3	A1	ADC	PA2	ADC12_IN 7	4	D52	USART_B_RX	PD6	USART2
5	A2	ADC	PC3	ADC12_IN 4	6	D53	USART_B_TX	PD5	USART2
7	A3	ADC	PB0	ADC12_IN 15	8	D54	USART_B_RTS	PD4	USART2

Pin	Pin names	Signal name	STM32 pin	MCU function	Pin	Pin names	Signal name	STM32 pin	MCU function
9	A4	ADC	PC1	ADC12_IN2	10	D55	USART_B_CTS	PD3	USART2
11	A5	ADC	PC0	ADC12_IN1	12	GND	-	-	-
13	D72	COMP1_INP	PB2	COMP1	14	D56	SAI_A_MCLK	PE2	SAI1_A
15	D71	COMP2_INP	PB6	COMP2	16	D57	SAI_A_FS	PE4	SAI1_A
17	D70	I2C_B_SMBA	PF2	I2C2	18	D58	SAI_A_SCK	PE5	SAI1_A
19	D69	I2C_B_SCL	PF1	I2C2	20	D59	SAI_A_SD	PE6	SAI1_A
21	D68	I2C_B_SDA	PF0	I2C2	22	D60	SAI_B_SD	PE3	SAI1_B
23	GND	-	-	-	24	D61	SAI_B_SCK	PF8	SAI1_B
25	D67	CAN_RX	PD0	CAN1	26	D62	SAI_B_MCLK	PF7	SAI1_B
27	D66	CAN_TX	PD1	CAN1	28	D63	SAI_B_FS	PF9	SAI1_B
29	D65	I/O	PG0	-	30	D64	I/O	PG1	-

Table 20. Pinout of ARDUINO®-included Zio connector CN10

Pin	Pin names	Signal name	STM32 pin	MCU function	Pin	Pin names	Signal name	STM32 pin	MCU function
1	AVDD	-	-	AVDD	2	D7	I/O	PF13	I/O
3	AGND	-	-	AGND	4	D6	TIM_A_PWM1	PE9	TIM1_CH1
5	GND	-	-	GND	6	D5	TIM_A_PWM2	PE11	TIM1_CH2
7	A6	ADC_A_IN	PB1	ADC12_IN16	8	D4	I/O	PF14	I/O
9	A7	ADC_B_IN	PC2	ADC12_IN3	10	D3	TIM_A_PWM3	PE13	TIM1_CH3
11	A8	ADC_C_IN	PA1	ADC12_IN6	12	D2	I/O	PF15	I/O
13	D26	QSPI_CLK	PA2	QSPI1	14	D1	USART_A_TX	PD8	USART3
15	D27	QSPI_IO3	PB10	QSPI1	16	D0	USART_A_RX	PD9	USART3
17	GND	-	-	-	18	D42	TIM_A_PWM1N	PE8	TIM1_CH1N
19	D28	QSPI_IO3	PE15	QSPI1	20	D41	TIM_A_ETR	PE7	TIM1_ETR
21	D29	QSPI_IO1	PB0	QSPI1	22	GND	-	-	-
23	D30	QSPI_IO0	PE12	QSPI1	24	D40	TIM_A_PWM2N	PE10	TIM1_CH2N
25	D31	QSPI_IO2	PE14	QSPI1	26	D39	TIM_A_PWM3N	PE12	TIM1_CH3N
27	GND	-	-	-	28	D38	TIM_A_BKIN2	PE14	TIM1_BKIN2
29	D32	TIM_C_PWM1	PA0	TIM2_CH1	30	D37	TIM_A_BKIN1	PE15	TIM1_BKIN
31	D33	TIM_D_PWM1	PA8	TIM1_CH1	32	D36	TIM_C_PWM2	PB10	TIM2_CH3
33	D34	TIM_B_ETR	PE0	TIM4_ETR	34	D35	TIM_C_PWM3	PB11	TIM2_CH4

7.2 ST morpho connector CN11 and CN12

The ST morpho connector consists of male pin header footprints CN11 and CN12 (not soldered by default). They can be used to connect the STM32 Nucleo-144 board to an extension board or a prototype/wrapping board placed on top of the STM32 Nucleo-144 board. All signals and power pins of the STM32 are available on the ST morpho connector. An oscilloscope, a logic analyzer, or a voltmeter can also probe this connector.

Figure 17. ST morpho connector

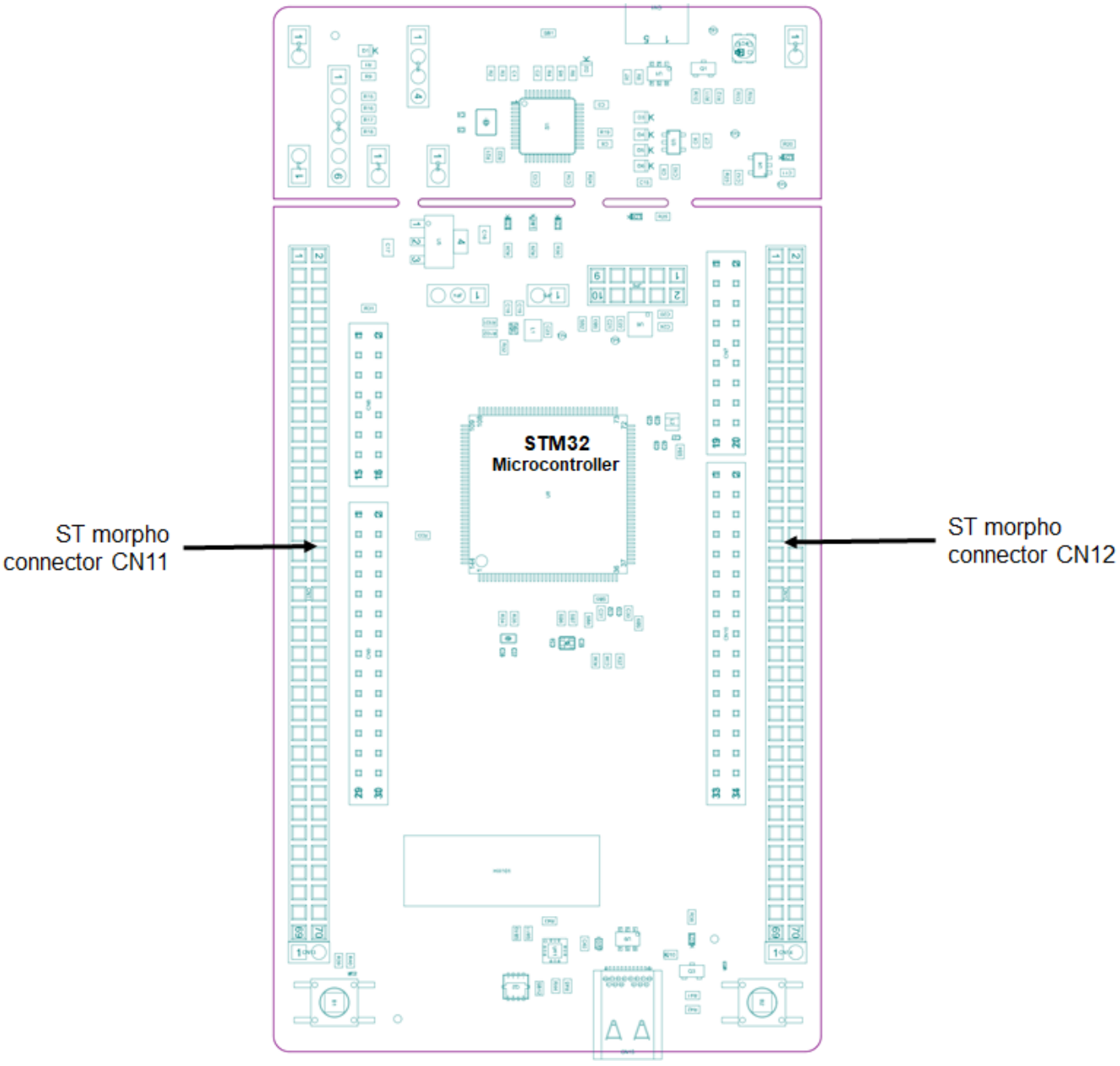


Table 21 shows the pin assignments for the STM32 on the ST morpho connector.

Table 21. Pin assignment of the ST morpho connector

CN11 odd pins		CN11 even pins		CN12 odd pins		CN12 even pins	
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	PC10	2	PC11	1	PC9	2	PC8
3	PC12	4	PD2	3	PB8	4	PC6
5	VDD	6	5V_EXT	5	PB9	6	NC
7	PH3_BOOT0(1)	8	GND	7	VREFP(2)	8	5V_STLK(3)
9	PF6	10	NC	9	GND	10	PD8
11	PF7	12	IOREF	11	PA5	12	PA12
13	PA13(4)	14	NRST	13	PA6	14	PA11
15	PA14(4)	16	3V3	15	PA7	16	NC
17	PA15	18	5V	17	PB6	18	PB11
19	GND	20	GND	19	PC7	20	GND
21	PB7	22	GND	21	PA9	22	PB2
23	PC13	24	VIN	23	PA8	24	PB1
25	PC14	26	NC	25	PB10	26	PB15
27	PC15	28	PA0	27	PB4	28	PB14
29	PH0	30	PA1	29	PB5	30	PB13
31	PH1	32	PA4	31	PB3	32	AGND
33	VBAT	34	PB0	33	PA10	34	NC
35	PC2	36	PC1	35	PA2	36	PF5
37	PC3	38	PC0	37	PA3	38	PF4
39	PD4	40	PD3	39	GND	40	PE8
41	PD5	42	PG2(5)	41	PD13	42	PF10
43	PD6	44	PG3(5)	43	PD12	44	PE7
45	PD7	46	PE2	45	PD11	46	PD14
47	PE3	48	PE4	47	PE10	48	PD15
49	GND	50	PE5	49	PE12	50	PF14
51	PF1	52	PF2	51	PE14	52	PE9
53	PF0	54	PF8	53	PE15	54	GND
55	PD1	56	PF9	55	PE13	56	PE11
57	PD0	58	PG1	57	PF13	58	PF3
59	PG0	60	GND	59	PF12	60	PF15
61	PE1	62	PE6	61	PG14(5)	62	PF11
63	PG9(5)	64	PG15(5)	63	GND	64	PE0
65	PG12(5)	66	PG10(5)	65	PD10	66	PG8(5)
67	NC	68	PG13(5)	67	PG7(5)	68	PG5(5)
69	PD9	70	NC	69	PG4(5)	70	PG6(5)

1. *The default state of BOOT0 is 0. It can be set to 1 when a jumper is plugged on the pins 5-7 of CN11.*
2. *V_{REFP} is not connected to CN12 by default (SB115 OFF).*
3. *5V_STLK is the 5V power signal, coming from the ST-LINK/V2-1 USB connector. It rises before the 5V signal of the board.*

4. *PA13 and PA14 are shared with SWD signals connected to ST-LINK/V2-1. If the ST-LINK part is not cut, it is not recommended to use them as I/O pins.*
5. *PG2 to PG15 can have a different I/O level to other I/O because supplied by VDDIO.*

8 Limitations

8.1 RSS/bootloader limitation

Issue observed:

The STM32L5 part soldered on NUCLEO-L552ZE-Q that embeds the bootloader V9.0 is affected by the limitations described in Section 6.11 RSS/bootloader.

Proposed workaround:

Refer to Section 6.11 RSS/bootloader to detail workaround.

Parts impacted:

This applies only to the NUCLEO-L552ZE-Q with the finished good (FG) **NUL552ZEQ$AU1** (Sticker available on the top side of the board).

8.2 SMPS limitation

Issue observed:

The STM32L5 part soldered on NUCLEO-L552ZE-Q embeds an internal SMPS. The sample revision rev B embeds two SMPS limitations: **SMPS regulation loss upon transiting into SMPS LP mode**, and **Unpredictable SMPS state at power-on**. Refer to errata sheet *STM32L552xx/562xx device errata* (ES0448) for more details.

Proposed workaround:

Refer to errata sheet *STM32L552xx/562xx device errata* (ES0448).

Parts impacted:

This applies only on the NUCLEO-L552ZE-Q with the finished goods (FG) **NUL552ZEQ$AU1** and **NUL552ZEQ $AU2** (Sticker available on the top side of the boards).

9 Federal Communications Commission (FCC) and Industry Canada (IC) Compliance Statements

9.1 FCC Compliance Statement

Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

Part 15.105

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception which can be determined by turning the equipment off and on, the user is encouraged to try to correct interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Note: Use only shielded cables.

Responsible party (in the USA)

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9.2 IC Compliance Statement

Industry Canada ICES-003 Compliance Label: *CAN ICES-3 (B) / NMB-3 (B)*.

10 CE conformity

10.1 Warning

EN 55032 / CISPR32 (2012) Class B product

Warning: this device is compliant with Class B of EN55032 / CISPR32. In a residential environment, this equipment may cause radio interference.

Avertissement : cet équipement est conforme à la Classe B de la EN55032 / CISPR 32. Dans un environnement résidentiel, cet équipement peut créer des interférences radio.

Revision history

Table 22. **Document revision history**

Date	Version	Changes
30-Sep-2019	1	Initial release
28-Jan-2020	2	Added: • Section 8 Limitations Updated: • Section 6.11 RSS/bootloader • Section 9 and Section 10 switched to Class B • Table 20
17-Mar-2020	3	Added NUL552ZEQ$AU2 to impacted parts in Section 8.2 SMPS limitation
30-Jun-2020	4	Updated Limitation regarding limited support to SFI through the bootloader towards JTAG

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