Reference Design:

HFRD-39.0 Rev 1; 05/09

REFERENCE DESIGN

40Gbps, Quad-SFP Half-Active Copper Cable Assembly



40Gbps, Quad-SFP Half-Active Copper Cable Assembly

Table of Contents

1	Overview	2
2	Obtaining Additional Information	2
3	High-Speed Copper Links	3
4	QSFP Requirements	3
5	Implementation	3
6	QSFP Management Interface	5
7	Evaluation	8
8	Supporting Documentation	10

1 Overview

High-Frequency Reference Design 39.0 (HFRD-39.0) is an active cable receiver for integration into a Quad-SFP (QSFP) cable assembly. This reference design is capable of rates up to 10.3125Gbps on each of its four links. It provides adjustable equalization for different cable lengths and reduces the impact of near-end crosstalk (NEXT) by regenerating the received signal before encountering interfering signals. regeneration step significantly This signal-to-noise increases the ratio, thereby improving bit-error margins and allowing longer cable spans. To support the testing and evaluation of the active cable assembly, a host adapter board (HFRD-32.0) is available to supply power and I^2C serial communication support; the adapter board also translates the QSFP high-speed signal connections to SMA connectors.

HFRD-39.0 contains an I^2C EEPROM to provide a compliant QSFP software interface, and four equalizers, the MAX3804, to recover the signals at the receiving end of the cable.

By supplying complete documentation, performance evaluation, and a fully assembled circuit board, HFRD-39.0 minimizes the need to experiment with active cable assemblies.



1.1 Features

- Schematics
- Bill of Materials
- Gerber plot files available
- Single 3.3V supply
- Adjustable equalization
- Regenerates weak signals before launching into the host-side receiver.
- PC board fits into QSFP shell

2 Obtaining Additional Information

Limited quantities of the 40Gbps, Quad-SFP Half-Active Copper Cable Assembly (HFRD-39.0) are available. For more information about this reference design or to obtain a board, send an email to: <u>https://support.maxim-ic.com/</u>.

3 High-Speed Copper Links

High-speed copper links operating over several meters of cable require compensation to correct for jitter induced by intersymbol interference (ISI). The loss mechanism of simple copper cable reduces higher-frequency content more severely than lowercontent. То achieve frequency acceptable performance, this disproportionate attenuation requires attention to several signal characteristics including: transition time, swing, crosstalk (cable dress and construction), and signal-to-noise ratio (SNR).



Figure 1. The QSFP half-active cable assembly relies on four MAX3804 equalizers to achieve a 10m span over copper cable.

Transition time and amplitude conflict with crosstalk and SNR. Attempts to improve an individual channel's performance by increasing swing and reducing transition time generate more interference for adjacent, low-level receive channels. The proximity of the transmit lines to the receive lines makes crosstalk unavoidable; however, it is possible to improve the SNR at the receiver by regenerating the signal, as done by HFRD-39.0, before it accumulates more noise.

4 **QSFP** Requirements

The specification released by the QSFP Multisource Agreement (MSA) committee requires that all status, monitor, and control functions be accessed through a serial communication link. For example, a receiver loss of signal (LOS) and transmit laser fault are now reported only through a register, which is read using I^2C , instead of the dedicated pins of an

SFP interface. In addition, all modules must report various measurements such as received power, temperature, and supply voltage. A microcontroller is needed for these latter measurements. The copper assembly configuration is mentioned in the MSA, but it is not described in detail and is left for creative interpretation. The MSA refers to a transmitter technology and connector type that can be copper, but the bulk of the specification is dominated by optical information. The copper assembly could be a full-featured device with microcontroller (see HFRD-31.0) or it could be a wire with an EEPROM. HFRD-39.0 takes liberties with this latter definition and adds an active device to the receive end of each channel. In effect, HFRD-39.0 is masquerading as a wire with an EEPROM. The only difference is that the actual wire is much longer than an entirely passive assembly.

5 Implementation

The MAX3804 can amplify small signals and frequency-dependent cable compensate for attenuation. A signal as small as 40mV_{P-P} at 5GHz can be regenerated to a $500mV_{P-P}$ swing. With the minimum transmitter output of a QSFP host at 500mV_{P-P} , this half-active copper assembly is limited to cable spans with approximately 20dB of loss at 5GHz. From a practical perspective, this translates to approximately 10 meters for large diameter wire and 5 meters for smaller diameter wire. Losses from the transmitter-side QSFP connector and transmission lines need to be kept to a minimum. See Figure 2.



Figure 2. Front and back of HFRD-39.0.

5.1 Construction

The recommended cable for this application is a multiconductor twin axial (i.e., balanced differential) cable, of which there are various types and gauges. W. L. Gore and Assoc. produces a wire named Eye-OpenerTM that has a modest, yet significant amount of compensation built into the wire conductor. By a clever selection of core conductor and plating, the Eye-Opener wire reduces ISI and thereby improves on jitter margin. Another cable candidate is Amphenol's SpectraStrip® SkewClear®.

The cable's weight and size are critical factors in most applications. A lighter weight can be achieved by shorter length or small diameter wire as defined by its gauge. The wire gauge is usually expressed in AWG (American Wire Gauge) units; a larger AWG number indicates a smaller wire diameter. For example, the expected loss for 28AWG is approximately 1.5 times the loss experienced with 24AWG.

The multiconductor cables from W.L. Gore and Amphenol have eight differential wire pairs. Each pair is wrapped in a thin metalized polyester foil with an accompanying bare (drain) wire to serve as a signal shield. The wrapping for each pair is labeled every few inches to aid in identification during assembly. The Eye-Opener wires are numbered from 1 to 4 and colored grey or blue. Rather than twisting, weaving, and dressing the individual pairs in an arbitrary fashion, refer to Figures 3 and 4 for wiring advice. The wiring task is greatly simplified by exploiting the symmetry in the wire arrangement within the cable bundle.

Finally, the wires within the module shell must be immobilized so that the solder connections to the circuit board do not break. It is recommended that a generous supply of nonconductive silicon adhesive be introduced around the cable-to-board termination to fill the remaining space and secure the connections.



Figure 3. Wire arrangement within W.L.Gore's Eye-Opener cable bundle and each pair's assignment relative to the board.



Figure 4. Wire arrangement within Amphenol's SpectraStrip cable bundle and each pair's assignment relative to the board.

5.2 Heat Dissipation

A QSFP module is allowed to dissipate as much as 3.5W. This reference design dissipates less than 500mW. The MAX3804 equalizer is packaged with a large pad on the bottom for cooling. This board is only slightly larger than the device itself and offers no significant heat dissipation. For this reference design, the cable's drain wires provide adequate heat conduction. When using a cable without the drain wires, additional thermal control is necessary.



Figure 5. HFRD-39.0 with 28AWG cable. Careful planning results in a neat and spaceefficient wire dress.

6 **QSFP Management Interface**

The QSFP standard requires an I^2C management interface for control and status reporting. This reference design provides only the most essential information that can be loaded into an EEPROM. A supporting reference design, HFRD-32.0, provides this I^2C interface and the appropriate connections for lab equipment. See Figure 8. This host adapter board and its associated graphical user interface (GUI) allow access through a Microsoft Windows®-based personal computer equipped with USB 2.0. Figures 9, 10, and 11 are examples of the GUI.



Figure 6. The QSFP Host Adapter board (HFRD-32.0) includes an USB-to-I²C interface, host-side supply monitor, QSFP interface connector, and SMA connectors for all of the data signals.

🖩 MAXIM Strategic Applications: QSFP Host Adapter									
Communication									
Initialize Module Found Module Module NOT Found Vende	le Found or Part Number: HFRD-39.0								
Host Supplies Receiver 3.30 V 48 mA 3.30 V 64 mA									
Monitor Interrupt Masks Controls Identification Read/Write Byte Options Available									
Click 'Refresh' to update this page.	Supported Standards								
General Characteristics	SONET OC 48, short reach								
Module ID QSFP	Ethernet								
Power Class Power Class 1 Module (1.5 W max)	10G Ethernet 10GBASE-SR								
CLEI Code Not Available	1G Ethernet 1000BASE-CX								
Connector Copper Pigtail	- Fiber Channel								
Data Encoding 648668	Link Length short distance (S)								
Bit Rate 10.0 Gbps	Technology Electrical inter-enclosure (EL)								
Extended Rate Select Not Available	Medium Twin Axial Pair (TW)								
Device Technology Copper	Speed Click or hover for more information.								
Wavelength Center Not Available	⊂ InfiniB and								
Wavelength Tol. Not Available	Technology IB 4X Copper Active								
Max. Temperature 70 C	Speed QDR Speed (10 Gb/s)								
Cable Length	Vendor								
Single-Mode Fiber Not Available	Name MAXIM INTEGRATED								
OM3 Mulit-Mode Fiber Not Available	OUI Not Available								
OM2 Mulit-Mode Fiber Not Available	Part Number HFRD-39.0								
OM1 Mulit-Mode Fiber Not Available	Revision A								
Copper 10 m	Serial Number 000000000000000000000000000000000000								
Check Sum (128-190) Check Sum (192-222)	Date Code 15 September 2008								
Stored 17 Stored 119	Lot Code								
Calculated 4 Calculated 119	Misc (224-255) Not Available								

6.1 HFRD-32.0 QSFP Host Adapter Software: Identification Page

Figure 7. A typical status display from HFRD-32.0 QSFP Host Adapter.



6.2 HFRD-32.0 QSFP Host Adapter Software: Bit-Level and Byte-Level Read/Write

Figure 8. HFRD-32.0 gives bit-level and byte-level access to all QSFP memory locations and contents.

7 Evaluation

7.1 Test Apparatus

The test apparatus is shown in Figure 9. The Agilent ParBERT[™] pattern generator provided the data to fill the channels and introduced the aggressor signals. The SyntheSys Research 12500B BERTScope[™] supplied the "victim" signal. The HFRD-32.0 host adapter board provided the interface between the lab equipment and the cable assembly. The Tektronix® CSA8000 oscilloscope produced the eye diagrams.

7.2 Results

Table 1 is a collection of eye diagrams for various data rates, cable lengths, and wire gauges. These images capture the entire signal path shown in Figure 9: QSFP connectors; approximately 5 inches of 6mil FR-4 microstrip, SMA connectors; and

aggressor signals of $1V_{P-P}$. The victim channel was acquired directly at the QSFP connector using a 5inch length of semirigid coax. The total path includes only one 5-inch span of FR4. The victim source was a low-jitter source (DJ < 10ps) from the BERTScope with a vertical eye opening of $500mV_{P-P}$, measured differentially, and without any pre-emphasis.

The eyes in Table 1 show excellent performance for the 5m, 28AWG cable and very good performance for the 10m, 24AWG cable. BER testing confirmed these eyes to be error free at all of the listed data rates.

Test results were different for the 10m, 26AWG cable at 10.3Gbps; the $500mV_{P-P}$ drive from the transmitter source was insufficient. Error-free operation at 10.3Gbps was achieved when the transmitter drive was increased to $750mV_{P-P}$. All of the other data rates shown here were error free.



Figure 9. Test apparatus fills all channels to evaluate performance in the presence of interfering aggressor signals.



 Table 1. End-to-End Performance for Various Cables and Bit Rates (Pattern: PRBS 2³¹ - 1, +25°C)

8 Supporting Documentation

8.1 HFRD-39.0 Schematic



Figure 10. Schematic for HFRD-39.0 high-speed data and equalizer. The cable is wired to J3.

8.2 Artwork, HFRD-39.0



Figure 11. Layer 1 (top).



Figure 12. Layer 2, ground reference for top-layer transmission lines.



Figure 13. Layer 3, supply routing and ground patch.



Figure 14. Layer 4, supply routing and ground patch.



Figure 15. Layer 5, ground reference for transmission lines of Layer 6.



Figure 16. Layer 6 as viewed looking through the top layer.



8.3 Component Placement, Front Side of HFRD-39.0

Figure 17. Top (front) layer. The receiver input portion of the cable is soldered at J3 at the top. J1 is the QSFP host interface at the bottom.



8.4 Component Placement, Back Side of HFRD-39.0

Figure 18. Bottom layer viewed from the bottom. The QSFP interface is at the bottom.

8.5 Mechanical Dimensions, HFRD-39.0



Figure 19. Dimensioned drawing and FR-4 board stackup (loss tangent = 0.02).

8.6 Bill of Materials

.

Qty	Reference	Value	Tolerance	Manufacturer	Description
25	C1-25	0.01µF	X7R, 6.3V		C0201X7R6R3-103KNP, Capacitor (0201)
1	L1				Filter Bead, Taiyo Yuden BK0603HM241-T, Digikey 587-1822-1-ND
4	R1-2 R4-5	10K	5%		Resistor (0201)
6	R3 R6-10	DNI	5%		Resistor (0201)
4	U1-4			Maxim	MAX3804ETE 12Gbps Equalizer
1	U6			Fairchild™	OR Gate Fairchild NC7S32P5X, SC70
1	U7			ATMEL®	2-Wire Serial EEPROM, AT24C02B in 8-pin TSSOP

8.7 Additional Materials Not Included

8-pair, shielded and balanced 100Ω cable

W.L. Gore Eye-Opener

24AWG: part no. E76025-N 24. 26AWG: part no. E76025-N 26.

28AWG: part no. E76025-N 28.

Amphenol SpectraStrip SkewClear,

24AWG: part no. 166-2499-998.

26AWG: part no. 166-2699-997.

28AWG: part no. 166-2899-997.

Eye-Opener is a trademark of W.L. Gore and Associates.

SpectraStrip and SkewClear are registered trademarks of Amphenol Corporation.

Microsoft Windows is a registered trademark of Microsoft Corporation.

ParBERT is a trademark of Agilent Technologies, Inc.

BERTScope is a trademark of SyntheSys Research.

Tektronix is a registered trademark of Tektronix, Inc.

Fairchild is registered trademark of Fairchild Semiconductor Corporation.

Atmel is registered trademark of Atmel Corporation.