MIC22600

1 MHz, 6A Integrated Switch Synchronous Buck Regulator

Features

- Input Voltage: 2.6V to 5.5V
- Output Voltage Adjustable Down to 0.7V
- Output Current Up to 6A
- Full Sequencing and Tracking Ability
- Power-on-Reset/Power Good
- Efficiency >90% Across a Broad Load Range
- Ultra-Fast Transient Response, Easy RC Compensation
- 100% Maximum Duty Cycle
- Fully Integrated MOSFET Switches
- Micropower Shutdown
- Thermal Shutdown and Current-Limit Protection
- 24-Pin 4 mm x 4 mm QFN
- 24-Pin ePad TSSOP
- –40°C to +125°C Junction Temperature Range

Applications

- High Power Density Point-of-Load Conversion
- Servers and Routers
- DVD Recorders
- Computing Peripherals
- Base Stations
- FPGAs, DSP, and Low Voltage ASIC Power

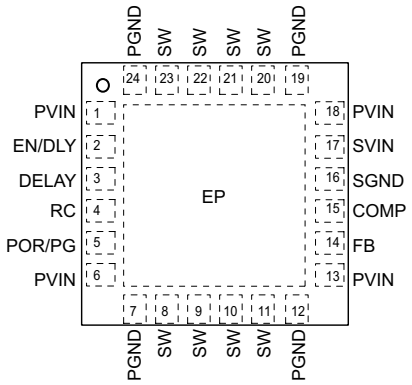
General Description

The MIC22600 is a high-efficiency, 6A, integrated switch, synchronous buck (step-down) regulator. The MIC22600 is optimized for highest efficiency and achieves more than 90% efficiency, while still switching at 1 MHz over a broad load range with only 1 µH inductor and down to 47 µF output capacitor. The ultra high-speed control loop keeps the output voltage within regulation even under extreme transient load swings commonly found in FPGAs and low voltage ASICs. The output voltage can be adjusted down to 0.7V to address all low voltage power needs. The MIC22600 offers a full range of sequencing and tracking options. The EN/DLY pin combined with the Power Good/POR pin allows multiple outputs to be sequenced in any way during turn-on and turn-off. The RC (Ramp Control) pin allows the device to be connected to another product in the MIC22xxx and/or MIC68xxx family, to keep the output voltages within a certain ΔV on start up.

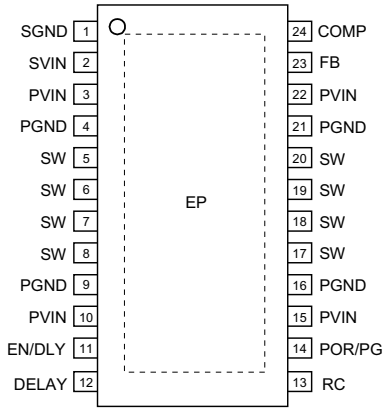
The MIC22600 is available in a 24-pin 4mm x 4mm QFN and thermally enhanced 24-pin ePad TSSOP with a junction operating range from –40°C to +125°C.

Package Types

MIC22600
24-Lead 4 mm x 4 mm QFN (ML)
(Top View)



MIC22600
24-Lead ePad TSSOP (TSE)
(Top View)



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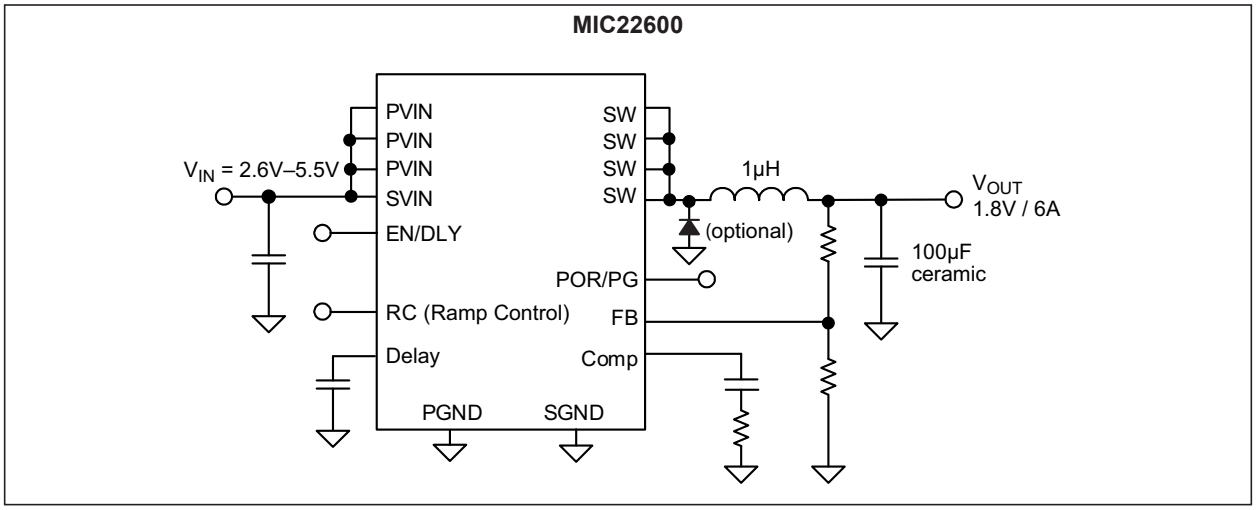
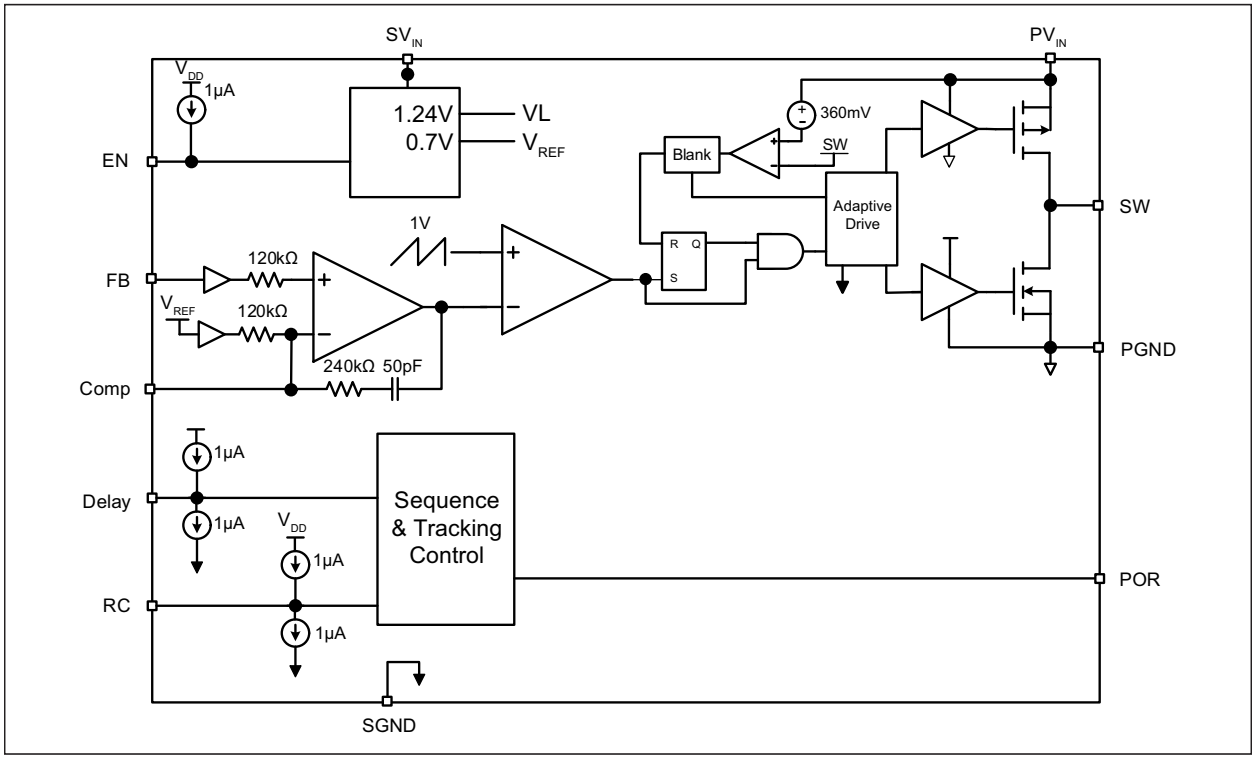
Typical Application Circuit



Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (SV_{IN}, PV_{IN}) ..... –0.3V to +6V
Output Switch Voltage (SW) ..... –0.3V to +6V
Output Switch Current (I_{SW}) ..... Internally Limited
Logic Input Voltage (EN, POR, DELAY) ..... –0.3V to V_{IN}
Control Voltage (RC, COMP, FB) ..... –0.3V to V_{IN}
ESD Rating (Note 1) ..... 2 kV

Operating Ratings ††

Supply Voltage (V_{IN}) ..... +2.6V to +5.5V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions recommended.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: T_A = +25°C with V_{IN} = V_{EN} = 3.3V; V_{OUT} = 1.8V, unless otherwise specified. **Bold** values indicate –40°C≤ T_J ≤ +125°C. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage Range		**2.6**	—	**5.5**	V	—
V_{IN} Turn-On Voltage Threshold		**2.4**	2.5	**2.6**	V	V_{IN} rising
UVLO Hysteresis		—	280	—	mV	—
Quiescent Current, PWM Mode		—	850	**1300**	µA	V_{EN} ≥ 1.34V; V_{FB} = 0.9V (not switching)
Shutdown Current	I_{SHDN}	—	5	**10**	µA	V_{EN} = 0V
Feedback Voltage	V_{FB}	0.693	0.7	0.707	V	±1%
		0.686	0.7	**0.714**	V	±2% (over temperature)
FB Pin Input Current		—	1	100	nA	—
Current Limit in PWM Mode	I_{LIM}	**6.5**	9	**11.5**	A	V_{FB} = 0.5*V_{NOM}
Output Voltage Line Regulation		—	0.2	—	%	V_{OUT} = 1.8V, V_{IN} = 2.6 to 5.5V, I_{LOAD} = 100 mA
Output Voltage Load Regulation		—	0.2	—	%	100 mA < I_{LOAD} < 6000 mA, V_{IN} = 3.3V
Maximum Duty Cycle		100	—	—	%	V_{FB} ≤ 0.5V
Switch ON-Resistance PFET		—	0.03	—	Ω	I_{SW} = 1000 mA; V_{FB} = 0.5V
Switch ON-Resistance NFET		—	0.025	—	Ω	I_{SW} = 1000 mA; V_{FB} = 0.9V
Oscillator Frequency	f_O	0.8	1	1.2	MHz	—
EN/DLY Threshold Voltage		**1.14**	1.24	**1.34**	V	—
EN/DLY Source Current		**0.6**	1	**1.8**	µA	V_{IN} = 2.6V to 5.5V
RC Pin Current	I_{RAMP}	0.5	1	1.7	µA	Ramp Control current

Note 1: Specification for packaged product only.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: T_A = +25°C with V_{IN} = V_{EN} = 3.3V; V_{OUT} = 1.8V, unless otherwise specified. **Bold** values indicate –40°C≤ T_J ≤ +125°C. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Power-on-Reset	$I_{PG(LEAK)}$	—	—	1	µA	V_{PORH} = 5.5V; POR = High
		—	—	**2**	µA	
Power-on-Reset	$V_{PG(LO)}$	—	130	—	mV	Output Logic Low Voltage (undervoltage condition), I_{POR} = 5 mA
Power-on-Reset	V_{PG}	**7.5**	10	**12.5**	%	Threshold,% of V_{OUT} below nominal
		—	2	—	%	Hysteresis
Overtemperature Shutdown		—	160	—	°C	—
Overtemperature Shutdown Hysteresis		—	20	—	°C	—

Note 1: Specification for packaged product only.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	–40	—	+125	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	+260	—	°C	Soldering, 10 sec.
Package Thermal Resistance						
Thermal Resistance, QFN 24-Ld	θ_{JC}	—	14	—	°C/W	—
	θ_{JA}	—	40	—	°C/W	—
Thermal Resistance, TSSOP ePad 24-Ld	θ_{JC}	—	12.9	—	°C/W	—
	θ_{JA}	—	32.2	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

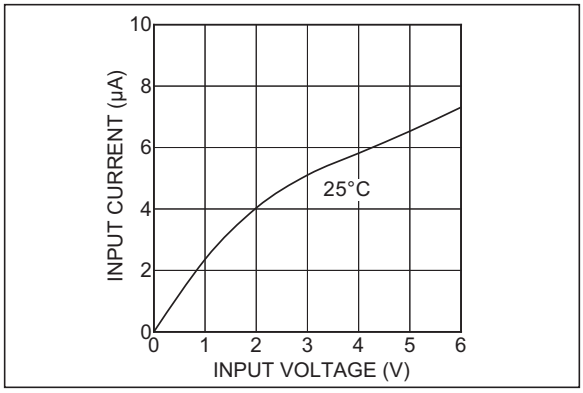

FIGURE 2-1: *Shutdown Current vs. Input Voltage.*

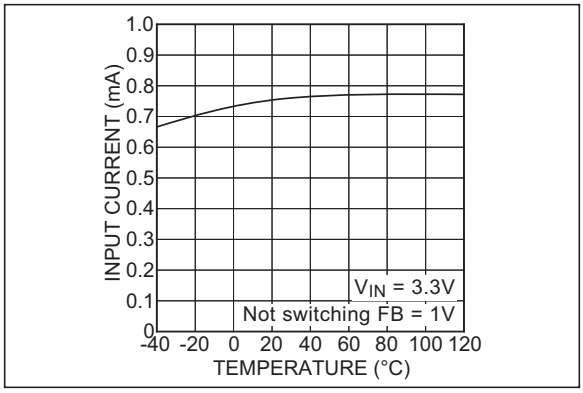

FIGURE 2-4: *Operating Current vs. Temperature.*

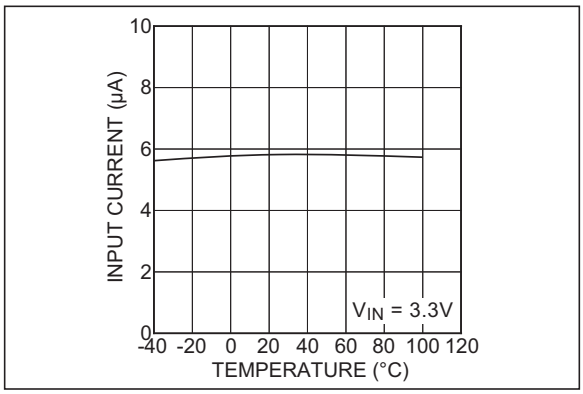

FIGURE 2-2: *Shutdown Current vs. Temperature.*

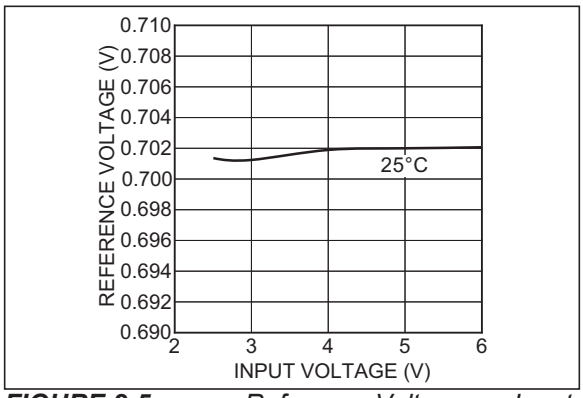

FIGURE 2-5: *Reference Voltage vs. Input Voltage.*

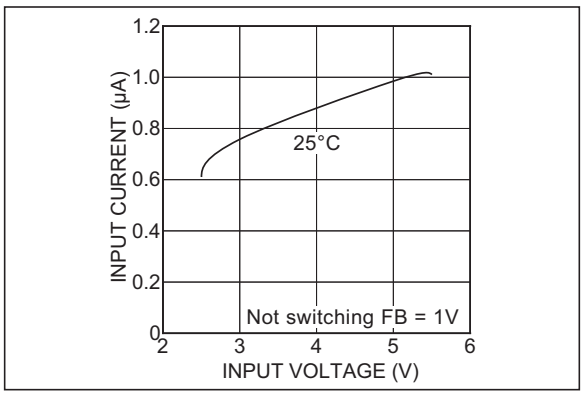

FIGURE 2-3: *Operating Current vs. Input Voltage.*

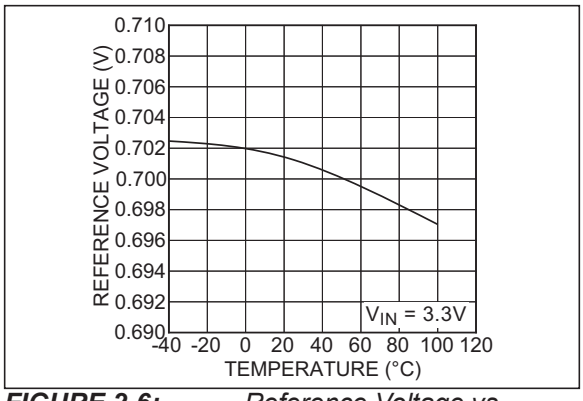

FIGURE 2-6: *Reference Voltage vs. Temperature.*

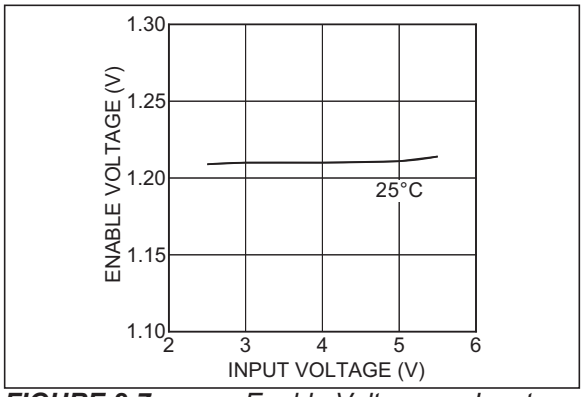

FIGURE 2-7: *Enable Voltage vs. Input Voltage.*

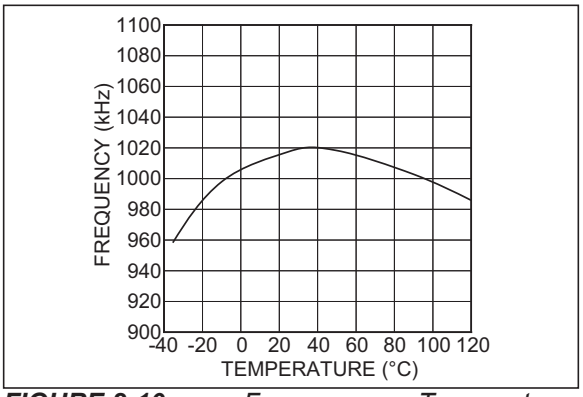

FIGURE 2-10: *Frequency vs. Temperature.*

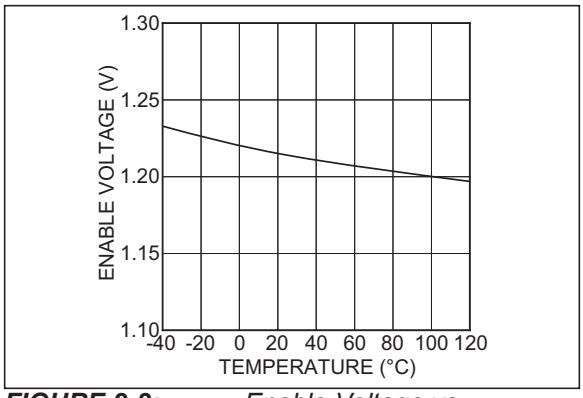

FIGURE 2-8: *Enable Voltage vs. Temperature.*

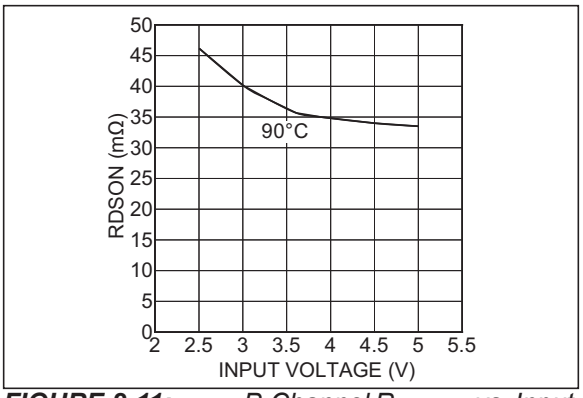

FIGURE 2-11: *P-Channel $R_{DS(ON)}$ vs. Input Voltage.*

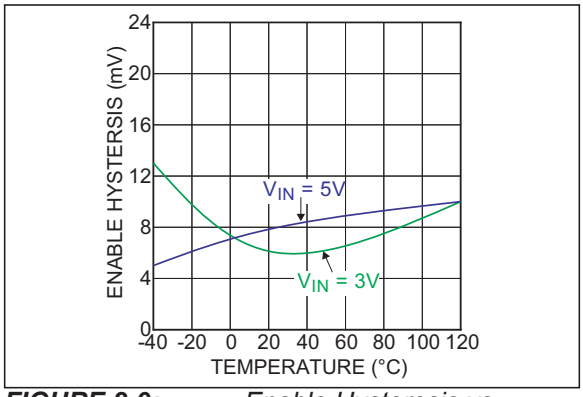

FIGURE 2-9: *Enable Hysteresis vs. Temperature.*

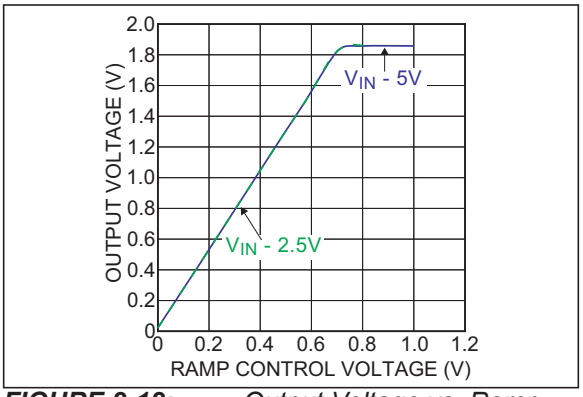

FIGURE 2-12: *Output Voltage vs. Ramp Control Voltage.*

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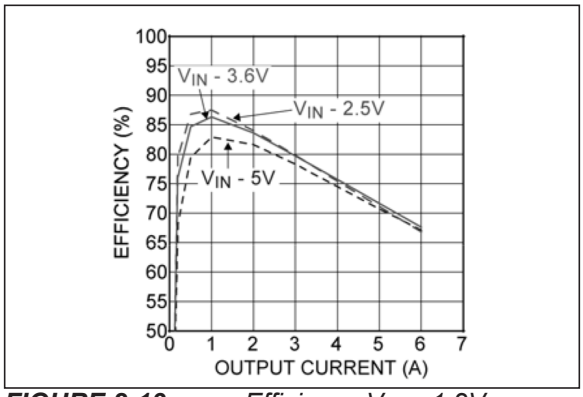

FIGURE 2-13: *Efficiency V_O = 1.2V.*

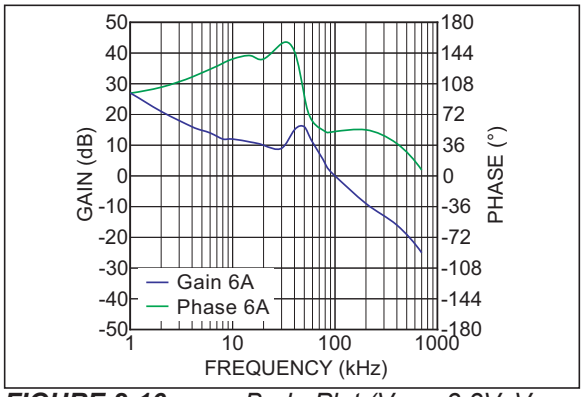

FIGURE 2-16: *Bode Plot (V_{IN} = 3.3V, V_O = 1.8V).*

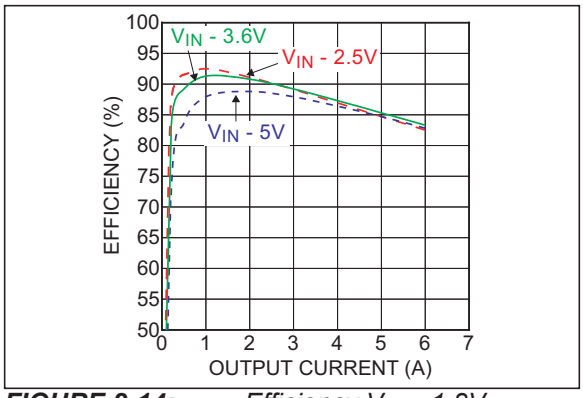

FIGURE 2-14: *Efficiency V_O = 1.8V.*

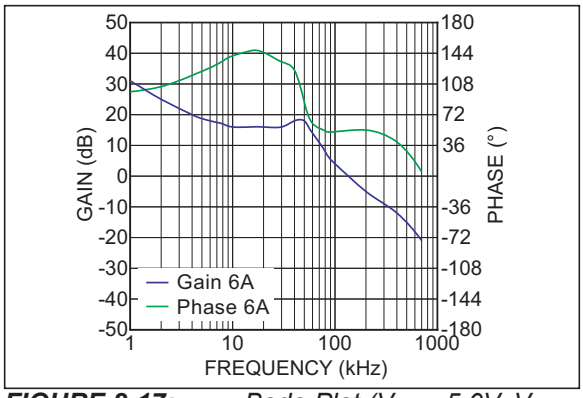

FIGURE 2-17: *Bode Plot (V_{IN} = 5.0V, V_O = 1.8V).*

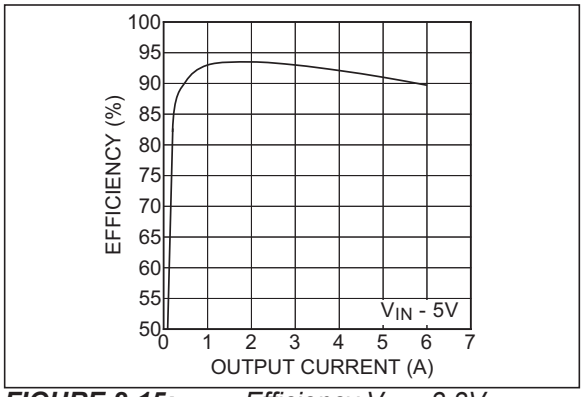

FIGURE 2-15: *Efficiency V_O = 3.3V.*

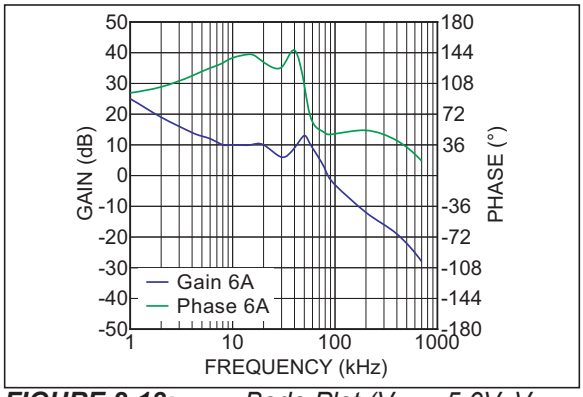

FIGURE 2-18: *Bode Plot (V_{IN} = 5.0V, V_O = 3.3V).*

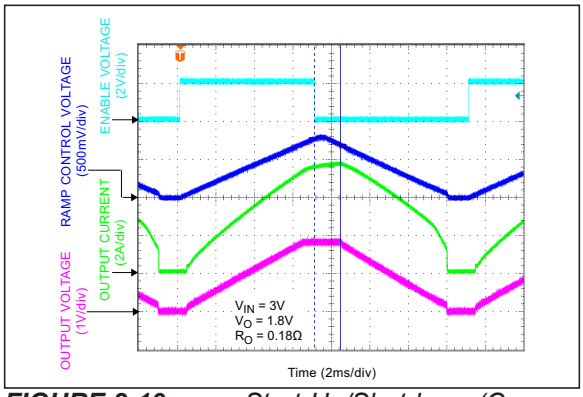

FIGURE 2-19: *Start-Up/Shutdown (C_{RC} = 10 nF).*

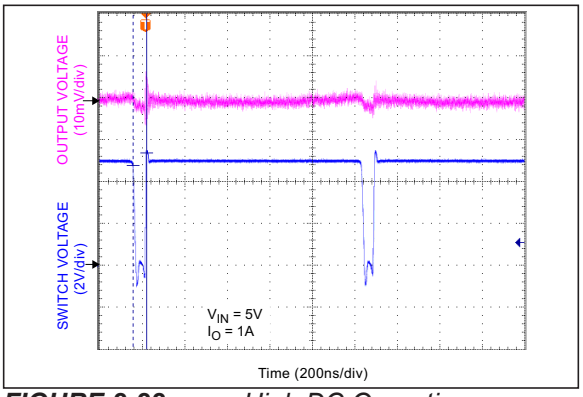

FIGURE 2-22: *High DC Operation.*

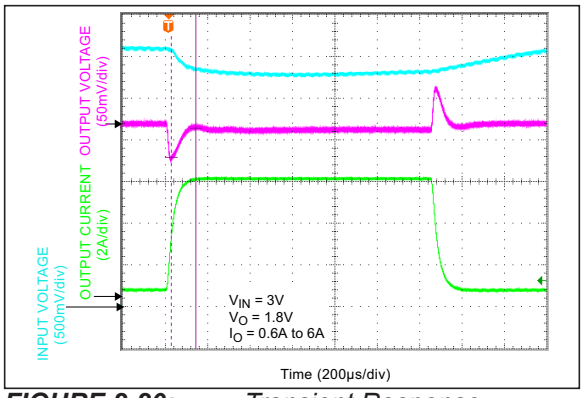

FIGURE 2-20: *Transient Response.*

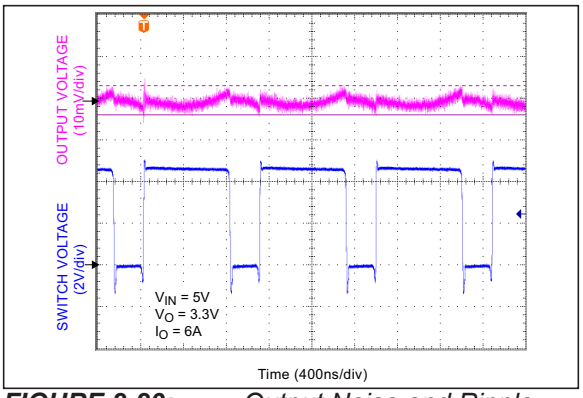

FIGURE 2-23: *Output Noise and Ripple.*

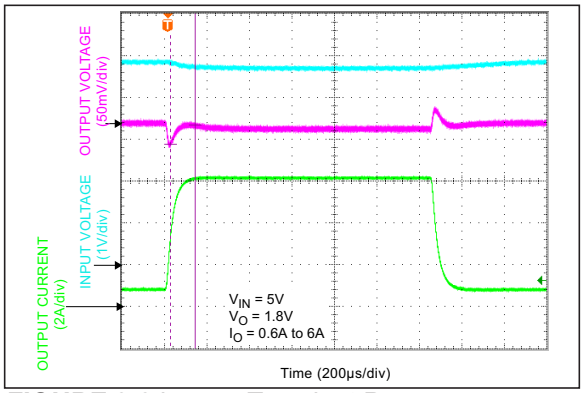

FIGURE 2-21: *Transient Response.*

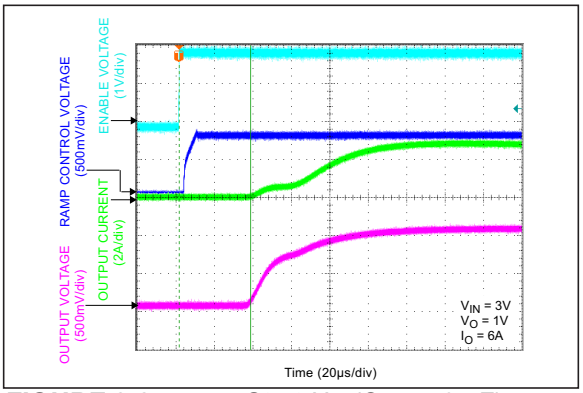

FIGURE 2-24: *Start-Up (C_{RC} = 0 nF).*

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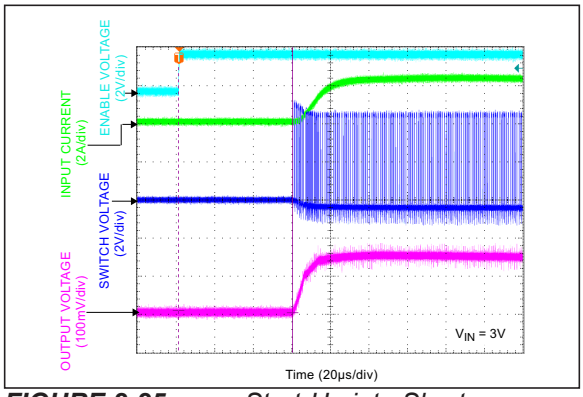

FIGURE 2-25: *Start-Up into Short.*

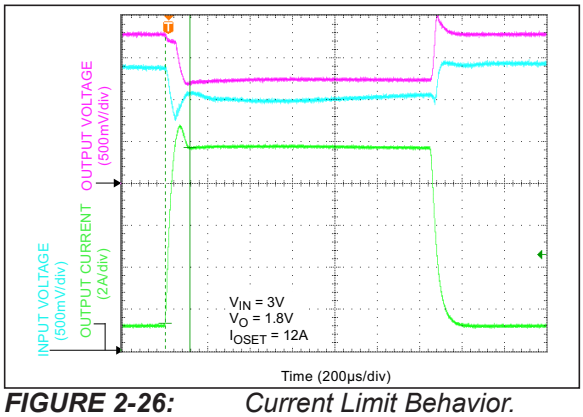

FIGURE 2-26: *Current Limit Behavior.*

Typical Circuits and Waveforms

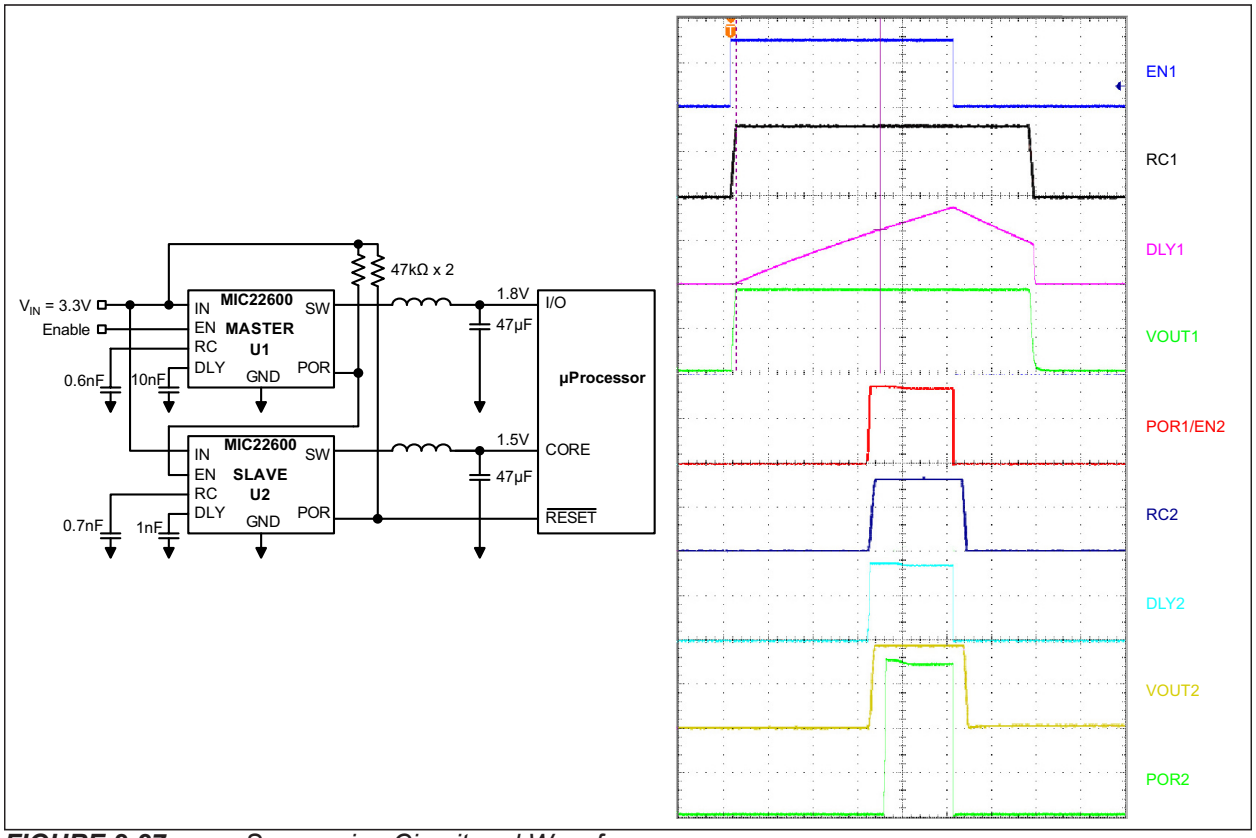

FIGURE 2-27: *Sequencing Circuit and Waveform.*

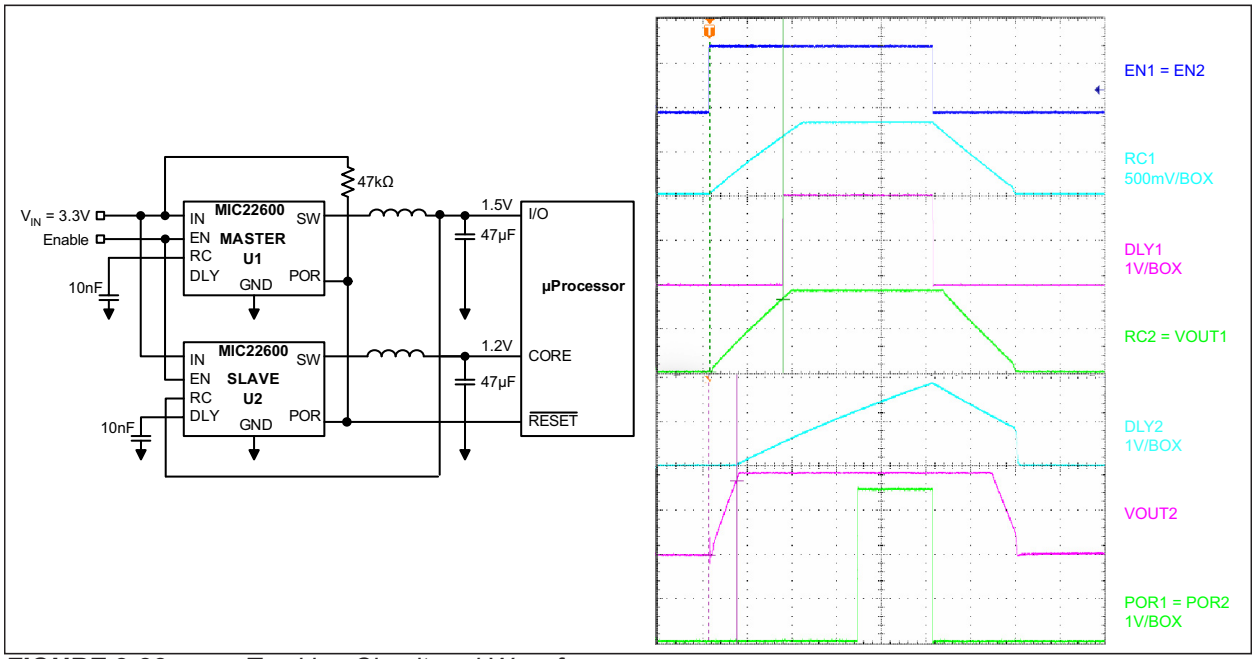

FIGURE 2-28: *Tracking Circuit and Waveform.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number QFN-24	Pin Number TSSOP-24	Pin Name	Description
1, 6, 13, 18	3, 10, 15, 22	PVIN	Power Supply Voltage (Input): Requires bypass capacitor to GND.
17	2	SVIN	Signal Power Supply Voltage (Input): Requires bypass capacitor to GND.
2	11	EN/DLY	EN/DLY (Input): When this pin is pulled higher than the enable threshold, the part will start up. Below this voltage, the device is in its low quiescent current mode. The pin has a 1 µA current source charging it to V_{IN}. By adding a capacitor to this pin a delay may easily be generated. The enable function will not operate with an input voltage lower than the min specified voltage.
4	13	RC	Ramp Control: Capacitor to ground from this pin determines slew rate of output voltage during start-up. This can be used for tracking capability as well as soft start. RC pin cannot be left floating. Use a minimum capacitor value of 220 pF or larger.
14	23	FB	Feedback: Input to the error amplifier, connect to the external resistor divider network to set the output voltage.
15	24	COMP	Compensation pin (Input): Place a RC network to GND to compensate the device, see applications section.
5	14	POR/PG	Power-on-Reset (Output): Open-drain output device indicates when the output is out of regulation and is active after the delay set by the DELAY pin.
7, 12, 19, 24	4, 9, 16, 21	PGND	Power Ground (Signal): Ground
16	1	SGND	Signal Ground (Signal): Ground
3	12	DELAY	DELAY (Input): Capacitor to ground sets internal delay timer. Timer delays power-on-reset (POR) output at turn-on and ramp down at turn-off.
8, 9, 10, 11, 20, 21, 22, 23	5, 6, 7, 8, 17, 18 19, 20	SW	Switch (Output): Internal power MOSFET output switches.
EP	EP	GND	Exposed Pad (Power): Must make a full connection to a GND plane for full output power to be realized.

4.0 FUNCTIONAL DESCRIPTION

4.1 PVIN, SVIN

PVIN is the input supply to the internal 30 mΩ P-Channel Power MOSFET. This should be connected externally to the SVIN pin. The supply voltage range is from 2.6V to 5.5V. A 10 µF ceramic is recommended for bypassing each PVIN supply.

4.2 EN/DLY

This pin is internally fed with a 1 µA current source from VIN. A delayed turn on is implemented by adding a capacitor to this pin. The delay is proportional to the capacitor value. The internal circuits are held off until EN/DLY reaches the enable threshold of 1.24V.

4.3 RC

RC allows the slew rate of the output voltage to be programmed by the addition of a capacitor from RC to ground. RC is internally fed with a 1 µA current source and V_{OUT} slew rate is proportional to the capacitor and the 1 µA source. RC pin cannot be left floating. Use a minimum capacitor value of 220 pF or larger.

4.4 DELAY

Adding a capacitor to this pin allows the delay of the POR signal.

When V_{OUT} reaches 90% of its nominal voltage, the DELAY pin current source (1 µA) starts to charge the external capacitor. At 1.24V, POR is asserted high.

4.5 COMP

The MIC22600 uses an internal compensation network containing a fixed frequency zero (phase lead response) and pole (phase lag response) which allows the external compensation network to be much simplified for stability. The addition of a single capacitor and resistor will add the necessary pole and zero for voltage mode loop stability using low value, low ESR ceramic capacitors.

4.6 FB

The feedback pin provides the control path to control the output. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage. Refer to the feedback section in the “Applications Information” for more detail.

4.7 POR

This is an open-drain output. A 47 kΩ resistor can be used for a pull-up to this pin. POR is asserted high when output voltage reaches 90% of nominal set voltage and after the delay set by C_{DELAY}. POR is asserted low without delay when enable is set low or when the output goes below the –10% threshold. For a Power Good (PG) function, the delay can be set to a minimum. This can be done by removing the DELAY capacitor.

4.8 SW

This is the connection to the drain (see Functional Block Diagram) of the internal P-Channel MOSFET and drain of the N-Channel MOSFET. This is a high frequency, high power connection. Therefore, traces should be kept as short and as wide as practical.

4.9 SGND

Internal signal ground for all low power sections.

4.10 PGND

Internal ground connection to the source of the internal N-Channel MOSFETs.

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5.0 APPLICATION INFORMATION

The MIC22600 is a 6A synchronous step-down regulator IC with a fixed 1 MHz, voltage mode PWM control scheme. The other features include tracking and sequencing control for controlling multiple output power systems, and power-on-reset.

5.1 Input Capacitor

A minimum 10 µF ceramic is recommended on each of the PVIN pins for bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics is not recommended.

5.2 Output Capacitor

The MIC22600 was designed specifically for the use of ceramic output capacitors and 22 µF is optimum output capacitor. 22 µF can be increased to 100 µF to improve transient performance. Because the MIC22600 is a voltage mode controller, the control loop relies on the inductor and output capacitor for compensation. For this reason, do not use excessively large output capacitors. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from the undesirable effect of their wide variation in capacitance over temperature, become resistive at high frequencies. Using Y5V or Z5U capacitors can cause instability in the MIC22600.

5.3 Inductor Selection

Inductor selection will be determined by the following (not necessarily in the order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC22600 is designed to use a 0.47 µH to 4.7 µH inductor.

Maximum current ratings of the inductor are generally given in two methods: permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor. The ripple can add as much as 1.2A to the output current level. The RMS rating should be chosen to be equal or greater than the current limit of the MIC22600 to prevent overheating in a fault condition. For best electrical performance, the inductor should be placed very close to the SW nodes of the IC.

It is important to test all operating limits before settling on the final inductor choice.

The size requirements refer to the area and height requirements that are necessary to fit a particular design. Please refer to the inductor dimensions on their data sheet.

DCR is inversely proportional to size and can represent a significant efficiency loss. Refer to the Efficiency Considerations section for a more detailed description.

5.4 EN/DLY Capacitor

EN/DLY sources 1 µA out of the IC to allow a startup delay to be implemented. The delay time is simply the time it takes 1 µA to charge C_{DLY} to 1.24V. Therefore:

EQUATION 5-1:

$$t_{DLY} = \frac{1.24 \times C_{DLY}}{1.10^{-6}}$$

5.5 Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power consumed.

EQUATION 5-2:

$$Efficiency\ \% = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}\right) \times 100$$

Maintaining high efficiency serves two purposes. It decreases power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it decreases consumption of current for battery powered applications. Reduced current drawn from a battery increases the devices operating time, particularly in hand-held devices.

There are mainly two loss terms in switching converters: conduction losses and switching losses. Conduction losses are simply the power losses due to VI or I^2R. For example, power is dissipated in the high side switch during the on cycle. The power loss is equal to the high-side MOSFET $R_{DS(ON)}$ multiplied by the RMS Switch Current squared (I_{SW}^2). During the off cycle, the low-side N-Channel MOSFET conducts, also dissipating power. Similarly, the inductor's DCR and capacitor's ESR also contribute to the I^2R losses. Device operating current also reduces efficiency by the product of the quiescent (operating) current and the supply voltage. The power consumed at 1 MHz frequency and power loss due to switching transitions

add up to switching losses. A free wheeling Schottky diode is recommended to use in parallel with synchronous N-MOSFET to improve the efficiency.

Figure 5-1 shows an efficiency curve. In the portion from 0A to 1A, efficiency losses are dominated by quiescent current losses, gate drive, and transition losses. In this case, lower supply voltages yield greater efficiency in that they require less current to drive the MOSFETs and have reduced input power consumption.

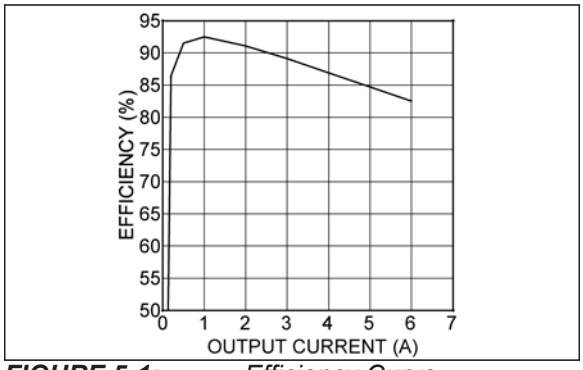

FIGURE 5-1: *Efficiency Curve.*

In the region of 1A to 6A, efficiency loss is dominated by MOSFET $R_{DS(ON)}$ and inductor DC losses. Higher input supply voltages will increase the Gate-to-Source voltage on the internal MOSFETs, reducing the internal $R_{DS(ON)}$. This improves efficiency by decreasing conduction loss in the device but the inductor DCR loss is inherent to the device. Inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

EQUATION 5-3:

$$L_{PD} = I_{OUT}^{2} \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as in Equation 5-4.

EQUATION 5-4:

$$EL = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{(V_{OUT} \times I_{OUT}) + L_{PD}}\right)\right] \times 100$$

Where:
EL = Efficiency loss value in percent.

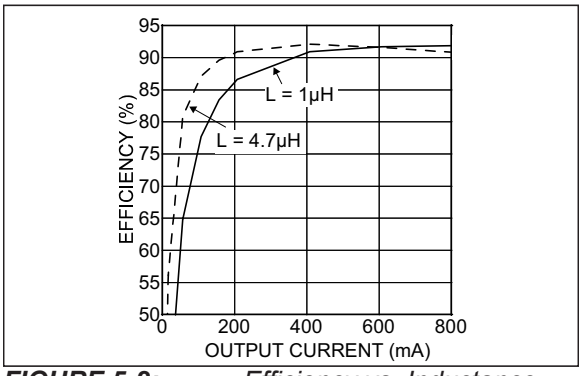

FIGURE 5-2: *Efficiency vs. Inductance.*

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

Alternatively, under lighter loads, the ripple current becomes a significant factor. When light load efficiencies become more critical, a larger inductor value maybe desired. Larger inductance reduces the peak-to-peak inductor ripple current, which minimizes losses. The graph in Figure 5-2 illustrates the effects of inductance value at light load.

5.6 Compensation

The MIC22600 has a combination of internal and external stability compensation to simplify the circuit for small, high efficiency designs. In such designs, voltage mode conversion is often the optimum solution. Voltage mode is achieved by creating an internal 1 MHz ramp signal and using the output of the error amplifier to modulate the pulse width of the switch node, thereby maintaining output voltage regulation. With a typical gain bandwidth of 100 kHz to 200 kHz, the MIC22600 is capable of extremely fast transient responses.

The MIC22600 is designed to be stable with a typical application using a 1 µH inductor and a 47 µF ceramic (X5R) output capacitor. These values can be varied dependent upon the trade off between size, cost and efficiency, keeping the LC natural frequency ideally less than 26 kHz to ensure stability can be achieved. The minimum recommended inductor value is 0.47 µH and minimum recommended output capacitor value is 22 µF. With a larger inductor, there is a reduced peak-to-peak current that yields a greater efficiency at lighter loads. A larger output capacitor will improve transient response by providing a larger hold up reservoir of energy to the output.

The integration of one pole-zero pair within the control loop greatly simplifies compensation. The optimum values for C_{COMP} (in series with a 20 kΩ resistor) are shown below.

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TABLE 5-1: COMPENSATION CAPACITOR SELECTION

L	C		
	22 µF - 47 µF	**47 µF - 100 µF**	**100 µF - 470 µF**
0.47 µH	0 pF - 10 pF (Note 1)	22 pF	33 pF
1 µH	0 pF - 15 pF (Note 2)	15 pF - 22 pF	33 pF
2.2 µH	15 pF - 33 pF	33 pF - 47 pF	100 pF - 220 pF

Note 1: V_{OUT} > 1.2V
2: V_{OUT} > 1V

5.7 Feedback

The MIC22600 provides a feedback pin to adjust the output voltage to the desired level. This pin connects internally to an error amplifier. The error amplifier then compares the voltage at the feedback to the internal 0.7V reference voltage and adjusts the output voltage to maintain regulation. The resistor divider network for a desired V_{OUT} is given by:

EQUATION 5-5:

$$R2 = \frac{R1}{\left(\frac{V_{OUT}}{V_{REF}} - 1\right)}$$

Where:
V_{REF} = 0.7V
V_{OUT} = The desired output voltage.

A 10 kΩ or lower resistor value from the output to the feedback is recommended because large feedback resistor values increase the impedance at the feedback pin, making the feedback node more susceptible to noise pick-up. A small capacitor (50 pF to 100 pF) across the lower resistor can reduce noise pick-up by providing a low impedance path to ground.

5.8 PWM Operation

The MIC22600 is a voltage mode, pulse width modulation (PWM) controller. By controlling the duty cycle, a regulated DC output voltage is achieved. As load or supply voltage changes, so does the duty cycle to maintain a constant output voltage. In cases where the input supply runs into a dropout condition, the MIC22600 will run at 100% duty cycle.

The MIC22600 provides constant switching at 1 MHz with synchronous internal MOSFETs. The internal MOSFETs include a high-side P-Channel MOSFET from the input supply to the switch pin and an N-Channel MOSFET from the switch pin-to-ground. Since the low-side N-Channel MOSFET provides the current during the off cycle, a freewheeling Schottky diode from the switch node-to-ground is not required.

PWM control provides fixed-frequency operation. By maintaining a constant switching frequency, predictable fundamental and harmonic frequencies are achieved.

5.9 Sequencing and Tracking

The MIC22600 provides additional pins to provide up/down sequencing and tracking capability for connecting multiple voltage regulators together.

5.9.1 EN/DLY PIN

The EN pin contains a trimmed, 1 µA current source that can be used with a capacitor to implement a fixed desired delay in some sequenced power systems. The threshold level for power on is 1.24V with a hysteresis of 20 mV.

5.9.2 DELAY PIN

The DELAY pin also has a 1 µA trimmed current source and a 1 µA current sink that acts with an external capacitor to delay the operation of the Power-on-Reset (POR) output. This can be used also in sequencing outputs in a sequenced system, but with the addition of a conditional delay between supplies; allowing a first up, last down power sequence.

After EN is driven high, V_{OUT} will start to rise (rate determined by RC capacitor). As the FB voltage goes above 90% of its nominal set voltage, DELAY begins to rise as the 1 µA source charges the external capacitor. When the threshold of 1.24V is crossed, POR is asserted high and DELAY continues to charge to a voltage SV_{IN}. When FB falls below 90% of nominal, POR is asserted low immediately. However, if EN is driven low, POR will fall immediately to the low state and DELAY will begin to fall as the external capacitor is discharged by the 1 µA current sink. When the threshold of ((V_{TP} + 1.24V) – 1.24V) is crossed (V_{TP} is the internal voltage clamp, V_{TP} = 0.9V), V_{OUT} will begin to fall at a rate determined by the RC capacitor. As the voltage change in both cases is 1.24V, both rising and falling delays are matched at:

EQUATION 5-6:

$$t_{POR} = \frac{1.24 \times C_{DLY}}{1.10^{-6}}$$

5.9.3 RC PIN

The RC pin provides a trimmed 1 µA current source/sink similar to the DELAY pin for accurate ramp-up (soft-start) and ramp-down control. This allows the MIC22600 to be used in systems requiring voltage tracking or ratio-metric voltage tracking at startup.

There are two ways of using the RC pin:

- Externally driven from a voltage source
- Externally attached capacitor sets output ramp up/down rate

In the first case, driving RC with a voltage from 0V to V_{REF} programs the output voltage between 0% and 100% of the nominal set voltage.

In the second case, the external capacitor sets the ramp up and ramp down time of the output voltage. The time is given by:

EQUATION 5-7:

$$t_{RAMP} = \frac{0.7 \times C_{RC}}{1.10^{-6}}$$

Where:

t_{RAMP} = The time from 0% to 100% nominal output voltage.

The RC pin cannot be left floating. Use a minimum capacitor value of 220 pF or larger.

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5.9.4 SEQUENCING AND TRACKING EXAMPLES

There are four distinct variations that are easily implemented using the MIC22600. The two sequencing variations are Delayed and Windowed. The two tracking variants are Normal and Ratio Metric. The following diagrams illustrate methods for connecting two MIC22600's to achieve these requirements.

Sequencing

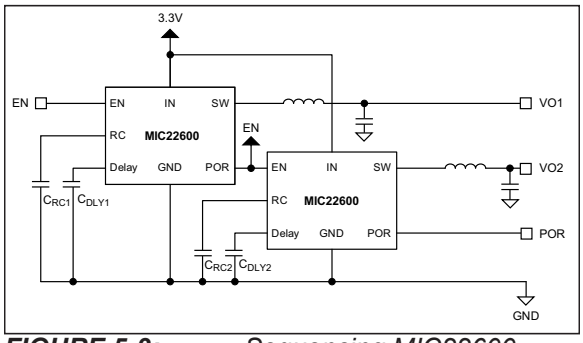

FIGURE 5-3: *Sequencing MIC22600 Circuit.*

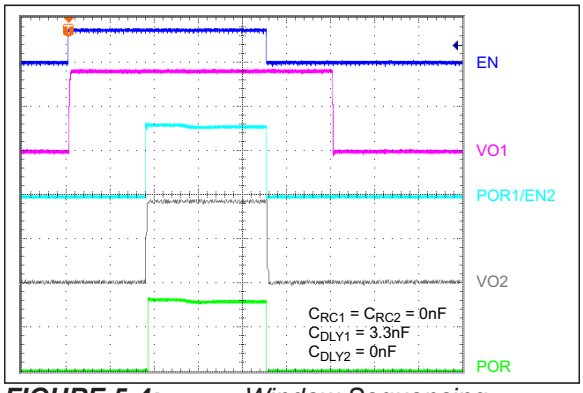

FIGURE 5-4: *Window Sequencing Example.*

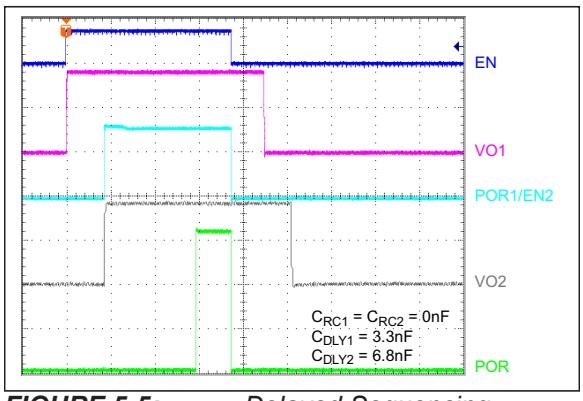

FIGURE 5-5: *Delayed Sequencing Example.*

Normal Tracking

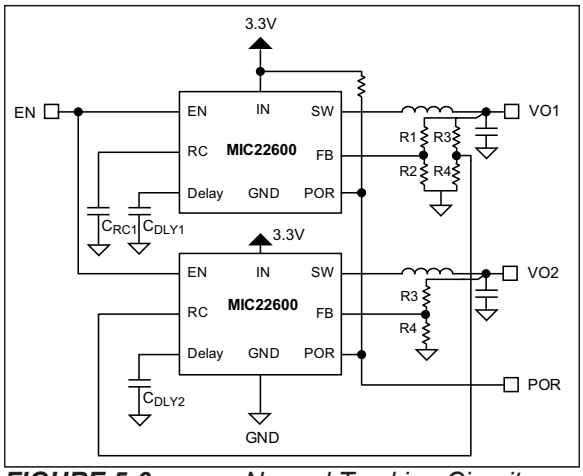

FIGURE 5-6: *Normal Tracking Circuit.*

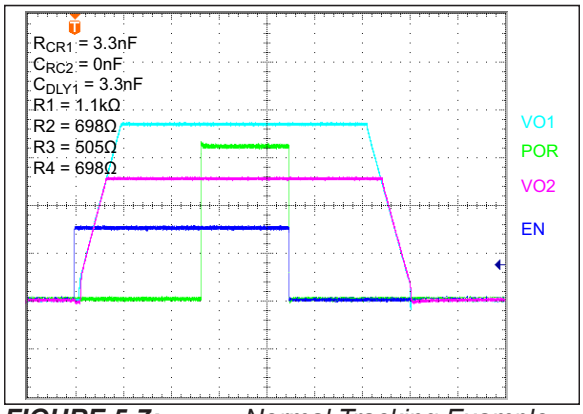

FIGURE 5-7: *Normal Tracking Example.*

Ratio Metric Tracking

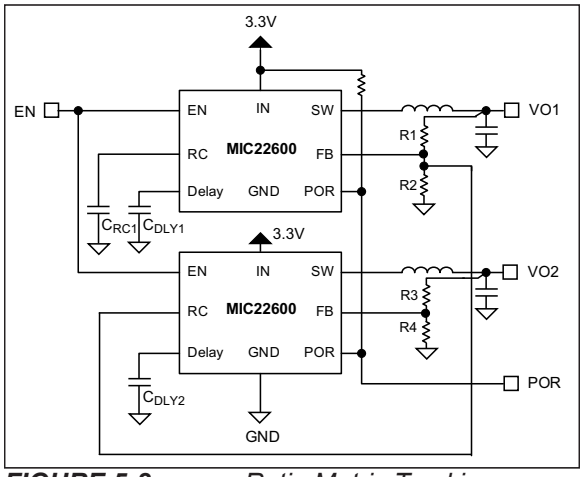

FIGURE 5-8: *Ratio Metric Tracking Circuit.*

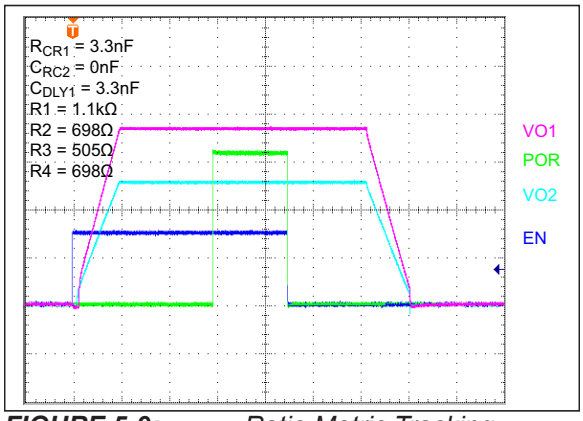

FIGURE 5-9: *Ratio Metric Tracking Example.*

DDR Memory V_{DD} and V_{TT} Tracking

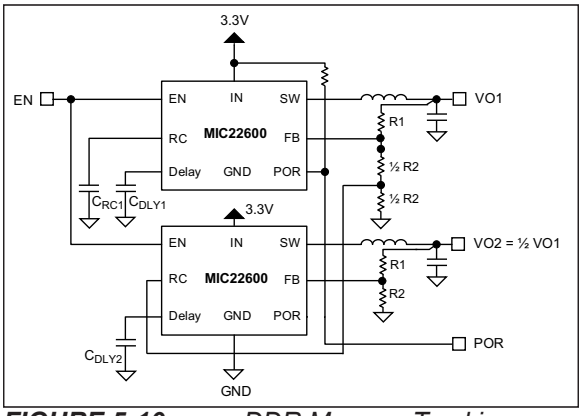

FIGURE 5-10: *DDR Memory Tracking Circuit.*

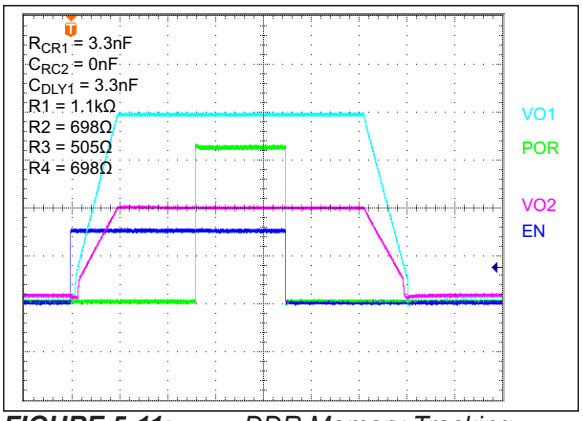

FIGURE 5-11: *DDR Memory Tracking Example.*

An alternative method here shows an example of a V_{DDQ} & V_{TT} solution for a DDR memory power supply. Note that POR is taken from VO1 as POR2 will not go high. This is because POR is set high when FB > 0.9 x V_{REF}. In this example, FB2 is regulated to ½V_{REF}.

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5.10 Current Limit

The MIC22600 is protected against overload in two stages. The first is to limit the current in the P-channel switch; the second is by overtemperature shutdown.

Current is limited by measuring the current through the high-side MOSFET during its power stroke and immediately switching off the driver when the preset limit is exceeded.

The circuit in Figure 5-12 describes the operation of the current-limit circuit. Because the actual $R_{DS(ON)}$ of the P-Channel MOSFET varies part-to-part, over temperature and with input voltage, simple IR voltage detection is not employed. Instead, a smaller copy of the Power MOSFET (Reference FET) is fed with a constant current that is directly proportional to the factory set current limit. This sets the current limit as a current ratio and is not dependent upon the $R_{DS(ON)}$ value. Current limit is set to 9A nominal. Variations in the scale factor K between the Power PFET and the reference PFET used to generate the limit threshold account for a relatively small inaccuracy.

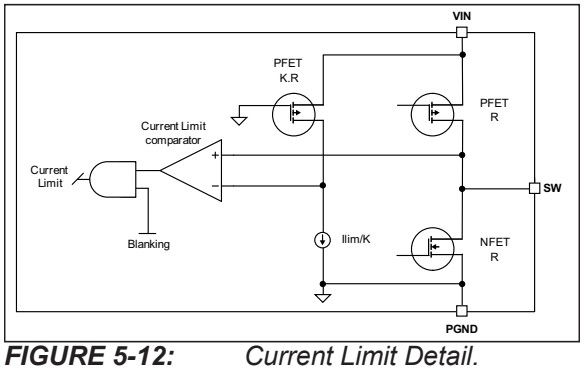

FIGURE 5-12: *Current Limit Detail.*

5.11 Thermal Considerations

The MIC22600 is packaged in a 4 mm x 4 mm QFN, a package that has excellent thermal performance equaling that of the larger TSSOP packages. This maximizes heat transfer from the junction to the exposed pad (ePad) that connects to the ground plane. The size of the ground plane attached to the exposed pad determines the overall thermal resistance from the junction to the ambient air surrounding the printed circuit board. The junction temperature for a given ambient temperature can be calculated using:

EQUATION 5-8:

$$T_J = T_A + P_{DISS} \times R\theta_{JA}$$

Where:

P_{DISS} = The power dissipated within the QFN package and is typically 1.5W at 6A load. This has been calculated for a 1 µH inductor and details can be found in Table 5-2 for reference.

$R\theta_{JA}$ = A combination of junction to case thermal resistance ($R\theta_{JC}$) and Case-to-Ambient thermal resistance ($R\theta_{CA}$), since thermal resistance of the solder connection from the ePad to the PCB is negligible; $R\theta_{CA}$ is the thermal resistance of the ground plane to ambient, so $R\theta_{JA} = R\theta_{JC} + R\theta_{CA}$.

T_A = The operating ambient temperature.

Example:

The Evaluation Board has two copper planes that contribute to an $R\theta_{JA}$ of approximately 25°C/W. The worst case $R\theta_{JC}$ of the QFN 4x4 is 14°C/W.

EQUATION 5-9:

$$R\theta_{JA} = R\theta_{JC} + R\theta_{CA}$$

$$R\theta_{JA} = 14°C/W + 25°C/W = 39°C/W$$

To calculate the junction temperature for a 50°C ambient:

EQUATION 5-10:

$$T_J = T_A + (P_{DISS} \times R\theta_{JA})$$

$$T_J = 50°C + (1.5W \times 39°C/W)$$

$$T_J = 108.5°C$$

This is below the maximum of 125°C.

TABLE 5-2: POWER DISSIPATION FOR 6A OUTPUT

V_{OUT} at 6A	V_{IN}				
	3V	3.5V	4V	4.5V	5V
1V	1.47W	1.50W	1.52W	1.54W	1.56W
1.2V	1.45W	1.47W	1.49W	1.51W	1.54W
1.8V	1.46W	1.45W	1.45W	1.47W	1.48W
2.5V	1.61W	1.53W	1.49W	1.47W	1.47W
3.3V	—	1.70W	1.62W	1.56W	1.53W

6.0 RIPPLE MEASUREMENTS

To properly measure ripple on either input or output of a switching regulator, a proper ring in tip measurement is required. Standard oscilloscope probes come with a grounding clip, or a long wire with an alligator clip. Unfortunately, for high-frequency measurements, this ground clip can pick up high frequency noise and erroneously inject it into the measured output ripple.

The standard evaluation board accommodates a home made version by providing probe points for both the input and output supplies and their respective grounds. This requires the removing of the oscilloscope probe sheath and ground clip from a standard oscilloscope probe and wrapping a non-shielded bus wire around the oscilloscope probe. If there does not happen to be any non-shielded bus wire immediately available, the leads from axial resistors will work. By maintaining the shortest possible ground lengths on the oscilloscope probe, true ripple measurements can be obtained.

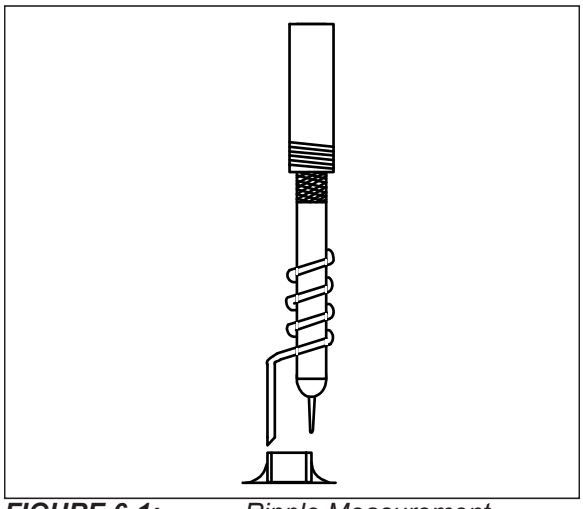

FIGURE 6-1: *Ripple Measurement.*

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PCB Layout Guidelines

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to ensure proper operation of the MIC22600 converter.

IC

- Place the IC close to the point of load (POL).
- Use fat traces to route the input and output power lines.
- The exposed pad (EP) on the bottom of the IC must be connected to the ground.
- Use several vias to connect the EP to the ground plane, layer 2.
- Signal and power grounds should be kept separate and connected at only one location.

Input Capacitor

- Place the input capacitor next.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Place a 22 µF/6.3V ceramic bypass capacitor next to each of the 4 PVIN pins.
- Keep both the VIN and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal, but not between the input capacitors and IC pins.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply when power is suddenly applied.

Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- To minimize noise, place a ground plane underneath the inductor.

Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

Diode

- Place the Schottky diode on the same side of the board as the IC and input capacitor.
- The connection from the Schottky diode’s Anode to the input capacitors ground terminal must be as short as possible.
- The diode’s Cathode connection to the switch node (SW) must be keep as short as possible.

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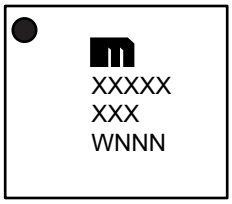
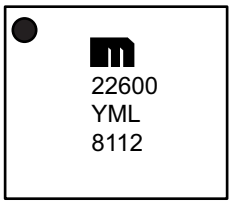
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

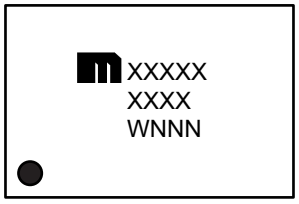
24-Lead QFN*



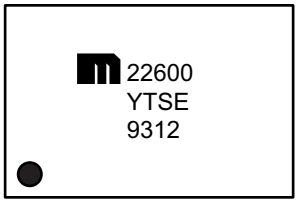
Example



24-Lead TSSOP*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

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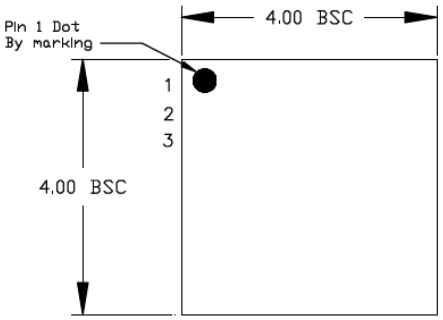
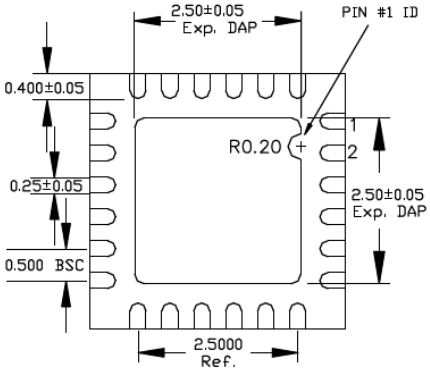
24-Lead QFN 4 mm x 4 mm Package Outline and Recommended Land Pattern

TITLE
24 LEAD QFN 4x4mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	QFN44-24LD-PL-1	UNIT	MM

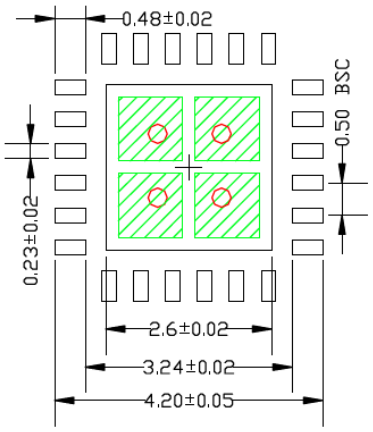


TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3

SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE: 4, 5

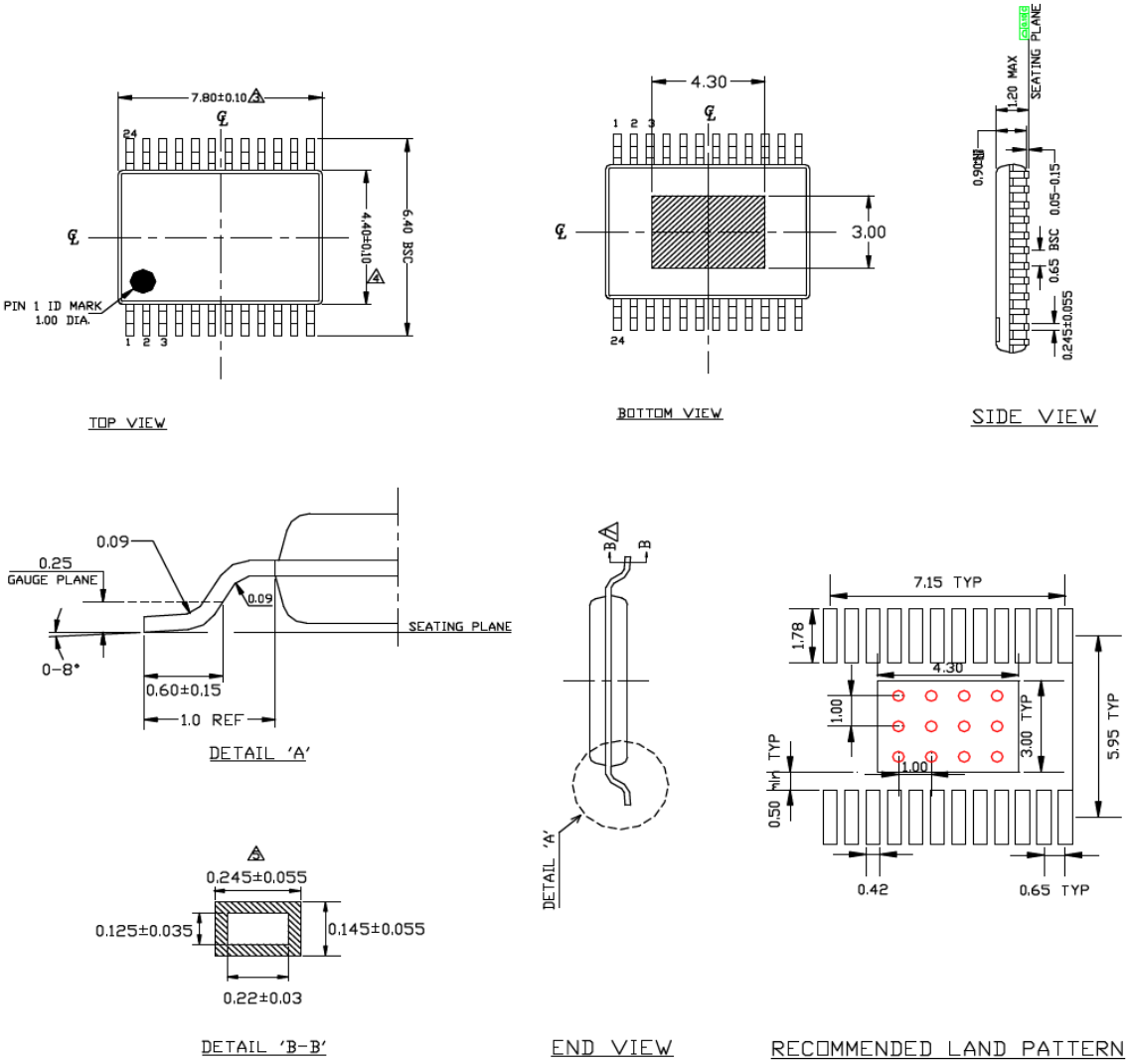
NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) Indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 1.00x1.00 MM IN SIZE, 1.20 MM PITCH.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

24-Lead TSSOP ePad Package Outline and Recommended Land Pattern

TITLE
24 LEAD TSSOP EPAD (4.3x3.0 EPAD) PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TSSOPEP-24LD-PL-1	UNIT	MM (INCH)



NOTE:
1. RED CIRCLES IN LAND PATTERN REPRESENT THERMAL VIAS. RECOMMENDED SIZE IS 0.30-0.35MM IN DIAMETER, 1.00 PITCH AND SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE
2. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS & BURR

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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APPENDIX A: REVISION HISTORY

Revision A (January 2020)

- Converted Micrel document MIC22600 to Microchip data sheet template DS20006288A.
- Minor grammatical text changes throughout.
- Evaluation Board Schematic, BOM, and PCB Layout sections from original data sheet moved to the part's Evaluation Board User's Guide.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	X	XX	-XX
Part No.	Junction Temp. Range	Package	Media Type

Device:	MIC22600:	1 MHz, 6A Integrated Switch Synchronous Buck Regulator
Junction Temperature Range:	Y =	–40°C to +125°C, RoHS-Compliant
Package:	ML =	24-Lead 4 mm x 4 mm QFN
	TSE =	24-Lead ePad TSSOP
Media Type:	<blank>=	62/Tube (TSSOP Package Only)
	TR =	2,500/Reel (TSSOP Package Only)
	TR =	5,000/Reel (QFN Package Only)

Examples:

a) MIC22600YML-TR: MIC22600, Adj. Output Voltage, –40°C to +125°C Temperature Range, 24-Lead QFN, 5,000/Reel

b) MIC22600YTSE: MIC22600, Adj. Output Voltage, –40°C to +125°C Temperature Range, 24-Lead TSSOP, 62/Tube

c) MIC22600YTSE-TR: MIC22600, Adj. Output Voltage, –40°C to +125°C Temperature Range, 24-Lead TSSOP, 2,5000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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