VCA2617



SBOS326 −AUGUST 2005

Dual, Variable Gain Amplifier

FEATURES

- **INDEPENDENT CHANNEL CONTROLS:**
  - **Gain Range: 48dB**
  - **Clamping Levels**
  - **Post-Gain: 0, +6dB**
- **LOW NOISE: 4.1nV/√Hz**
- **LOW POWER: 52mW/Channel**
- **BANDWIDTH: 50MHz**
- **HARMONIC DISTORTION: −53dBc at 5MHz**
- **CROSSTALK: −61dB at 5MHz**
- **5V SINGLE SUPPLY**
- **POWER-DOWN MODE**
- **SMALL QFN-32 PACKAGE (5x5mm)**

APPLICATIONS

- **MEDICAL AND INDUSTRIAL ULTRASOUND SYSTEMS**
  - **Suitable for 10-Bit and 12-Bit Systems**
- **TEST EQUIPMENT**
- **SONAR**

DESCRIPTION

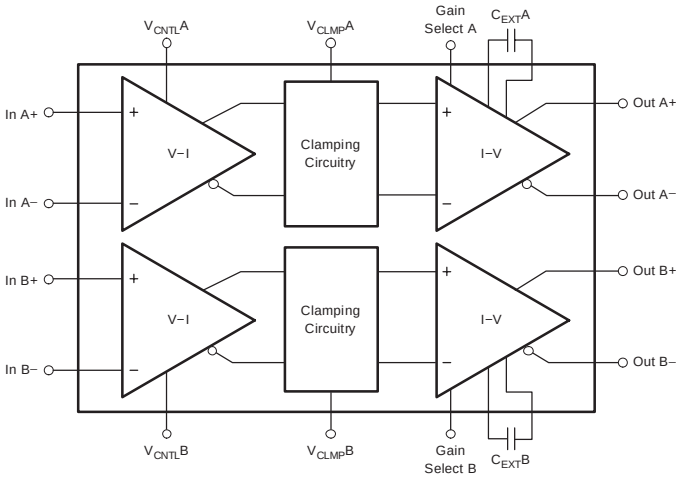
The VCA2617 is a dual-channel, continuously variable, voltage-controlled gain amplifier well-suited for a variety of ultrasound systems as well as applications in proximity detectors and test equipment. The VCA2617 uses a true variable-gain amplifier architecture, achieving very good noise performance at low gains, while not sacrificing high gain distortion performance.

Following a linear-in-dB response, the VCA2617 gain can be varied over a 48dB range with a 0.2V to 2.3V control voltage. Two separate high-impedance control inputs allow for a channel independent variation of the gains. Each channel of the VCA2617 can be configured to provide a gain range of −10dB to 38dB, or −16dB to 32dB, depending on the gain select pin ($\overline{HG}$). This post-gain feature allows the user to optimize the output swing of VCA2617 for a variety of high-speed analog-to-digital converters (ADC). As a means to improve system overload recovery time, the VCA2617 also provides an internal clamping circuitry where an externally applied voltage sets the desired output clamping level.

The VCA2617 operates on a single +5V supply while consuming only 52mW per channel. It is available in a small QFN-32 package (5x5mm).

RELATED PRODUCTS

PART NUMBER	DESCRIPTION
VCA2615	Dual, Low-Noise, Variable-Gain Amplifier with Preamp



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ABSOLUTE MAXIMUM RATINGS(1)

Power Supply (V_{DD})	+6V
VCA2617 Analog Input	−0.3V to (+V_S + 0.3V)
Logic Input	−0.3V to (+V_S + 0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	−40°C to +150°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage. Exposure to absolute maximum conditions for extended periods may affect device reliability.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
VCA2617	QFN−32	RHB	−40°C to +85°C	VCA2617	VCA2617RHBT	Tape and Reel, 250
					VCA2617RHBR	Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

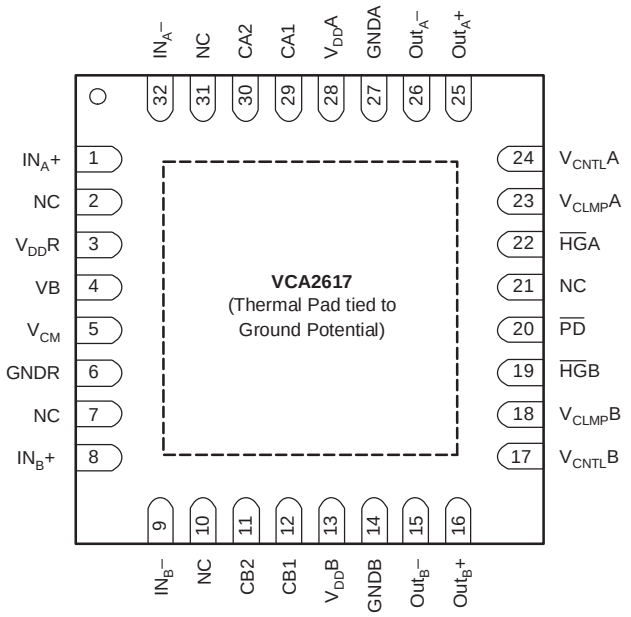
ELECTRICAL CHARACTERISTICS

All specifications at T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground, differential output ($1V_{PP}$), CA, CB = 3.9µF, single-ended input configuration, f_{IN} = 5MHz, $\overline{HG}$ = Low (High-Gain Mode), V_{CNTL} = 2.3V, unless otherwise noted.

PARAMETER	CONDITIONS	VCA2617 MIN	VCA2617 TYP	VCA2617 MAX	UNIT
VARIABLE GAIN AMPLIFIER					
Input Resistance	Single-Ended		300		kΩ
Input Capacitance			8		pF
Maximum Input Voltage	Linear Operation(1); Each Input				
Differential			2.0		V_{PP}
Single-Ended			1.0		V_{PP}
Input Voltage Noise	Gain = 45dB, R_S = 0Ω		4.1		$nV/\sqrt{Hz}$
Input Current Noise	Independent of Gain		1		$pA/\sqrt{Hz}$
Noise Figure			13.3		dB
Input Common-Mode Voltage	Internal		2.5		V
Bandwidth			50		MHz
Clipping Voltage Range (V_{CLMP})			0.25 to 2.6		V
Clipping Voltage Variation	V_{CLMP} = 0.5V, VCA_{OUT} = $1.0V_{PP}$		±75		mV
Maximum Capacitive Output Loading	50Ω in Series		80		pF
Slew Rate			100		V/µs
Maximum Output Signal(1)			6		V_{PP}
Output Common-Mode Voltage			2.5		V
Output Impedance	at 5MHz, Single-Ended, Either Output		3		Ω
Output Short-Circuit Current			60		mA
2nd-Harmonic Distortion	V_{OUT} = $1V_{PP}$, V_{CNTL} = 1.5V	−43	−53		dBc
3rd-Harmonic Distortion	V_{OUT} = $1V_{PP}$, V_{CNTL} = 1.5V	−43	−62		dBc
Overload Distortion (2nd-Harmonic)	Input Signal = $1V_{PP}$, V_{CNTL} = 2V		−40		dBc
Crosstalk			−61		dB
Delay Matching			±1		ns
ACCURACY					
Gain Slope	V_{CNTL} = 0.4V to 2.0V		22		dB/V
Gain Error(2)	V_{CNTL} = 0.4V to 2.0V	−2	±0.9	+2	dB
Gain Range	V_{CNTL} = 0.2V to 2.3V		48		dB
	V_{CNTL} = 0.4V to 2.0V		35.5		dB
Gain Range ($\overline{HG}$)	$\overline{HG}$ = 0 (+6dB); VGA High Gain; V_{CNTL} = 0.2V to 2.3V		−10 to +38		dB
	$\overline{HG}$ = 1 (0dB); VGA Low Gain; V_{CNTL} = 0.2V to 2.3V		−16 to +32		dB
Output Offset Voltage, Differential			±50		mV
Channel-to-Channel Gain Matching	V_{CNTL} = 0.4V to 2.0V		±0.8		dB
GAIN CONTROL INTERFACE (V_{CNTL})					
Input Voltage Range			0.2 to 2.3		V
Input Resistance			1		MΩ
Response Time	42dB Gain Change; to 90% Signal Level		0.5		µs
DIGITAL INPUTS(3), (4)					
($\overline{HGA}$, $\overline{HGB}$, $\overline{PD}$)					
V_{IH}, High-Level Input Voltage		2.0			V
V_{IL}, Low-Level Input Voltage				0.8	V
Input Resistance			1		MΩ
Input Capacitance			5		pF
POWER SUPPLY					
Supply Voltage		4.75	5.0	5.25	V
Power Dissipation			105	125	mW
Power-Down			22		mW
Power-Up Response Time			25		µs
Power-Down Response Time			2		µs
THERMAL CHARACTERISTICS					
Temperature Range	Ambient, Operating	−40		+85	°C
Thermal Resistance, θ_{JA}	Soldered Pad; Four-Layer PCB with Thermal Vias		36.7		°C/W
θ_{JC}			4.0		°C/W

(1) 2nd, 3rd-harmonic distortion less than or equal to −30dBc.
(2) Referenced to best fit dB-linear curve.
(3) Parameters ensured by design; not production tested.
(4) Do not leave inputs floating; no internal pull-up/pull-down resistors.

PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION	PIN	DESIGNATOR	DESCRIPTION
1	IN_A+	Channel A +Input	17	$V_{CNTL}B$	Channel B Gain Control Voltage Input
2	NC	No Internal Connection	18	$V_{CLMP}B$	Channel B Clamp Voltage
3	$V_{DD}R$	Reference Supply	19	$\overline{HG}B$	Channel B High/Low Output Gain (High = Low Gain)
4	VB	Bias Voltage, 0.1µF Bypass Capacitor	20	$\overline{PD}$	Power Down (Active High)
5	V_{CM}	Common-mode Voltage, 0.1µF Bypass Capacitor	21	NC	No Internal Connection
6	GNDR	Internal Reference Ground	22	$\overline{HG}A$	Channel A High/Low Output Gain (High = Low Gain)
7	NC	No Internal Connection	23	$V_{CLMP}A$	Channel A Clamp Voltage
8	IN_B+	Channel B+ Input	24	$V_{CNTL}A$	Channel A Gain Control Voltage Input
9	$IN_B−$	Channel B− Input	25	Out_A+	Channel A+ Output
10	NC	No Internal Connection	26	$Out_A−$	Channel A− Output
11	CB2	Channel B, External Coupling Capacitor	27	GNDA	Channel A Ground
12	CB1	Channel B, External Coupling Capacitor	28	$V_{DD}A$	Channel A Supply
13	$V_{DD}B$	Channel B Supply	29	CA1	Channel A; External Coupling Capacitor
14	GNDB	Channel B Ground	30	CA2	Channel A; External Coupling Capacitor
15	$Out_B−$	Channel B− Output	31	NC	No Internal Connection
16	Out_B+	Channel B+ Output	32	$IN_A−$	Channel A− Input

TYPICAL CHARACTERISTICS

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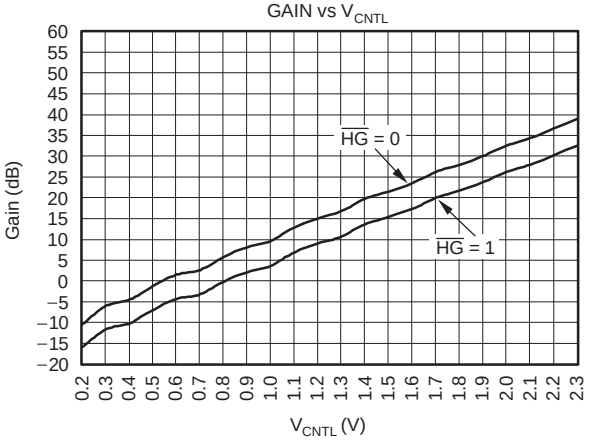


Figure 1

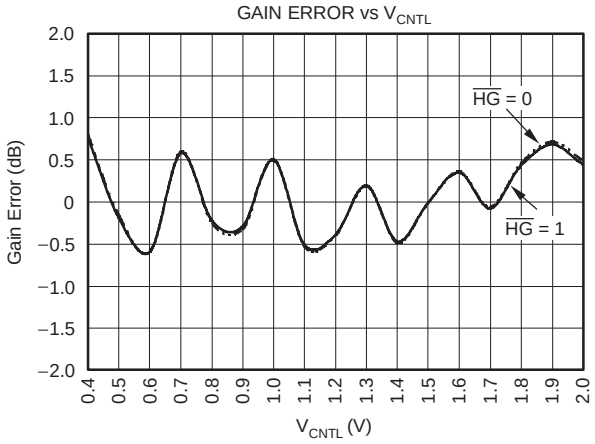


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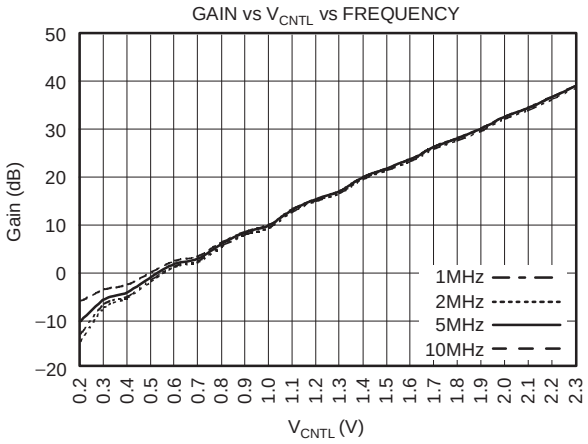


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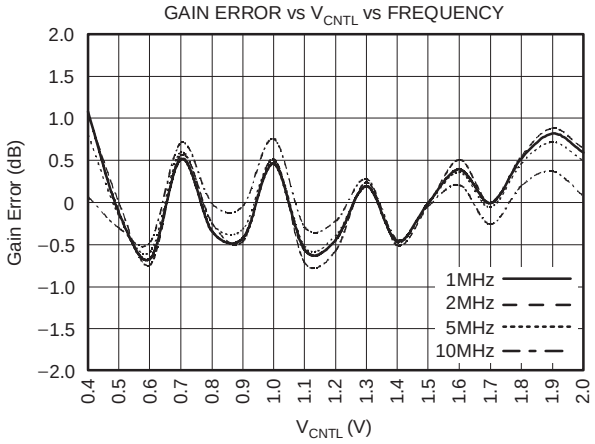


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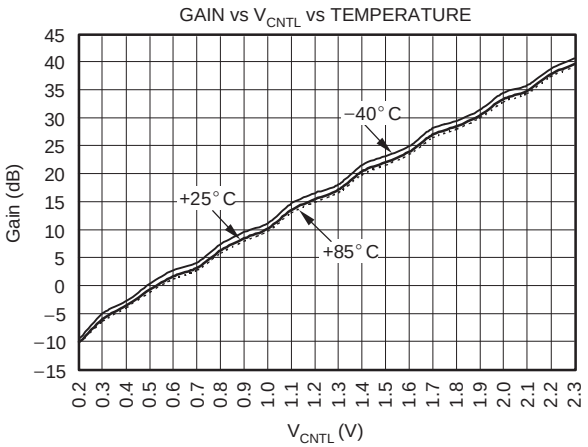


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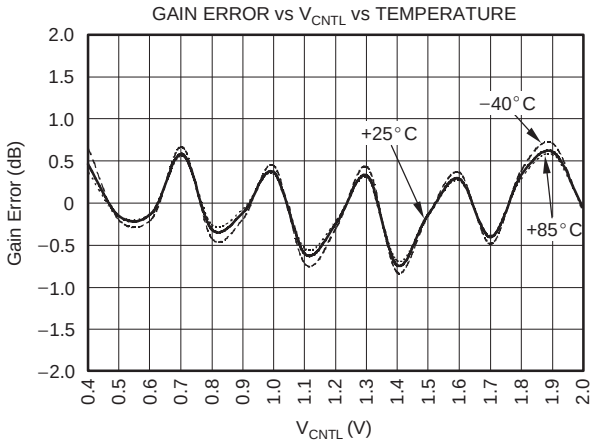


Figure 6

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground, differential output ($1V_{PP}$), CA, CB = 3.9µF, single-ended input configuration, f_{IN} = 5MHz, $\overline{HG}$ = Low (High-Gain Mode), V_{CNTL} = 2.3V, unless otherwise noted.

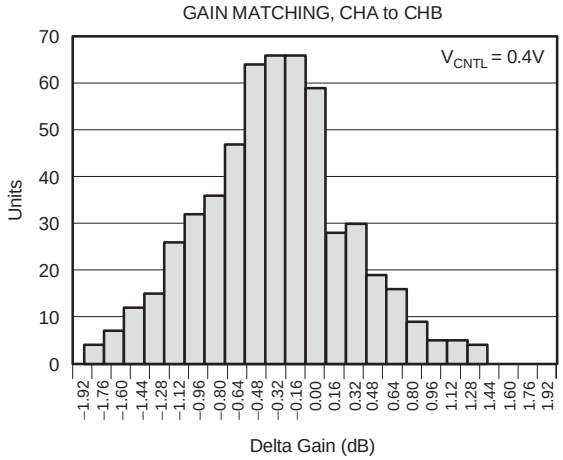


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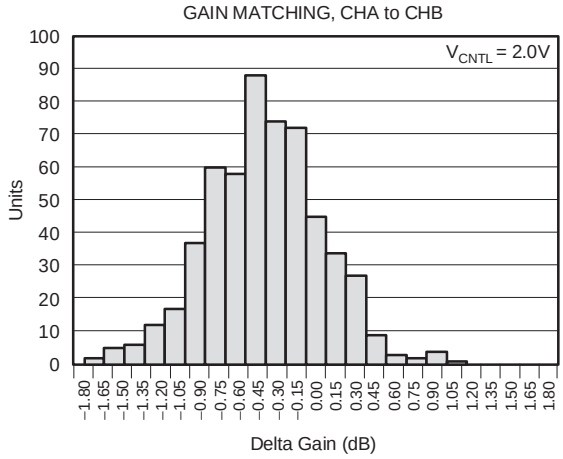


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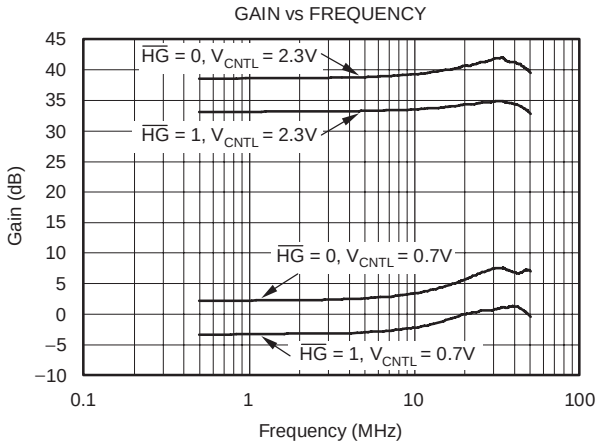


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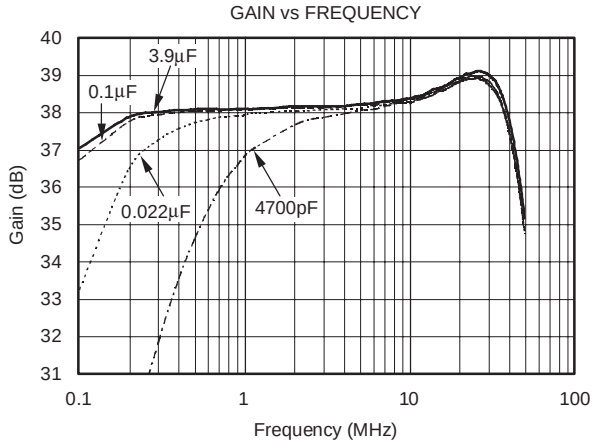


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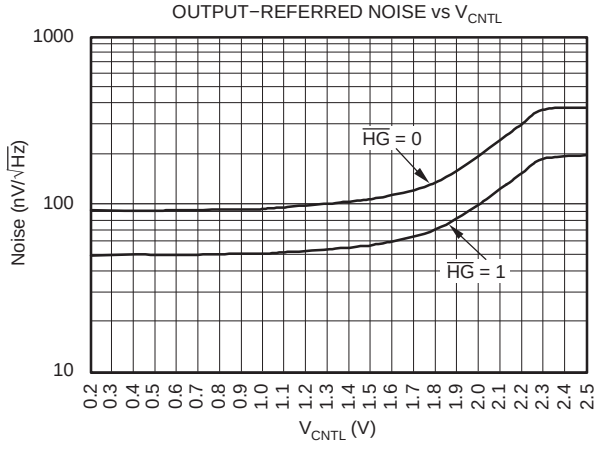


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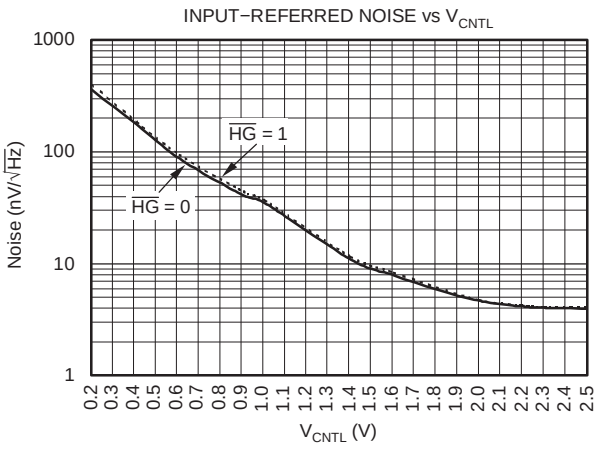


Figure 12

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground, differential output ($1V_{PP}$), CA, CB = 3.9µF, single-ended input configuration, f_{IN} = 5MHz, $\overline{HG}$ = Low (High-Gain Mode), V_{CNTL} = 2.3V, unless otherwise noted.

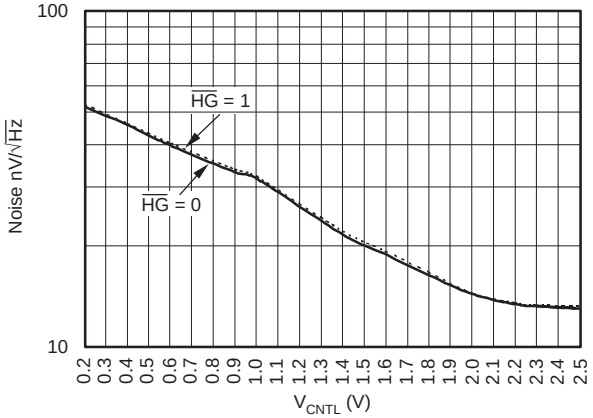


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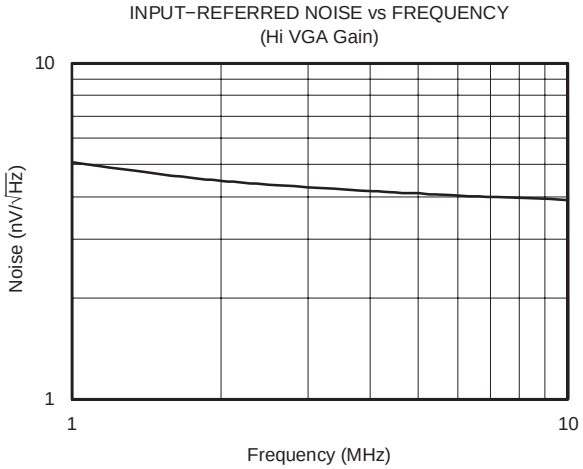


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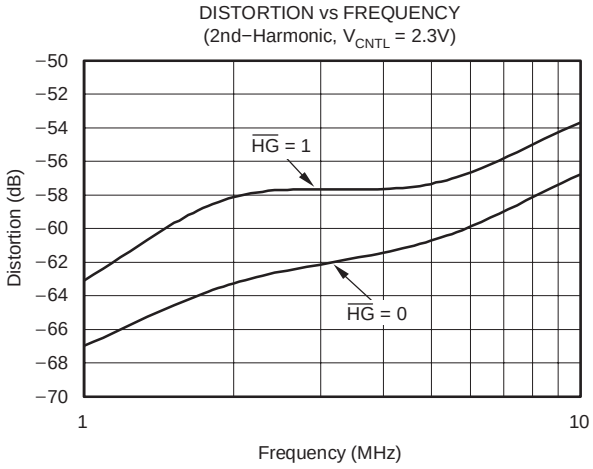


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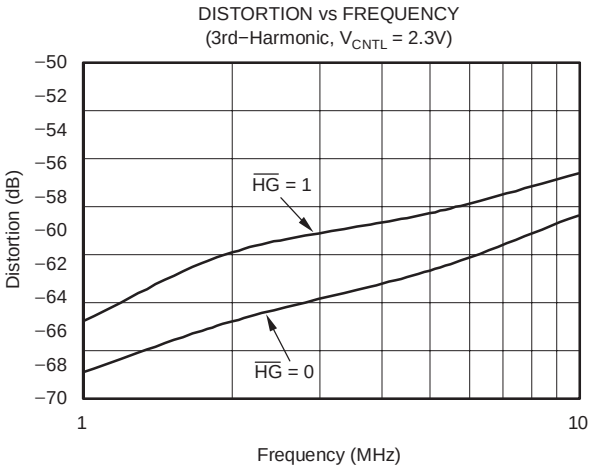


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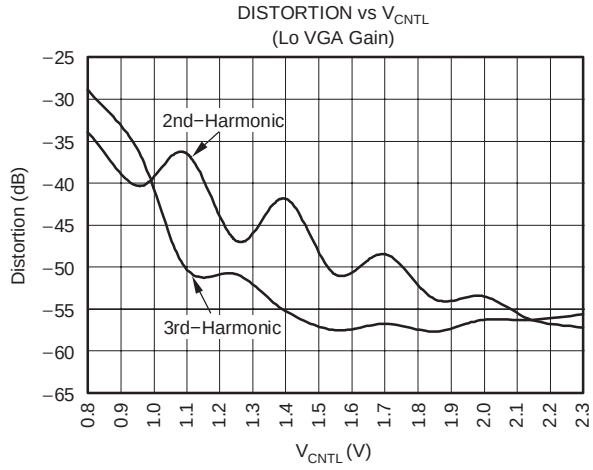


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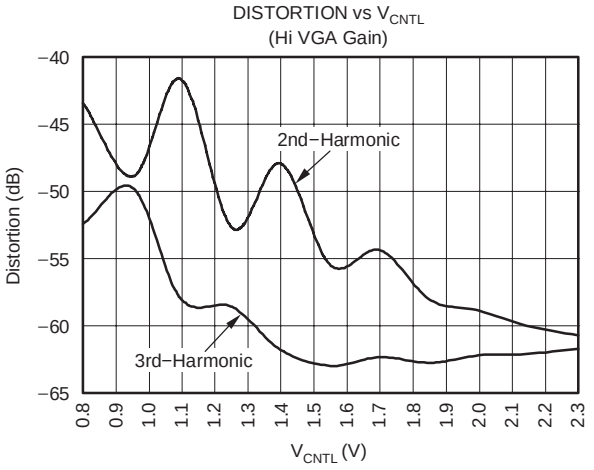


Figure 18

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground, differential output ($1V_{PP}$), CA, CB = 3.9µF, single-ended input configuration, f_{IN} = 5MHz, $\overline{HG}$ = Low (High-Gain Mode), V_{CNTL} = 2.3V, unless otherwise noted.

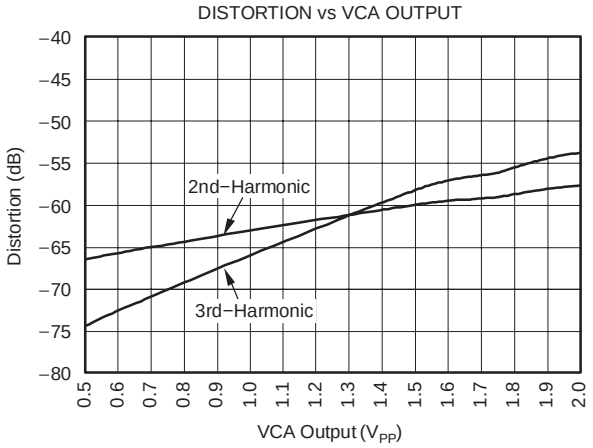


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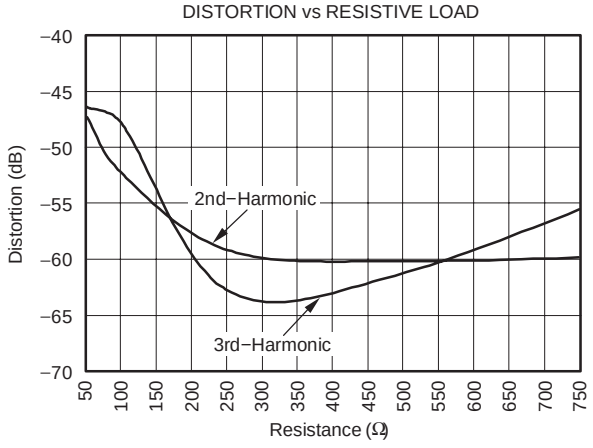


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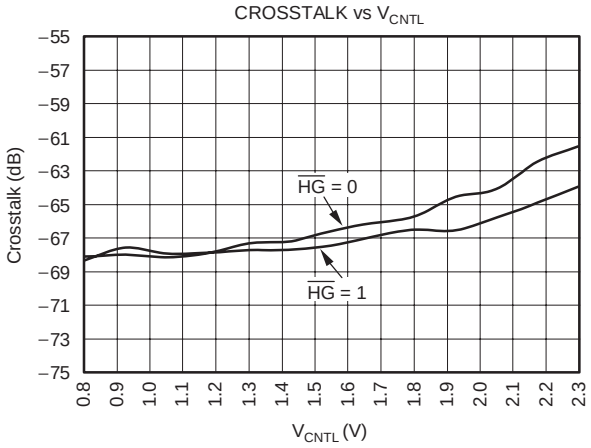


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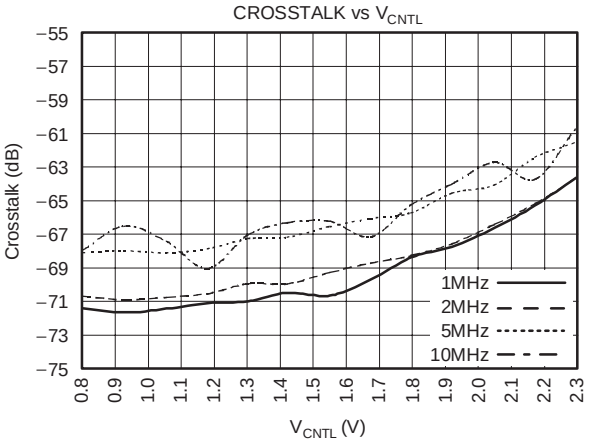


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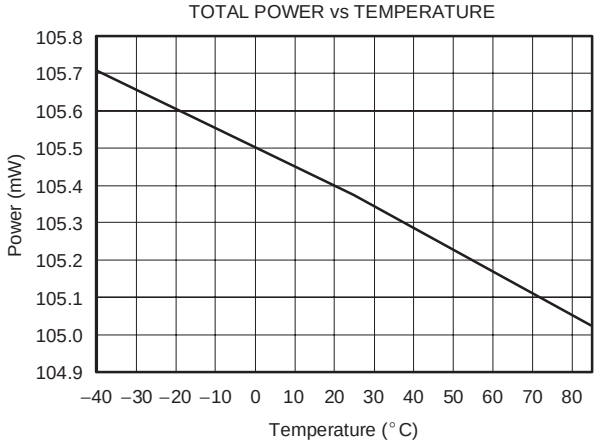


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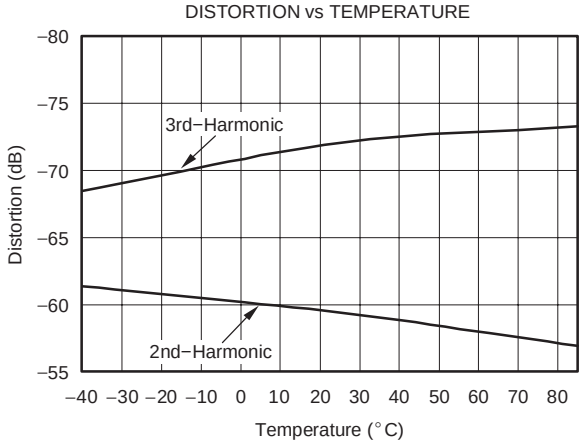


Figure 24

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground, differential output ($1V_{PP}$), CA, CB = 3.9µF, single-ended input configuration, f_{IN} = 5MHz, $\overline{HG}$ = Low (High-Gain Mode), V_{CNTL} = 2.3V, unless otherwise noted.

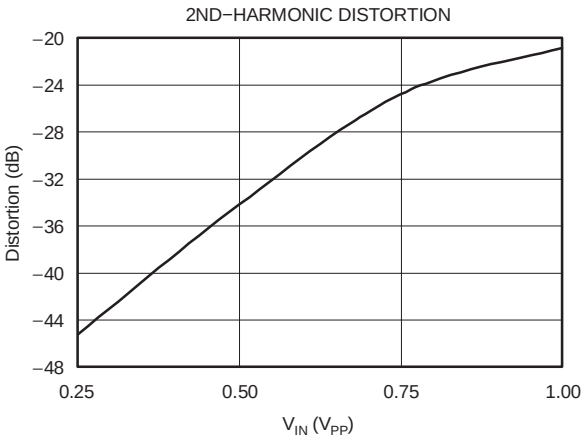


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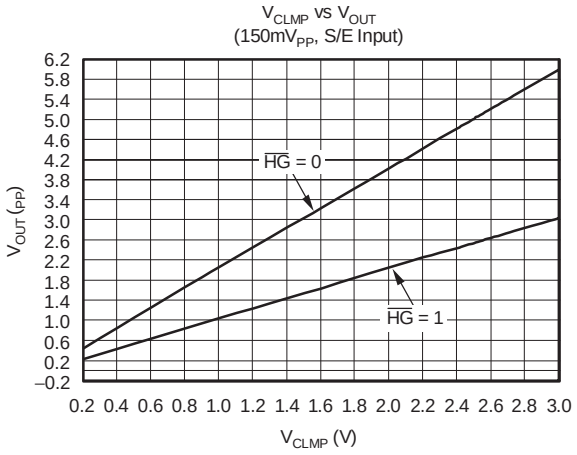


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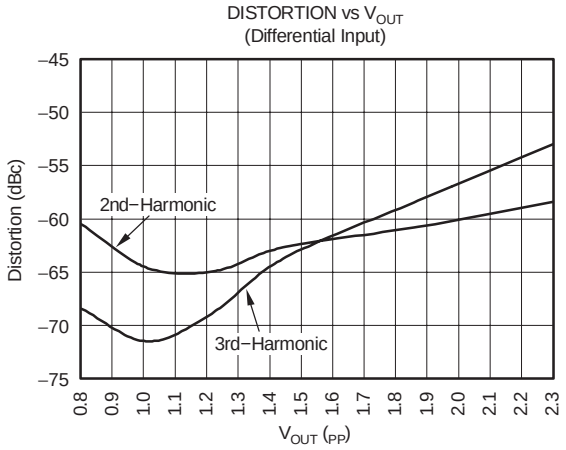


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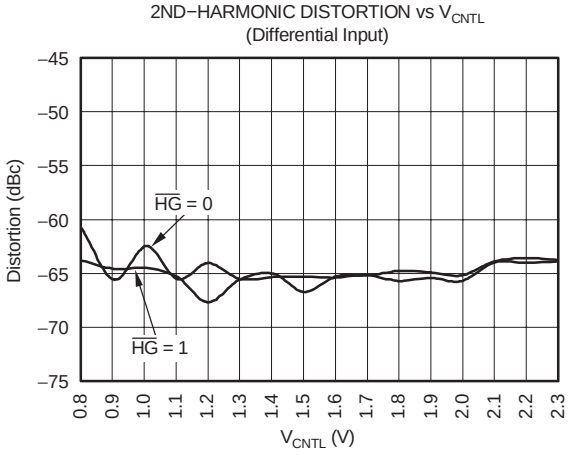


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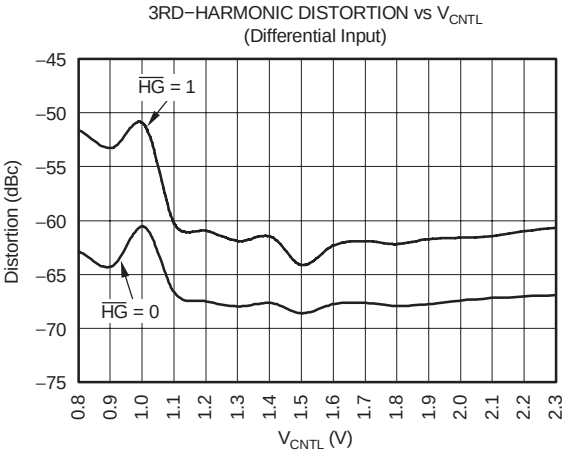


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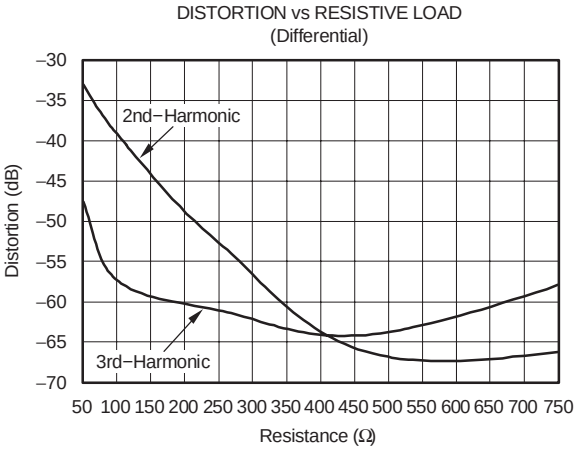


Figure 30

TYPICAL CHARACTERISTICS (continued)

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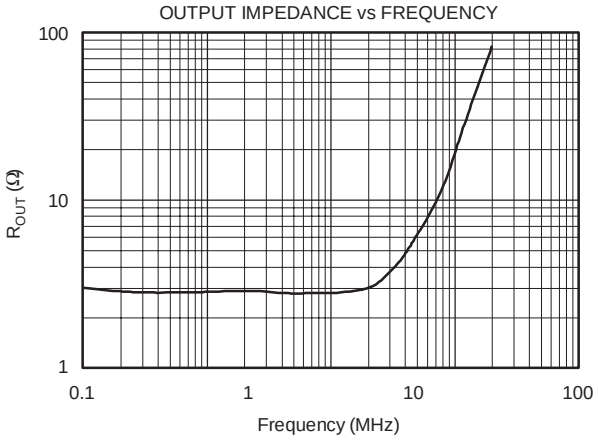


Figure 31

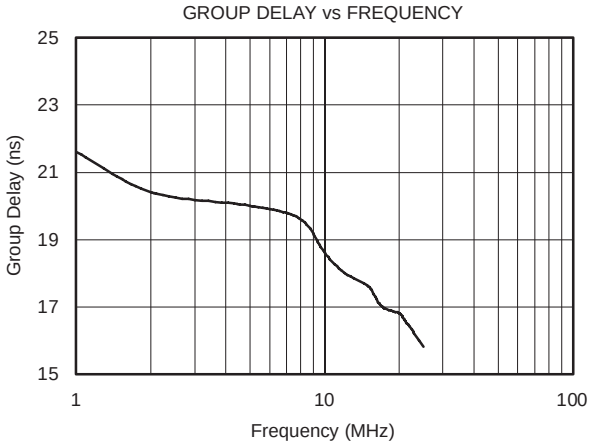


Figure 32

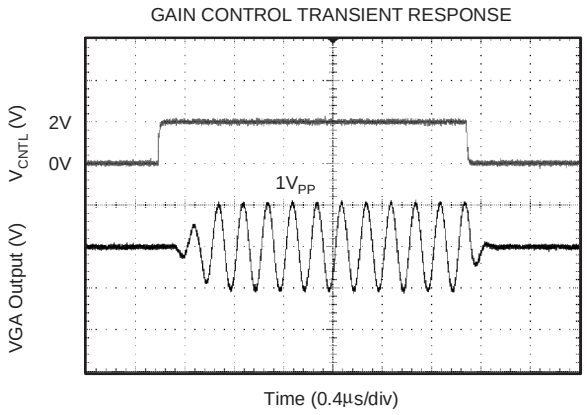


Figure 33

THEORY OF OPERATION

The VCA2617 is a dual-channel variable gain amplifier (VGA) with each channel being independant. The VGA is a true variable-gain amplifier, achieving lower noise output at lower gains. The output amplifier has two gains, allowing for further optimization with different analog-to-digital converters. Figure 34 shows a simplified block diagram of a single channel of the dual-channel system. The VGA can be powered down in order to conserve system power when necessary.

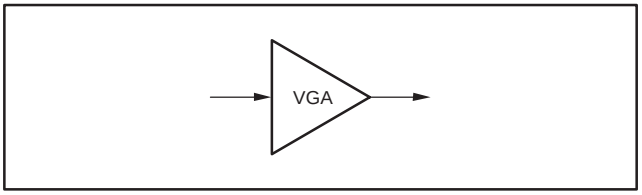


Figure 34. Simplified Block Diagram of VCA2617

VGA—OVERVIEW

The VGA that is used with the VCA2617 is a true variable-gain amplifier; as the gain is reduced, the noise contribution from the VGA itself is also reduced. This design is in contrast with another popular device architecture (used by the VCA2619), where an effective VCA characteristic is obtained by a voltage-variable attenuator succeeded by a fixed-gain amplifier. At the highest gain, systems with either architecture are dominated by the noise produced at the input to either the fixed or variable gain amplifier. At low gains, however, the noise output is dominated by the contribution from the VGA. Therefore, the overall system with lower VGA gain will produce less noise.

The following example will illustrate this point. Figure 34 shows a block diagram of the variable-gain amplifier; Figure 35 shows a block diagram of a variable attenuation attenuator followed by a fixed gain amplifier. For purposes of this example, let us assume the performance characteristics shown in Table 1; these values are the typical performance data of the VCA2617 and the VCA2619.

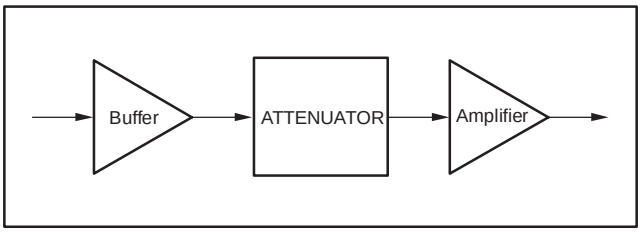


Figure 35. Block Diagram of Older VCA Models

Table 1. Gain and Noise Performance of Various VCA Blocks

BLOCK	GAIN (Loss) dB	NOISE nV/$\sqrt{Hz}$
Buffer	0	3.9
Attenuator (VCA2619)	0	2.2
Attenuator (VCA2619)	−40	2.2
VCA1 (VCA2617)	40	4.1
VCA1 (VCA2617)	0	90
VCA1 (VCA2619)	40	3.9

When the block diagram shown in Figure 34 has a gain of 40dB, the noise referred to the input (RTI) is:

$$\text{Total Noise (RTI)} = 4.1\text{nV}/\sqrt{\text{Hz}} \quad (1)$$

When the block diagram shown in Figure 35 has the combined gain of 60dB, the noise referred to the input (RTI) is given by the expression:

$$\text{Total Noise (RTI)} = \sqrt{(\text{Buffer Noise})^2 + (\text{ATTEN Noise})^2 + (\text{VCA Noise})^2}$$
$$= \sqrt{(3.9)^2 + (2.2)^2 + (3.9)^2} = 5.9\text{nV}/\sqrt{\text{Hz}} \quad (2)$$

Repeating the above measurements for both VCA configurations when the overall gain is 10dB yields the following results:

For the VCA with a variable gain amplifier (Figure 34):

$$\text{Total Noise (RTI)} = 90\text{nV}/\sqrt{\text{Hz}} \quad (3)$$

For the VCA with a variable attenuation attenuator (Figure 35):

$$\text{Total Noise} = \sqrt{(3.9)^2 + (2.2)^2 + (2.0/0.10)^2}$$
$$= 14\text{nV}/\sqrt{\text{Hz}} \quad (4)$$

The VGA has a continuously-variable gain range of 48dB with the ability to select either of two options. The gain of the VGA can either be varied from −10dB to 38dB, or from −16dB to 32dB. The VGA output can be programmed to clip at a predetermined voltage that is selected by the user. When the user applies a voltage to the V_{CLMP}-pin, the output will have a peak-to-peak voltage that is given by the graph shown in Figure 26.

VOLTAGE-CONTROLLED AMPLIFIER (VCA)—DETAIL

Figure 36 shows a simplified schematic of the VCA. The VCA2617 is a true voltage-controlled amplifier, with the gain expressed in dB directly proportional to a control signal. This architecture compares to the older VCA products where a voltage-controlled attenuator was followed by a fixed-gain amplifier. With a variable-gain amplifier, the output noise diminishes as the gain reduces. A variable-gain amplifier, where the output amplifier gain is fixed, will not show diminished noise in this manner. Refer to Table 2, which shows a comparison between the noise performance at different gains for the VCA2617 and the older VCA2619.

Table 2. Noise vs Gain (R_G = 0)

PRODUCT	GAIN (dB)	NOISE RTI (nV/$\sqrt{Hz}$)
VCA2617	40	4.1
VCA2617	0	100
VCA2619	40	5.9
VCA2619	0	500

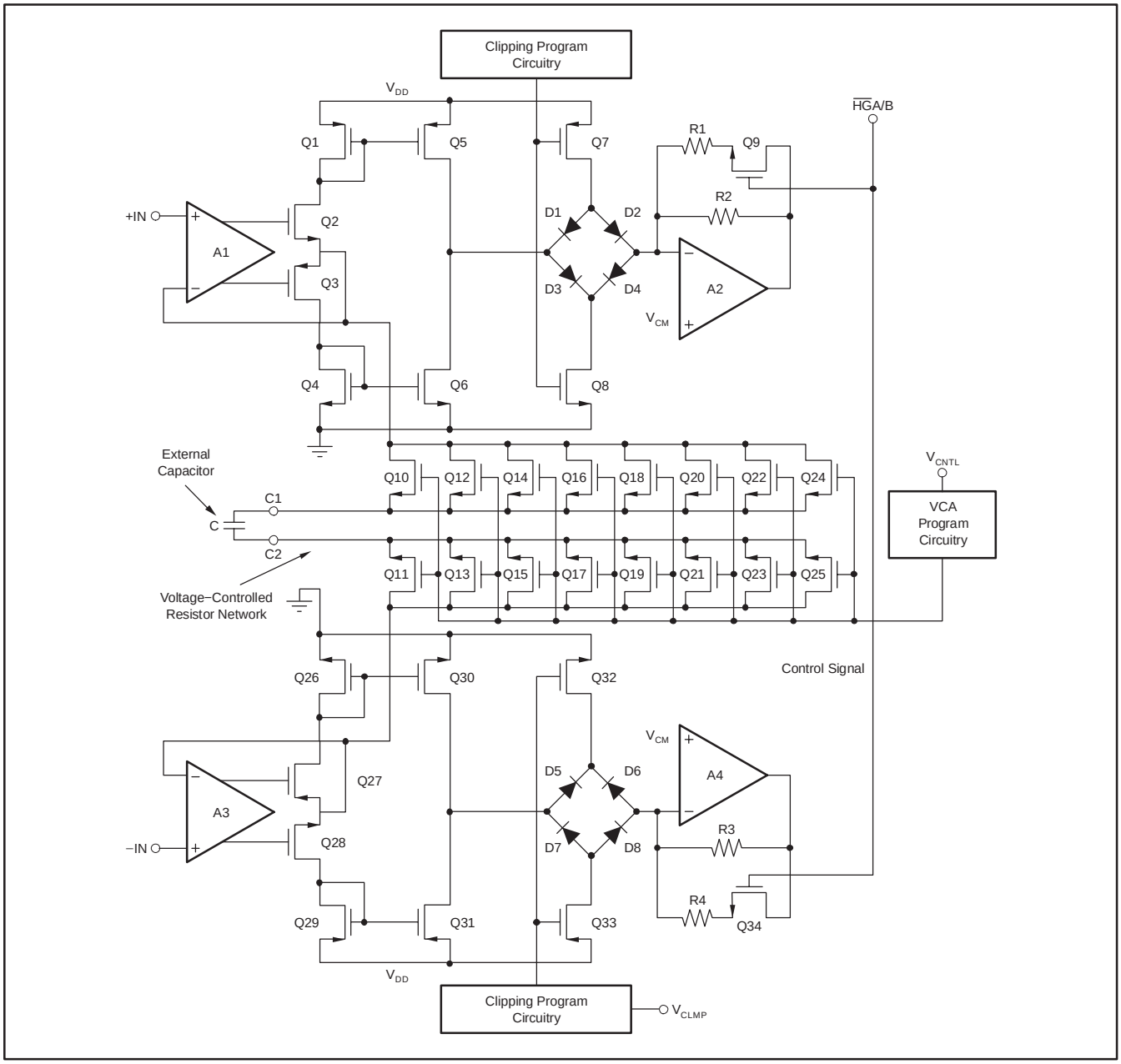


Figure 36. Block Diagram of VCA

The VCA accepts a differential input at the +IN and −IN terminals. Amplifier A1, along with transistors Q2 and Q3, forms a voltage follower that buffers the +IN signal to be able to drive the voltage-controlled resistor. Amplifier A3, along with transistors Q27 and Q28, plays the same role as A1. The differential signal applied to the voltage-controlled resistor network is converted to a current that flows through transistors Q1 through Q4. Through the mirror action of transistors Q1/Q5 and Q4/Q6, a copy of this same current flows through Q5 and Q6. Assuming that the signal current is less than the programmed clipping current (that is, the current flowing through transistors Q7 and Q8), the signal current will then go through the diode bridge (D1 through D4) and be sent through either R2 or R1, depending upon the state of Q9. This signal current multiplied by the feedback resistor associated with amplifier A2, determines the signal voltage that is designated −OUT. Operation of the circuitry associated with A3 and A4 is identical to the operation of the previously described function to create the signal +OUT.

A1 and its circuitry form a voltage-to-current converter, while A2 and its circuitry form a current-to-voltage converter. This architecture was adapted because it has excellent signal-handling capability. A1 has been designed to handle a large voltage signal without overloading, and the various mirroring devices have also been sized to handle large currents. Good overload capability is achieved as both the input and output amplifier are not required to amplify voltage signals. Voltage amplification occurs when the input voltage is converted to a current; this current in turn is converted back to a voltage as amplifier A2 acts as a transimpedance amplifier. The overall gain of the output amplifier A2 can be altered by 6dB by the action of the $\overline{HG}$ signal. This enables more optimum performance when the VCA interfaces with either a 10-bit or 12-bit analog-to-digital converter (ADC). An external capacitor (C) is required to provide a low impedance connection to join the two sections of the resistor network. Capacitor C could be replaced by a short-circuit. By providing a DC connection, the output offset will be a function of the gain setting. Typically, the offset at this point is ±10mV; thus, if the gain varies from 1 to 100, the output offset would vary from ±10mV to ±100mV.

VARIABLE GAIN CHARACTERISTICS

Transistors Q10, Q12, Q14, Q16, Q18, Q20, Q22, and Q24 form a variable resistor network that is programmed in an exponential manner to control the gain. Transistors Q11, Q13, Q15, Q17, Q19, Q21, Q23, and Q25 perform the same function. These two groups of FET variable resistors are configured in this manner to balance the capacitive loading on the total variable-resistor network. This balanced configuration is used to keep the second harmonic component of the distortion low. The common source connection associated with each group of FET variable resistors is brought out to an external pin so that an external capacitor can be used to make an AC connection. This connection is necessary to achieve an adequate low-frequency bandwidth because the coupling capacitor would be too large to include within the monolithic chip. The value of this variable resistor ranges in value from 15Ω to 5000Ω to achieve a gain range of about 48dB. The low-frequency bandwidth is then given by the formula:

$$\text{Low Frequency BW} = 1/2\pi RC \quad (5)$$

where:

R is the value of the attenuator.

C is the value of the external coupling capacitor.

For example, if a low-frequency bandwidth of 500kHz was desired and the value of R was 10Ω, then the value of the coupling capacitor would be 0.05µF.

One of the benefits of this method of gain control is that the output offset is independent of the variable gain of the output amplifier. The DC gain of the output amplifier is extremely low; any change in the input voltage is blocked by the coupling capacitor, and no signal current flows through the variable resistor. This method also means that any offset voltage existing in the input is stored across this coupling capacitor; when the resistor value is changed, the DC output will not change. Therefore, changes in the control voltage do not appear in the output signal. Figure 37 shows the output waveform resulting from a step change in the control voltage, and Figure 38 shows the output voltage resulting when the control voltage is a full-scale ramp.

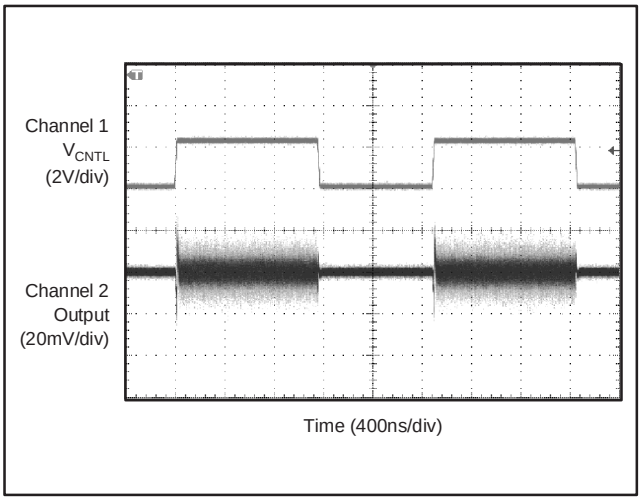


Figure 37. Response to Step Change of V_{CNTL}

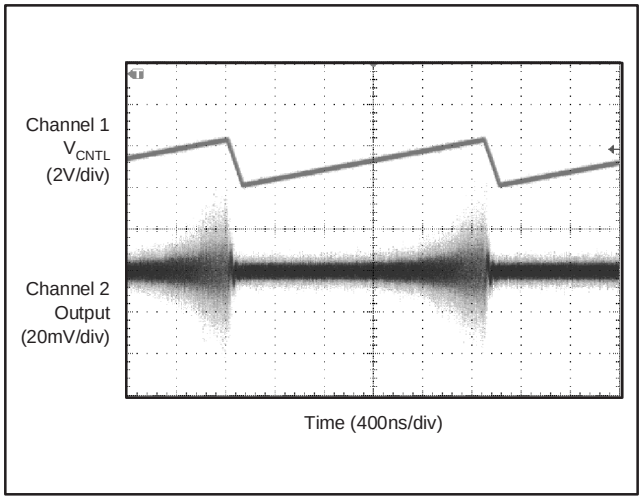


Figure 38. Response to Ramp Change of V_{CNTL}

The exponential gain control characteristic is achieved through a piecewise approximation to a perfectly smooth exponential curve. Eight FETs, operated as variable resistors whose value is progressively 1/2 of the value of the adjacent parallel FET, are turned on progressively, or their value is lowered to create the exponential gain characteristic. This characteristic can be shown in the following way. An exponential such as $y = e^x$ increases in the y dimension by a constant ratio as the x dimension increases by a constant linear amount. In other words, for a constant ($x1 - x2$), the ratio e^{x1}/e^{x2} remains the same.

When FETs used as variable resistors are placed in parallel, the attenuation characteristic that is created behaves according to this same exponential characteristic at discrete points as a function of the control voltage. It does not perfectly obey an ideal exponential characteristic at other points; however, an 8-section approximation yields a ±1dB error to an ideal curve.

PROGRAMMABLE CLIPPING

The clipping level of the VCA2617 can be programmed to a desired output. The programming feature is useful when matching the clipped level from the output of the VCA to the full-scale range of a subsequent VCA, in order to prevent the VCA from generating false spectral signals; see the circuit diagram shown in Figure 39. The signal node at the drain junction of Q5 and Q6 is sent to the diode bridge formed by diode-connected transistors, D1 through D4. The diode bridge output is determined by the current that flows through transistors Q7 and Q8. The maximum current that can then flow into the summing node of A2 is this same current; consequently, the maximum voltage output of A2 is this same current multiplied by the feedback resistor associated with A2. The maximum output voltage of A2, which would be the clipped output, can then be controlled by adjusting the current that flows through Q7 and Q8; see the circuit diagram shown in Figure 36. The circuitry of A1, R1, and Q1 converts the clamp voltage (V_{CLMP}) to a current that controls equal and opposite currents flowing through transistors Q5 and Q6.

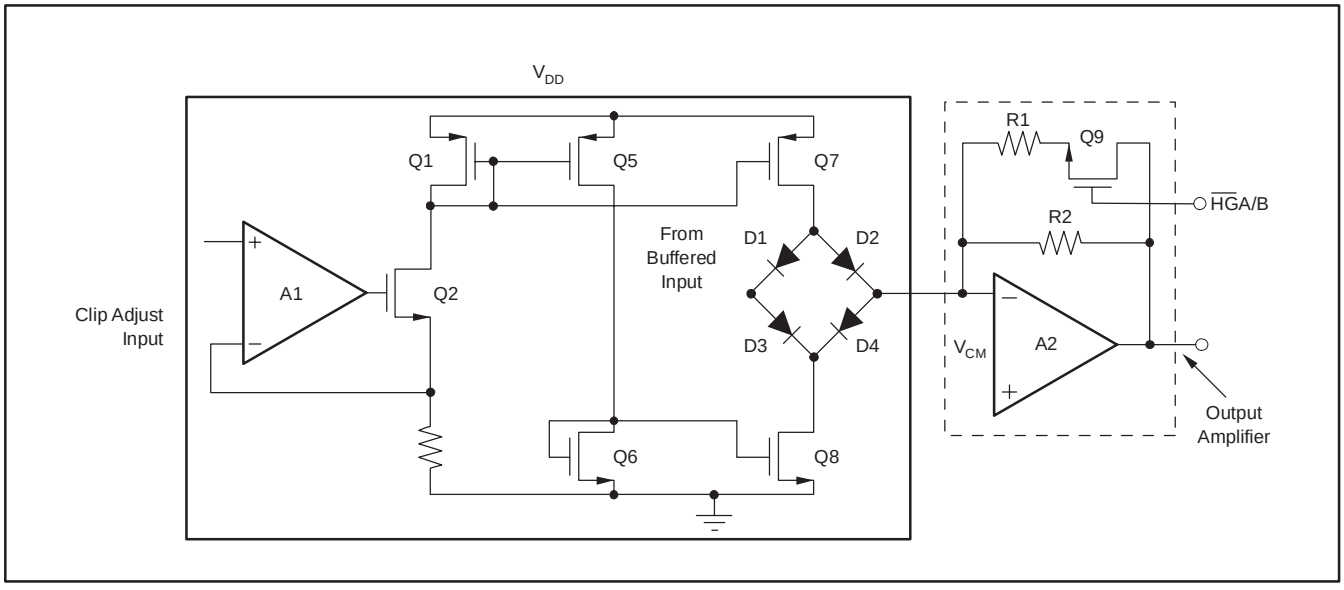


Figure 39. Clipping Level Adjust Circuitry

When $\overline{HG}$ = 0, the previously described circuitry is designed so that the value of the V_{CLMP} signal is equal to the peak differential signal developed between $+V_{OUT}$ and $-V_{OUT}$. When $\overline{HG}$ = 1, the differential output will be equal to the clamp voltage. This method of controlled clipping also achieves fast and clean settling waveforms at the output of the VCA, as shown in Figure 40 through Figure 43. The sequence of waveforms demonstrate the clipping performance during various stages of overload.

In a typical application, the VCA2617 will drive an anti-aliasing filter, which in turn will drive an ADC. Many modern ADCs, such as the ADS5270, are well-behaved with as much as 2x overload. This means that the clipping level of the VCA should be set to overcome the loss in the filter such that the clipped input to the ADC is just slightly over the full-scale input. By setting the clipping level in this manner, the lowest harmonic distortion level will be achieved without interfering with the overload capability of the ADC.

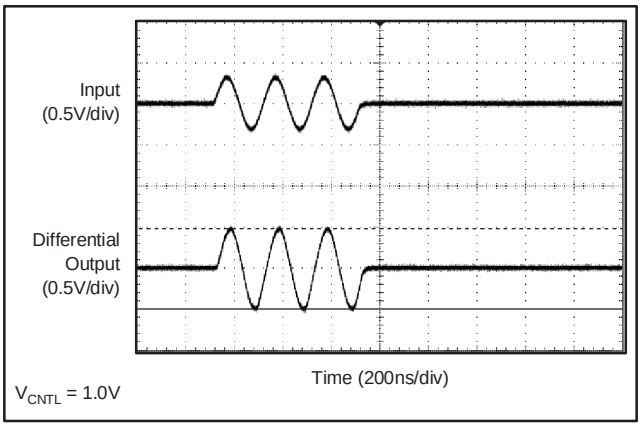


Figure 40. Before Overload (630mV$_{PP}$ Input)

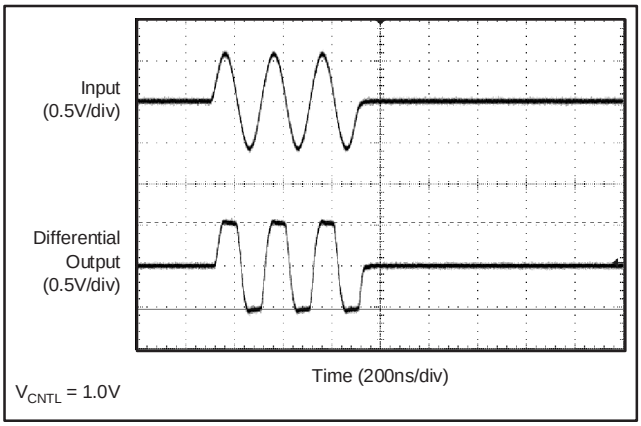


Figure 42. Overload (1.5V$_{PP}$ Input)

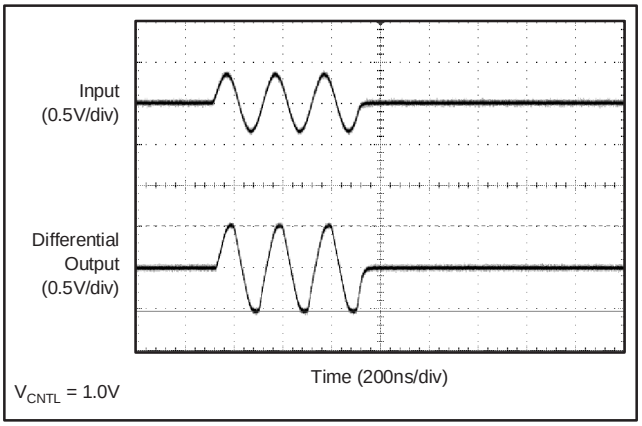


Figure 41. Approaching Overload (700mV$_{PP}$ Input)

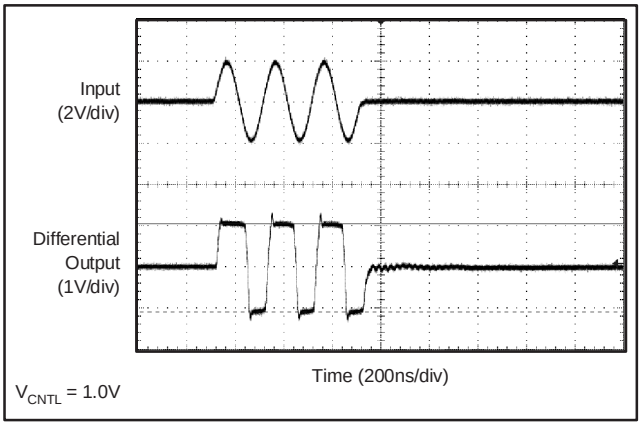


Figure 43. Extreme Overload (3.8V$_{PP}$ Input)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VCA2617RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VCA 2617	Samples
VCA2617RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VCA 2617	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

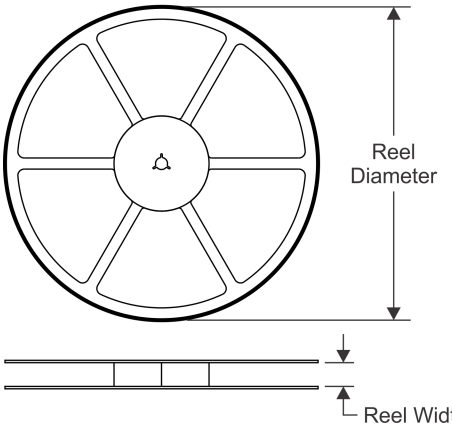
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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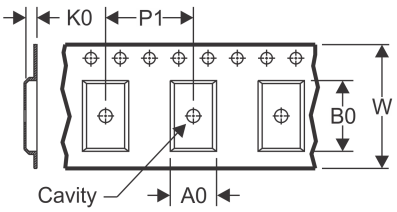
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

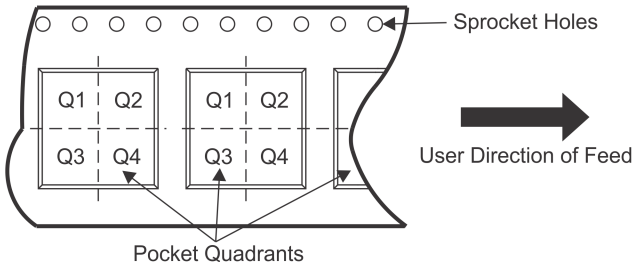


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

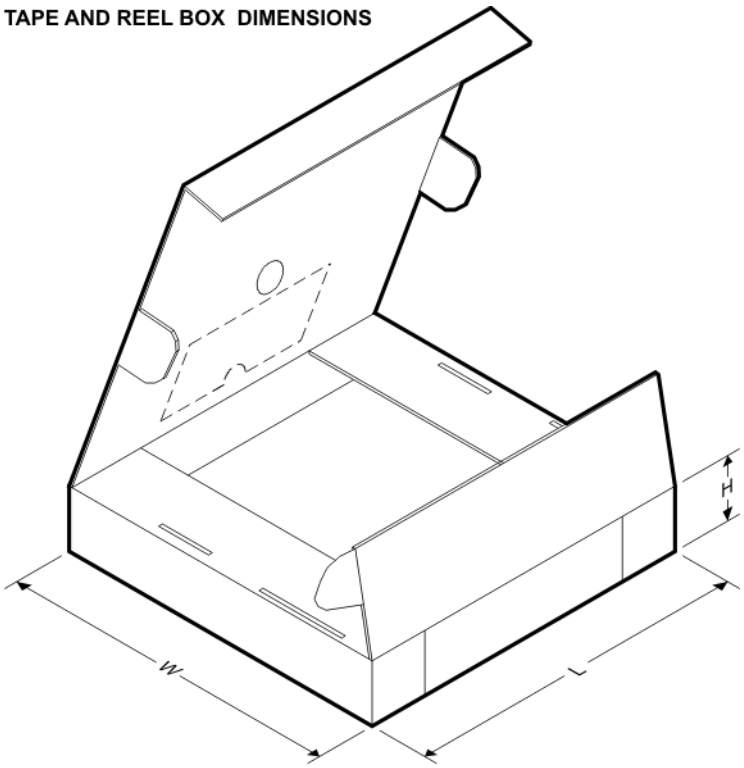
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VCA2617RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
VCA2617RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VCA2617RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
VCA2617RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

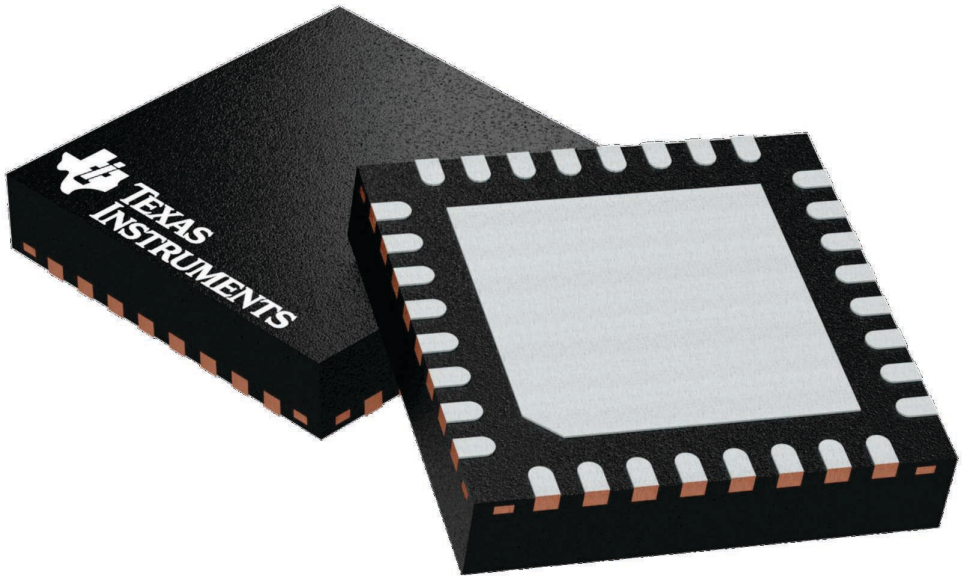
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

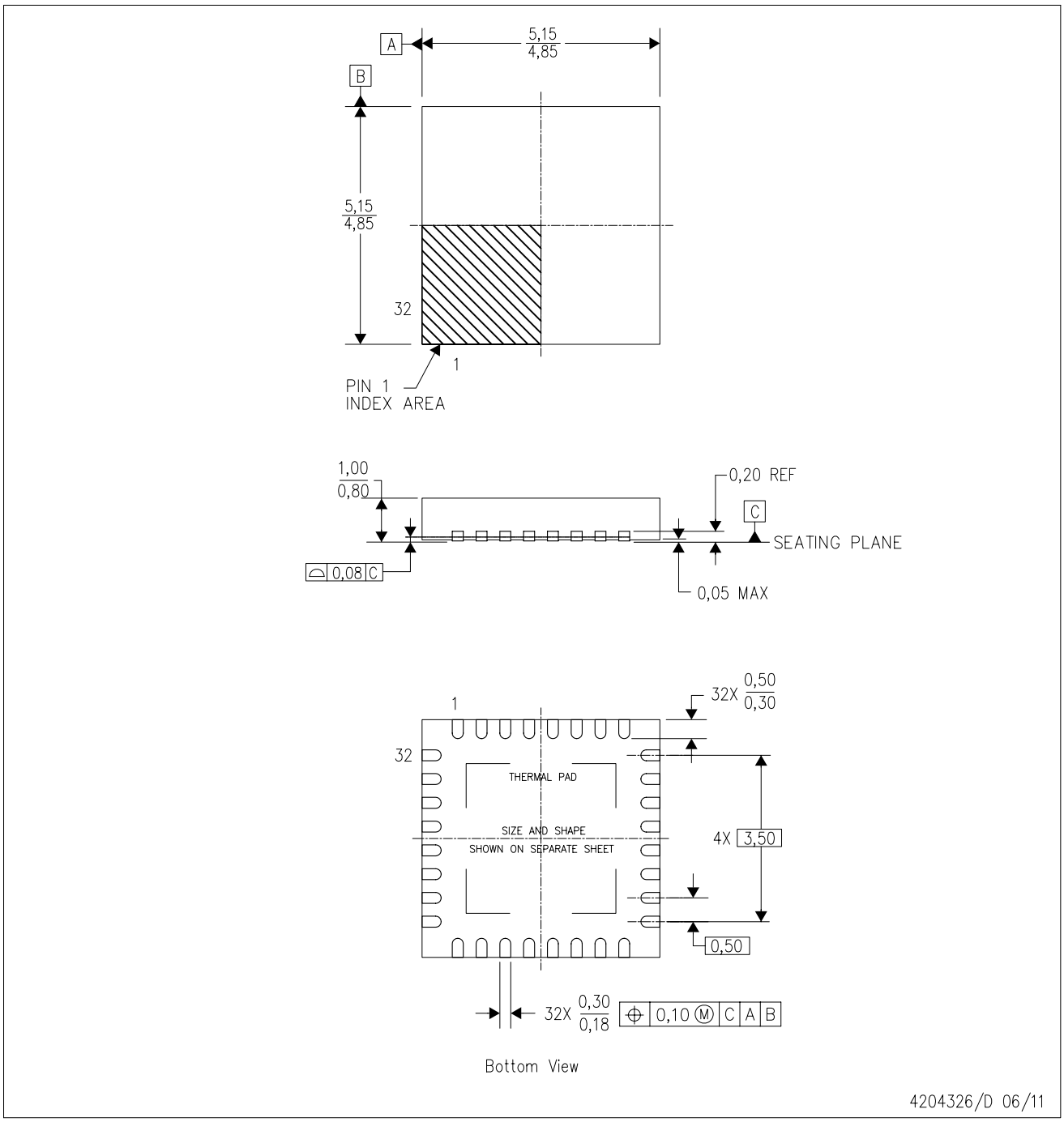
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

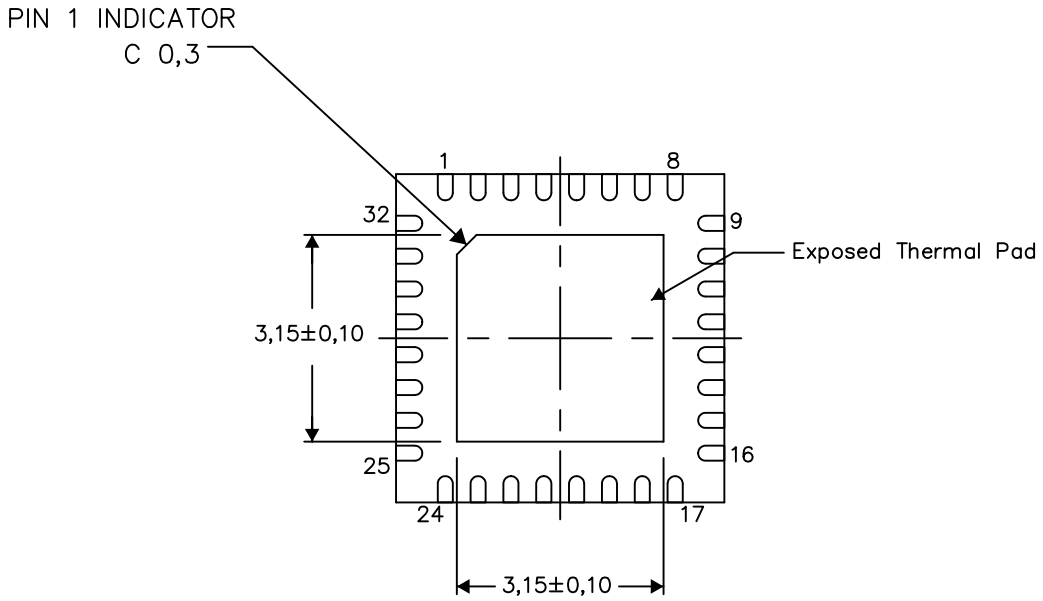
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



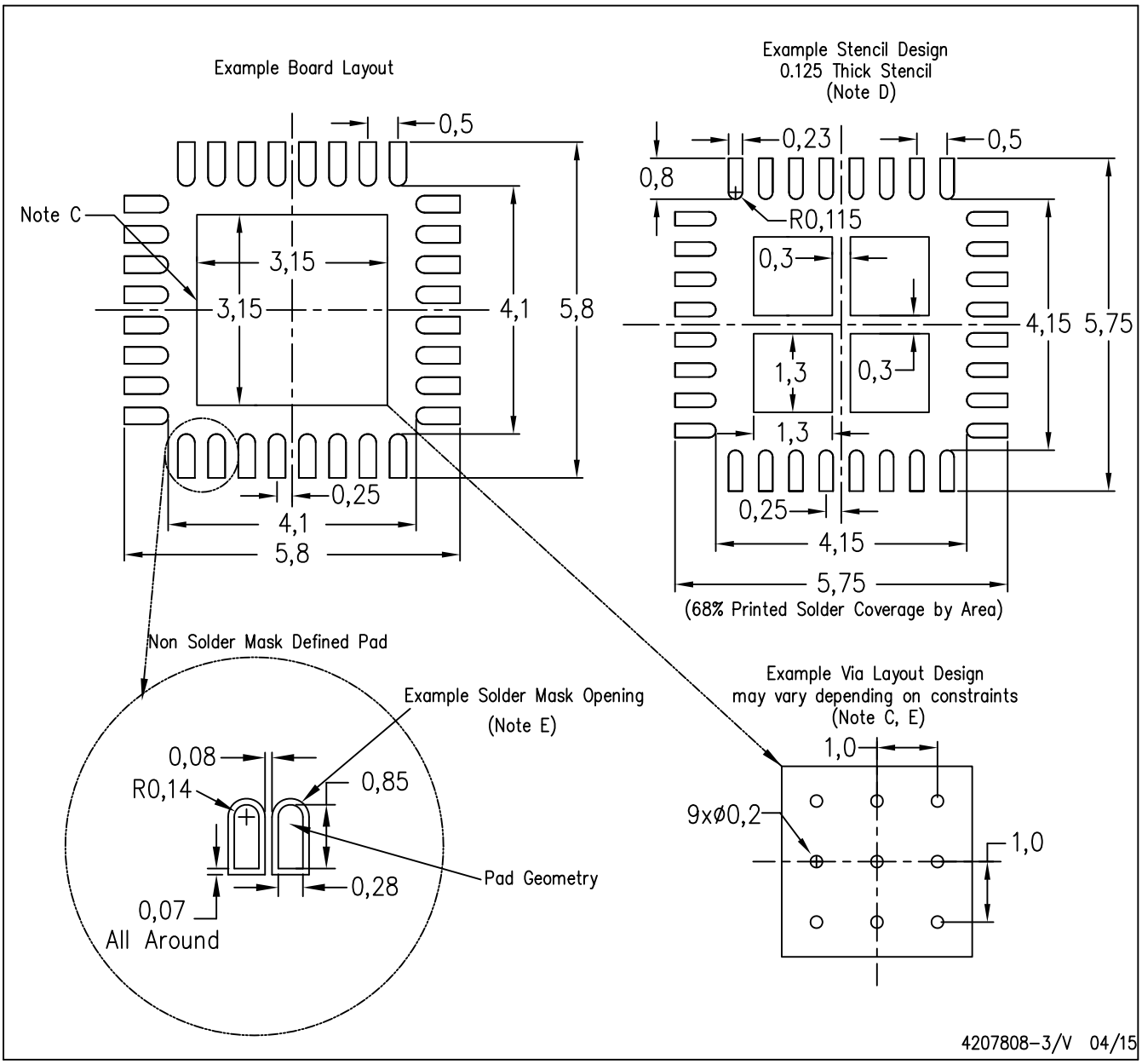
Bottom View

Exposed Thermal Pad Dimensions

4206356–3/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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