Two output ultra-low additive phase noise PCIe Gen 1 to 5, and UPI/QPI fanout buffer

Features

- One differential input which accepts any differential format.
- Two differential HCSL outputs
- Ultra-low additive jitter: 32fs (in 12kHz to 20MHz integration band at 400MHz clock frequency)
- Supports clock frequencies from 0 to 400MHz
- Supports 2.5V or 3.3V power supplies for HCSL outputs
- Embedded Low Drop Out (LDO) Voltage regulator provides superior Power Supply Noise Rejection
- Maximum output to output skew of 50ps
- Individual Output Enable pin for each differential pair
- Transfers Spread-Spectrum without attenuation

Ordering Information

ZL40262LDG1	20 pin QFN	Trays
ZL40262LDF1	20 pin QFN	Tape and Reel

Package size: 4 x 4 mm

-40°C to +85°C

Applications

- PCI Express generation 1/2/3/4/5 clock distribution
- UPI/QPI clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- High performance microprocessor clock distribution
- Test Equipment

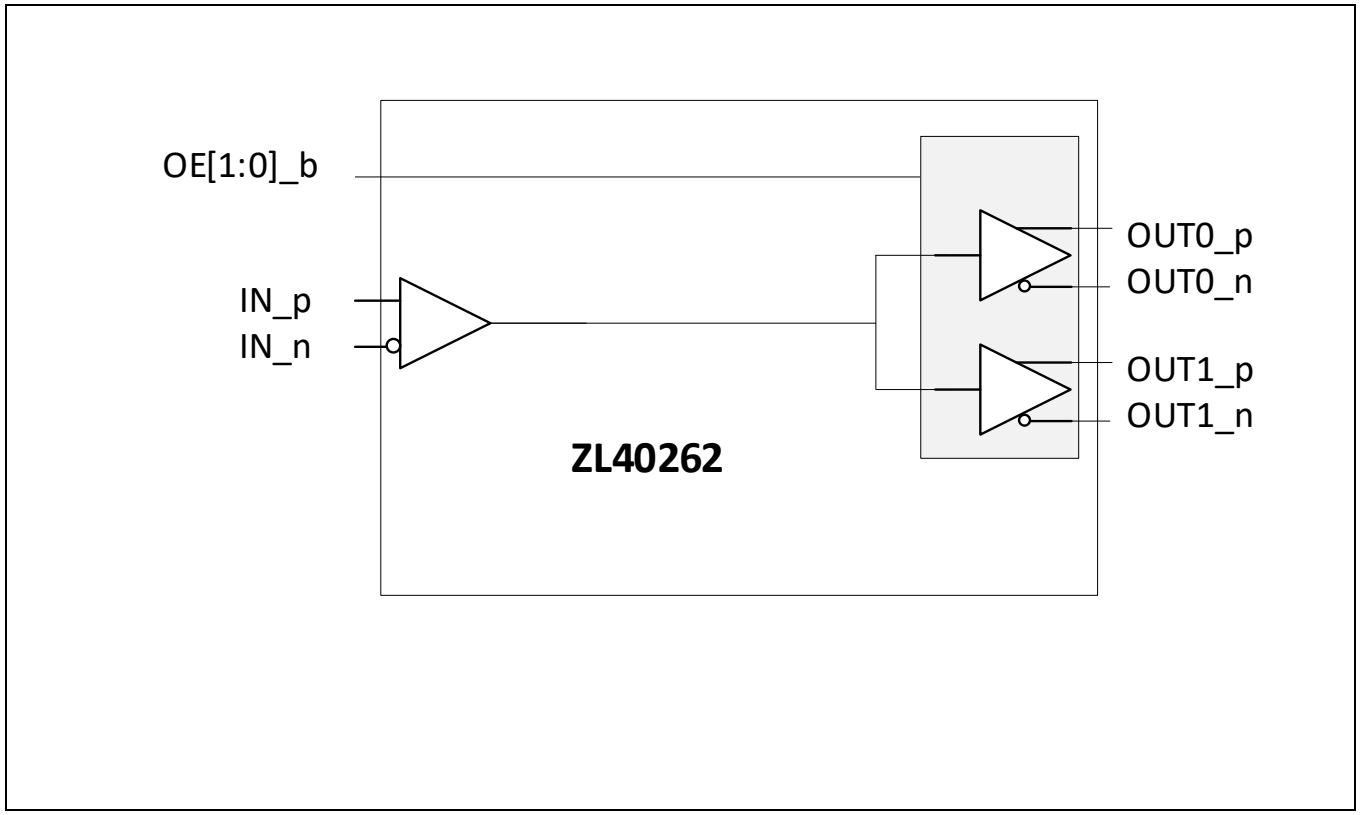


Figure 1. Functional Block Diagram

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Pin Diagram

The device is packaged in a 4x4mm 20-pin QFN.

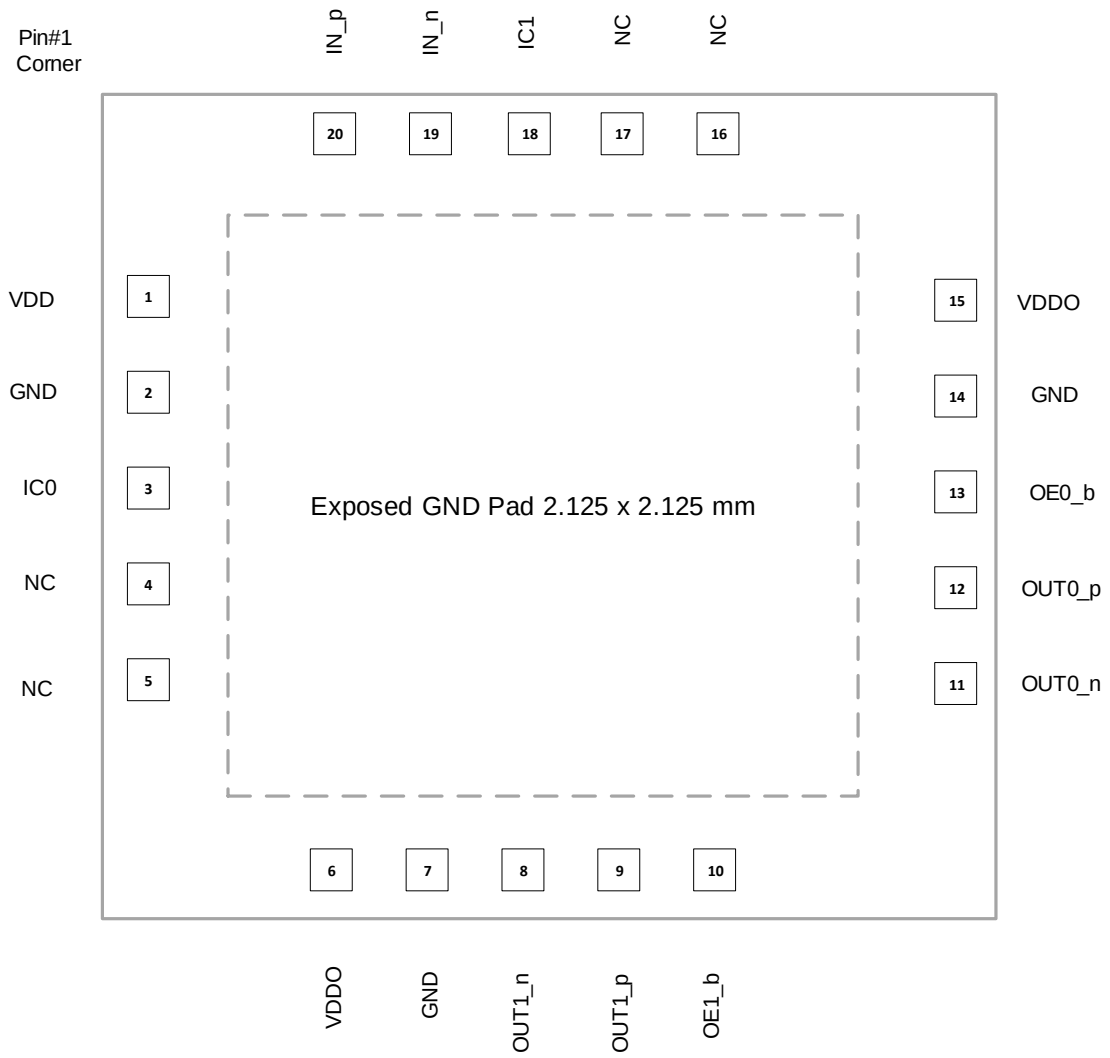


Figure 2. Pin Diagram

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Pin Descriptions

All device inputs and outputs are HCSL unless described otherwise. The I/O column uses the following symbols: I – input, I_{PU} – input with 300kΩ internal pull-up resistor, I_{PD} – input with 300kΩ internal pull-down resistor, I_{APU} – input with 31kΩ internal pull-up resistor, I_{APD} – input with 30kΩ internal pull-down resistor, $I_{APU/APD}$ – input biased to VDD/2 with 60kΩ internal pull-up and pull-down resistors (30 kΩ equivalent), O – output, I/O – Input/Output pin, NC-No connect pin, P – power supply pin.

Table 1Pin Descriptions

#	Name	I/O	Description
Input Reference			
20 19	IN_p IN_n	I_{APD} $I_{APU/APD}$ I_{APD} $I_{APU/APD}$	**Input Differential or Single Ended Reference** Input frequency range 0Hz to 400MHz. Non-inverting inputs (_p) are pulled down with internal 30kΩ pull-down resistors. Inverting inputs (_n) are pulled up and pulled down with 60kΩ internal resistors (30kΩ equivalent) to keep inverting input voltages at VDD/2 when inverting inputs are left floating (device fed with a single ended reference).
Output Clocks			
12 11 9 8	OUT0_p OUT0_n OUT1_p OUT1_n	O	**Ultra-Low Additive Jitter Differential HCSL Outputs 0 to 1** Output frequency range 0 to 400MHz
Control			
13 10	OE0_b OE1_b	I_{PD}	**Output Enable.** Logic level on these pins enables/disables corresponding outputs. OEn_b: 0 → OUTn_p/n: Active OEn_b: 1 → OUTn_p/n: High-Z (outputs p/n will be low/low because of 50Ω shunt resistors—see recommended output termination)
Power and Ground			

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1	VDD	P	**Positive Supply Voltage.** Connect to 3.3V or 2.5V supply.
6 15	VDDO	P	**Positive Supply Voltage for Differential Outputs** Connect 3.3V or 2.5V power supply. VDDO does not have to be connected to the same voltage level as VDD.
3 18	IC0 IC1	I_{PD}	**Internal Connection** For normal operation connect to VDD or pull-up with 1kΩ resistor.
4 5 16 17	NC	NC	**No Connect** Leave open
2 7 14	GND	P	**Ground** Connect to the ground
E-Pad	GND	P	**Ground.** Connect to the ground

Functional Description

The ZL40262 is an ultra-low additive jitter, low power 1 to 2 HCSL fanout buffer.

The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

Clock Inputs

The following blocks diagram shows how to terminate different signals fed to the ZL40262 inputs.

Figure 3 and Figure 4 show how to terminate the input when driven from an HCSL driver.

The input buffer in ZL40262 in a native HCSL receiver so other differential formats need to be AC coupled as shown in Figure 5 and Figure 6 for LVPECL and LVDS signals respectively.

Figure 7 shows how to terminate a single ended output such as LVCMOS. Ideally, resistors R1 and R2 should be 100Ω each and Ro + Rs should be 50Ω so that the transmission line is terminated at both ends with characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor R_S should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (Table 5). The source resistors of Rs = 270Ω could be used for standard LVCMOS driver. This will provide 516mV of voltage swing for 3.3V LVCMOS driver with load current of (3.3V/2) *(1/(270Ω + 50Ω)) = 5.16mA.
For optimum performance both differential input pins (_p and _n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.

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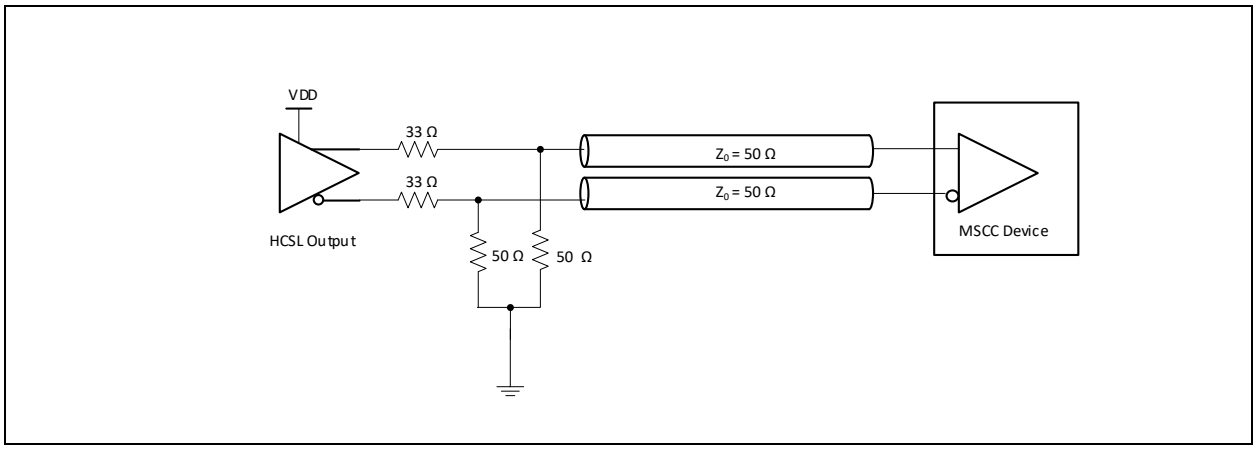


Figure 3. Input driven by source terminated HCSL

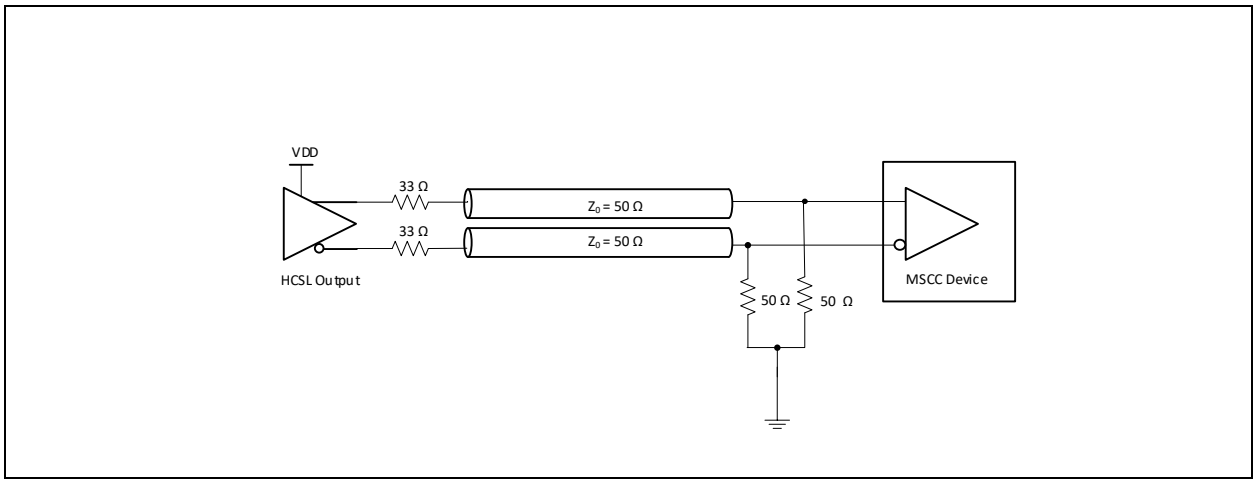


Figure 4. Input driven by receiver terminated HCSL

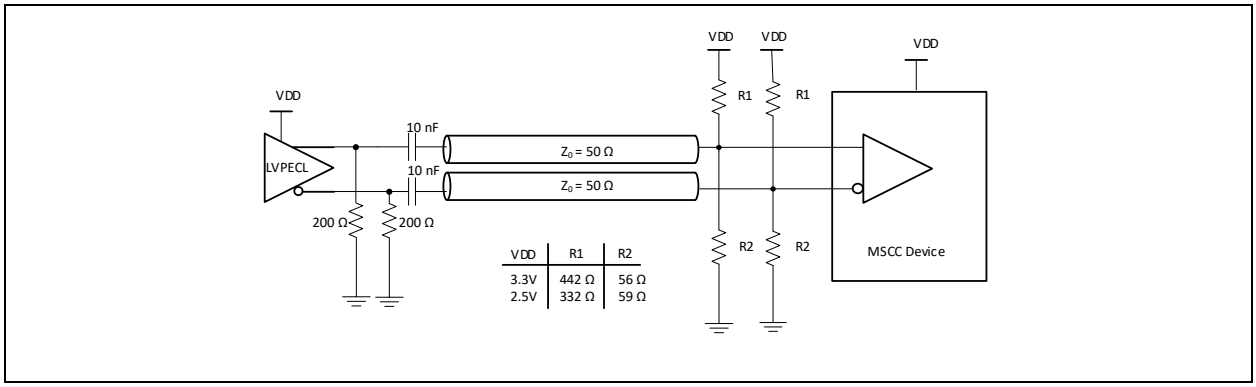


Figure 5. Input driven by AC coupled LVPECL output

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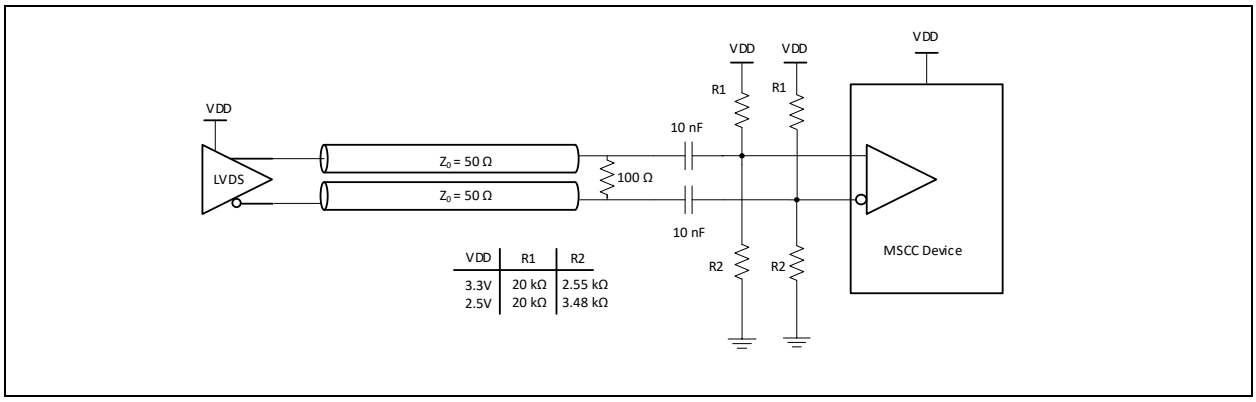


Figure 6. Input driven by AC coupled LVDS

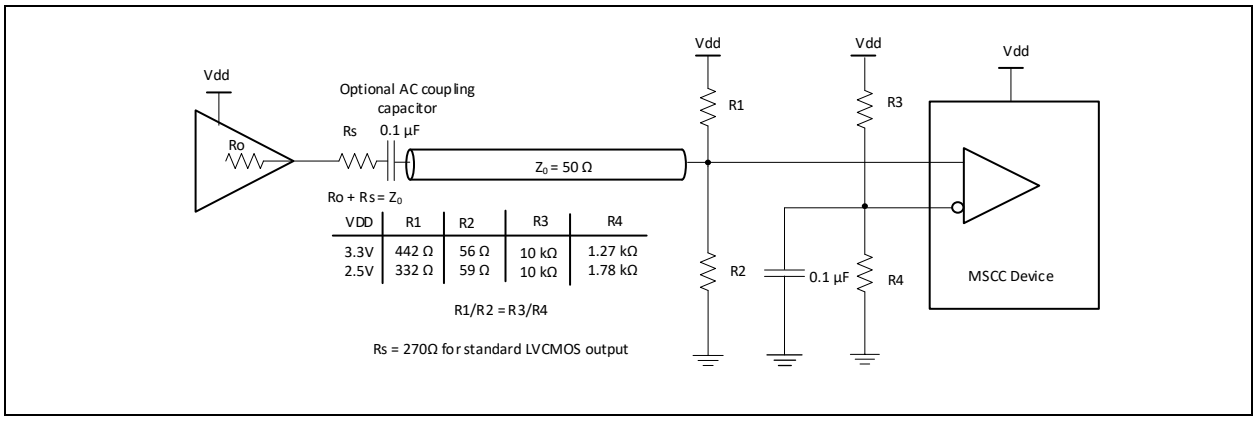


Figure 7. Input driven by a single ended output

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Clock Outputs

Differential HCSL outputs should be terminated as shown in Figure 8 or Figure 9.

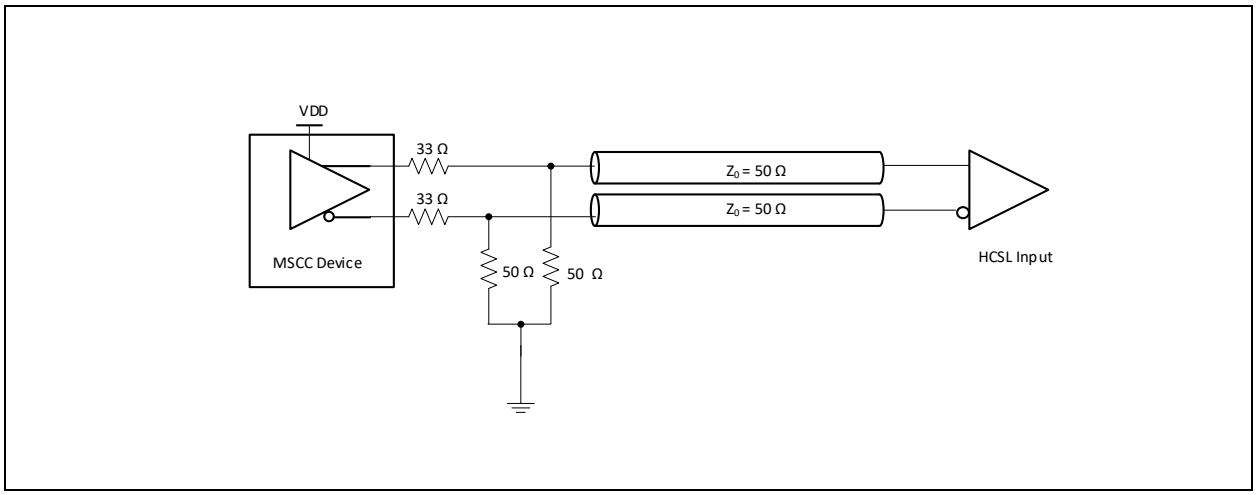


Figure 8. Source terminated HCSL

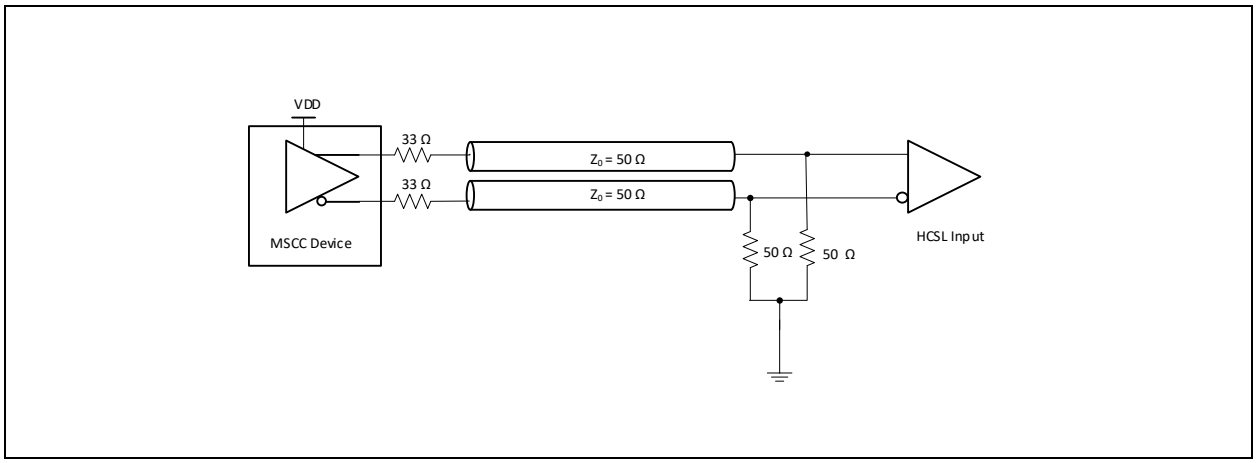


Figure 9. Receiver terminated HCSL

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Termination of unused outputs

Unused outputs should be left unconnected.

Power Consumption

The device total power consumption can be calculated as:

$P_T = P_S + P_C + P_{O_DIFF}$

Where:

$P_S = V_{DD} * I_S$	Core power consumed by the input buffer. The static current (I_S) is specified in Table 4.
$P_C = V_{DDO} * I_{DD_CM}$	Common output power shared between two outputs. The current I_{DD_CM} is specified in Table 4.
$P_{O_DIF} = V_{DDO} * I_{DD_HCSL} * N$	Output power where output current per output (I_{DD_HCSL}) is specified in Table 4. N is number of enabled outputs.

Power dissipated inside the device can be calculated by subtracting power dissipated in termination/biasing resistors from the power consumption:

$P_D = P_T – N * P_{HCSL}$

Where:

$P_{HCSL} = (V_{SW} / 50\Omega)^2 * (50\Omega + 33\Omega)$	V_{SW} is voltage swing of HCSL output. 50Ω is termination resistance and 33Ω is series resistance of the HCSL output.

Power Supply Filtering

Each power pin (VDD and VDDO) should be decoupled with 0.1µF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example, 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board each power supply could optionally be further insulated with low resistance ferrite bead with 10µF and 1µF capacitors. Following figure shows the standard and optional decoupling method.

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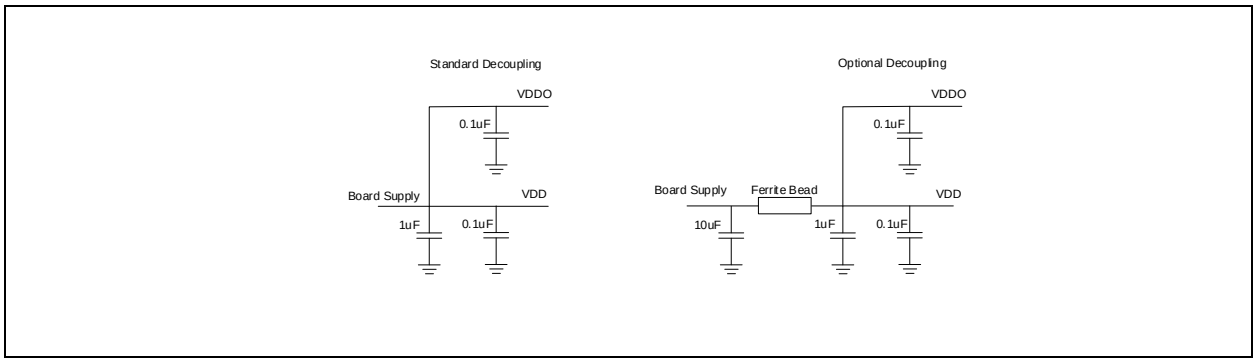


Figure 10. Power Supply Filtering

Power Supplies and Power-up Sequence

The device has two different power supplies: VDD and VDDO which should always be connected to the same voltage supply. Voltages supported by each of these power supplies are specified in Table 3.

VDD and VDDO should always be turned on and off at the same time.

Device Control

ZL40262 outputs are controlled via OE[1:0]_b pins. When an OE_b pin is low the corresponding outputs will be active and when this pin is high the output will be high-Z. When the output driver is in high-Z mode, the output pins will be pulled low via external 50Ω HCSL termination resistors.

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Typical phase noise performance

The following plots show typical phase noise performance for 100 MHz, 133 MHz and 400 MHz respectively.

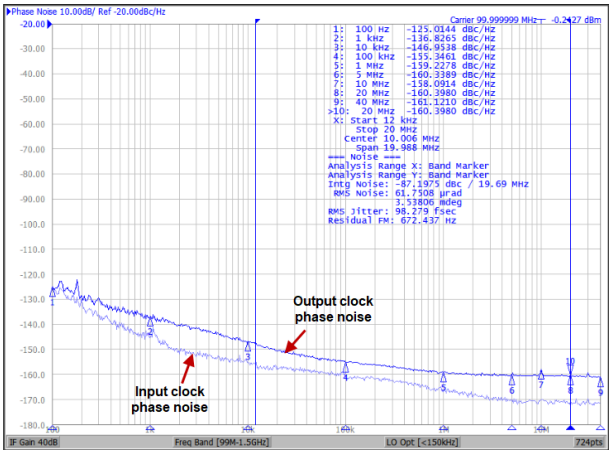


Figure 11. 100MHz HCSL Phase Noise

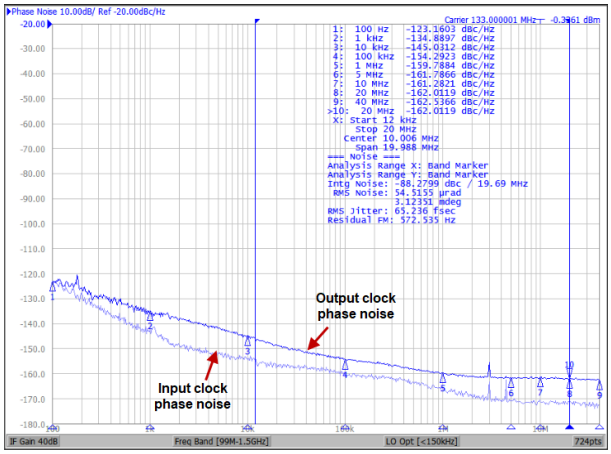


Figure 12. 133MHz HCSL Phase Noise

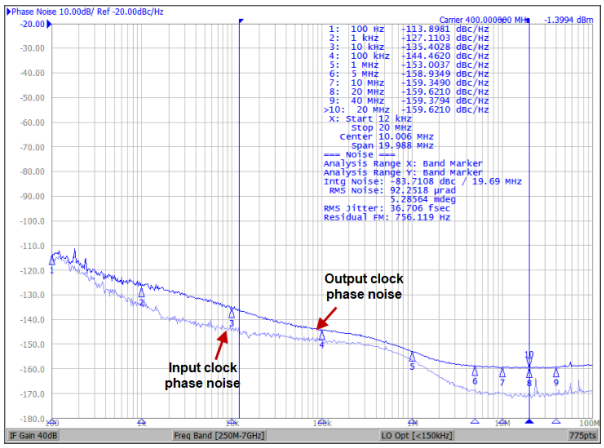


Figure 13. 400MHz HCSL Phase Noise

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AC and DC Electrical Characteristics

Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings*

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage (3.3V)	V_{DD} /V_{DDO}	-0.5		4.6	V	
2	Supply voltage (2.5V)	V_{DD} /V_{DDO}	-0.5		3.5	V	
3	Storage temperature	T_{ST}	-55		125	°C	

* Exceeding these values may cause permanent damage
* Functional operation under these conditions is not implied
* Voltages are with respect to ground (GND) unless otherwise stated

Recommended Operating Conditions

Table 3 Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage 3.3V	V_{DD} /V_{DDO}	3.135	3.30	3.465	V	
2	Supply voltage 2.5V	V_{DD} /V_{DDO}	2.375	2.50	2.625	V	
5	Operating temperature	T_A	-40	25	85	°C	
6	Input voltage	V_{DD-IN}	- 0.3		V_{DD} + 0.3	V	

* Voltages are with respect to ground (GND) unless otherwise stated
* The device core supports two power supply modes (3.3V and 2.5V)

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Table 4 Current consumption

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Core device current	$I_{s_3.3V}$		49	53	mA	VDD= 3.3V+5%
		$I_{s_2.5V}$		48	53	mA	VDD = 2.5V+5%
2	Common output current	$I_{DD_CM_3.3V}$		5.24	5.82	mA	VDDO= 3.3V+5%
		$I_{DD_CM_2.5V}$		4.72	5.32	mA	VDDO= 2.5V+5%
3	Current dissipation per HCSL output	$I_{DD_HCSL_3.3V}$		14.92	17.18	mA	VDDO= 3.3V+5%
		$I_{DD_HCSL_2.5V}$		14.61	16.62	mA	VDDO= 2.5V+5%

Table 5 Input Characteristics*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1a	CMOS high-level input voltage for control inputs	$V_{CIH_3.3V}$	0.7 * V_{DD}			V	V_{DD} = 3.3V
1b	CMOS high-level input voltage for control inputs	$V_{CIH_2.5V}$	0.8 * V_{DD}			V	V_{DD} = 2.5V
2	CMOS low-level input voltage for control inputs	V_{CIL}			0.32 * V_{DD}	V	
3	CMOS input leakage current for control inputs (includes current due to pull down resistors)	I_{IL}	-25		50	µA	V_I = V_{DD} or 0 V
4	Differential input common mode voltage for IN_p/n	V_{CM}	0.1		0.8	V	
5	Differential input voltage for IN_p/n	V_{ID}	0.2		V_{DD} + 0.3	V	
6	Differential input leakage current for IN_p/n (includes current due to pull-up and pull-down resistors)	I_{IL}	-150		150	µA	V_I = 2V or 0V
7	Single ended input voltage for IN_p	V_{SI}	-0.3		2.7	V	VDD = 3.3V or 2.5V
8	Single ended input common mode voltage IN_p	V_{SIC}	0.1		0.8	V	VDD = 3.3V or 2.5V
9	Single ended input voltage swing for IN_p	V_{SID}	0.3		1.3	V	VDD = 3.3V or 2.5V
10	Input frequency (differential)	f_{IN}	0		400	MHz	
11	Input duty cycle	dc	35%		65%		
13	Input slew rate	slew	0.6	2		V/ns	
14	Input pull-up/ pull-down resistance	R_{PU}/R_{PD}		60		kΩ	
15	Input pull-down resistance for IN_p	R_{PD}		30		kΩ	
16	Control input (OE_b) pull-down resistance	R_{PDOE}		300		kΩ	

* Values are over Recommended Operating Conditions
* Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V)
(1) low frequency only

Table 6 Power Supply Rejection Ratio for VDD = VDDO = 3.3V*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	PSRR for HCSL output	$PSRR_{HCSL}$		-80.7		dBc	f_{IN} = 100 MHz
				-76.4			f_{IN} = 133 MHz
				-66.5			f_{IN} = 400 MHz

* Values are over Recommended Operating Conditions
* Noise injected to VDD/VDDO power supply with frequency 100 kHz and amplitude 100 mVpp
* PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot

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Table 7 Power Supply Rejection Ratio for VDD = VDDO = 2.5V*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
3	PSRR for HCSL output	$PSRR_{HCSL}$		-73.5		dBc	f_{IN} = 100 MHz
				-69.8			f_{IN} = 133 MHz
				-61.2			f_{IN} = 400 MHz

* Values are over Recommended Operating Conditions
* Noise injected to VDD/VDDO power supply with frequency 100 kHz and amplitude 100 mVpp
* PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot

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Table 8 HCSL Outputs for VDDO = 3.3V*

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	Rising edge rate	Rise_rate	1.3	1.7	2	V/ns	(2), (3)
2	Falling edge rate	Fall_rate	1.3	1.7	2	V/ns	(2), (3)
3	Differential High Voltage	V_{IH}	0.6		0.9	V	(2)
4	Differential Low Voltage	V_{IL}	-0.9		-0.6	V	(2)
5	Single ended high voltage	V_{SIH}	0.6	0.74	0.85	V	DC Measurement
6	Single ended low voltage	V_{SIL}	-0.01	0	0.01	V	DC Measurement
7	Absolute Crossing Voltage	V_{CROSS}	0.26	0.32	0.38	V	(1), (4), (5)
8	Variation of V_{CROSS} over all rising clock edges	ΔV_{CROSS}	0.039	0.050	0.061	V	(1), (4), (9)
9	Ring back voltage margin	V_{RB}	0.534	0.674	0.809	V	(2), (11)
10	Time before V_{RB} is allowed	t_{STABLE}	4.6			ns	(2), (11)
11	Cycle-to-cycle additive jitter	T_{JCC}		6.5	8.1	ps peak to peak	(2)
12	Absolute Maximum voltage	V_{MAX}			0.92		(1), (7)
13	Absolute Minimum voltage	V_{MIN}	-0.05				(1), (8)
14	Output Duty-Cycle (when input has 50% duty-cycle)	Duty_cycle	48	50	52	%	(2)
15	Rising to falling edge matching	r/f match			15	%	(1), (12)
16	Clock Source DC impedance (CK)	$Z_{C\text{-}DC_CK}$	49	50	51	Ω	DC Measurement (1), (13)
17	Clock Source DC impedance (CK#)	$Z_{C\text{-}DC_CK\#}$	49	50	51	Ω	DC Measurement (1), (13)
18	Output frequency	F_{MAX}	0		400	MHz	
19	Output to output skew	t_{OOSK}			50	ps	
20	Device to device output skew	t_{DOOSK}			129	ps	
21	Input to output delay	t_{IOD}	0.75	0.84	1	ns	
22	Output enable time	t_{EN}			3	cycles	
23	Output disable time	t_{DIS}			3	cycles	

* Values are over Recommended Operating Conditions

(1) Measurement taken from single ended waveform

(2) Measurement taken from differential waveform.

(3) Measured from -150 mV to +150 mV on the differential waveform (derived from CK minus CK#) The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 17

(4) Measured at crossing point where the instantaneous voltage value of the rising edge of CK equals the falling edge of CK# . See Figure 14

(5) Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 14.

(6) This requirement, from PCI Express Base Specification, Revision 4.0 is applicable only to clock generators and not to buffers. A clock buffer is a transparent device whose output clock period follows the input clock period.

(7) Defined as the maximum instantaneous voltage including overshoot. See Figure 14.

(8) Defined as the minimum instantaneous voltage including undershoot. See Figure 14.

(9) Defined as the total variation of all crossing voltages of Rising CK and Falling CK# This is the maximum allowed variance in VCROSS for any particular system. See Figure 15.

(10) The PPM requirement from PCIe Express Base Specification, Revision 4.0 is related to clock generation devices. This requirement is not applicable to buffers because buffer's output frequency accuracy is identical to the frequency accuracy of the source driving the buffer.

(11) TSTABLE is the time the differential clock must maintain a minimum ±150 mV differential voltage after20 rising/falling edges before it is allowed to droop back into the VRB ±100 mV differential range. See Figure 18.

(12) Matching applies to rising edge rate for CKx and falling edge rate for CK#x. It is measured using a ±75 mV window centered on the median cros point where CKx rising meets CK#x falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of CKx should be compared to the Fall Edge Rate of CK#x the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 16.

(13) Clock DC impedance tolerance depends only on the tolerance of external 50Ω shunt resistors used in HCSL. The test used resistors with +/-1% tolerance.

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Table 9 HCSL (PCIe) Jitter Performance for VDDO = 3.3V

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	Additive Jitter as per PCIe 1.0 (1.5MHz to 22MHz)	$T_{jPCIe_1.0}$		1.2	1.45	ps pk-pk	Input clock: 100 MHz
2	Additive Jitter as per PCIe 2.0 high band (1.5MHz to 50MHz)	$T_{jPCIe_2.0_high}$		134	163	fs RMS	Input clock: 100 MHz
3	Additive Jitter as per PCIe 2.0 low band (10kHz to 1.5MHz)	$T_{jPCIe_2.0_low}$		31	48	fs RMS	Input clock: 100 MHz
4	Additive Jitter as per PCIe 2.0 mid band (5MHz to 16MHz)	$T_{jPCIe_2.0_mid}$		105	130	fs RMS	Input clock: 100 MHz
5	Additive Jitter as per PCIe 3.0 (PLL_BW = 2 to 5MHz, CDR = 10MHz)	$T_{jPCIe_3.0}$		33	41	fs RMS	Input clock: 100 MHz
6	Additive Jitter as per PCIe 4.0 (PLL_BW = 2 to 5MHz, CDR = 10MHz)	$T_{jPCIe_4.0}$		33	41	fs RMS	Input clock: 100 MHz
7	Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 to 1.8MHz, CDR for 32 GT/s CC)	$T_{jPCIe_5.0}$		13	16	fs RMS	Input clock: 100 MHz
8	Additive jitter as per Intel QPI 9.6Gbps	T_{jQPI}		61	75	fs RMS	Input clock: 100 MHz
9	Additive RMS jitter in 1MHz to 20MHz band	$T_{j_1M_20M}$		87	106	fs RMS	Input clock: 100 MHz
				56	68	fs RMS	Input clock: 133 MHz
				26	34	fs RMS	Input clock: 400 MHz
10	Additive RMS jitter in 12kHz to 20MHz band	$T_{j_12k_20M}$		91	112	fs RMS	Input clock: 100 MHz
				60	75	fs RMS	Input clock: 133 MHz
				32	48	fs RMS	Input clock: 400 MHz
11	Noise floor	NF		-161	-159	dBc/Hz	Input clock: 100 MHz
				-162	-161	dBc/Hz	Input clock: 133 MHz
				-160	-157	dBc/Hz	Input clock: 400 MHz

* Values are over Recommended Operating Conditions

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Table 10 HCSL Outputs for VDDO = 2.5V*

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	Rising edge rate	Rise_rate	1.3	1.6	1.9	V/ns	(2), (3)
2	Falling edge rate	Fall_rate	1.3	1.6	1.9	V/ns	(2), (3)
3	Differential High Voltage	V_{IH}	0.6		0.9	V	(2)
4	Differential Low Voltage	V_{IL}	-0.9		-0.6	V	(2)
5	Single ended high voltage	V_{SIH}	0.58	0.71	0.84	V	DC Measurement
6	Single ended low voltage	V_{SIL}	-0.01	0	0.01	V	DC Measurement
7	Absolute Crossing Voltage	V_{CROSS}	0.25	0.31	0.37	V	(1), (4), (5)
8	Variation of V_{CROSS} over all rising clock edges	ΔV_{CROSS}	0.04	0.05	0.06	V	(1), (4), (9)
9	Ring back voltage margin	V_{RB}	0.514	0.660	0.791	V	(2), (11)
10	Time before V_{RB} is allowed	t_{STABLE}	4.6			ns	(2), (11)
11	Additive Cycle-to-cycle jitter	T_{JCC}		5.5	7.1	ps peak to peak	(2)
12	Absolute Maximum voltage	V_{MAX}			0.90		(1), (7)
13	Absolute Minimum voltage	V_{MIN}	-0.05				(1), (8)
14	Output Duty-Cycle (when input has 50% duty-cycle)	Duty_cycle	48	50	52	%	(2)
15	Rising to falling edge matching	r/f match			15	%	(1), (12)
16	Clock Source DC impedance (CK)	$Z_{C\text{-}DC_CK}$	49	50	51	Ω	DC Measurement (1), (13)
17	Clock Source DC impedance (CK#)	$Z_{C\text{-}DC_CK\#}$	49	50	51	Ω	DC Measurement (1), (13)
18	Output frequency	F_{MAX}	0		400	MHz	
19	Output to output skew	t_{OOSK}			50	ps	
20	Device to device output skew	t_{DOOSK}			129	ps	
21	Input to output delay	t_{IOD}	0.75	0.85	1	ns	
22	Output enable time	t_{EN}			3	cycles	
23	Output disable time	t_{DIS}			3	cycles	

* Values are over Recommended Operating Conditions

(1) Measurement taken from single ended waveform

(2) Measurement taken from differential waveform.

(3) Measured from -150 mV to +150 mV on the differential waveform (derived from CK minus CK#) The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 17

(4) Measured at crossing point where the instantaneous voltage value of the rising edge of CK equals the falling edge of CK# . See Figure 14

(5) Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 14.

(6) This requirement, from PCI Express Base Specification, Revision 4.0 is applicable only to clock generators and not to buffers. A clock buffer is a transparent device whose output clock period follows the input clock period.

(7) Defined as the maximum instantaneous voltage including overshoot. See Figure 14.

(8) Defined as the minimum instantaneous voltage including undershoot. See Figure 14.

(9) Defined as the total variation of all crossing voltages of Rising CK and Falling CK# This is the maximum allowed variance in VCROSS for any particular system. See Figure 15.

(10) The PPM requirement from PCIe Express Base Specification, Revision 4.0 is related to clock generation devices. This requirement is not applicable to buffers because buffer's output frequency accuracy is identical to the frequency accuracy of the source driving the buffer.

(11) TSTABLE is the time the differential clock must maintain a minimum ±150 mV differential voltage after20 rising/falling edges before it is allowed to droop back into the VRB ±100 mV differential range. See Figure 18.

(12) Matching applies to rising edge rate for CKx and falling edge rate for CK#x. It is measured using a ±75 mV window centered on the median cros point where CKx rising meets CK#x falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of CKx should be compared to the Fall Edge Rate of CK#x the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 16.

(13) Clock DC impedance tolerance depends only on the tolerance of external 50Ω shunt resistors used in HCSL. The test used resistors with +/-1% tolerance.

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Table 11 HCSL (PCIe) Jitter Performance for VDDO = 2.5V

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	Additive Jitter as per PCIe 1.0 (1.5MHz to 22MHz)	$T_{jPCIe_1.0}$		1.03	1.27	ps pk-pk	Input clock: 100MHz
2	Additive Jitter as per PCIe 2.0 high band (1.5MHz to 50MHz)	$T_{jPCIe_2.0_high}$		115	143	fs RMS	Input clock: 100MHz
3	Additive Jitter as per PCIe 2.0 low band (10kHz to 1.5MHz)	$T_{jPCIe_2.0_low}$		28	46	fs RMS	Input clock: 100MHz
4	Additive Jitter as per PCIe 2.0 mid band (5MHz to 16MHz)	$T_{jPCIe_2.0_mid}$		91	113	fs RMS	Input clock: 100MHz
5	Additive Jitter as per PCIe 3.0 (PLL_BW = 2 to 5MHz, CDR = 10MHz)	$T_{jPCIe_3.0}$		29	36	fs RMS	Input clock: 100MHz
6	Additive Jitter as per PCIe 4.0 (PLL_BW = 2 to 5MHz, CDR = 10MHz)	$T_{jPCIe_4.0}$		29	36	fs RMS	Input clock: 100MHz
7	Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 to 1.8MHz, CDR for 32 GT/s CC)	$T_{jPCIe_4.0}$		11	14	fs RMS	Input clock: 100MHz
8	Additive jitter as per Intel QPI 9.6Gbps	T_{jQPI}		53	67	fs RMS	Input clock: 100MHz
9	Additive RMS jitter in 1MHz to 20MHz band	$T_{j_1M_20M}$		75	94	fs RMS	Input clock: 100 MHz
				51	64	fs RMS	Input clock: 133 MHz
				26	33	fs RMS	Input clock: 400 MHz
10	Additive RMS jitter in 12kHz to 20MHz band	$T_{j_12k_20M}$		79	99	fs RMS	Input clock: 100 MHz
				55	68	fs RMS	Input clock: 133 MHz
				32	47	fs RMS	Input clock: 400 MHz
11	Noise floor	N_F		-162	-159	dBc/Hz	Input clock: 100 MHz
				-163	-161	dBc/Hz	Input clock: 133 MHz
				-160	-158	dBc/Hz	Input clock: 400 MHz

* Values are over Recommended Operating Conditions

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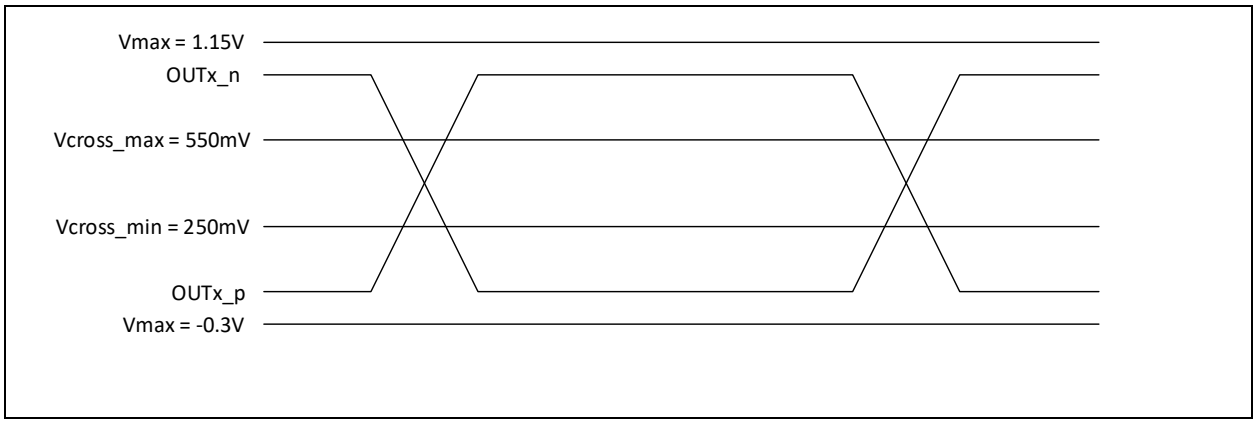


Figure 14. Single-Ended Measurement Points for Absolute Cross Point and Swing

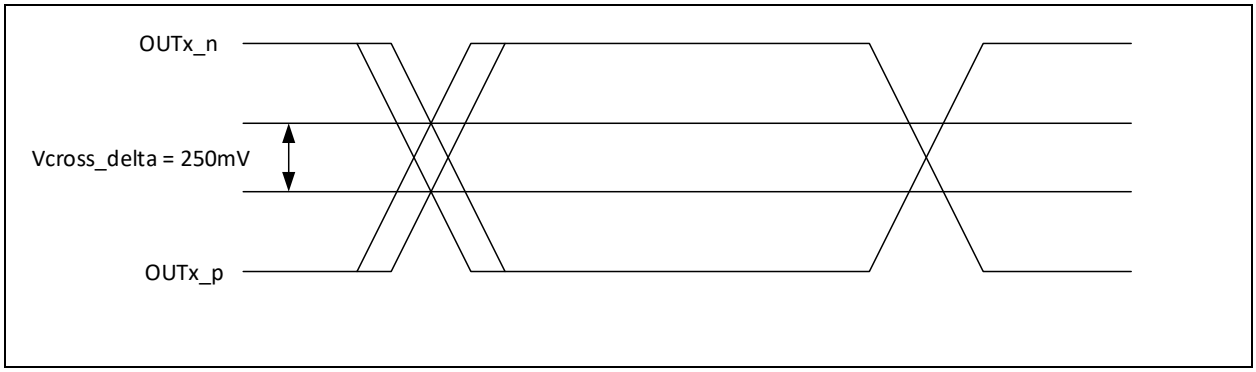


Figure 15. Single-Ended Measurement Points for Delta Cross Point

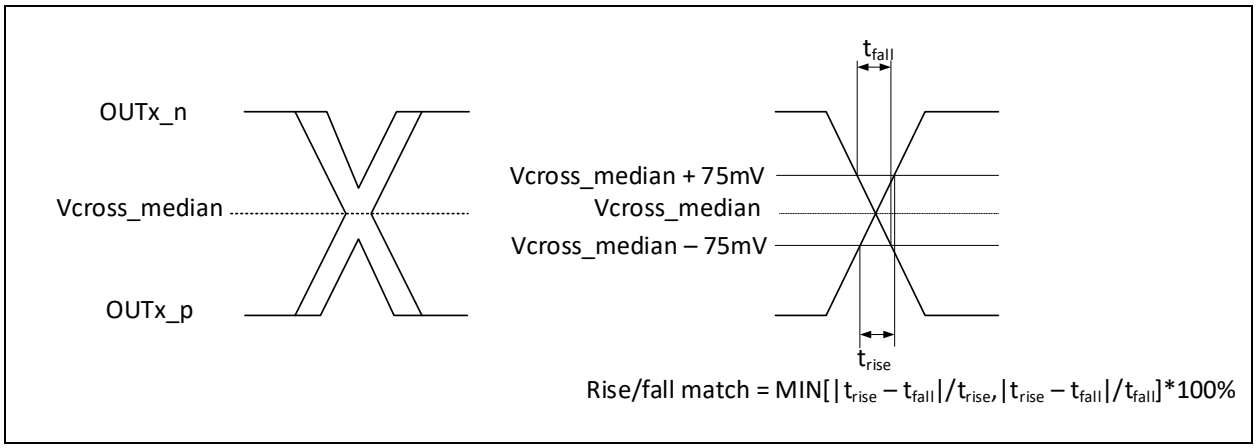


Figure 16. Single-Ended Measurement Points for Rise and Fall Time Matching

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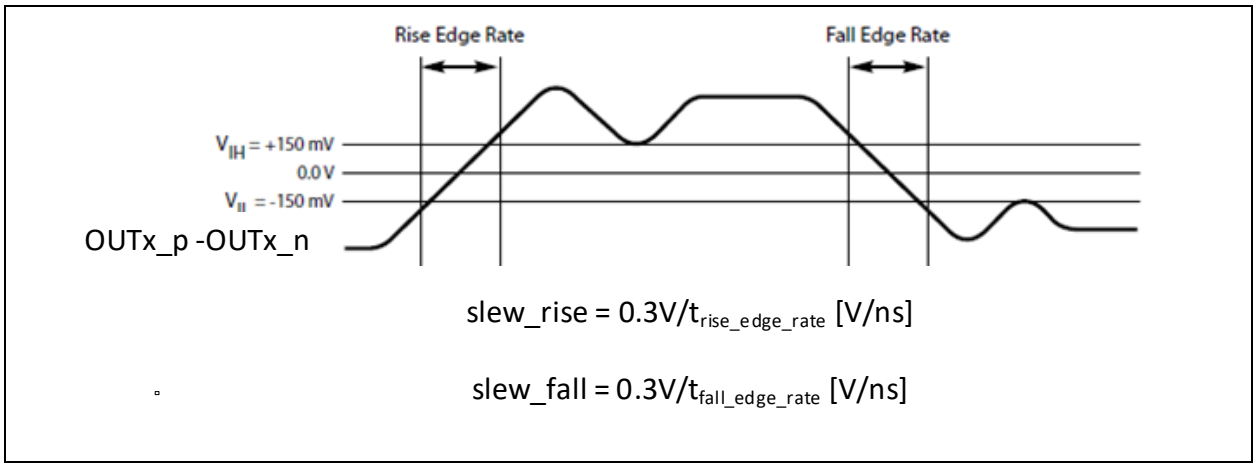


Figure 17. Differential Measurement Points for Rise and Fall Time

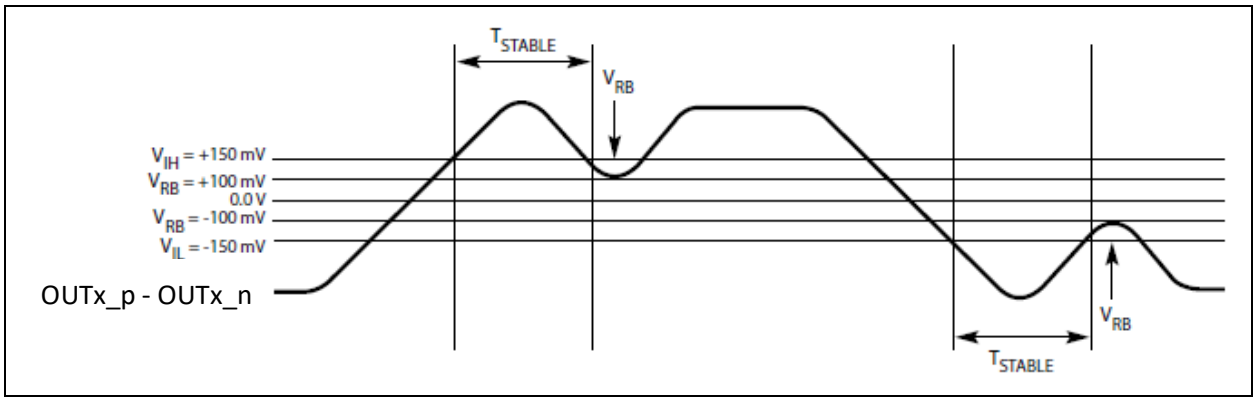


Figure 18. Differential Measurement Points for Ringback

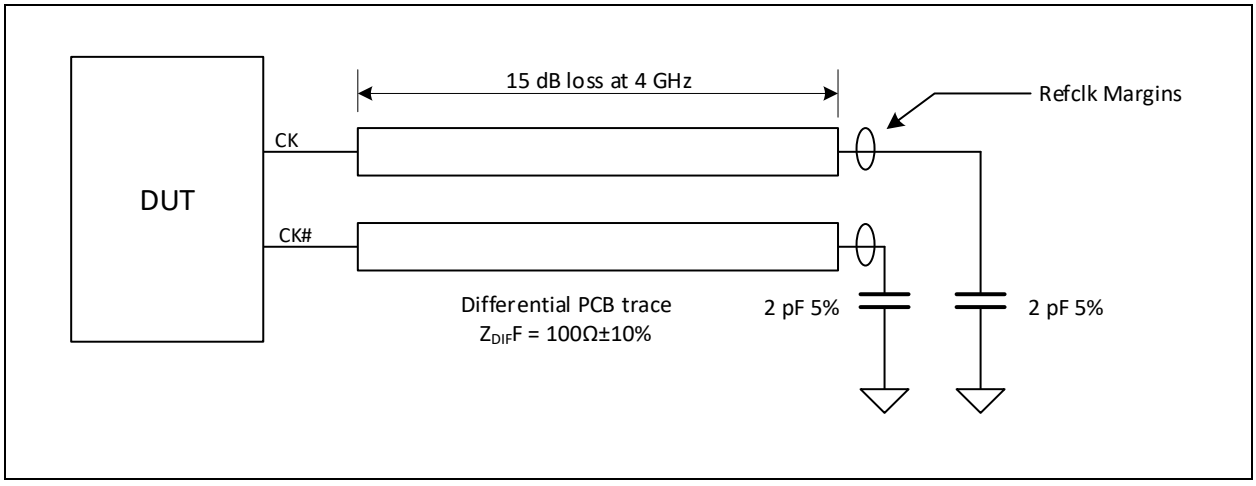


Figure 19. Test Circuit

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Table 12 4x4mm QFN Package Thermal Properties

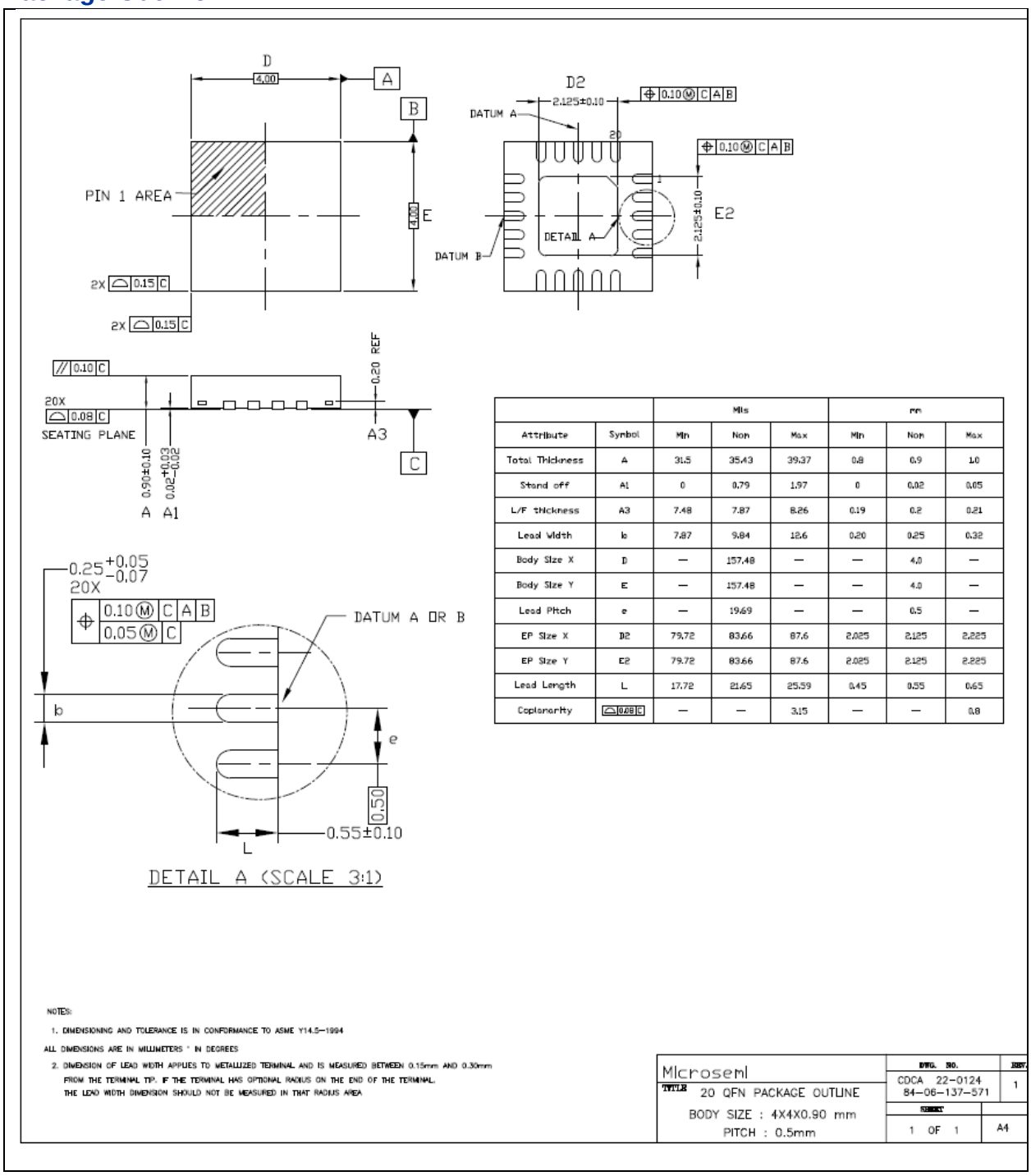
Parameter	Symbol	Conditions	Value	Units
Maximum Ambient Temperature	T_A		85	°C
Maximum Junction Temperature	T_{JMAX}		125	°C
Junction to Ambient Thermal Resistance(1)	θ_{JA}	still air	34	°C/W
		1m/s airflow	28.9	
		2.5m/s airflow	27.0	
Junction to Board Thermal Resistance	θ_{JB}		15.4	°C/W
Junction to Case Thermal Resistance	θ_{JC}		25.9	°C/W
Junction to Pad Thermal Resistance(2)	θ_{JP}	Still air	8.1	°C/W
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	Still air	1.0	°C/W

(1) Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on a 4-layer JEDEC standard test board and dissipating maximum power

(2) Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package)

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Package Outline



		Mls			mm		
Attribute	Symbol	Min	Nom	Max	Min	Nom	Max
Total Thickness	A	31.5	35.43	39.37	0.8	0.9	1.0
Stand off	A1	0	0.79	1.97	0	0.02	0.05
L/F thickness	A3	7.48	7.87	8.26	0.19	0.2	0.21
Lead Width	b	7.87	9.84	12.6	0.20	0.25	0.32
Body Size X	D	—	157.48	—	—	4.0	—
Body Size Y	E	—	157.48	—	—	4.0	—
Lead Pitch	e	—	19.69	—	—	0.5	—
EP Size X	D2	79.72	83.66	87.6	2.025	2.125	2.225
EP Size Y	E2	79.72	83.66	87.6	2.025	2.125	2.225
Lead Length	L	17.72	21.65	25.59	0.45	0.55	0.65
Coplanarity	0.08 C	—	—	3.15	—	—	0.8

NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5–1994

ALL DIMENSIONS ARE IN MILLIMETERS ' IN DEGREES

2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Microsemi	DWG. NO.	REV.
TITLE: 20 QFN PACKAGE OUTLINE	CDCA 22-0124 84-06-137-571	1
BODY SIZE : 4X4X0.90 mm	SHEET	
PITCH : 0.5mm	1 OF 1	A4

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Change history:

June 2019 revision-Initial release

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Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

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