
PIC18F26/45/46Q10 Family Silicon Errata and Data Sheet Clarifications

The PIC18F26/45/46Q10 devices that you have received conform functionally to the current device data sheet (DS40001996C), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F26/45/46Q10 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID
		A5
PIC18F26Q10	0x7180	0xA045
PIC18F45Q10	0x7140	0xA045
PIC18F46Q10	0x7120	0xA045



Important: Refer to the **Device/Revision ID** section in the current “**PIC18F2X/4XQ10 Memory Programming Specification**” (DS40001874) for more detailed information on Device Identification and Revision IDs for your specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions
				A5
Electrical Specifications	Sleep current	1.1.1	Higher current after DFM write	X
Resets	$\overline{\text{RMCLR}}$ Flag	1.2.1	POR may clear the $\overline{\text{RMCLR}}$ bit by mistake	X
CWG	Auto shutdown sources	1.3.1	CLC2 and CLC6 not available	X
ADCC	FVR reference	1.4.1	Missing codes when FVR used as reference	X
ADCC	Burst average	1.4.2	ADCNT may not increment	X
ADCC	ADCRC (FRC) oscillator	1.4.3	Oscillator continues to run in sleep after conversion	X
ADCC	ADC Conversions	1.4.4	Unreliable conversion results with fast falling slew rate	X
Windowed Watchdog Timer	Window Operation	1.5.1	Window feature of the WWDT does not operate correctly in DOZE mode	X
NVM	NVMERR	1.6.1	NVMERR bit is set by device Reset after being cleared by software	X
NVM	Self Writes	1.6.2	Do not write above 100° C	X
MSSP	SPI	1.7.1	SSPBUF may be corrupted by writes to other GPR/SFRs	X
Oscillator	HFINTOSC	1.8.1	5% variation over temperature range	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

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1. Silicon Errata Issues



Notice: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Electrical Specifications

1.1.1 Sleep Current - Higher Sleep Current after DFM Write Operation

When performing a DFM write operation during Sleep mode, once the write operation has completed, the system clock will stay active. This means that while the device remains in this state, a higher Sleep current will be experienced.

Work around

Once the DFM write operation is completed, wake the device out of Sleep mode and re-execute a new Sleep command.

Affected Silicon Revisions

A5							
X							

1.2 Module: Resets

1.2.1 RMCLR Flag in PCON0 Register by Mistake

On an initial power-up of the device, or when executing a software Reset, the PCON0 flag bit for MCLR Reset (\overline{RMCLR}) may be improperly cleared by a Power-on Reset (\overline{POR}) or software Reset (\overline{RI}), thereby indicating a false MCLR event.

Work around

None.

Affected Silicon Revisions

A5							
X							

1.3 Module: Complementary Waveform Generator (CWG)

1.3.1 CWG Auto-Shutdown Sources

Shutdown sources AS6E (CLC2_out) and AS7E (CLC6_out) are not available.

Work around

Route the CLC output through PPS to an output pin and use the AS0E source selection (Pin selected by CWGxPPS) and PPS controls to select the same pin as the shutdown source.

Affected Silicon Revisions

A5							
X							

1.4 Module: Analog-to-Digital Converter with Computation (ADCC)

1.4.1 Missing Codes with FVR Reference

Using the FVR as the positive voltage reference for the ADC can cause an increase in missing codes.

Work around

Method 1:

Increase the bit conversion time, known as TAD, to 8 μs or higher.

Method 2:

Use V_{DD} as the positive voltage reference to the ADC.

Affected Silicon Revisions

A5							
X							

1.4.2 ADC² Burst Average Mode

When the ADC² is operated in Burst Average mode (ADMD = 0b011 in the ADCON2 register) while enabling non-continuous operation and double-sampling (ADCONT = 0 in the ADCON0 register and ADDSEN = 1 in the ADCON1 register), the value in the ADCNT register does not increment beyond '0b1' toward the value in the ADRPT register.

Work around

When operating the ADC² in Burst Average mode with double-sampling, enable continuous operation of the module (ADCONT = 1 in the ADCON0 register) and set the Stop-on-Interrupt bit (ADS0I bit in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and re-trigger ADC² as necessary.

If the CPU is in Low-Power Sleep mode, alternatively the ADC² in non-continuous Burst Average mode can be operated with single ADC conversion (ADDSEN = 0 in the ADCON1 register) compromising noise

immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in the software.

Affected Silicon Revisions

A5							
X							

1.4.3 ADCRC (FRC) Oscillator Operation in Sleep

If the part is in Sleep and the ADCRC (FRC) oscillator is used as clock source to the ADC, the oscillator continues to run after the conversion is complete. This will increase the current consumption in Sleep mode. The oscillator will stop after the device exits Sleep mode and resumes normal code execution.

Work around

None.

Affected Silicon Revisions

A5							
X							

1.4.4 Unreliable Conversion Results with Fast Falling Slew Rate

When the ADC input falls by greater than 3.2V, with a slew rate faster than $-11V/\mu s$, the next ADC conversion will have the MSb improperly set. This is likely to happen when the ADC input channel is switched from one with a high input level to another with a low input level.

Work around

When switching between input channels, discard the first conversion result after the switch. Subsequent conversions will not be affected.

Affected Silicon Revisions

A5							
X							

1.5 Module: Windowed Watchdog Timer (WWDT)

1.5.1 Window Operation in DOZE Mode

When the Windowed mode of operation is enabled in DOZE mode, a window violation error is issued even though the window is open and has been armed. This condition occurs only when the window size is set to a value other than 100% open.

Work around

Method 1:

Use the Windowed mode of operation in any other than DOZE mode. If disabling the DOZE mode is not an option, use the WWDT module without the Window being enabled.

Method 2:

If the device is in DOZE mode, perform the arming process for the window in NORMAL mode and return to the DOZE mode.

Method 3:

If there is an ISR in the application code, the arming within the window can be done inside the ISR with the ROI bit of the CPUDOZE register being set.

Affected Silicon Revisions

A5							
X							

1.6 Module: Nonvolatile Memory (NVM)

1.6.1 NVMERR

When a Reset is issued while an NVM high voltage operation is in progress, the NVMERR bit in the NVMCON0 register is set as expected. After clearing the NVMERR bit, if a Reset reoccurs, the NVMERR bit is set again regardless of whether an NVM operation is in progress or not. A successful write operation will clear the NVMERR condition.

Work around

None.

Affected Silicon Revisions

A5							
X							

1.6.2 PFM Writes above 100° Celsius

Do not perform write operations on the Program Flash Memory (PFM) when the temperature is above 100 degrees Celsius.

Work around

Perform PFM writes below 100 degrees Celsius.

Affected Silicon Revisions

A5							
X							

1.7 Module: Master Synchronous Serial Port (MSSP)

1.7.1 MSSP SPI Slave Mode

When operating in SPI Slave mode, if the incoming SCK clock signal arrives during any of the conditions below, the SSPBUF transmit Shift register may become corrupted. The transmitted slave byte cannot be ensured to be correct, and the state of the WCOL bit may or may not indicate a write collision.

These conditions include:

- A write to an SFR
- A write to RAM following an SFR read
- A write to RAM prior to an SFR read

Work around

Method 1 (Interrupt based using \overline{SS}):

1. Connect the \overline{SS} line to both the \overline{SS} input and either an INT or IOC input pin.
2. Enable INT or IOC interrupts (interrupt on falling edge if available, otherwise check that $\overline{SS} == 0$ when the interrupt occurs).
3. Load SSPBUF with the data to be transmitted.
4. Continue program execution.
5. When the Interrupt Service Routine (ISR) is invoked, do either of the following:
 - 5.1. Add a delay that ensures the first SCK clock will be complete, or
 - 5.2. Poll SSPSTAT.BF (`while(BF == 0)`) and wait for the transmission/reception to complete.

Method 2 (Bit polling based using \overline{SS}):

1. Load SSPBUF with the data to be transmitted.
2. Poll the \overline{SS} line and wait for the \overline{SS} to go active (`while(!PORTx. \overline{SS} == 0)`).
3. When \overline{SS} is active ($\overline{SS} == 0$), do either of the following:
 - 3.1. Add a delay that ensures the first SCK clock will be complete, or
 - 3.2. Poll SSPSTAT.BF (`while(BF == 0)`), and wait for the transmission/reception to complete.

Once one of these two methods are complete, it is safe to return to program execution.

Method 3 (\overline{SS} not available):

1. Load SSPBUF with the data to be transmitted.
2. Poll SSPSTAT.BF (`while(BF == 0)`), and wait for the transmission/reception to complete.

Affected Silicon Revisions

A5							
X							

1.8 Module: Oscillator

1.8.1 Internal HFINTOSC Oscillator Varies Up To 5%

The internal HFINTOSC oscillator varies in frequency up to 5% over the voltage and temperature range.

Work around

For systems requiring more precision, use an external crystal or ceramic resonator in one of the External Oscillator modes.

Affected Silicon Revisions

A5							
X							

2. Data Sheet Clarifications

2.1 None

There are no known data sheet clarifications as of this publication date.

3. Revision History

Doc Rev.	Date	Comments
B	05/2019	Added oscillator drift erratum. Removed data sheet clarifications.
A	03/2019	Initial document release.

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