High Efficiency, Ground-Referenced Class-G Headphone Amplifier

Data Sheet

SSM2932

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FEATURES

- Ground-referenced Class-G output stage
- Very high efficiency for portable applications
- 1.7 mA typical quiescent current
- 50 mW per channel into 16 Ω load (with 3.3 V supply)
- 98 dB signal-to-noise ratio (SNR), A-weighted
- 90 dB power supply rejection ratio at 217 Hz
- 2.5 V to 3.6 V supply range
- Selectable gain: 0 dB or 6 dB
- High-Z output mode for sharing of output jack
- 1 µA shutdown current
- Short-circuit protection
- Pop-and-click reduction circuitry
- 8 kV ESD protection on output terminals
- 16-ball, 0.4 mm pitch WLCSP (1.64 mm × 1.64 mm)
- −40°C to +85°C operating temperature range

APPLICATIONS

- Cell phones
- Smartphones/multimedia phones
- Digital cameras
- Portable media players
- Phone accessories
- PDAs

GENERAL DESCRIPTION

The SSM2932 is a stereo headphone amplifier capable of delivering 50 mW of continuous output power per channel into 16 Ω single-ended loads at the 1% THD + N threshold. The stereo headphone drivers are high efficiency, true ground-referenced Class-G technology.

The SSM2932 incorporates a gain control pin that selects a gain of 0 dB or 6 dB. The ground-referenced output scheme eliminates the need for large dc blocking capacitors, reducing system cost and board area. The Class-G amplifier is fine-tuned to maximize battery life, a critical task in portable applications. The device maximizes battery life by modulating the amplifier power supply rail to match the output demand without consuming excessive supply current, thus reducing power dissipation during typical audio playback.

The SSM2932 is specified over the industrial temperature range of −40°C to +85°C. It has output short-circuit protection as well as ESD protection to 8 kV (human body model). The SSM2932 is available in a 16-ball, 1.64 mm × 1.64 mm wafer level chip scale package (WLCSP).

FUNCTIONAL BLOCK DIAGRAM

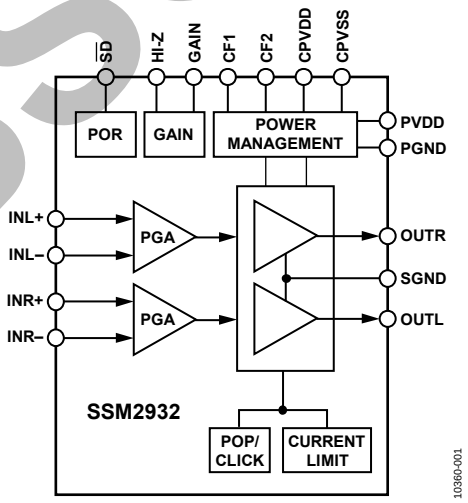


Figure 1.

Rev. 0

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REVISION HISTORY

2/12—Revision 0: Initial Version

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SPECIFICATIONS

PVDD = 3.0 V, C_{CF} = 1 µF, C_{CPVDD} = C_{CPVSS} = 2.2 µF, R_L = 32 Ω, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Voltage Gain	A_V	Input voltage = 100 mV rms				
		GAIN pin high		6		dB
		GAIN pin low		0		dB
Output Power	P_O	f = 1 kHz, THD = 1%				
		R_L = 16 Ω, one channel		85		mW
		R_L = 32 Ω, one channel		50		mW
		R_L = 16 Ω, stereo		40		mW
		R_L = 32 Ω, stereo		45		mW
Total Harmonic Distortion Plus Noise	THD + N	P_O = 10 mW per channel		0.01		%
Gain Matching	ΔA_V				1	%
Frequency Range		Ripple within ±0.5 dB	20		20,000	Hz
Differential Input Impedance	Z_{IN}		12	18	34.5	kΩ
CHARGE PUMP						
Oscillator Frequency	f_{OSC0}	Idle mode, V_{OUT} = 0 V		54		kHz
	f_{OSC1}	Active mode		550		kHz
Headphone Amplifier Supply						
Positive Rail	V_{CPVDD}	Efficiency mode: V_{OUT} < 0.2 V rms		PVDD/2		V
		High power mode: V_{OUT} > 0.2 V rms		2.2		V
Negative Rail	V_{CPVSS}	Efficiency mode: V_{OUT} < 0.2 V rms		−PVDD/2		V
		High power mode: V_{OUT} > 0.2 V rms		−2.2		V
Output Voltage Threshold	V_{TH1}	Transition from efficiency mode to high power mode		285		mV
	V_{TH2}	Transition from high power mode to efficiency mode		375		mV
Charge Pump Transition Time	$t_{RELEASE}$	Charge pump transition from high power mode to efficiency mode		0.8		ms
	t_{ATTACK}	Charge pump transition from efficiency mode to high power mode		10		µs
NOISE PERFORMANCE						
Output Voltage Noise	e_n	BW = 20 kHz, A-weighted, gain = 0 dB		12		µV rms
Signal-to-Noise Ratio	SNR	A-weighted		98		dB
Pop-and-Click Noise	V_{CP}			−60		dBV
Channel Separation	X_{TALK}	Single-ended, 1 V rms, P_O = 31 mW		86		dB
OUTPUT CHARACTERISTICS						
Output Offset Voltage	$\|V_{OS}\|$				0.25	mV
Capacitive Output Drive	C_{LOAD}			150		pF
Slew Rate	SR			1.25		V/µs
STARTUP AND SHUTDOWN		Measured from $\overline{SD}$ rising edge				
Start-Up Time	t_{SU}			20		ms
Shutdown Time	t_{SD}			36		µs
POWER SUPPLY		0°C < T_A < 70°C				
Supply Voltage Range	PVDD	Guaranteed from PSRR test	2.5		3.6	V
Quiescent Current	I_{DD}	R_L = 32 Ω + 200 pF; gain = 0 dB, PVDD = 3 V		1.7		mA
Shutdown Current	I_{SD}	$\overline{SD}$ = GND		1		µA
Power Supply Rejection Ratio	PSRR	V_{RIPPLE} = 100 mV_{PEAK}, gain = 0 dB				
		f = 217 Hz		90		dB
		f = 1 kHz		84		dB
		f = 10 kHz		62		dB

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DIGITAL INPUT SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Input Voltage High	V_{IH}			1.2		V
Input Voltage Low	V_{IL}			0.5		V
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{DD}			±1	µA
Input Capacitance	C_{IN}				5	pF

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Analog Supply Voltage (PVDD)	3.75 V
Input Voltage	1.8 V_{PEAK}
Output ESD, Human Body Model	8 kV
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Ball, 1.64 mm × 1.64 mm WLCSP	66	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

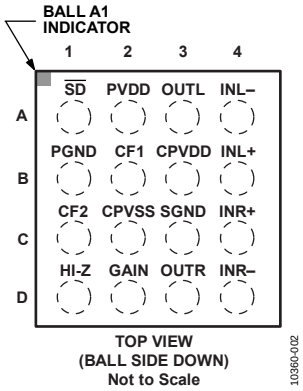


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	$\overline{SD}$	Shutdown Control
B1	PGND	Power Ground
C1	CF2	Charge Pump Flying Capacitor, Terminal 2
D1	HI-Z	Output Impedance Select
A2	PVDD	Power Supply
B2	CF1	Charge Pump Flying Capacitor, Terminal 1
C2	CPVSS	Charge Pump Negative Supply
D2	GAIN	Gain Control
A3	OUTL	Left Channel Headphone Output
B3	CPVDD	Charge Pump Positive Supply
C3	SGND	Headphone Sense Ground
D3	OUTR	Right Channel Headphone Output
A4	INL–	Left Channel Inverting Input
B4	INL+	Left Channel Noninverting Input
C4	INR+	Right Channel Noninverting Input
D4	INR–	Right Channel Inverting Input

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TYPICAL PERFORMANCE CHARACTERISTICS

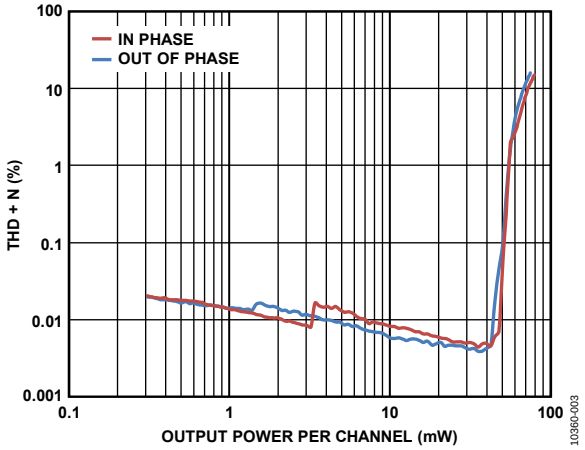


Figure 3. THD + N vs. Output Power, PVDD = 3.6 V, R_L = 32 Ω

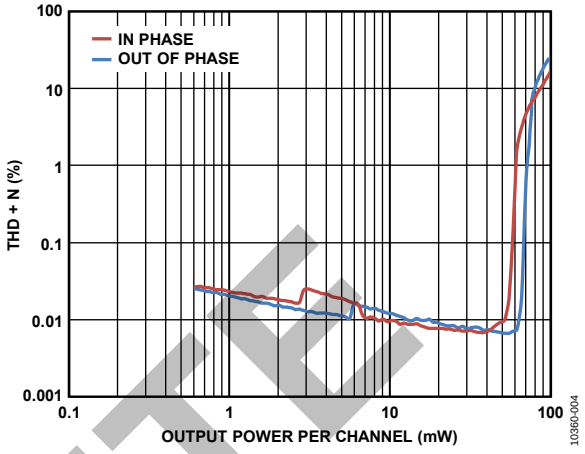


Figure 6. THD + N vs. Output Power, PVDD = 3.6 V, R_L = 16 Ω

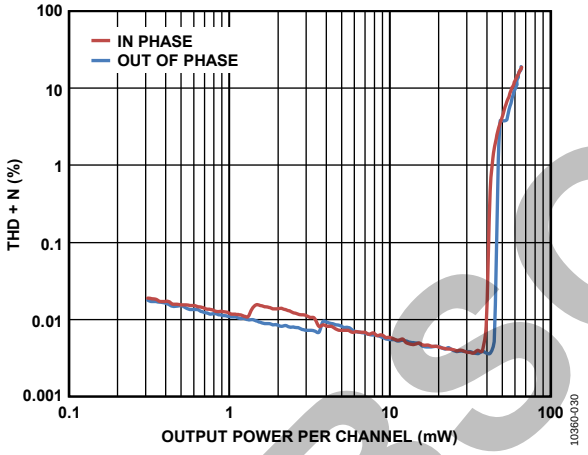


Figure 4. THD + N vs. Output Power, PVDD = 3.0 V, R_L = 32 Ω

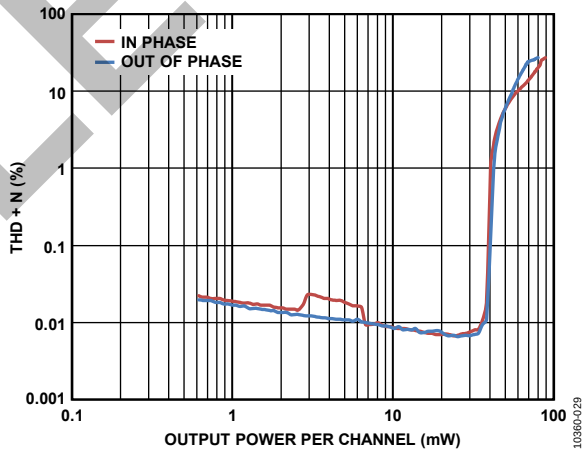


Figure 7. THD + N vs. Output Power, PVDD = 3.0 V, R_L = 16 Ω

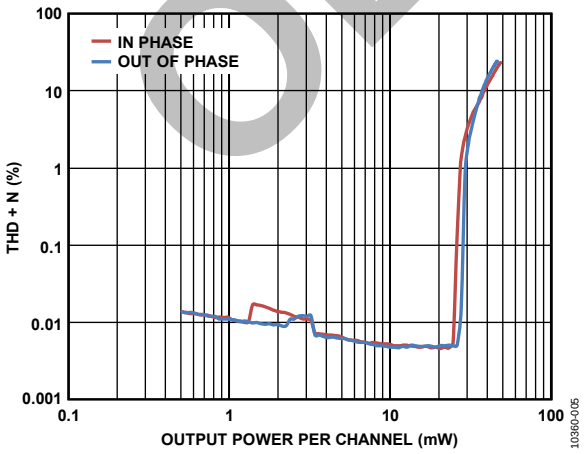


Figure 5. THD + N vs. Output Power, PVDD = 2.5 V, R_L = 32 Ω

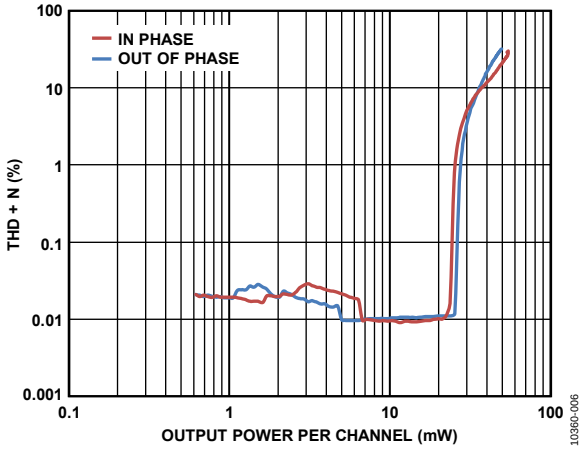


Figure 8. THD + N vs. Output Power, PVDD = 2.5 V, R_L = 16 Ω

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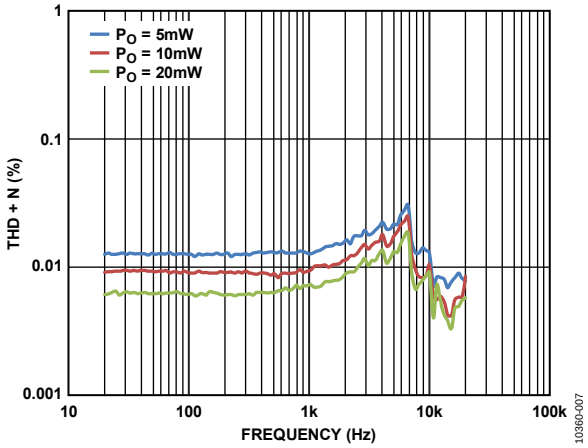


Figure 9. THD + N vs. Frequency, PVDD = 3.6 V, R_L = 32 Ω

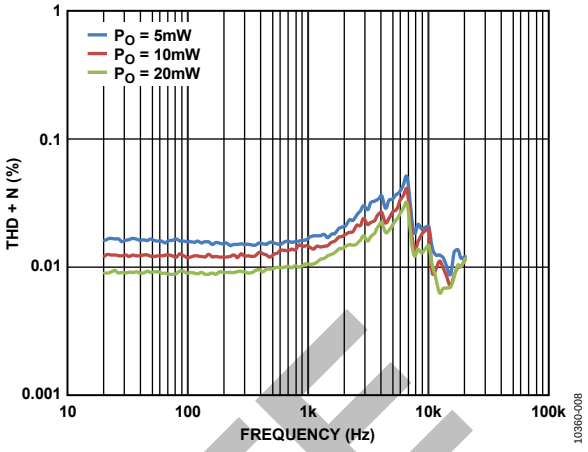


Figure 12. THD + N vs. Frequency, PVDD = 3.6 V, R_L = 16 Ω

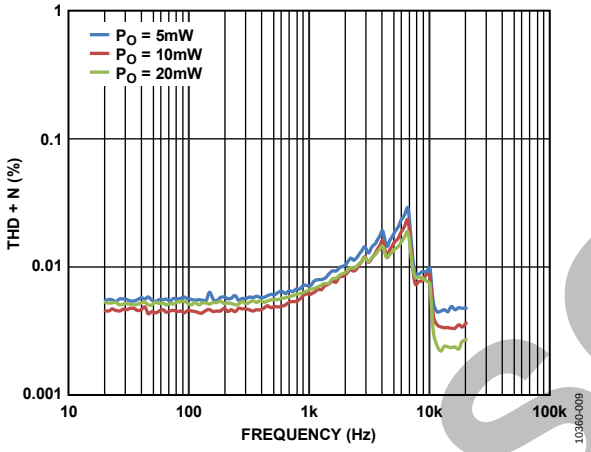


Figure 10. THD + N vs. Frequency, PVDD = 2.5 V, R_L = 32 Ω

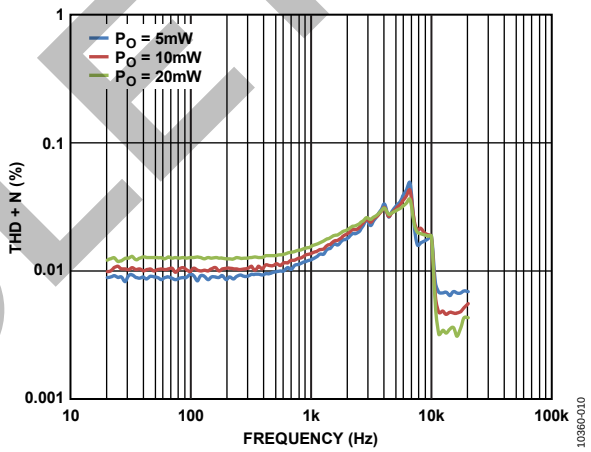


Figure 13. THD + N vs. Frequency, PVDD = 2.5 V, R_L = 16 Ω

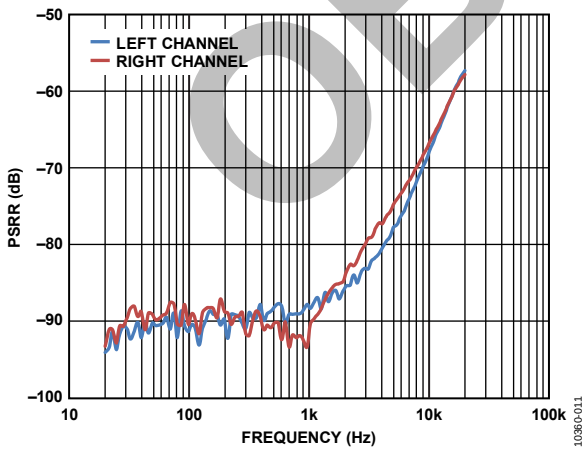


Figure 11. PSRR vs. Frequency, PVDD = 3.0 V, R_L = 32 Ω

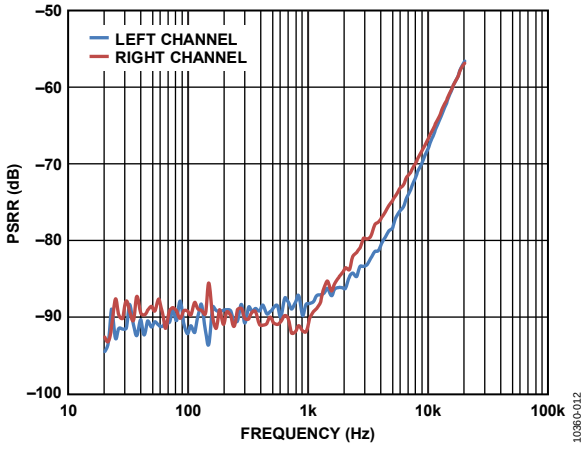


Figure 14. PSRR vs. Frequency, PVDD = 3.0 V, R_L = 16 Ω

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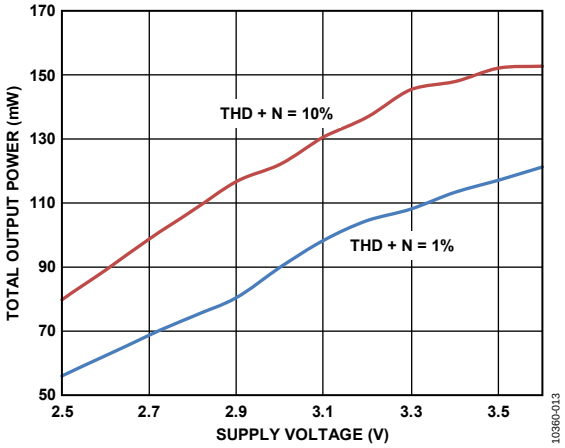


Figure 15. Output Power vs. Supply Voltage, R_L = 32 Ω

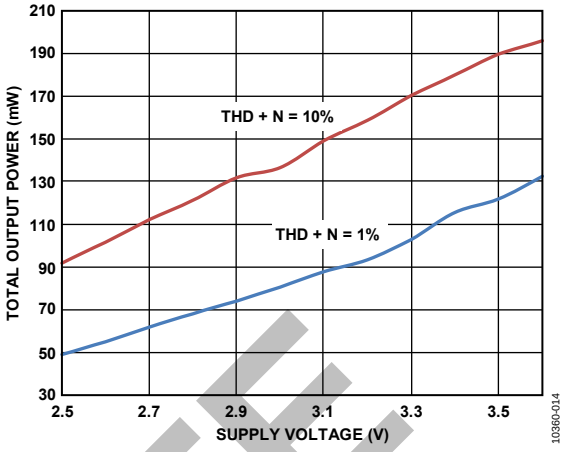


Figure 18. Output Power vs. Supply Voltage, R_L = 16 Ω

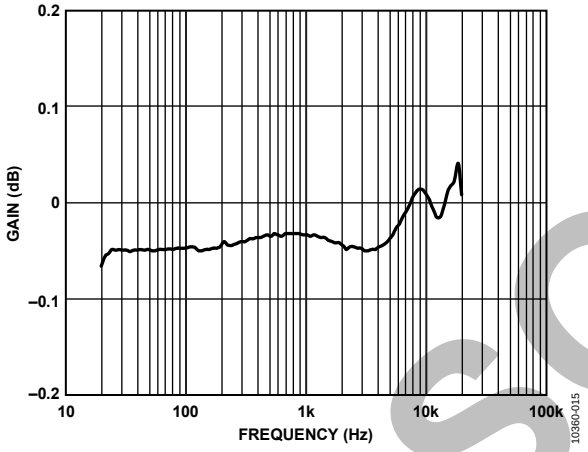


Figure 16. Frequency Response, PVDD = 3.0 V

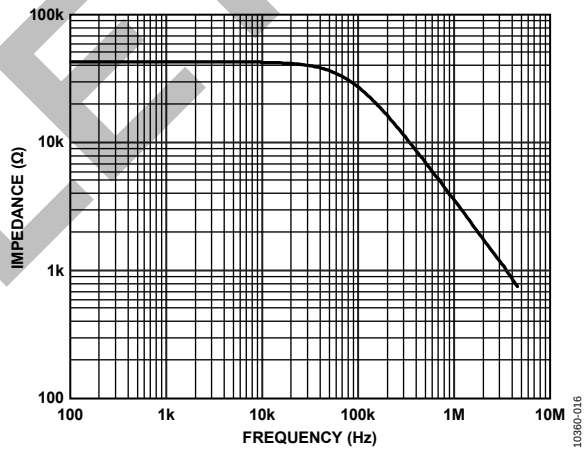


Figure 19. High-Z Mode Output Impedance vs. Frequency

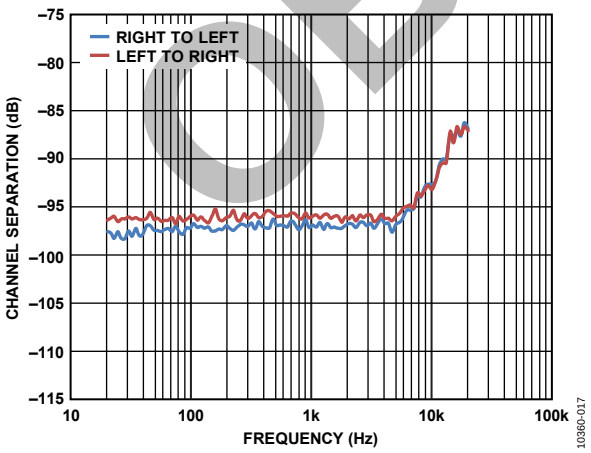


Figure 17. Channel Separation vs. Frequency, PVDD = 3.0 V, R_L = 32 Ω

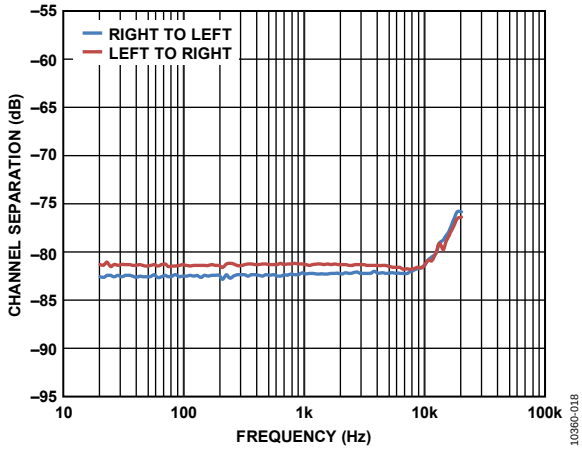


Figure 20. Channel Separation vs. Frequency, PVDD = 3.0 V, R_L = 16 Ω

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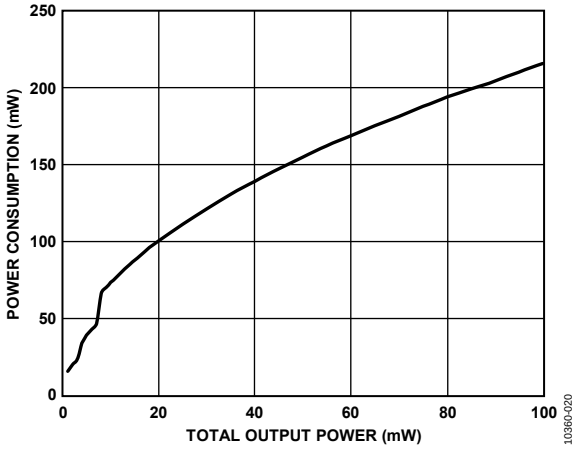


Figure 21. Power Consumption vs. Output Power, PVDD = 3.0 V, R_L = 32 Ω

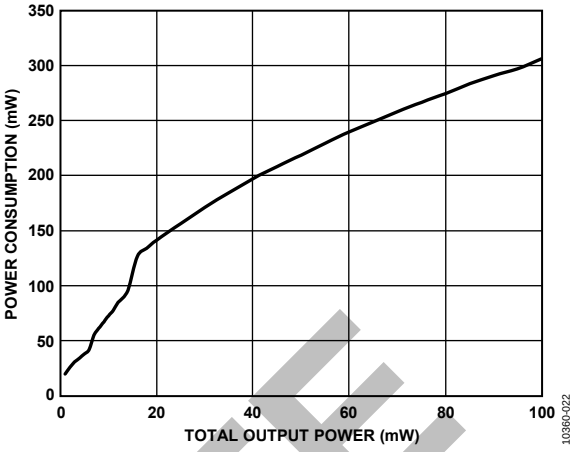


Figure 24. Power Consumption vs. Output Power, PVDD = 3.0 V, R_L = 16 Ω

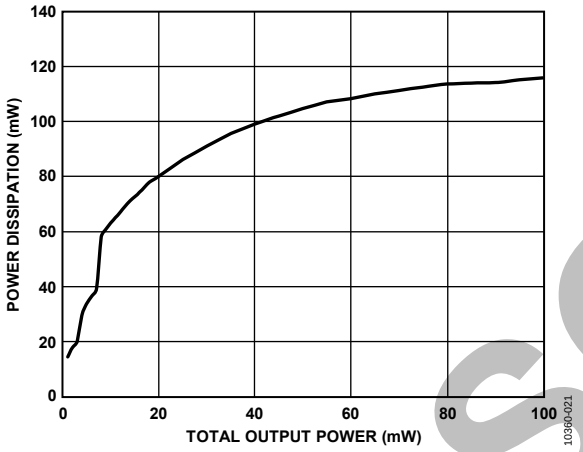


Figure 22. Power Dissipation vs. Output Power, PVDD = 3.0 V, R_L = 32 Ω

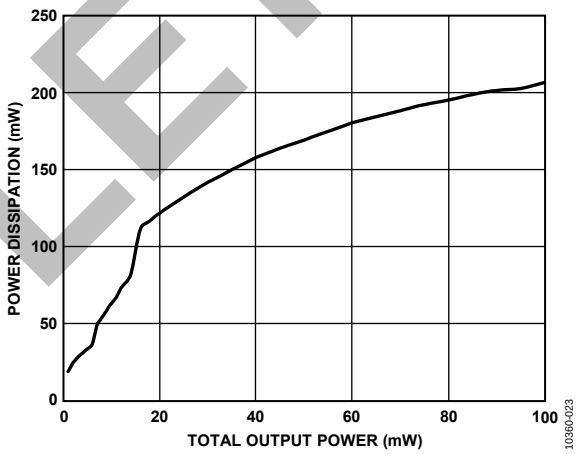


Figure 25. Power Dissipation vs. Output Power, PVDD = 3.0 V, R_L = 16 Ω

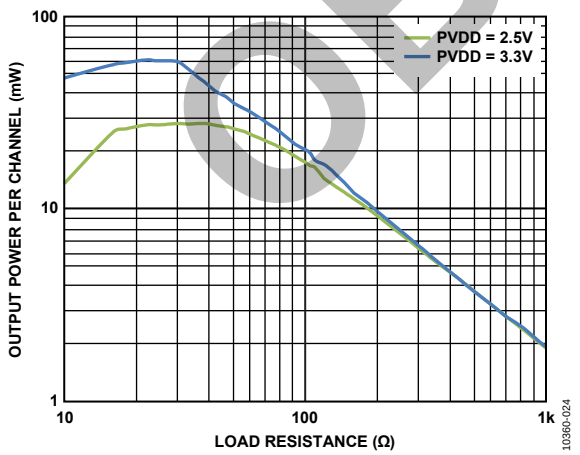


Figure 23. Maximum Output Power per Channel vs. Load Resistance, Flying Capacitor = 1 µF, THD + N = 1%

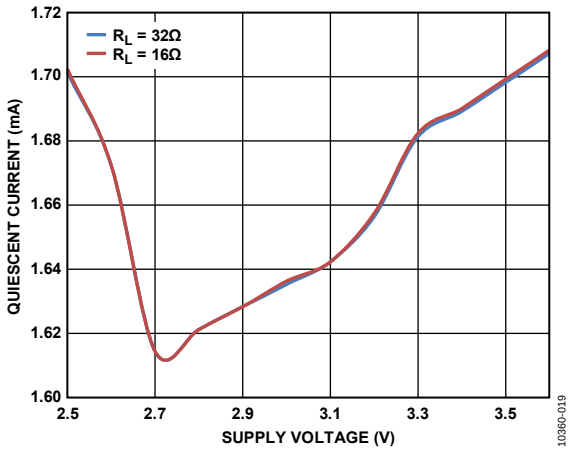


Figure 26. Quiescent Current vs. Supply Voltage

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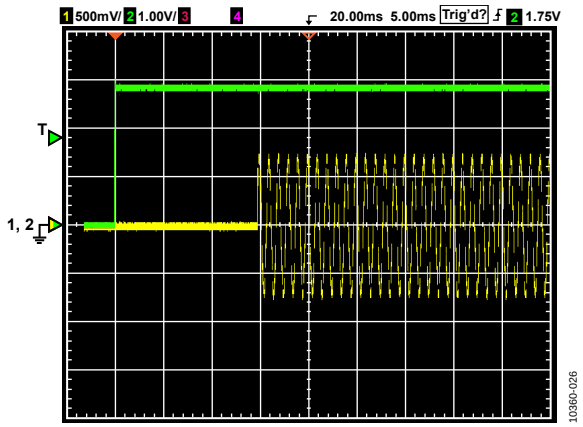


Figure 27. Start-Up Waveform vs. Time

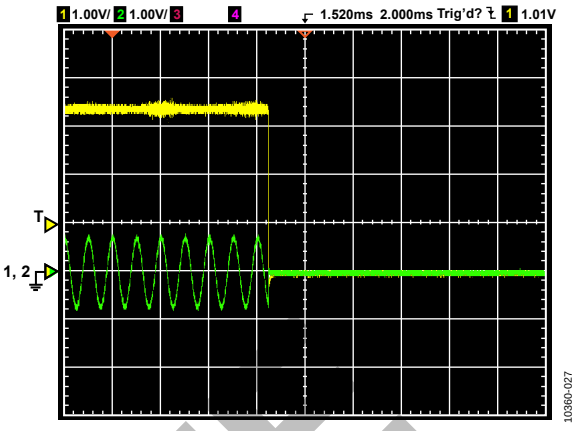


Figure 29. Shutdown Waveform vs. Time

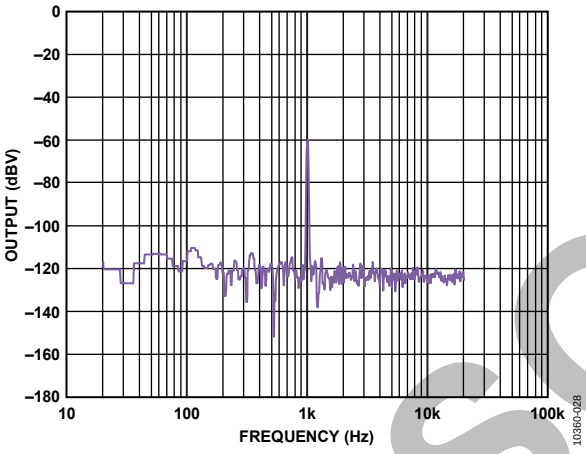


Figure 28. Output Spectrum vs. Frequency, PVDD = 3.0 V, R_L = 32 Ω

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THEORY OF OPERATION

The SSM2932 provides a high efficiency Class-G stereo headphone output that is true ground-referenced; therefore, no external coupling capacitors are required for connection to the headphones. The headphones can be connected directly to the headphone output pins, OUTL (Ball A3) and OUTR (Ball D3). The headphone amplifier uses the supply provided at PVDD (Ball A2). This supply voltage must be decoupled with a 1 µF electrolytic capacitor, along with a 100 nF ceramic X7R capacitor.

The headphone amplifier uses Class-G architecture and generates the required power supplies with a built-in charge pump that uses a flying capacitor connected across CF1 (Ball B2) and CF2 (Ball C1). The charge pump switching frequency is approximately 54 kHz in the idle state with no input signal detected and 550 kHz when a signal is present. The generated supply voltages are available at CPVDD (Ball B3, positive rail) and CPVSS (Ball C2, negative rail).

The supply voltage of the headphone amplifier depends on the input signal to the amplifier. For lower input signal levels, the positive and negative rails are lowered, typically to ±PVDD/2. As the signal level increases, CPVDD and CPVSS are raised to ±2.2 V. This rail switching allows the amplifier to achieve higher efficiency.

In most typical usage conditions, the amplifier works on the lower CPVDD and CPVSS voltages (±PVDD/2), thereby consuming less power. In addition, because the amplifier generates the positive and negative rails, the output amplifier is true ground-referenced, thereby eliminating the need for large coupling capacitors to drive the load.

For best audio performance, it is recommended that 2.2 µF, X7R ceramic decoupling capacitors be used for CPVDD and CPVSS. These capacitors serve as a reservoir for the headphone amplifier.

The headphone amplifier has built-in short-circuit protection and, therefore, shuts down in the event of a short circuit on the headphone outputs.

The amplifier is designed to drive headphones with a minimum impedance of 16 Ω. Capacitive loads of up to 150 pF are supported.

AMPLIFIER GAIN

The SSM2932 amplifier gain can be set to either 0 dB or 6 dB by applying the appropriate logic level to the GAIN pin (see Table 6).

Table 6. Amplifier Gain and GAIN Pin Logic Levels

Amplifier Gain	GAIN Pin Logic Level
0 dB	Low (≤0.5 V)
6 dB	High (≥1.2 V)

AMPLIFIER SHUTDOWN

Shutdown of the SSM2932 amplifier is controlled by the $\overline{SD}$ pin. If a logic low is applied to this pin, the amplifier becomes inactive and draws only minimal current from the supply.

Table 7. Amplifier Shutdown

Amplifier State	$\overline{SD}$ Pin Logic Level
Shutdown	Low (≤0.5 V)
Power-On	High (≥1.2 V)

HIGH OUTPUT IMPEDANCE

The SSM2932 has a HI-Z control pin that mutes the amplifier and sets the output to a high impedance. If both HI-Z and $\overline{SD}$ are set high, the amplifier remains in a high impedance state. This feature allows the headphone output jack to be shared for other functions such as video output or data transmission.

GROUND SENSE

SGND (Ball C3) is provided for sensing the dc potential at the headphone jack. It is recommended that SGND be connected directly to the ground pin of the headphone jack to ensure the lowest dc offset at the amplifier output and to eliminate pop-and-click noises when the amplifier is turned on or off. In addition, connecting the SGND ball directly to the ground pin of the headphone jack helps to reduce crosstalk between the left and right channel outputs. A dc path between the SGND pin and the system ground must also be provided.

LAYOUT

Care must be taken to lay out PCB traces and wires properly between the amplifier, load, and power supply. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. Ensure that track widths are at least 200 mil per inch of track length for lowest DCR, and use at least 1 oz or 2 oz copper thickness to minimize resistance. A poor layout increases voltage drops, consequently affecting efficiency. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance.

Proper grounding guidelines help to improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. The PCB traces that connect the output pins to the load, as well as the PCB traces to the supply pins, should be as wide as possible to maintain the minimum trace resistances. It is also recommended that a large ground plane be used for minimum impedances. The SGND pin should be connected directly to the ground pin of the headphone jack.

OBSOLETE

In addition, good PCB layout isolates critical analog paths from sources of high interference. High frequency circuits (analog and digital) should be separated from low frequency circuits.

Properly designed multilayer PCBs can reduce EMI emissions and increase immunity to the RF field by a factor of 10 or more compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted by signal crossover.

If the system has separate analog and digital ground and power planes, the analog ground plane should be directly beneath the analog power plane, and, similarly, the digital ground plane should be directly beneath the digital power plane. There should be no overlap between analog and digital ground planes or between analog and digital power planes.

OBSOLETE

TYPICAL APPLICATION CIRCUIT

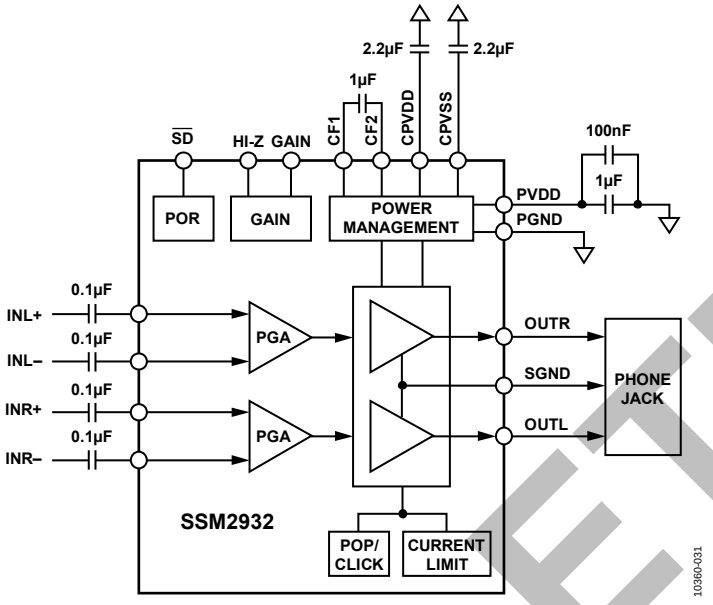


Figure 30. Application Circuit (Differential Input Configuration)

OBSOLETE

OUTLINE DIMENSIONS

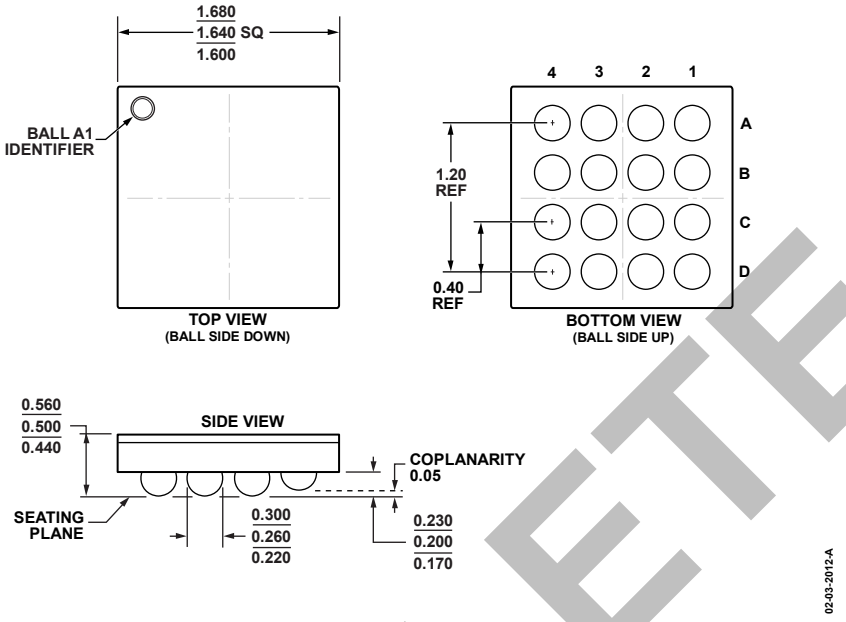


Figure 31. 16-Ball Wafer Level Chip Scale Package [WLCSP]
1.6 mm × 1.6 mm Body
(CB-16-11)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
SSM2932ACBZ-RL	−40°C to +85°C	16-Ball Wafer Level Chip Scale Package [WLCSP]	CB-16-11
SSM2932ACBZ-R7	−40°C to +85°C	16-Ball Wafer Level Chip Scale Package [WLCSP]	CB-16-11
EVAL-SSM2932Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

OBSOLETE

NOTES

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