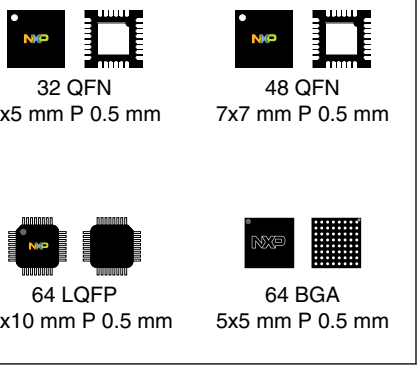
K32 L2B Microcontroller

48 MHz Arm® Cortex®-M0+ and 64/128/256 KB Flash

K32L2B31Vxx0A
K32L2B21Vxx0A
K32L2B11Vxx0A

The K32 L2B series is optimized for cost-sensitive and battery-powered applications requiring low-power USB connectivity and an optional segment LCD (SLCD). The product offers:

- Optional low power segment LCD up to 24x8 or 28x4
- USB FS 2.0 device without requiring an external crystal
- Embedded ROM with boot loader for flexible program upgrade
- High accuracy internal voltage and clock reference
- FlexIO to support any standard and customized serial peripheral emulation
- Down to 54 uA/MHz in very low power run mode and 1.96 uA in deep sleep mode (RAM + RTC retained)



Core Processor

- Arm® Cortex®-M0+ core up to 48 MHz

Memories

- 64/128/256 KB program flash memory
- 32 KB SRAM
- 16 KB ROM with build-in bootloader
- 32-byte backup register

System

- 4-channel asynchronous DMA controller
- Watchdog
- Low-leakage wakeup unit
- Two-pin Serial Wire Debug (SWD) programming and debug interface
- Micro Trace Buffer
- Bit manipulation engine
- Interrupt controller

Clocks

- 48 MHz high accuracy (up to 0.5%) internal reference clock
- 8 MHz/2 MHz high accuracy (up to 3%) internal reference clock
- 1 KHz reference clock active under all low-power modes (except VLLS0)
- 32–40 KHz and 3–32 MHz crystal oscillator

Peripherals

- SLCD supporting up to 24x8 or 28x4 segments
- USB full-speed 2.0 device controller supporting crystal-less operation
- One UART module supporting ISO7816, operating up to 1.5 Mbit/s
- Two low-power UART modules supporting asynchronous operation in low-power modes
- Two I2C modules and I2C0 supporting up to 1 Mbit/s
- Two 16-bit SPI modules supporting up to 24 Mbit/s
- One FlexIO module supporting emulation of additional UART, SPI, I2C, PWM and other serial modules, etc.
- One 16-bit 818 ksps ADC module with high accuracy internal voltage reference (Vref) and up to 16 channels
- High-speed analog comparator containing a 6-bit DAC for programmable reference input
- One 12-bit DAC
- 1.2 V internal voltage reference

I/O

- Up to 50 general-purpose input/output pins (GPIO) and 6 high-drive pad

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range: –40 to 105 °C

Packages

- 64 LQFP 10mm x 10mm, 0.5 mm pitch, 1.6 mm thickness
- 64 MAPBGA 5mm x 5mm, 0.5 mm pitch, 1.23 mm thickness
- 48 QFN 7mm x 7mm, 0.5 mm pitch, 0.65 mm thickness
- 32 QFN 5mm x 5mm, 0.5 mm pitch, 0.65 mm thickness

Low Power

- Down to 54 µA/MHz in very low power run mode
- Down to 1.96 µA in VLLS3 mode (RAM + RTC retained)
- Six flexible static modes

Timers

- One 6-channel Timer/PWM module
- Two 2-channel Timer/PWM modules
- One low-power timer
- Periodic interrupt timer
- Real time clock

Security and Integrity

- 80-bit unique identification number per chip
- Advanced flash security

Related Resources

Type	Description	Resource
Selector Guide	The NXP Selector Guide is a web-based tool that features interactive application wizards and a dynamic product selector.	Selector Guide
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K32L2B3xRM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	K32L2B_1N71K[1]
Package drawing	Package dimensions are provided in package drawings.	64-LQFP: 98ASS23234W, 64-MAPBGA: 98ASA00420D, 32-QFN: 98ASA00615D, 48-QFN: 98ASA00616D[1]

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

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1 Ordering information

The following chips are available for ordering.

Table 1. Ordering information

Product	Memory		Package		IO and ADC channel			Serial Interface
Part number	Flash (KB)	SRAM (KB)	Pin count	Package	GPIOs	GPIOs (INT/HD)[1]	ADC channels (SE/DP)	SLCD
K32L2B31VLH0A	256	32	64	LQFP	50	31/6	16/2	Yes
K32L2B31VMP0A	256	32	64	MAPBGA	50	31/6	16/2	Yes
K32L2B31VFT0A	256	32	48	QFN	36	24/6	14/1	—
K32L2B31VFM0A	256	32	32	QFN	23	19/6	7/0	—
K32L2B21VLH0A	128	32	64	LQFP	50	31/6	16/2	Yes
K32L2B21VMP0A	128	32	64	MAPBGA	50	31/6	16/2	Yes
K32L2B21VFT0A	128	32	48	QFN	36	24/6	14/1	—
K32L2B21VFM0A	128	32	32	QFN	23	19/6	7/0	—
K32L2B11VLH0A	64	32	64	LQFP	50	31/6	16/2	Yes
K32L2B11VMP0A	64	32	64	MAPBGA	50	31/6	16/2	Yes
K32L2B11VFT0A	64	32	48	QFN	36	24/6	14/1	—
K32L2B11VFM0A	64	32	32	QFN	23	19/6	7/0	—

1. INT: interrupt pin numbers; HD: high drive pin numbers

2 Overview

The following figure shows the system diagram of this device

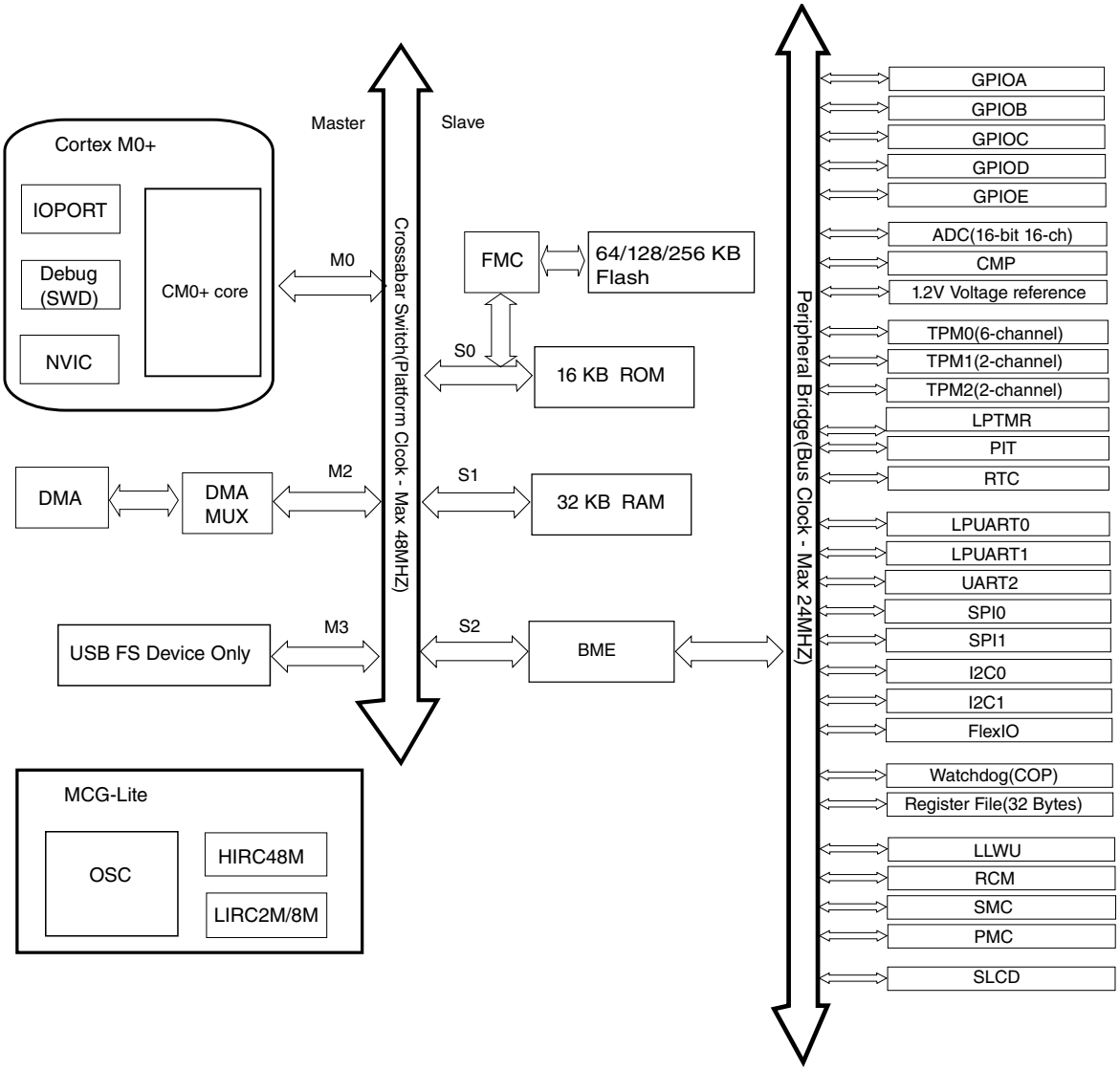


Figure 1. System diagram

The crossbar switch connects bus masters and slaves using a crossbar switch structure. This structure allows up to four bus masters to access different bus slaves simultaneously, while providing arbitration among the bus masters when they access the same slave.

2.1 System features

The following sections describe the high-level system features.

2.1.1 Arm Cortex-M0+ core

The enhanced Arm Cortex M0+ is the member of the Cortex-M series of processors targeting microcontroller cores focused on very cost sensitive, low power applications. It has a single 32-bit AMBA AHB-Lite interface and includes an NVIC component. It also has hardware debug functionality including support for simple program trace capability. The processor supports the ARMv6-M instruction set (Thumb) architecture including all but three 16-bit Thumb opcodes (52 total) plus seven 32-bit instructions. It is upward compatible with other Cortex-M profile processors.

2.1.2 NVIC

The Nested Vectored Interrupt Controller supports nested interrupts and 4 priority levels for interrupts. In the NVIC, each source in the IPR registers contains two bits. It also differs in number of interrupt sources and supports 32 interrupt vectors.

The Cortex-M family uses a number of methods to improve interrupt latency to up to 15 clock cycles for Cortex-M0+. It also can be used to wake the MCU core from Wait and VLPW modes.

2.1.3 AWIC

The asynchronous wake-up interrupt controller (AWIC) is used to detect asynchronous wake-up events in Stop mode and signal to clock control logic to resume system clocking. After clock restarts, the NVIC observes the pending interrupt and performs the normal interrupt or event processing. The AWIC can be used to wake MCU core from Stop and VLPS modes.

Wake-up sources are listed as below:

Table 2. AWIC stop wake-up sources

Wake-up source	Description
Available system resets	$\overline{\text{RESET}}$ pin when LPO is its clock source
Low-voltage detect	Power management controller—functional in Stop mode
Low-voltage warning	Power management controller—functional in Stop mode
Pin interrupts	Port control module—any enabled pin interrupt is capable of waking the system
ADC	The ADC is functional when using internal clock source or external crystal clock
CMP0	Interrupt in normal or trigger mode
I^2Cx	Address match wakeup

Table continues on the next page...

Table 2. AWIC stop wake-up sources (continued)

Wake-up source	Description
LPUART0 , LPUART1	Any enabled interrupt can be a source as long as the module remains clocked
UART2	Active edge on RXD
RTC	Alarm or seconds interrupt
NMI	$\overline{\text{NMI}}$ pin
TPMx	Any enabled interrupt can be a source as long as the module remains clocked
LPTMR	Any enabled interrupt can be a source as long as the module remains clocked
SPIx	Slave mode interrupt
FlexIO	Any enabled interrupt can be a source as long as the module remains clocked

2.1.4 Memory

This device has the following features:

- 32 KB of embedded RAM accessible (read/write) at CPU clock speed with 0 wait states.
- The non-volatile memory is divided into two arrays
  - Up to 256 KB of embedded program memory
  - 16 KB ROM (built-in bootloader to support UART, I2C, USB, and SPI interfaces)

  The program flash memory contains a 16-byte flash configuration field that stores default protection settings and security information. The page size of program flash is 1 KB.

  The protection setting can protect 32 regions of the program flash memory from unintended erase or program operations.

  The security circuitry prevents unauthorized access to RAM or flash contents from debug port.

- System register file

  This device contains a 32-byte register file that is powered in all power modes.

  Also, it retains contents during low power modes and is reset only during a power-on reset.

2.1.5 Reset and boot

The following table lists all the reset sources supported by this device.

NOTE

In the following table, Y means the specific module, except for the registers, bits or conditions mentioned in the footnote, is reset by the corresponding Reset source. N means the specific module is not reset by the corresponding Reset source.

Table 3. Reset source

Reset sources	Descriptions	Modules								
		PMC	SIM	SMC	RCM	LLWU	Reset pin is negated	RTC	LPTMR	Others
POR reset	Power-on reset (POR)	Y	Y	Y	Y	Y	Y	Y	Y	Y
System resets	Low-voltage detect (LVD)	Y[1]	Y	Y	Y	Y	Y	N	Y	Y
	Low leakage wakeup (LLWU) reset	N	Y[2]	N	Y	N	Y[3]	N	N	Y
	External pin reset ($\overline{\text{RESET}}$)	Y[1]	Y[2]	Y[4]	Y	Y	Y	N	N	Y
	Computer operating properly (COP) watchdog reset	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Stop mode acknowledge error (SACKERR)	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Software reset (SW)	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Lockup reset (LOCKUP)	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	MDM DAP system reset	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
Debug reset	Debug reset	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y

1. Except PMC_LVDSC1[LVDV] and PMC_LVDSC2[LVWV]
2. Except SIM_SOPT1
3. Only if $\overline{\text{RESET}}$ is used to wake from VLLS mode.
4. Except SMC_PMCTRL, SMC_STOPCTRL, SMC_PMSTAT
5. Except RCM_RPFC, RCM_RPFW, RCM_FM

The CM0+ core adds support for a programmable Vector Table Offset Register (VTOR) to relocate the exception vector table after reset. This device supports booting from:

- internal flash
- ROM

The Flash Option (FOPT) register in the Flash Memory module (FTFA_FOPT) allows the user to customize the operation of the MCU at boot time. The register contains read-only bits that are loaded from the NVM's option byte in the flash configuration field. Below is boot flow chart for this device.

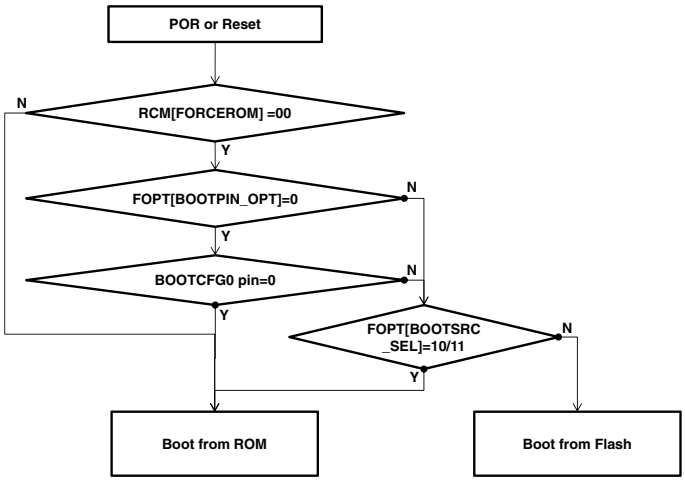


Figure 2. Boot flow chart

The blank chip is default to boot from ROM and remaps the vector table to ROM base address, otherwise, it remaps to flash address.

2.1.6 Clock options

This chip provides a wide range of sources to generate the internal clocks. These sources include internal resistor capacitor (IRC) oscillators, external oscillators, external clock sources, and ceramic resonators. These sources can be configured to provide the required performance and optimize the power consumption.

The IRC oscillators include the high-speed internal resister capacitor (HIRC) oscillator, the low-speed internal resister capacitor (LIRC) oscillator, and the low power oscillator (LPO).

The HIRC oscillator generates a 48 MHz clock and synchronizes with the USB clock in full speed mode to achieve the required accuracy.

The LIRC oscillator generates an 8 MHz or 2 MHz clock, and default to 8 MHz system clock on reset. The LIRC oscillator cannot be used in any VLLS modes.

The LPO generates a 1 kHz clock and cannot be used in VLLS0 mode.

The system oscillator supports low frequency crystals (32 kHz to 40 kHz), high frequency crystals (3 MHz to 32 MHz), and ceramic resonators (3 MHz to 32 MHz). An external clock source, DC to 48 MHz, can be used as the system clock through the EXTAL0 pin. The external oscillator also supports a low speed external clock (32.768 kHz) on the RTC_CLKIN pin for use with the RTC.

For more details on the clock operations and configurations, see Reference Manual.

The following figure is a high level block diagram of the clock generation.

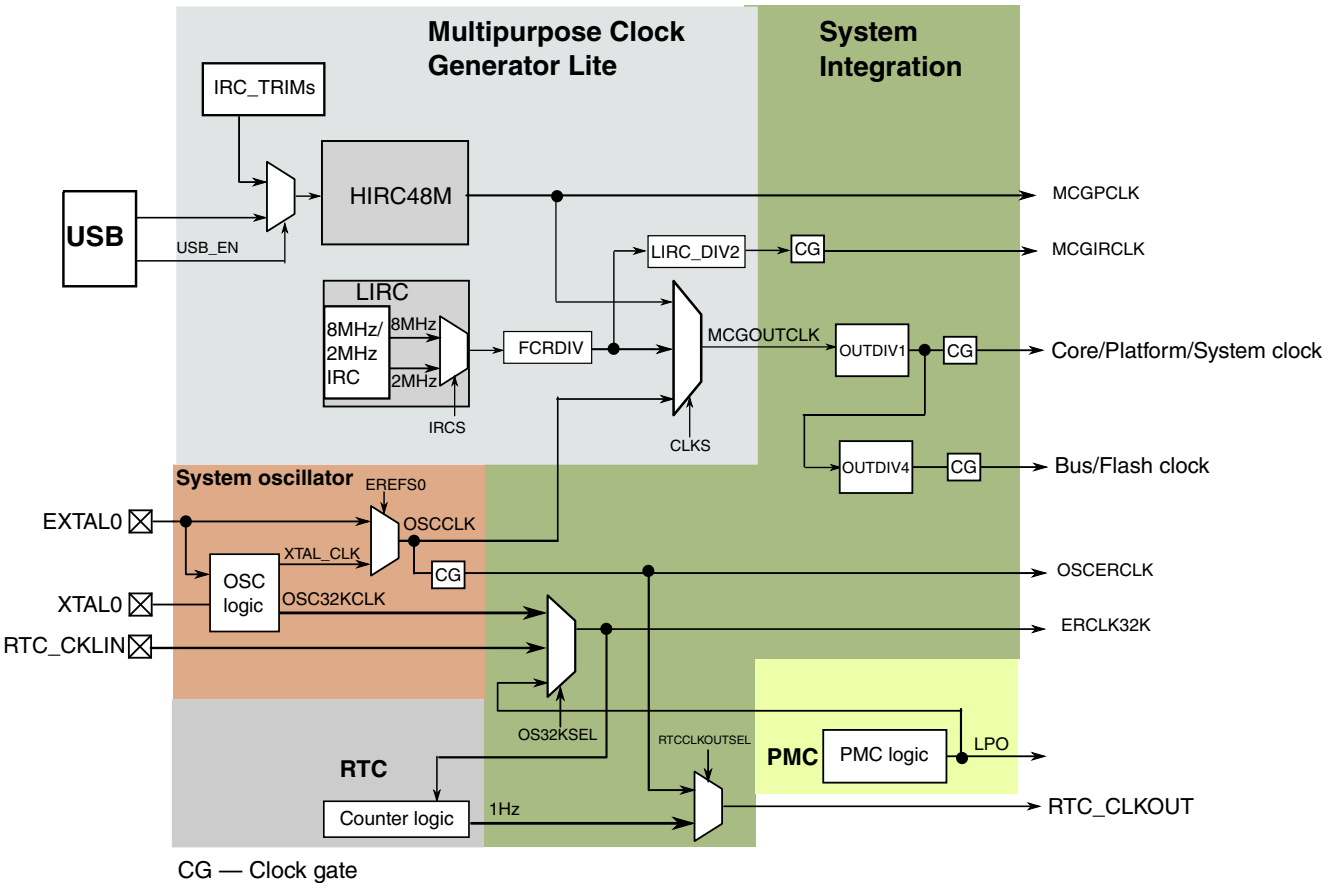


Figure 3. Clock block diagram

In order to provide flexibility, many peripherals can select from multiple clock sources for operation. This enables the peripheral to select a clock that will always be available during operation in various operational modes.

The following table summarizes the clocks associated with each module.

Table 4. Module clocks

Module	Bus interface clock	Internal clocks	I/O interface clocks
Core modules			

Table continues on the next page...

Table 4. Module clocks (continued)

Module	Bus interface clock	Internal clocks	I/O interface clocks
Arm Cortex-M0+ core	Platform clock	Core clock	—
NVIC	Platform clock	—	—
DAP	Platform clock	—	SWD_CLK
System modules			
DMA	System clock	—	—
DMA Mux	Bus clock	—	—
Port control	Bus clock	—	—
Crossbar Switch	Platform clock	—	—
Peripheral bridges	System clock	Bus clock	—
LLWU, PMC, SIM, RCM	Bus clock	LPO	—
Mode controller	Bus clock	—	—
MCM	Platform clock	—	—
COP watchdog	Bus clock	LPO, Bus Clock, MCGIRCLK, OSCERCLK	—
Clocks			
MCG_Lite	Bus clock	MCGOUTCLK, MCGPCLK, MCGIRCLK, OSCERCLK, ERCLK32K	—
OSC	Bus clock	OSCERCLK	—
Memory and memory interfaces			
Flash Controller	Platform clock	Flash clock	—
Flash memory	Flash clock	—	—
Analog			
ADC	Bus clock	OSCERCLK	—
CMP	Bus clock	—	—
Internal Voltage Reference (VREF)	Bus clock	—	—
Timers			
TPM	Bus clock	TPM clock	TPM_CLKIN0, TPM_CLKIN1
PIT	Bus clock	—	—
LPTMR	Bus clock	LPO, OSCERCLK, MCGPCLK, ERCLK32K	—
RTC	Bus clock	ERCLK32K	RTC_CLKOUT, RTC_CLKIN
Communication interfaces			
USB FS (Device Only)	System clock	USB FS clock	—
SPI0	Bus clock	—	SPI0_SCK
SPI1	System clock	—	SPI1_SCK
I^2C0	System Clock	—	I2C0_SCL
I^2C1	System Clock	—	I2C1_SCL

Table continues on the next page...

Table 4. Module clocks (continued)

Module	Bus interface clock	Internal clocks	I/O interface clocks
LPUART0, LPUART1	Bus clock	LPUART0 clock LPUART1 clock	—
UART2	Bus clock	—	—
FlexIO	Bus clock	FlexIO clock	—
Human-machine interfaces			
GPIO	Platform clock	—	—

2.1.7 Security

Security state can be enabled via programming flash configuration field (0x40e). After enabling device security, the SWD port cannot access the memory resources of the MCU, and ROM boot loader is also limited to access flash and not allowed to read out flash information via ROM boot loader commands.

Access interface	Secure state	Unsecure operation
SWD port	Cannot access memory source by SWD interface	The debugger can write to the Flash Mass Erase in Progress field of the MDM-AP Control register to trigger a mass erase (Erase All Blocks) command
ROM boot loader Interface (UART/I2C/SPI/USB)	Limit access to the flash, cannot read out flash content	Send “FlashEraseAllUnsecureh" command or attempt to unlock flash security using the backdoor key

This device features 80-bit unique identification number, which is programmed in factory and loaded to SIM register after power-on reset.

2.1.8 Power management

The Power Management Controller (PMC) expands upon Arm’s operational modes of Run, Sleep, and Deep Sleep, to provide multiple configurable modes. These modes can be used to optimize current consumption for a wide range of applications. The WFI or WFE instruction invokes a Wait or a Stop mode, depending on the current configuration. For more information on Arm’s operational modes, See the Arm® Cortex User Guide.

The PMC provides Run (Run), and Very Low Power Run (VLPR) configurations in Arm's Run operation mode. In these modes, the MCU core is active and can access all peripherals. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption. The configuration that matches the power versus performance requirements of the application can be selected.

The PMC provides Wait (Wait) and Very Low Power Wait (VLPW) configurations in Arm's Sleep operation mode. In these modes, even though the MCU core is inactive, all of the peripherals can be enabled and operate as programmed. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption.

The PMC provides Stop (Stop), Very Low Power Stop (VLPS), Low Leakage Stop (LLS), and Very Low Leakage Stop (VLLS) configurations in Arm's Deep Sleep operational mode. In these modes, the MCU core and most of the peripherals are disabled. Depending on the requirements of the application, different portions of the analog, logic, and memory can be retained or disabled to conserve power.

The Nested Vectored Interrupt Controller (NVIC), the Asynchronous Wake-up Interrupt Controller (AWIC), and the Low Leakage Wake-Up Controller (LLWU) are used to wake up the MCU from low power states. The NVIC is used to wake up the MCU core from WAIT and VLPW modes. The AWIC is used to wake up the MCU core from STOP and VLPS modes. The LLWU is used to wake up the MCU core from LLS and VLLSx modes.

For additional information regarding operational modes, power management, the NVIC, AWIC, or the LLWU, please refer to the Reference Manual.

The following table provides information about the state of the peripherals in the various operational modes and the modules that can wake MCU from low power modes.

Table 6. Peripherals states in different operational modes

Core mode	Device mode	Descriptions
Run mode	Run	In Run mode, all device modules are operational.
	Very Low Power Run	In VLPR mode, all device modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled.
Sleep mode	Wait	In Wait mode, all peripheral modules are operational. The MCU core is placed into Sleep mode.
	Very Low Power Wait	In VLPW mode, all peripheral modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled. The MCU core is placed into Sleep mode.

Table continues on the next page...

Table 6. Peripherals states in different operational modes (continued)

Core mode	Device mode	Descriptions
Deep sleep	Stop	In Stop mode, most peripheral clocks are disabled and placed in a static state. Stop mode retains all registers and SRAMs while maintaining Low Voltage Detection protection. In Stop mode, the ADC, CMP, LPTMR, RTC, and pin interrupts are operational. The NVIC is disabled, but the AWIC can be used to wake up from an interrupt.
	Very Low Power Stop	In VLPS mode, the contents of the SRAM are retained. The CMP (low speed), ADC, OSC, RTC, LPTMR, TPM, FlexIO, LPUART, USB, and DMA are operational, LVD and NVIC are disabled, AWIC is used to wake up from interrupt.
	Low Leakage Stop	In LLS mode, the contents of the SRAM and the 32-byte system register file are retained. The CMP (low speed), LLWU, LPTMR, and RTC are operational. The ADC, DMA, FlexIO, I2C, LPUART, MCG-Lite, NVIC, PIT, SPI, TPM, UART, USB, and COP are static, but retain their programming. The GPIO, and VREF are static, retain their programming, and continue to drive their previous values.
	Very Low Leakage Stop	In VLLS modes, most peripherals are powered off and will resume operation from their reset state when the device wakes up. The LLWU, LPTMR, and RTC are operational in all VLLS modes. In VLLS3, the contents of the SRAM and the 32-byte system register file are retained. The CMP (low speed), and PMC are operational. The GPIO, and VREF are not operational but continue driving. In VLLS1, the contents of the 32-byte system register file are retained. The CMP (low speed), and PMC are operational. The GPIO, and VREF are not operational but continue driving. In VLLS0, the contents of the 32-byte system register file are retained. The PMC is operational. The GPIO is not operational but continues driving. The POR detection circuit can be enabled or disabled.

2.1.9 LLWU

The LLWU module is used to wake MCU from low leakage power mode (LLS and VLLSx) and functional only on entry into a low-leakage power mode. After recovery from LLS, the LLWU is immediately disabled. After recovery from VLLSx, the LLWU continues to detect wake-up events until the user has acknowledged the wake-up event.

This device uses 8 external wakeup pin inputs and 4 internal modules as wakeup sources to the LLWU module.

The following is internal peripheral and external pin inputs as wakeup sources to the LLWU module.

Table 7. Wakeup source

LLWU pin	Module source or pin name
LLWU_P5	PTB0
LLWU_P6	PTC1
LLWU_P7	PTC3
LLWU_P8	PTC4
LLWU_P9	PTC5
LLWU_P10	PTC6
LLWU_P14	PTD4
LLWU_P15	PTD6
LLWU_M0IF	LPTMR0
LLWU_M1IF	CMP0
LLWU_M2IF	Reserved
LLWU_M3IF	Reserved
LLWU_M4IF	Reserved
LLWU_M5IF	RTC alarm
LLWU_M6IF	Reserved
LLWU_M7IF	RTC seconds

2.1.10 Debug controller

This device supports standard Arm 2-pin SWD debug port. It provides register and memory accessibility from the external debugger interface, basic run/halt control plus 2 breakpoints and 2 watchpoints.

It also supports trace function with the Micro Trace Buffer (MTB), which provides a simple execution trace capability for the Cortex-M0+ processor.

2.1.11 COP

The COP monitors internal system operation and forces a reset in case of failure. It can run from bus clock, LPO, 8/2 MHz internal oscillator or external crystal oscillator. Optional window mode can detect deviations in program flow or system frequency.

The COP has the following features:

- Support multiple clock input, 1 kHz clock(LPO), bus clock, 8/2 MHz internal reference clock, external crystal oscillator
- Can work in Stop/VLPS and Debug mode

- Configurable for short and long timeout values, the longest timeout is up to 262 seconds
- Support window mode

2.2 Peripheral features

The following sections describe the features of each peripherals of the chip.

2.2.1 Segment LCD (SLCD)

The SLCD module is a CMOS charge pump voltage inverter that is designed for low-voltage and low-power operation. SLCD is designed to generate the appropriate waveforms to drive multiplexed numeric, alphanumeric, or custom segment LCD panels. SLCD also has several timing and control settings that can be software configured depending on the application's requirements. Timing and control consists of registers and control logic for:

- LCD frame frequency
- Duty cycle selection
- Front plane/back plane selection and enabling
- Blink modes and frequency
- Operation in low-power modes

2.2.2 BME

The Bit Manipulation Engine (BME) provides hardware support for atomic read-modify-write memory operations to the peripheral address space in Cortex-M0+ based microcontrollers. It reduces up to 30% of the code size and up to 9% of the cycles for bit-oriented operations to peripheral registers.

The BME supports unsigned bit field extract, load-and-set 1-bit, load-and-clear 1-bit, bit field insert, logical AND/OR/XOR operations with byte, halfword or word-sized data type.

2.2.3 DMA and DMAMUX

The DMA controller module enables fast transfers of data, which provides an efficient way to move blocks of data with minimal processor interaction. The DMA controller in this device implements four channels which can be routed from up to 63 DMA request sources through DMA MUX module. Some of the peripheral request sources have asynchronous DMA capability which can be used to wake MCU from Stop mode. The peripherals which have such capability include . The DMA channel 0 and 1 can be periodically triggered by PIT via DMA MUX.

Main features are listed below:

- Dual-address transfers via 32-bit master connection to the system bus and data transfers in 8-, 16-, or 32-bit blocks
- Supports programmable source and destination address and transfer size, optional modulo addressing from 16 bytes to 256 KB
- Automatic updates of source and destination addresses
- Auto-alignment feature for source or destination accesses allows block transfers to occur at the optimal size based on the address, byte count,and programmed size, which significantly improves the speed of block transfer
- Automatic single or double channel linking allows the current DMA channel to automatically trigger a DMA request to the linked channels without CPU intervention

For more information on asynchronous DMA, see AN4631.

2.2.4 TPM

This device contains three low power TPM modules (TPM). All TPM modules are functional in Stop/VLPS mode if the clock source is enabled.

The TPM features include:

- TPM clock mode is selectable from external clock input, internal clock source, external crystal input clock, MCGIRCLK clock or clocking from MCGFLLCLK and MCGPLLCLK/2
- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- TPM includes a 16-bit counter
- Includes 6 channels that can be configured for input capture, output compare, edge-aligned PWM mode, or center-aligned PWM mode
- Support the generation of an interrupt and/or DMA request per channel or counter overflow

- Support selectable trigger input to optionally reset or cause the counter to start or stop incrementing
- Support the generation of hardware triggers when the counter overflows and per channel

2.2.5 ADC

This device contains one ADC module. This ADC module supports hardware triggers from TPM, LPTMR, PIT, RTC, external trigger pin and CMP output. It supports wakeup of MCU in low power mode when using internal clock source or external crystal clock.

ADC module has the following features:

- Linear successive approximation algorithm with up to 16-bit resolution
- Up to four pairs of differential and 17 single-ended external analog inputs
- Support selectable 16-bit, 13-bit, 11-bit, and 9-bit differential output mode, or 16-bit, 12-bit, 10-bit, and 8-bit single-ended output modes
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Selectable clock source up to four
- Operation in low-power modes for lower noise
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable hardware conversion trigger
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor
- Hardware average function up to 32x
- Selectable voltage reference: external or alternate
- Self-calibration mode

2.2.5.1 Temperature sensor

This device integrates one temperature sensor internally connected to the input channel of AD26, see for details of the linearity factor.

The sensor provides good linearity, but it has to be calibrated to gain good accuracy, see also AN3031. We recommend to use internal reference voltage as ADC reference with long sample time.

2.2.6 VREF

The Voltage Reference (VREF) can supply an accurate voltage output (1.2V typically) trimmed in 0.5 mV steps. It can be used in applications to provide a reference voltage to external devices or used internally as a reference to analog peripherals such as the ADC or CMP.

The VREF supports the following programmable buffer modes:
- Bandgap on only, used for stabilization and startup
- High power buffer mode
- Low-power buffer mode
- Buffer disabled

The VREF voltage output signal, bonded on VREFH for 48 QFN, 64 LQFP and 64 MAPBGA packages and on PTE30 for 32 QFN packages, can be used by both internal and external peripherals in low and high power buffer mode. A 100 nF capacitor must always be connected between this pin and VSSA if the VREF is used. This capacitor must be as close to VREF_OUT pin as possible.

2.2.7 CMP

The device contains one high-speed comparator and two 8-input multiplexers for both the inverting and non-inverting inputs of the comparator. Each CMP input channel connects to both muxes.

The CMP includes one 6-bit DAC, which provides a selectable voltage reference for various user application cases. Besides, the CMP also has several module-to-module interconnects in order to facilitate ADC triggering, TPM triggering, and interfaces.

The CMP has the following features:
- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable interrupt on rising-edge, falling-edge, or both rising or falling edges of the comparator output
- Selectable inversion on comparator output
- Capability to produce a wide range of outputs such as sampled, digitally filtered
- External hysteresis can be used at the same time that the output filter is used for internal functions
- Two software selectable performance levels: shorter propagation delay at the expense of higher power and Low power with longer propagation delay

- DMA transfer support
- Functional in all modes of operation except in VLLS0 mode
- The filter functions are not available in Stop, VLPS, LLS, or VLLSx modes
- Integrated 6-bit DAC with selectable supply reference source and can be power down to conserve power
- Two 8-to-1 channel mux

2.2.8 DAC

The 12-bit Digital-to-Analog Converter (DAC) is a low-power, general-purpose DAC. The output of the DAC can be placed on an external pin or set as one of the inputs to the analog comparator, op-amps, or ADC.

The features of the DAC module include:

- On-chip programmable reference generator output. The voltage output range is from 1⁄4096 Vin to Vin, and the step is 1⁄4096 Vin, where Vin is the input voltage.
- Vin can be selected from two reference sources.
- Static operation in Normal Stop mode.
- 2-word data buffer supported with multiple operation modes.
- DMA support.

2.2.9 RTC

The RTC is an always powered-on block that remains active in all low power modes. The time counter within the RTC is clocked by a 32.768 kHz clock sourced from an external crystal using the oscillator or clock directly from RTC_CLKIN pin.

RTC is reset on power-on reset, and a software reset bit in RTC can also initialize all RTC registers.

The RTC module has the following features

- 32-bit seconds counter with roll-over protection and 32-bit alarm
- 16-bit prescaler with compensation that can correct errors between 0.12 ppm and 3906 ppm
- Register write protection with register lock mechanism
- 1 Hz square wave or second pulse output with optional interrupt

2.2.10 PIT

The Periodic Interrupt Timer (PIT) is used to generate periodic interrupt to the CPU. It has two independent channels and each channel has a 32-bit counter. Both channels can be chained together to form a 64-bit counter.

Channel 0 can be used to periodically trigger DMA channel 0, and channel 1 can be used to periodically trigger DMA channel 1. Either channel can be programmed as an ADC trigger source, or TPM trigger source. Channel 0 can be programmed to trigger DAC.

The PIT module has the following features:

- Each 32-bit timers is able to generate DMA trigger
- Each 32-bit timers is able to generate timeout interrupts
- Two timers can be cascaded to form a 64-bit timer
- Each timer can be programmed as ADC/TPM trigger source
- Timer 0 is able to trigger DAC

2.2.11 LPTMR

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The LPTMR module has the following features:

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wakeup from any low-power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter

2.2.12 UART

This device contains a basic universal asynchronous receiver/transmitter (UART) module with DMA function supported. Generally, this module is used in RS-232, RS-485, and other communications. It also supports LIN slave operation and ISO7816.

The UART module has the following features:

- Full-duplex operation
- 13-bit baud rate selection with /32 fractional divide, based on the module clock frequency
- Programmable 8-bit or 9-bit data format
- Programmable transmitter output polarity
- Programmable receive input polarity
- Up to 14-bit break character transmission.
- 11-bit break character detection option
- Two receiver wakeup methods with idle line or address mark wakeup
- Address match feature in the receiver to reduce address mark wakeup ISR overhead
- Ability to select MSB or LSB to be the first bit on wire
- Support for ISO 7816 protocol to interface with SIM cards and smart cards
- Receiver framing error detection
- Hardware parity generation and checking
- 1/16 bit-time noise detection
- DMA interface

2.2.13 LPUART

This product contains two Low-Power UART modules, both of their clock sources are selectable from IRC48M, IRC8M/2M or external crystal clock, and can work in Stop and VLPS modes. They also support 4x to 32x data oversampling rate to meet different applications.

The LPUART module has the following features:

- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4x to 32x
- Transmit and receive baud rate can operate asynchronous to the bus clock and can be configured independently of the bus clock frequency, support operation in Stop mode
- Interrupt, DMA or polled operation
- Hardware parity generation and checking
- Programmable 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods
    - Idle line wakeup
    - Address mark wakeup
    - Receive data match
- Automatic address matching to reduce ISR overhead:

    - Address mark matching
    - Idle line address matching
    - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity

2.2.14 SPI

This device contains two SPI modules. SPI modules support 8-bit and 16-bit modes. FIFO function is available only on SPI1 module.

The SPI modules have the following features:

- Full-duplex or single-wire bidirectional mode
- Programmable transmit bit rate
- Double-buffered transmit and receive data register
- Serial clock phase and polarity options
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Programmable 8- or 16-bit data transmission length
- Receive data buffer hardware match feature
- 64-bit FIFO mode for high speed/large amounts of data transfers
- Support DMA

2.2.15 I2C

This device contains two I2C modules, which support up to 1 Mbits/s by dual buffer features, and address match to wake MCU from the low power mode.

I2C modules support DMA transfer, and the interrupt condition can trigger DMA request when DMA function is enabled.

The I2C modules have the following features:

- Support for *system management bus (SMBus) specification, version 2*
- Software programmable for one of 64 different serial clock frequencies
- Software-selectable acknowledge bit
- Arbitration-lost interrupt with automatic mode switching from master to slave

- Calling address identification interrupt
- START and STOP signal generation and detection
- Repeated-START signal generation and detection
- Acknowledge bit generation and detection
- Bus busy detection
- General call recognition
- 10-bit address extension
- Programmable input glitch filter
- Low power mode wakeup on slave address match
- Range slave address support
- DMA support
- Double buffering support to achieve higher baud rate

2.2.16 USB

This device contains one USB module which implements a USB2.0 full-speed compliant peripheral and interfaces to the on-chip USBFS transceiver. It implements keep-alive feature to avoid re-enumerating when exiting from low power modes and enables HIRC48M to allow crystal-less USB operation.

The USBFS has the following features:

- USB 1.1 and 2.0 compliant full-speed device controller
- 16 bidirectional end points
- DMA or FIFO data stream interfaces
- Low-power consumption
- HIRC48 with clock-recovery is supported to eliminate the 48 MHz crystal. It is used for USB device-only implementation.
- USB keeps alive in low power mode down to VLPS and is able to wake MCU from low power mode

2.2.17 FlexIO

The FlexIO is a highly configurable module providing a wide range of protocols including, but not limited to UART, I2C, SPI, Camera IF, LCD RGB, PWM/Waveform generation. The module supports programmable baud rates independent of bus clock frequency, with automatic start/stop bit generation.

The FlexIO module has the following features:

- Functional in VLPR/VLPW/Stop/VLPS mode provided the clock it is using remains enabled
- Four 32-bit double buffered shift registers with transmit, receive, and data match modes, and continuous data transfer
- The timing of the shifter's shift, load and store events are controlled by the highly flexible 16-bit timer assigned to the shifter
- Two or more shifters can be concatenated to support large data transfer sizes
- Each 16-bit timers operates independently, supports for reset, enable and disable on a variety of internal or external trigger conditions with programmable trigger polarity
- Flexible pin configuration supporting output disabled, open drain, bidirectional output data and output mode
- Supports interrupt, DMA or polled transmit/receive operation

2.2.18 Port control and GPIO

The Port Control and Interrupt (PORT) module provides support for port control, digital filtering, and external interrupt functions. The GPIO data direction and output data registers control the direction and output data of each pin when the pin is configured for the GPIO function. The GPIO input data register displays the logic value on each pin when the pin is configured for any digital function, provided the corresponding Port Control and Interrupt module for that pin is enabled.

The PORT module has the following features:

- all PIN support interrupt enable
- Configurable edge (rising, falling, or both) or level sensitive interrupt type
- Support DMA request
- Asynchronous wake-up in low-power modes
- Configurable pullup, pulldown, and pull-disable on select pins
- Configurable high and low drive strength on selected pins
- Configurable fast and slow slew rates on selected pins
- Configurable passive filter on selected pins
- Individual mux control field supporting analog or pin disabled, GPIO, and up to chip-specific digital functions
- Pad configuration fields are functional in all digital pin muxing modes.

The GPIO module has the following features:

- Port Data Input register visible in all digital pin-multiplexing modes
- Port Data Output register with corresponding set/clear/toggle registers

- Port Data Direction register
- GPIO support single-cycle access via fast GPIO.

3 Memory map

This device contains various memories and memory-mapped peripherals which are located in a 4 GB memory space. The following figure shows the system memory and peripheral locations

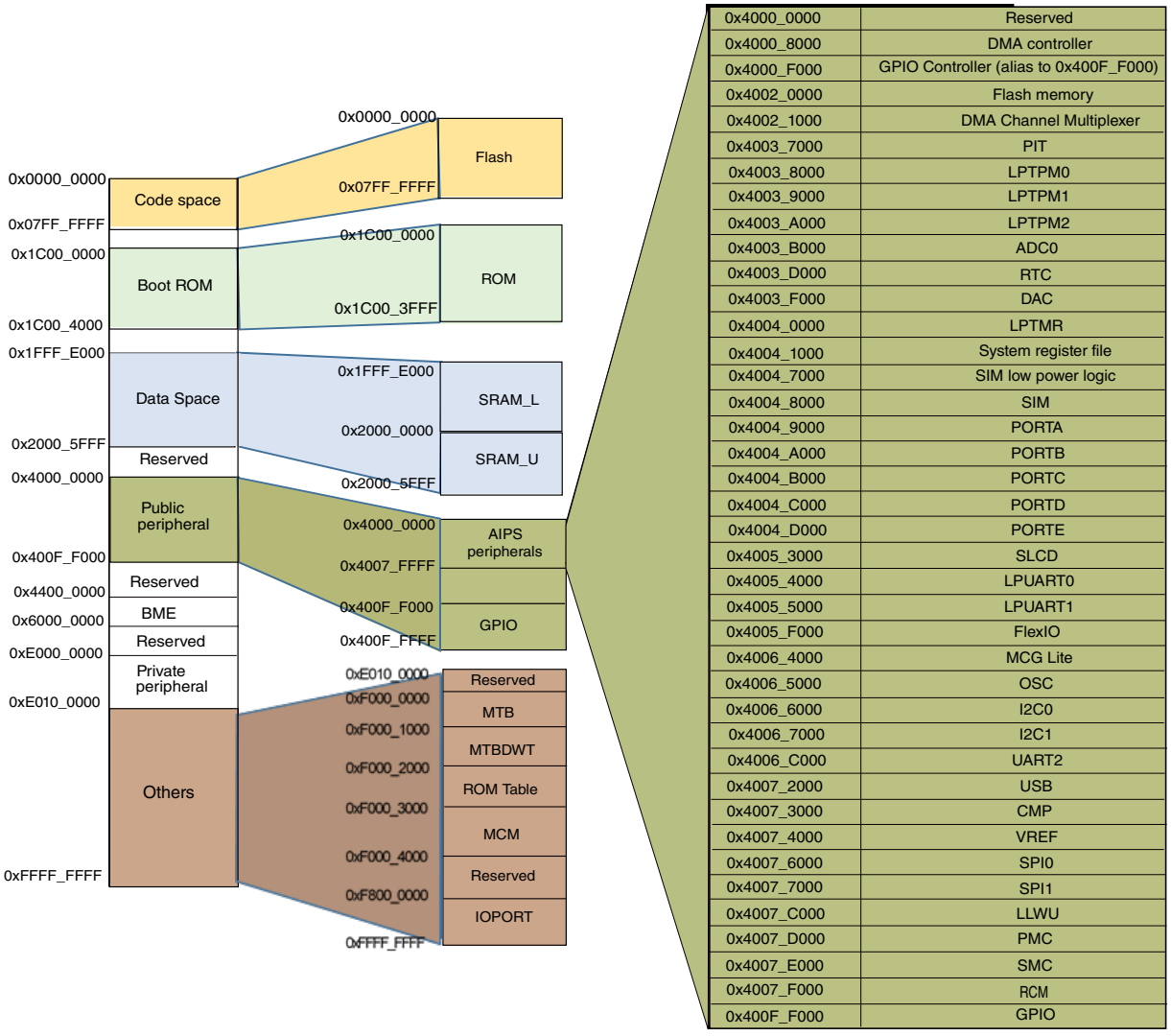


Figure 4. Memory map

4 Pinouts

4.1 K32 L2B Signal Multiplexing and Pin Assignments (LQFP and MAPBGA)

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

VREFH can act as VREF_OUT when VREFV1 module is enabled.

64 MAP BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
A1	1	PTE0	LCD_P48	LCD_P48	PTE0/ CLKOUT32K	SPI1_MISO	LPUART1_TX	RTC_CLKOUT	CMP0_OUT	I2C1_SDA	LCD_P48
B1	2	PTE1	LCD_P49	LCD_P49	PTE1	SPI1_MOSI	LPUART1_RX		SPI1_MISO	I2C1_SCL	LCD_P49
—	3	VDD	VDD	VDD							
C4	4	VSS	VSS	VSS							
E1	5	USB0_DP	USB0_DP	USB0_DP							
D1	6	USB0_DM	USB0_DM	USB0_DM							
E2	7	VOUT33	VOUT33	VOUT33							
D2	8	VREGIN	VREGIN	VREGIN							
G1	9	PTE20	LCD_P59/ ADC0_DP0/ ADC0_SE0	LCD_P59/ ADC0_DP0/ ADC0_SE0	PTE20		TPM1_CH0	LPUART0_TX		FXIO0_D4	LCD_P59
F1	10	PTE21	LCD_P60/ ADC0_DM0/ ADC0_SE4a	LCD_P60/ ADC0_DM0/ ADC0_SE4a	PTE21		TPM1_CH1	LPUART0_RX		FXIO0_D5	LCD_P60
G2	11	PTE22	ADC0_DP3/ ADC0_SE3	ADC0_DP3/ ADC0_SE3	PTE22		TPM2_CH0	UART2_TX		FXIO0_D6	
F2	12	PTE23	ADC0_DM3/ ADC0_SE7a	ADC0_DM3/ ADC0_SE7a	PTE23		TPM2_CH1	UART2_RX		FXIO0_D7	
F4	13	VDDA	VDDA	VDDA							
G4	14	VREFH	VREFH	VREFH							
G3	15	VREFL	VREFL	VREFL							
F3	16	VSSA	VSSA	VSSA							
H1	17	PTE29	CMP0_IN5/ ADC0_SE4b	CMP0_IN5/ ADC0_SE4b	PTE29		TPM0_CH2	TPM_CLKIN0			

64 MAP BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
H2	18	PTE30	DAC0_OUT/ ADC0_SE23/ CMP0_IN4	DAC0_OUT/ ADC0_SE23/ CMP0_IN4	PTE30		TPM0_CH3	TPM_CLKIN1	LPUART1_TX	LPTMR0_ ALT1	
H3	19	PTE31	DISABLED		PTE31		TPM0_CH4				
H4	20	PTE24	DISABLED		PTE24		TPM0_CH0		I2C0_SCL		
H5	21	PTE25	DISABLED		PTE25		TPM0_CH1		I2C0_SDA		
D3	22	PTA0	SWD_CLK		PTA0		TPM0_CH5				SWD_CLK
D4	23	PTA1	DISABLED		PTA1	LPUART0_RX	TPM2_CH0				
E5	24	PTA2	DISABLED		PTA2	LPUART0_TX	TPM2_CH1				
D5	25	PTA3	SWD_DIO		PTA3	I2C1_SCL	TPM0_CH0				SWD_DIO
G5	26	PTA4	NMI_b		PTA4	I2C1_SDA	TPM0_CH1				NMI_b
F5	27	PTA5	DISABLED		PTA5	USB_CLKIN	TPM0_CH2				
H6	28	PTA12	DISABLED		PTA12		TPM1_CH0				
G6	29	PTA13	DISABLED		PTA13		TPM1_CH1				
G7	30	VDD	VDD	VDD							
H7	31	VSS	VSS	VSS							
H8	32	PTA18	EXTAL0	EXTAL0	PTA18		LPUART1_RX	TPM_CLKIN0			
G8	33	PTA19	XTAL0	XTAL0	PTA19		LPUART1_TX	TPM_CLKIN1		LPTMR0_ ALT1	
F8	34	PTA20	RESET_b		PTA20						RESET_b
F7	35	PTB0/ LLWU_P5	LCD_P0/ ADC0_SE8	LCD_P0/ ADC0_SE8	PTB0/ LLWU_P5	I2C0_SCL	TPM1_CH0				LCD_P0
F6	36	PTB1	LCD_P1/ ADC0_SE9	LCD_P1/ ADC0_SE9	PTB1	I2C0_SDA	TPM1_CH1				LCD_P1
E7	37	PTB2	LCD_P2/ ADC0_SE12	LCD_P2/ ADC0_SE12	PTB2	I2C0_SCL	TPM2_CH0				LCD_P2
E8	38	PTB3	LCD_P3/ ADC0_SE13	LCD_P3/ ADC0_SE13	PTB3	I2C0_SDA	TPM2_CH1				LCD_P3
E6	39	PTB16	LCD_P12	LCD_P12	PTB16	SPI1_MOSI	LPUART0_RX	TPM_CLKIN0	SPI1_MISO		LCD_P12
D7	40	PTB17	LCD_P13	LCD_P13	PTB17	SPI1_MISO	LPUART0_TX	TPM_CLKIN1	SPI1_MOSI		LCD_P13
D6	41	PTB18	LCD_P14	LCD_P14	PTB18		TPM2_CH0				LCD_P14
C7	42	PTB19	LCD_P15	LCD_P15	PTB19		TPM2_CH1				LCD_P15
D8	43	PTC0	LCD_P20/ ADC0_SE14	LCD_P20/ ADC0_SE14	PTC0		EXTRG_IN	audioUSB_ SOF_OUT	CMP0_OUT		LCD_P20
C6	44	PTC1/ LLWU_P6/ RTC_CLKIN	LCD_P21/ ADC0_SE15	LCD_P21/ ADC0_SE15	PTC1/ LLWU_P6/ RTC_CLKIN	I2C1_SCL		TPM0_CH0			LCD_P21
B7	45	PTC2	LCD_P22/ ADC0_SE11	LCD_P22/ ADC0_SE11	PTC2	I2C1_SDA		TPM0_CH1			LCD_P22
C8	46	PTC3/ LLWU_P7	LCD_P23	LCD_P23	PTC3/ LLWU_P7	SPI1_SCK	LPUART1_RX	TPM0_CH2	CLKOUT		LCD_P23
E3	47	VSS	VSS	VSS							

64 MAP BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
E4	—	VDD	VDD	VDD							
C5	48	VLL3	VLL3	VLL3							
A6	49	VLL2	VLL2/ LCD_P4	VLL2/ LCD_P4	PTC20						LCD_P4
B5	50	VLL1	VLL1/ LCD_P5	VLL1/ LCD_P5	PTC21						LCD_P5
B4	51	VCAP2	VCAP2/ LCD_P6	VCAP2/ LCD_P6	PTC22						LCD_P6
A5	52	VCAP1	VCAP1/ LCD_P39	VCAP1/ LCD_P39	PTC23						LCD_P39
B8	53	PTC4/ LLWU_P8	LCD_P24	LCD_P24	PTC4/ LLWU_P8	SPI0_SS	LPUART1_TX	TPM0_CH3			LCD_P24
A8	54	PTC5/ LLWU_P9	LCD_P25	LCD_P25	PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2			CMP0_OUT	LCD_P25
A7	55	PTC6/ LLWU_P10	LCD_P26/ CMP0_IN0	LCD_P26/ CMP0_IN0	PTC6/ LLWU_P10	SPI0_MOSI	EXTRG_IN		SPI0_MISO		LCD_P26
B6	56	PTC7	LCD_P27/ CMP0_IN1	LCD_P27/ CMP0_IN1	PTC7	SPI0_MISO	audioUSB_ SOF_OUT		SPI0_MOSI		LCD_P27
C3	57	PTD0	LCD_P40	LCD_P40	PTD0	SPI0_SS		TPM0_CH0		FXIO0_D0	LCD_P40
A4	58	PTD1	LCD_P41/ ADC0_SE5b	LCD_P41/ ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1		FXIO0_D1	LCD_P41
C2	59	PTD2	LCD_P42	LCD_P42	PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO	FXIO0_D2	LCD_P42
B3	60	PTD3	LCD_P43	LCD_P43	PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI	FXIO0_D3	LCD_P43
A3	61	PTD4/ LLWU_P14	LCD_P44	LCD_P44	PTD4/ LLWU_P14	SPI1_SS	UART2_RX	TPM0_CH4		FXIO0_D4	LCD_P44
C1	62	PTD5	LCD_P45/ ADC0_SE6b	LCD_P45/ ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5		FXIO0_D5	LCD_P45
B2	63	PTD6/ LLWU_P15	LCD_P46/ ADC0_SE7b	LCD_P46/ ADC0_SE7b	PTD6/ LLWU_P15	SPI1_MOSI	LPUART0_RX		SPI1_MISO	FXIO0_D6	LCD_P46
A2	64	PTD7	LCD_P47	LCD_P47	PTD7	SPI1_MISO	LPUART0_TX		SPI1_MOSI	FXIO0_D7	LCD_P47

4.2 K32 L2B Signal Multiplexing and Pin Assignments (QFN)

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

32 QFN	48 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	1	VDD	VDD	VDD							
—	7	PTE20	ADC0_DP0/ ADC0_SE0	ADC0_DP0/ ADC0_SE0	PTE20		TPM1_CH0	LPUART0_TX		FXIO0_D4	

32 QFN	48 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	8	PTE21	ADC0_DM0/ ADC0_SE4a	ADC0_DM0/ ADC0_SE4a	PTE21		TPM1_CH1	LPUART0_RX		FXIO0_D5	
—	10	VREFH	VREFH	VREFH							
—	11	VREFL	VREFL	VREFL							
—	13	PTE29	CMP0_IN5/ ADC0_SE4b	CMP0_IN5/ ADC0_SE4b	PTE29		TPM0_CH2	TPM_CLKIN0			
—	15	PTE24	DISABLED		PTE24		TPM0_CH0		I2C0_SCL		
—	16	PTE25	DISABLED		PTE25		TPM0_CH1		I2C0_SDA		
—	29	PTB2	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	TPM2_CH0				
—	30	PTB3	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	TPM2_CH1				
—	31	PTB16	DISABLED		PTB16	SPI1_MOSI	LPUART0_RX	TPM_CLKIN0	SPI1_MISO		
—	32	PTB17	DISABLED		PTB17	SPI1_MISO	LPUART0_TX	TPM_CLKIN1	SPI1_MOSI		
—	33	PTC0	ADC0_SE14	ADC0_SE14	PTC0		EXTRG_IN	audioUSB_ SOF_OUT	CMP0_OUT		
—	41	PTD0	DISABLED		PTD0	SPI0_SS		TPM0_CH0		FXIO0_D0	
—	42	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1		FXIO0_D1	
—	43	PTD2	DISABLED		PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO	FXIO0_D2	
—	44	PTD3	DISABLED		PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI	FXIO0_D3	
1	—	PTE0	DISABLED		PTE0/ CLKOUT32K	SPI1_MISO	LPUART1_TX	RTC_CLKOUT	CMP0_OUT	I2C1_SDA	
2	2	VSS	VSS	VSS							
3	3	USB0_DP	USB0_DP	USB0_DP							
4	4	USB0_DM	USB0_DM	USB0_DM							
5	5	VOUT33	VOUT33	VOUT33							
6	6	VREGIN	VREGIN	VREGIN							
7	9	VDDA	VDDA	VDDA							
8	12	VSSA	VSSA	VSSA							
9	14	PTE30	DAC0_OUT/ ADC0_SE23/ CMP0_IN4	DAC0_OUT/ ADC0_SE23/ CMP0_IN4	PTE30		TPM0_CH3	TPM_CLKIN1	LPUART1_TX	LPTMR0_ ALT1	
10	17	PTA0	SWD_CLK		PTA0		TPM0_CH5				SWD_CLK
11	18	PTA1	DISABLED		PTA1	LPUART0_RX	TPM2_CH0				
12	19	PTA2	DISABLED		PTA2	LPUART0_TX	TPM2_CH1				
13	20	PTA3	SWD_DIO		PTA3	I2C1_SCL	TPM0_CH0				SWD_DIO
14	21	PTA4	NMI_b		PTA4	I2C1_SDA	TPM0_CH1				NMI_b
15	22	VDD	VDD	VDD							
16	23	VSS	VSS	VSS							
17	24	PTA18	EXTAL0	EXTAL0	PTA18		LPUART1_RX	TPM_CLKIN0			
18	25	PTA19	XTAL0	XTAL0	PTA19		LPUART1_TX	TPM_CLKIN1		LPTMR0_ ALT1	
19	26	PTA20	RESET_b		PTA20						RESET_b

32 QFN	48 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
20	27	PTB0/ LLWU_P5	ADC0_SE8	ADC0_SE8	PTB0/ LLWU_P5	I2C0_SCL	TPM1_CH0				
21	28	PTB1	ADC0_SE9	ADC0_SE9	PTB1	I2C0_SDA	TPM1_CH1				
22	34	PTC1/ LLWU_P6/ RTC_CLKIN	ADC0_SE15	ADC0_SE15	PTC1/ LLWU_P6/ RTC_CLKIN	I2C1_SCL		TPM0_CH0			
23	35	PTC2	ADC0_SE11	ADC0_SE11	PTC2	I2C1_SDA		TPM0_CH1			
24	36	PTC3/ LLWU_P7	DISABLED		PTC3/ LLWU_P7	SPI1_SCK	LPUART1_RX	TPM0_CH2	CLKOUT		
25	37	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_SS	LPUART1_TX	TPM0_CH3			
26	38	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2			CMP0_OUT	
27	39	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_MOSI	EXTRG_IN		SPI0_MISO		
28	40	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_MISO	audioUSB_ SOF_OUT		SPI0_MOSI		
29	45	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI1_SS	UART2_RX	TPM0_CH4		FXIO0_D4	
30	46	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5		FXIO0_D5	
31	47	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI1_MOSI	LPUART0_RX		SPI1_MISO	FXIO0_D6	
32	48	PTD7	DISABLED		PTD7	SPI1_MISO	LPUART0_TX		SPI1_MOSI	FXIO0_D7	

4.3 Pin properties

The following table lists the pin properties of 64 LQFP/MAPBGA package.

64 LQFP	64 MAPBGA	Pin name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
1	A1	PTE0	ND	Hi-Z	—	SS	N	N	N
2	B1	PTE1	ND	Hi-Z	—	SS	N	N	N

Table continues on the next page...

64 LQFP	64 MAPBGA	Pin name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
3	—	VDD	—	—	—	—	—	—	—
4	C4	VSS	—	—	—	—	—	—	—
5	E1	USB0_DP	—	—	—	—	—	—	—
6	D1	USB0_DM	—	—	—	—	—	—	—
7	E2	VOUT33	—	—	—	—	—	—	—
8	D2	VREGIN	—	—	—	—	—	—	—
9	G1	PTE20	ND	Hi-Z	—	SS	N	N	N
10	F1	PTE21	ND	Hi-Z	—	SS	N	N	N
11	G2	PTE22	ND	Hi-Z	—	SS	N	N	N
12	F2	PTE23	ND	Hi-Z	—	SS	N	N	N
13	F4	VDDA	—	—	—	—	—	—	—
14	G4	VREFH	—	—	—	—	—	—	—
15	G3	VREFL	—	—	—	—	—	—	—
16	F3	VSSA	—	—	—	—	—	—	—
17	H1	PTE29	ND	Hi-Z	—	SS	N	N	N
18	H2	PTE30	ND	Hi-Z	—	SS	N	N	N
19	H3	PTE31	ND	Hi-Z	—	SS	N	N	N
20	H4	PTE24	ND	Hi-Z	—	SS	N	N	N
21	H5	PTE25	ND	Hi-Z	—	SS	N	N	N
22	D3	PTA0	ND	L	PD	SS	N	N	Y
23	D4	PTA1	ND	Hi-Z	—	SS	N	N	Y
24	E5	PTA2	ND	Hi-Z	—	SS	N	N	Y
25	D5	PTA3	ND	H	PU	FS	N	N	Y
26	G5	PTA4	ND	H	PU	SS	N	N	Y
27	F5	PTA5	ND	Hi-Z	—	SS	N	N	Y
28	H6	PTA12	ND	Hi-Z	—	SS	N	N	Y
29	G6	PTA13	ND	Hi-Z	—	SS	N	N	Y
30	G7	VDD	—	—	—	—	—	—	—
31	H7	VSS	—	—	—	—	—	—	—

Table continues on the next page...

64 LQFP	64 MAPBGA	Pin name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
32	H8	PTA18	ND	Hi-Z	—	SS	N	N	Y
33	G8	PTA19	ND	Hi-Z	—	SS	N	N	Y
34	F8	PTA20	ND	H	PU	SS	Y	Y	Y
35	F7	PTB0/LLWU_P5	HD	Hi-Z	—	SS	N	N	N
36	F6	PTB1	HD	Hi-Z	—	SS	N	N	N
37	E7	PTB2	ND	Hi-Z	—	SS	N	N	N
38	E8	PTB3	ND	Hi-Z	—	SS	N	N	N
39	E6	PTB16	ND	Hi-Z	—	FS	N	N	N
40	D7	PTB17	ND	Hi-Z	—	FS	N	N	N
41	D6	PTB18	ND	Hi-Z	—	SS	N	N	N
42	C7	PTB19	ND	Hi-Z	—	SS	N	N	N
43	D8	PTC0	ND	Hi-Z	—	SS	N	N	Y
44	C6	PTC1/LLWU_P6/ RTC_CLKIN	ND	Hi-Z	—	SS	N	N	Y
45	B7	PTC2	ND	Hi-Z	—	SS	N	N	Y
46	C8	PTC3/LLWU_P7	HD	Hi-Z	—	FS	N	N	Y
47	E3	VSS	—	—	—	—	—	—	—
—	E4	VDD	—	—	—	—	—	—	—
48	C5	VLL3	—	—	—	—	—	—	—
49	A6	VLL2	—	—	—	—	—	—	—
50	B5	VLL1	—	—	—	—	—	—	—
51	B4	VCAP2	—	—	—	—	—	—	—
52	A5	VCAP1	—	—	—	—	—	—	—
53	B8	PTC4/LLWU_P8	HD	Hi-Z	—	FS	N	N	Y
54	A8	PTC5/LLWU_P9	ND	Hi-Z	—	FS	N	N	Y
55	A7	PTC6/LLWU_P10	ND	Hi-Z	—	FS	N	N	Y
56	B6	PTC7	ND	Hi-Z	—	FS	N	N	Y
57	C3	PTD0	ND	Hi-Z	—	SS	N	N	Y
58	A4	PTD1	ND	Hi-Z	—	SS	N	N	Y

Table continues on the next page...

64 LQFP	64 MAPBGA	Pin name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
59	C2	PTD2	ND	Hi-Z	—	SS	N	N	Y
60	B3	PTD3	ND	Hi-Z	—	SS	N	N	Y
61	A3	PTD4/LLWU_P14	ND	Hi-Z	—	FS	N	N	Y
62	C1	PTD5	ND	Hi-Z	—	FS	N	N	Y
63	B2	PTD6/LLWU_P15	HD	Hi-Z	—	FS	N	N	Y
64	A2	PTD7	HD	Hi-Z	—	FS	N	N	Y

The following table lists the pin properties of 32/48 QFN package.

32 QFN	48 QFN	Pin name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
—	1	VDD	—	—	—	—	—	—	—
—	7	PTE20	ND	Hi-Z	—	SS	N	N	N
—	8	PTE21	ND	Hi-Z	—	SS	N	N	N
—	10	VREFH	—	—	—	—	—	—	—
—	11	VREFL	—	—	—	—	—	—	—
—	13	PTE29	ND	Hi-Z	—	SS	N	N	N
—	15	PTE24	ND	Hi-Z	—	SS	N	N	N
—	16	PTE25	ND	Hi-Z	—	SS	N	N	N

Table continues on the next page...

32 QFN	48 QFN	Pin name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
—	29	PTB2	ND	Hi-Z	—	SS	N	N	N
—	30	PTB3	ND	Hi-Z	—	SS	N	N	S
—	31	PTB16	ND	Hi-Z	—	FS	N	N	N
—	32	PTB17	ND	Hi-Z	—	FS	N	N	N
—	33	PTC0	ND	Hi-Z	—	SS	N	N	Y
—	41	PTD0	ND	Hi-Z	—	SS	N	N	Y
—	42	PTD1	ND	Hi-Z	—	SS	N	N	Y
—	43	PTD2	ND	Hi-Z	—	SS	N	N	Y
—	44	PTD3	ND	Hi-Z	—	SS	N	N	Y
1	—	PTE0	ND	Hi-Z	—	SS	N	N	N
2	2	VSS	—	—	—	—	—	—	—
3	3	USB0_DP	—	—	—	—	—	—	—
4	4	USB0_DM	—	—	—	—	—	—	—
5	5	VOUT33	—	—	—	—	—	—	—
6	6	VREGIN	—	—	—	—	—	—	—
7	9	VDDA	—	—	—	—	—	—	—
8	12	VSSA	—	—	—	—	—	—	—
9	14	PTE30	ND	Hi-Z	—	SS	N	N	N
10	17	PTA0	ND	L	PD	SS	N	N	Y
11	18	PTA1	ND	Hi-Z	—	SS	N	N	Y
12	19	PTA2	ND	Hi-Z	—	SS	N	N	Y
13	20	PTA3	ND	H	PU	FS	N	N	Y
14	21	PTA4	ND	H	PU	SS	N	N	Y
15	22	VDD	—	—	—	—	—	—	—
16	23	VSS	—	—	—	—	—	—	—
17	24	PTA18	ND	Hi-Z	—	SS	N	N	Y
18	25	PTA19	ND	Hi-Z	—	SS	N	N	Y
19	26	PTA20	ND	H	PU	SS	Y	Y	Y
20	27	PTB0/LLWU_P5	HD	Hi-Z	—	SS	N	N	N

Table continues on the next page...

32 QFN	48 QFN	Pin name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
21	28	PTB1	HD	Hi-Z	—	SS	N	N	N
22	34	PTC1/LLWU_P6/ RTC_CLKIN	ND	Hi-Z	—	SS	N	N	Y
23	35	PTC2	ND	Hi-Z	—	SS	N	N	Y
24	36	PTC3/LLWU_P7	HD	Hi-Z	—	FS	N	N	Y
25	37	PTC4/LLWU_P8	HD	Hi-Z	—	FS	N	N	Y
26	38	PTC5/LLWU_P9	ND	Hi-Z	—	FS	N	N	Y
27	39	PTC6/LLWU_P10	ND	Hi-Z	—	FS	N	N	Y
28	40	PTC7	ND	Hi-Z	—	FS	N	N	Y
29	45	PTD4/LLWU_P14	ND	Hi-Z	—	FS	N	N	Y
30	46	PTD5	ND	Hi-Z	—	FS	N	N	Y
31	47	PTD6/LLWU_P15	HD	Hi-Z	—	FS	N	N	Y
32	48	PTD7	HD	Hi-Z	—	FS	N	N	Y

Properties	Abbreviation	Descriptions
Driver strength	ND	Normal drive
	HD	High drive
Default status after POR	Hi-Z	High impendence
	H	High level
	L	Low level
Pullup/ pulldown setting after POR	PD	Pulldown
	PU	Pullup
Slew rate after POR	FS	Fast slew rate
	SS	Slow slew rate
Passive Pin Filter after POR	N	Disabled
	Y	Enabled
Open drain	N	Disabled[1]
	Y	Enabled[2]
Pin interrupt	Y	Yes

1. When I2C module is enabled and a pin is functional for I2C, this pin is (pseudo-) open drain enabled. When UART or LPUART module is enabled and a pin is functional for UART or LPUART, this pin is (pseudo-) open drain configurable.
2. PTA20 is a true open drain pin that must never be pulled above VDD.

4.4 Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

4.4.1 Core modules

Table 9. SWD signal descriptions

Chip signal name	Module signal name	Description	I/O
SWD_DIO	SWD_DIO	Serial Wire Debug Data Input/Output The SWD_DIO pin is used by an external debug tool for communication and device control. This pin is pulled up internally.	Input / Output
SWD_CLK	SWD_CLK	Serial Wire Clock This pin is the clock for debug logic when in the Serial Wire Debug mode. This pin is pulled down internally.	Input

4.4.2 System modules

Table 10. System signal descriptions

Chip signal name	Module signal name	Description	I/O
$\overline{\text{NMI}}$	—	Non-maskable interrupt **NOTE:** Driving the $\overline{\text{NMI}}$ signal low forces a non-maskable interrupt, if the $\overline{\text{NMI}}$ function is selected on the corresponding pin.	I
$\overline{\text{RESET}}$	—	Reset bidirectional signal	I/O
VDD	—	MCU power	I
VSS	—	MCU ground	I

Table 11. LLWU signal descriptions

Chip signal name	Module signal name	Description	I/O
LLWU_Pn	LLWU_Pn	Wakeup inputs	I

4.4.3 Clock modules

Table 12. OSC signal descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL0	EXTAL	External clock/Oscillator input	I
XTAL0	XTAL	Oscillator output	O

4.4.4 Analog

This table presents the signal descriptions of the ADC0 module.

Table 13. ADC0 signal descriptions

Chip signal name	Module signal name	Description	I/O
ADC0_DPn	DADP3–DADP0	Differential Analog Channel Inputs	I
ADC0_DMn	DADM3–DADM0	Differential Analog Channel Inputs	I
ADC0_SEn	AD*n*	Single-Ended Analog Channel Inputs	I
VREFH	V_{REFSH}	Voltage Reference Select High	I
VREFL	V_{REFSL}	Voltage Reference Select Low	I
VDDA	V_{DDA}	Analog Power Supply	I
VSSA	V_{SSA}	Analog Ground	I
EXTRG_IN	ADHWT	Hardware trigger	I

This table presents the signal descriptions of the CMP0 module.

Table 14. CMP0 signal descriptions

Chip signal name	Module signal name	Description	I/O
CMP0_IN[5:0]	IN[5:0]	Analog voltage inputs	I
CMP0_OUT	CMPO	Comparator output	O

Table 15. VREF signal descriptions

Chip signal name	Module signal name	Description	I/O
VREF_OUT	VREF_OUT	Internally-generated voltage reference output	O

4.4.5 Timer Modules

Table 16. TPM0 signal descriptions

Chip signal name	Module signal name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM0_CH[5:0]	TPM_CHn	TPM channel (n = 5 to 0). A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O
EXTRG_IN	ADHWT	Hardware trigger	I

Table 17. TPM1 signal descriptions

Chip signal name	Module signal name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM1_CH[1:0]	TPM_CHn	TPM channel (n = 1 to 0). A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O
EXTRG_IN	ADHWT	Hardware trigger	I

Table 18. TPM2 signal descriptions

Chip signal name	Module signal name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM2_CH[1:0]	TPM_CHn	TPM channel (n = 1 to 0). A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O
EXTRG_IN	ADHWT	Hardware trigger	I

Table 19. LPTMR0 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPTMR0_ALT[3:1]	LPTMR0_ALT*n*	Pulse Counter Input pin	I

Table 20. RTC signal descriptions

Chip signal name	Module signal name	Description	I/O
RTC_CLKOUT[1]	RTC_CLKOUT	1 Hz square-wave output or OSCERCLK	O

1. RTC_CLKOUT can also be driven with OSCERCLK via SIM control bit SIM_SOPT[RCTCLKOUTSEL]

4.4.6 Communication interfaces

Table 21. USB FS OTG Signal Descriptions

Chip signal name	Module signal name	Description	I/O
USB0_DM	usb_dm	USB D- analog data signal on the USB bus.	I/O
USB0_DP	usb_dp	USB D+ analog data signal on the USB bus.	I/O
USB_CLKIN	—	Alternate USB clock input	I

Table 22. SPI0 signal descriptions

Chip signal name	Module signal name	Description	I/O
SPI0_MISO	MISO	Master Data In, Slave Data Out	I/O
SPI0_MOSI	MOSI	Master Data Out, Slave Data In	I/O
SPI0_SCLK	SPSCK	SPI Serial Clock	I/O
SPI0_PCS0	$\overline{SS}$	Slave Select	I/O

Table 23. SPI1 signal descriptions

Chip signal name	Module signal name	Description	I/O
SPI1_MISO	MISO	Master Data In, Slave Data Out	I/O
SPI1_MOSI	MOSI	Master Data Out, Slave Data In	I/O
SPI1_SCLK	SPSCK	SPI Serial Clock	I/O
SPI1_PCS0	$\overline{SS}$	Slave Select	I/O

Table 24. I²C0 signal descriptions

Chip signal name	Module signal name	Description	I/O
I2C0_SCL	SCL	Bidirectional serial clock line of the I²C system.	I/O
I2C0_SDA	SDA	Bidirectional serial data line of the I²C system.	I/O

Table 25. I²C1 signal descriptions

Chip signal name	Module signal name	Description	I/O
I2C1_SCL	SCL	Bidirectional serial clock line of the I²C system.	I/O
I2C1_SDA	SDA	Bidirectional serial data line of the I²C system.	I/O

Table 26. LPUART0 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPUART0_TX	TxD	Transmit data	I/O
LPUART0_RX	RxD	Receive data	I

Table 27. LPUART1 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPUART1_TX	TxD	Transmit data	I/O
LPUART1_RX	RxD	Receive data	I

Table 28. UART2 signal descriptions

Chip signal name	Module signal name	Description	I/O
UART2_TX	TxD	Transmit data	O
UART2_RX	RxD	Receive data	I

Table 29. FlexIO signal descriptions

Chip signal name	Module signal name	Description	I/O
FXIO0_Dx	FXIO_Dn (n=0...7)	Bidirectional FlexIO Shifter and Timer pin inputs/outputs	I/O
EXTRG_IN	ADHWT	Hardware trigger	I

4.4.7 Human-machine interfaces (HMI)

Table 30. GPIO Signal Descriptions

Chip signal name	Module signal name	Description	I/O
PTA[20:0]	PORTA20–PORTA0	General-purpose input/output	I/O
PTB[19:0]	PORTB19–PORTB0	General-purpose input/output	I/O
PTD[7:0]	PORTD7–PORTD0	General-purpose input/output	I/O
PTE[31:0]	PORTE31–PORTE0	General-purpose input/output	I/O

Table 31. LCD Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LCD_Pn	LCD_P[63:0] . 64 LCD front plane/back plane	Configurable front plane/back plane driver that connects directly to the display. LCD_P[63:0] can operate as GPIO pins	O
V_{LL1}, V_{LL2}, V_{LL3}	V_{LL1}, V_{LL2}, V_{LL3}. LCD bias voltages	LCD bias voltages (requires external capacitors when charge pump is used).	I/O
V_{cap1}, V_{cap2}	V_{cap1}, V_{cap2}. LCD charge pump capacitance.	Charge pump capacitor pins.	O

4.5 K32 L2B LQFP and MAPBGA pinouts

Figure below shows the 64 LQFP pinouts

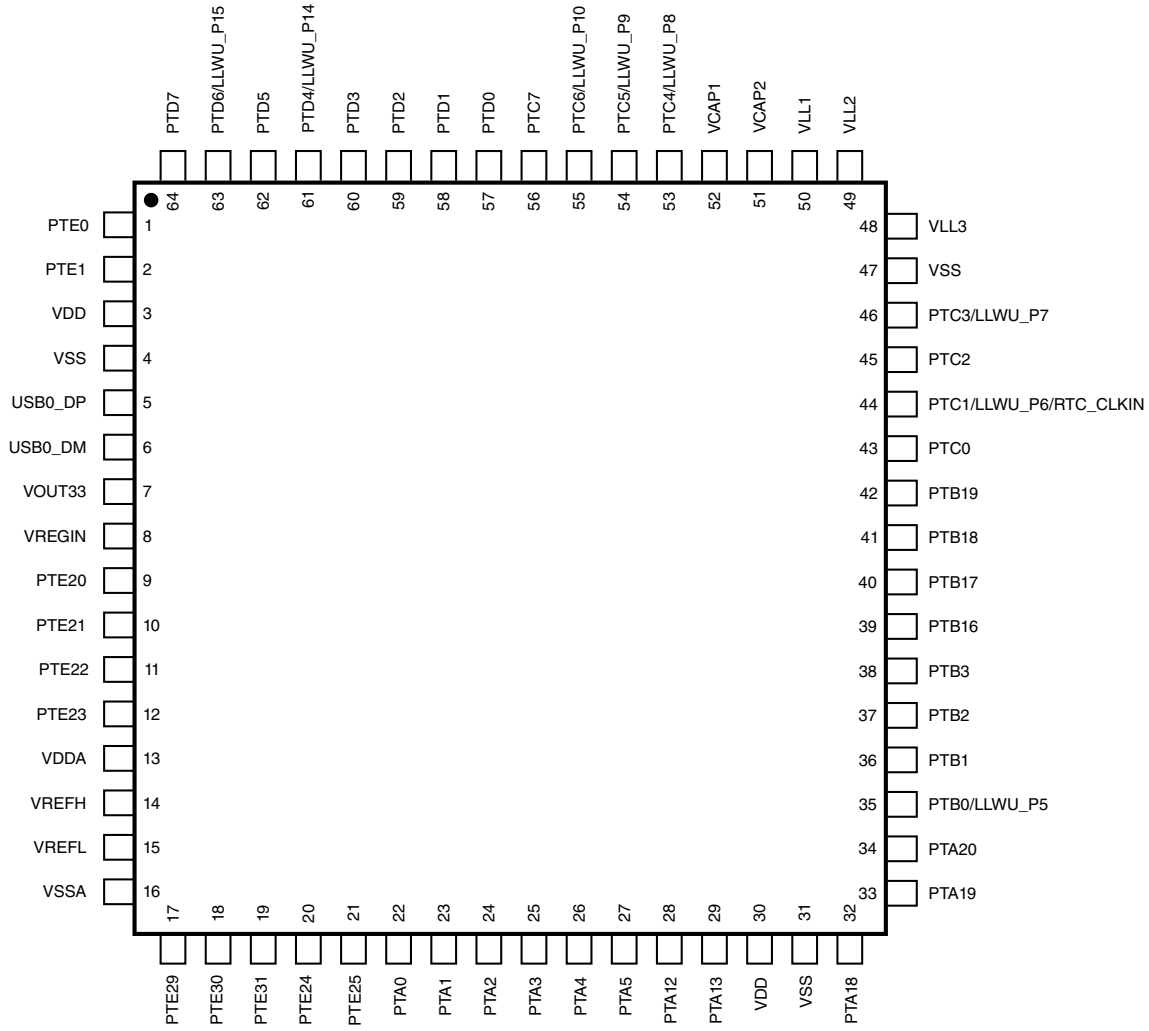


Figure 5. 64 LQFP Pinout diagram

Figure below shows the 64 MAPBGA pinouts

	1	2	3	4	5	6	7	8	
A	PTE0	PTD7	PTD4/ LLWU_P14	PTD1	VCAP1	VLL2	PTC6/ LLWU_P10	PTC5/ LLWU_P9	A
B	PTE1	PTD6/ LLWU_P15	PTD3	VCAP2	VLL1	PTC7	PTC2	PTC4/ LLWU_P8	B
C	PTD5	PTD2	PTD0	VSS	VLL3	PTC1/ LLWU_P6/ RTC_CLKIN	PTB19	PTC3/ LLWU_P7	C
D	USB0_DM	VREGIN	PTA0	PTA1	PTA3	PTB18	PTB17	PTC0	D
E	USB0_DP	VOUT33	VSS	VDD	PTA2	PTB16	PTB2	PTB3	E
F	PTE21	PTE23	VSSA	VDDA	PTA5	PTB1	PTB0/ LLWU_P5	PTA20	F
G	PTE20	PTE22	VREFL	VREFH	PTA4	PTA13	VDD	PTA19	G
H	PTE29	PTE30	PTE31	PTE24	PTE25	PTA12	VSS	PTA18	H
	1	2	3	4	5	6	7	8	

Figure 6. 64 MAPBGA Pinout diagram

4.6 K32 L2B QFN Pinouts

The figure below shows the 32 QFN pinouts.

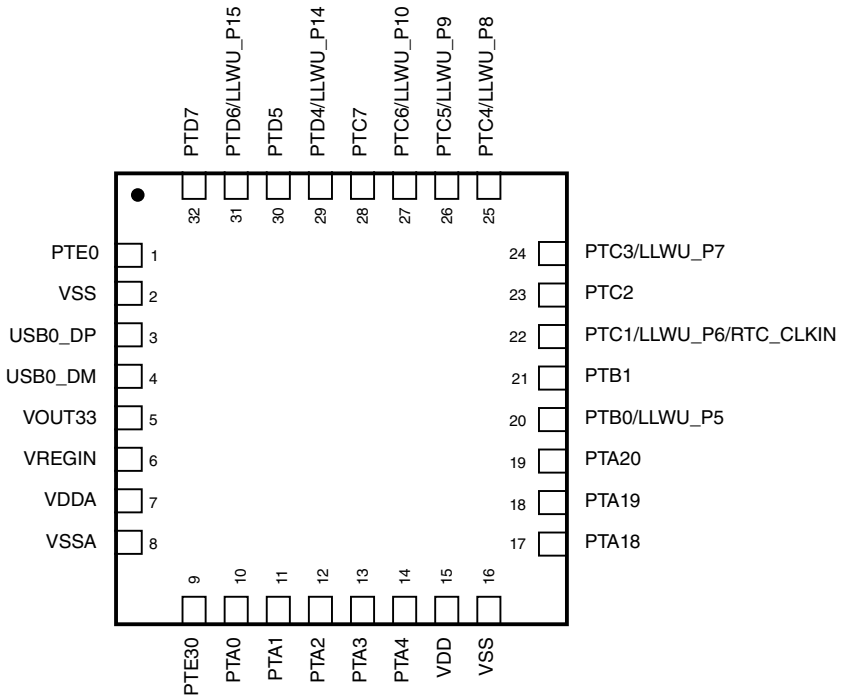


Figure 7. 32 QFN Pinout diagram (transparent top view)

The figure below shows the 48 QFN pinouts.

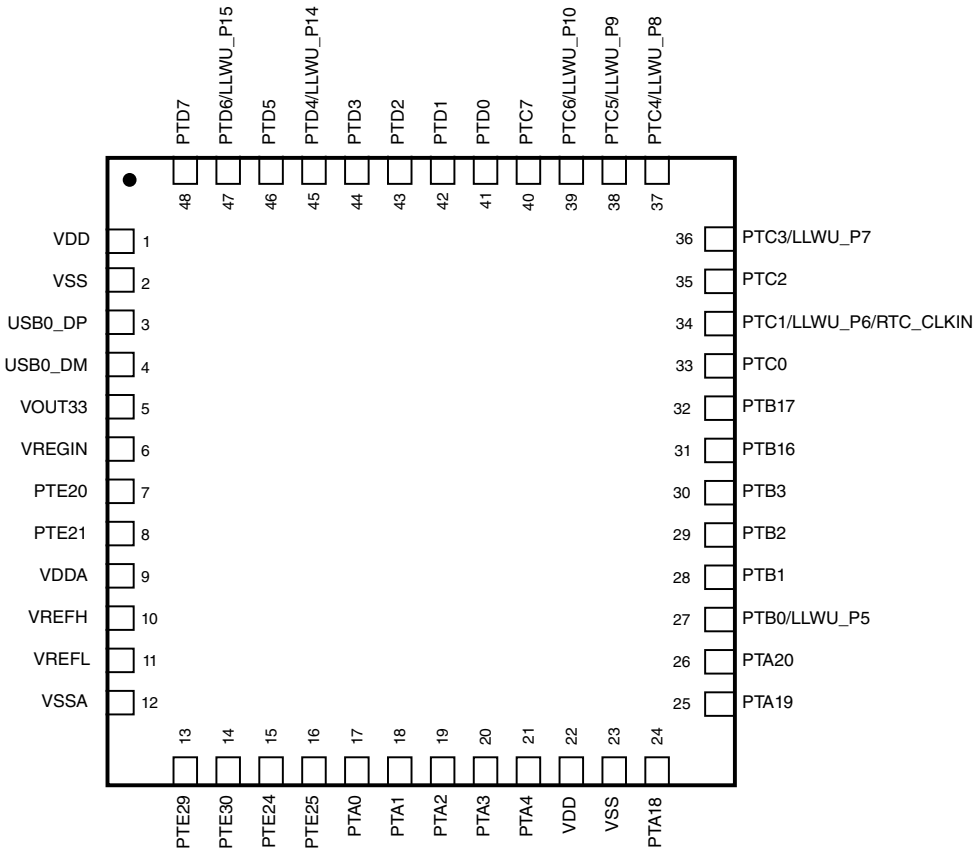


Figure 8. 48 QFN Pinout diagram (transparent top view)

4.7 Package dimensions

The following figures show the dimensions of the package options for the devices supported by this document.

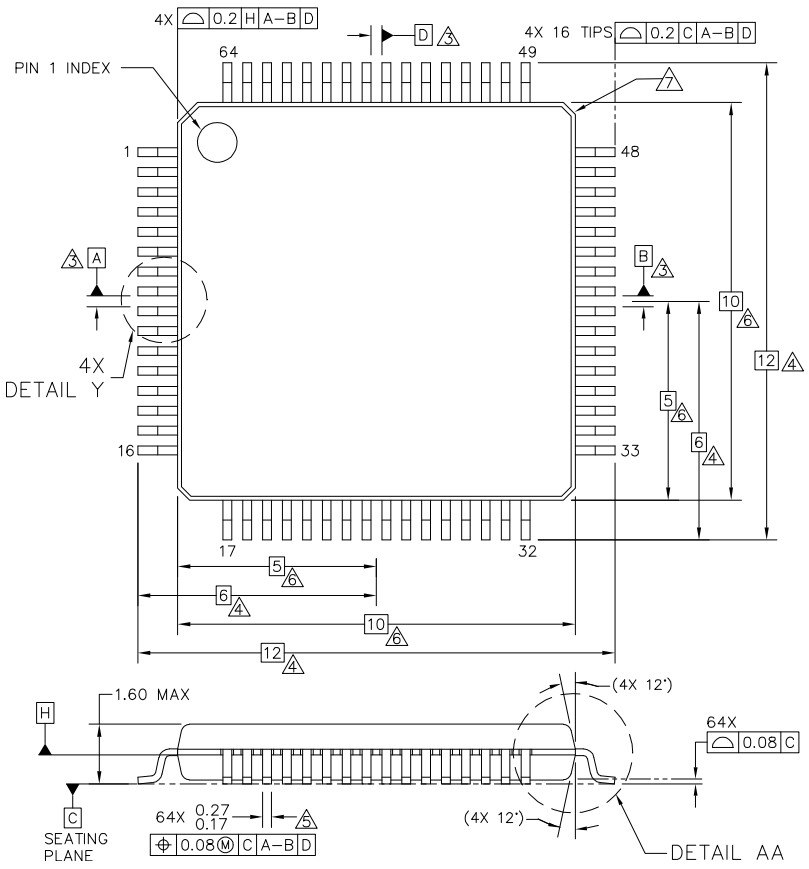
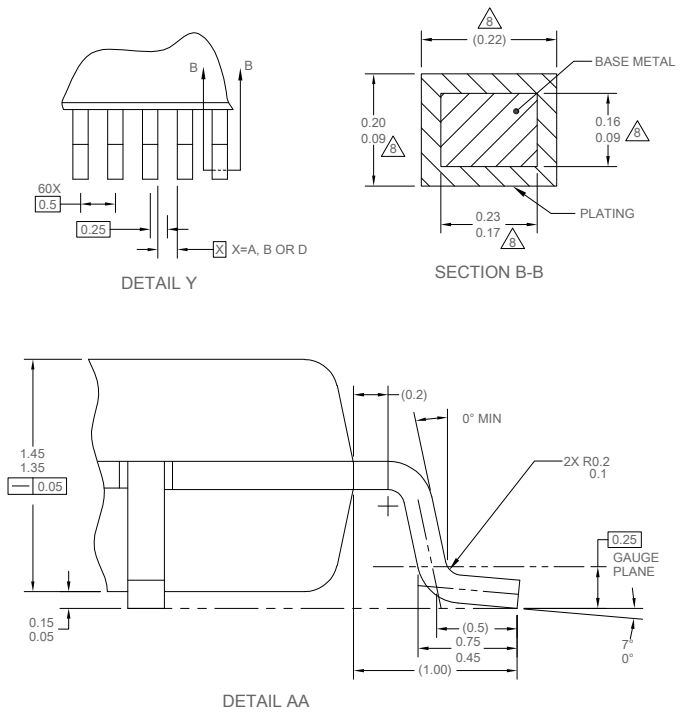


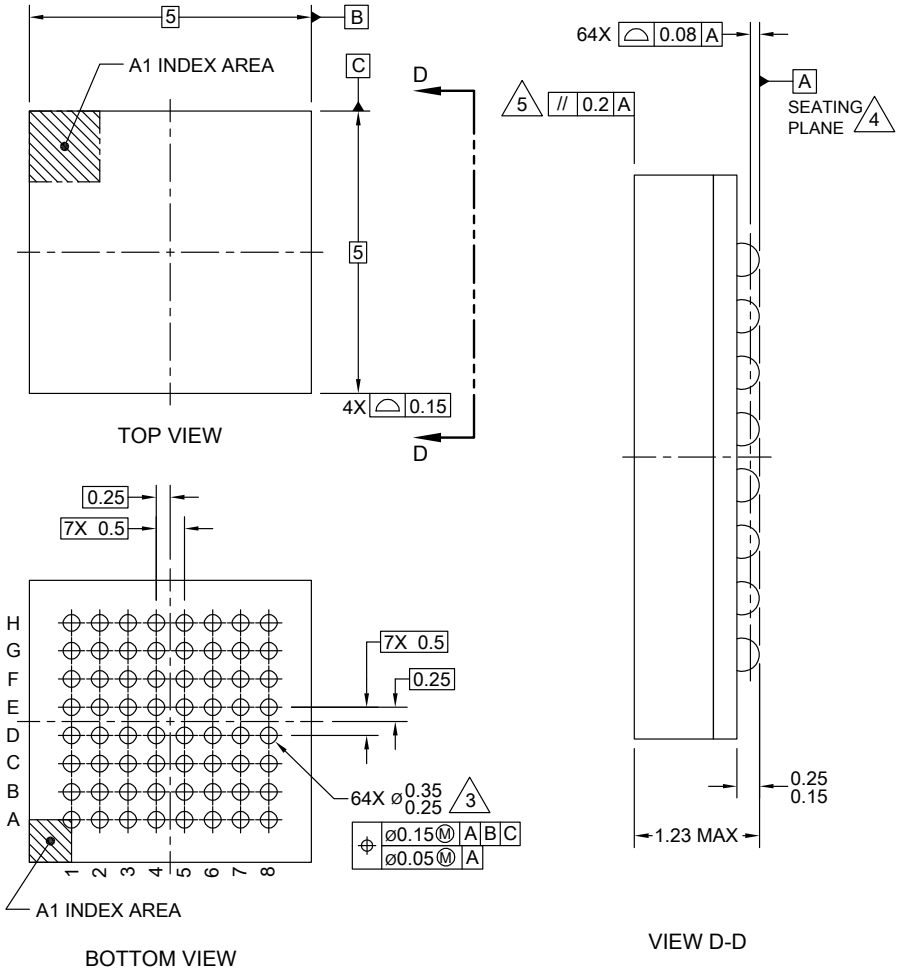
Figure 9. 64-pin LQFP package dimensions 1



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINDE AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

Figure 10. 64-pin LQFP package dimensions 2



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 11. 64-pin MAPBGA package dimension

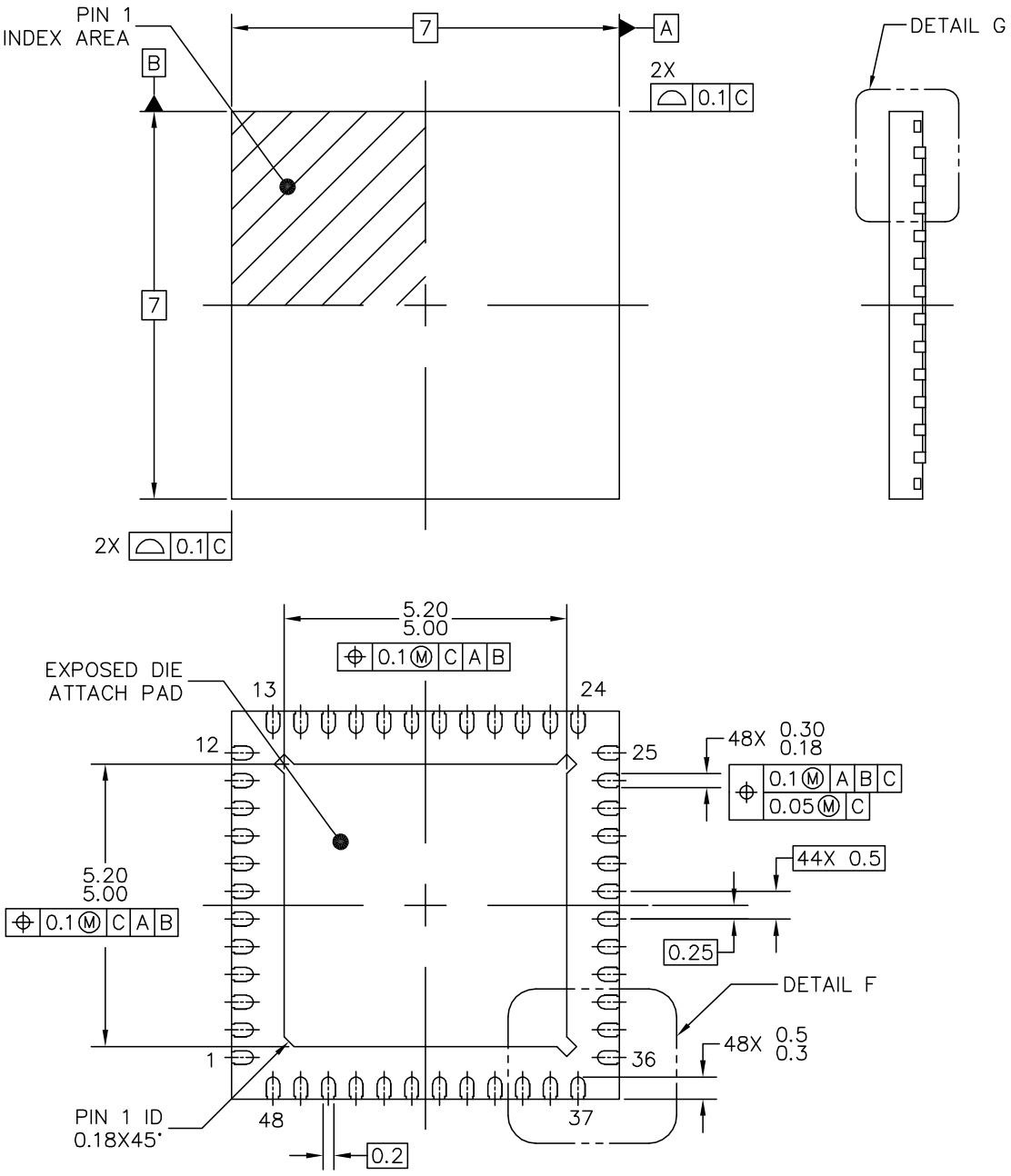
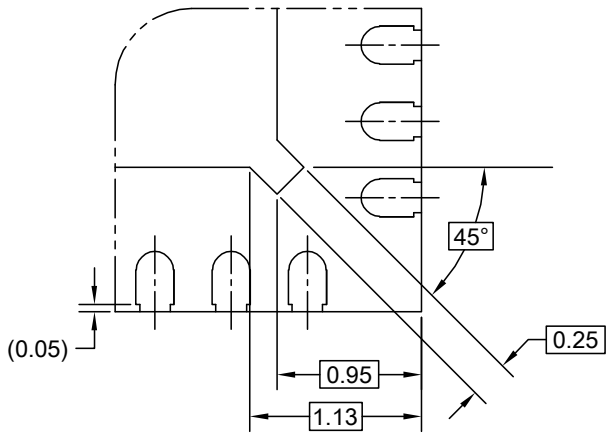
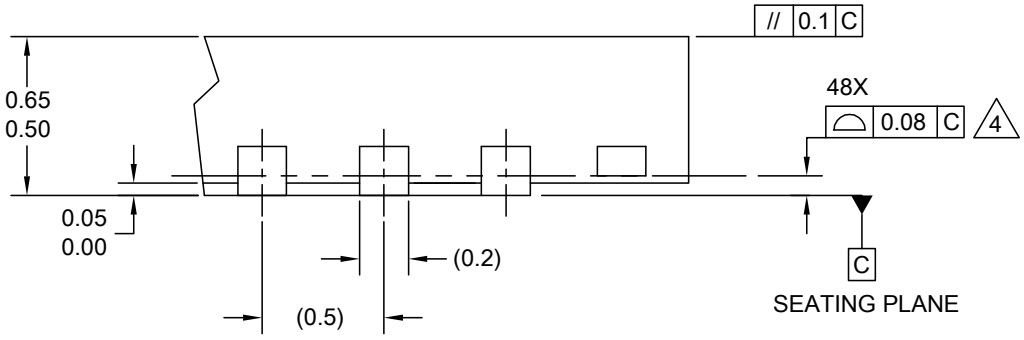


Figure 12. 48-pin QFN package dimension 1



DETAIL F



DETAIL G
VIEW ROTATED 90°CW

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THIS IS A NON-JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

Figure 13. 48-pin QFN package dimension 2

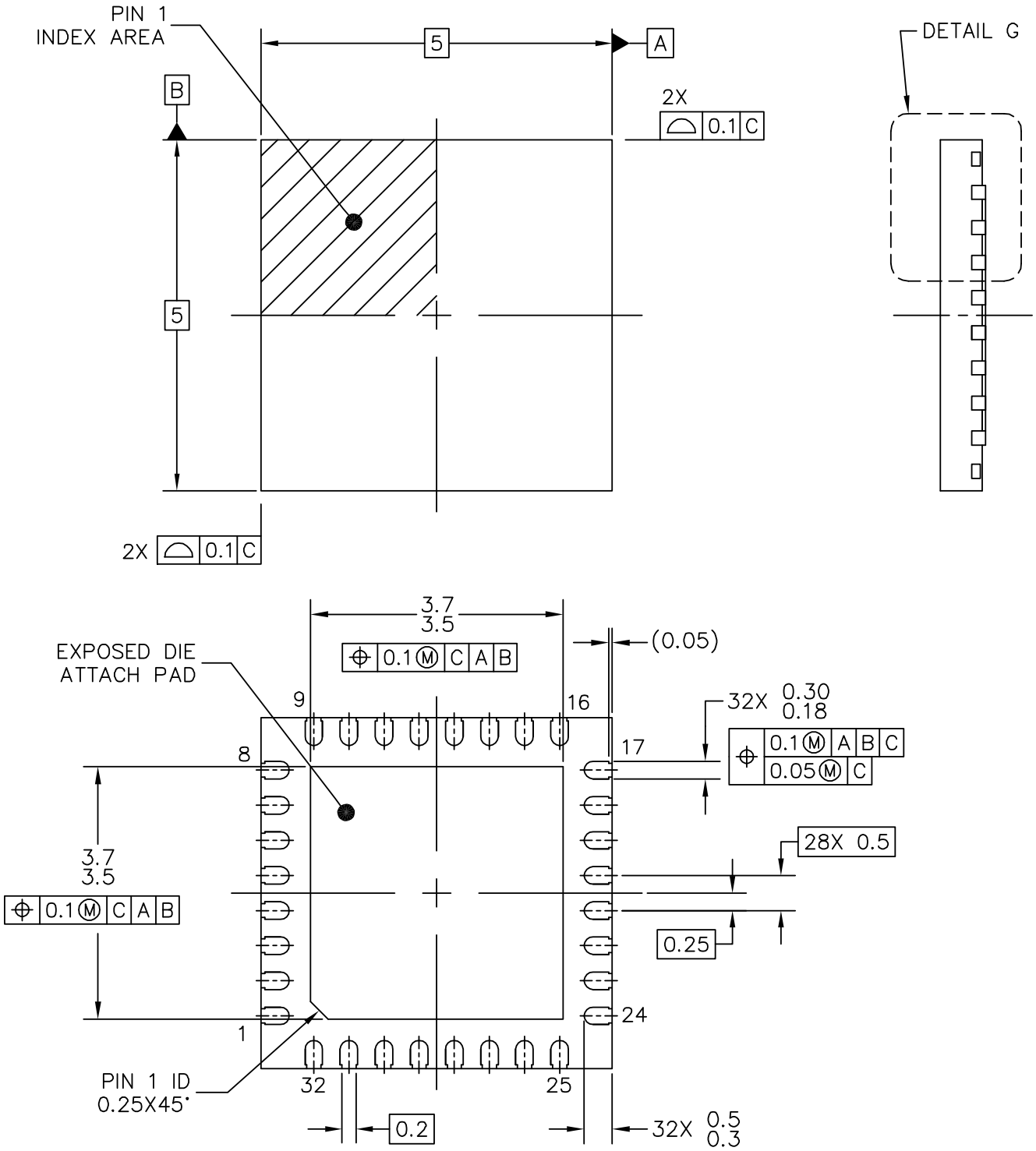
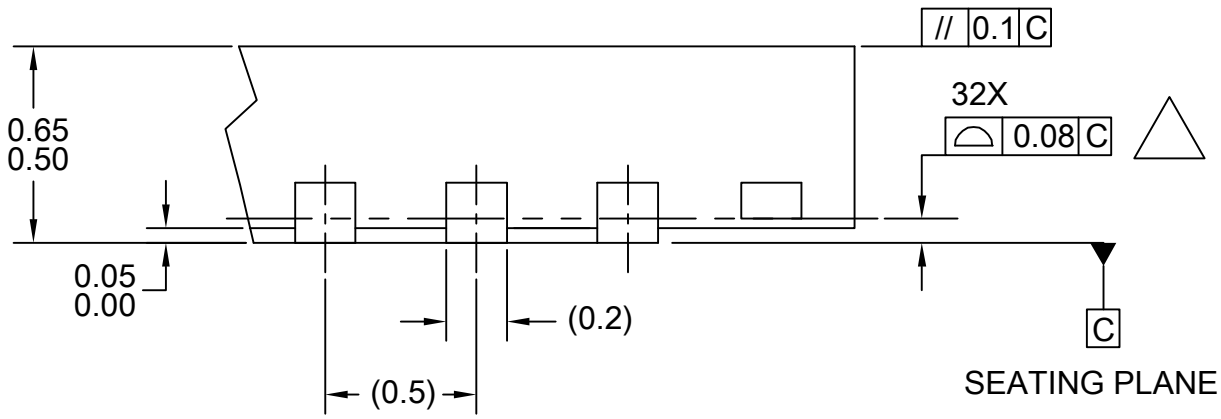


Figure 14. 32-pin QFN package dimension 1



DETAIL G
VIEW ROTATED 90°CW

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THIS IS A NON-JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

Figure 15. 32-pin QFN package dimension 2

5 Electrical characteristics

5.1 Ratings

5.1.1 Thermal handling ratings

Table 32. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.1.2 Moisture handling ratings

Table 33. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.1.3 ESD handling ratings

Table 34. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

5.1.4 Voltage and current operating ratings

Table 35. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA

Table continues on the next page...

Table 35. Voltage and current operating ratings (continued)

Symbol	Description	Min.	Max.	Unit
V_{IO}	IO pin input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB_DP}	USB_DP input voltage	–0.3	3.63	V
V_{USB_DM}	USB_DM input voltage	–0.3	3.63	V
V_{REGIN}	USB regulator input	–0.3	6.0	V

5.2 General

5.2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

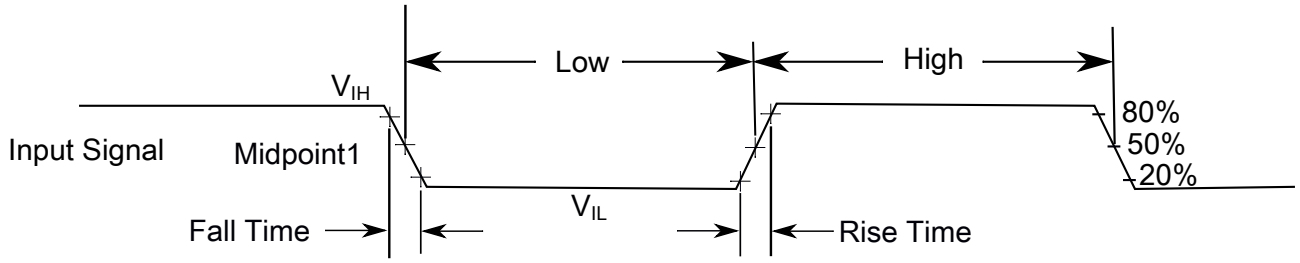


Figure 16. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L=30 pF loads
- Slew rate disabled
- Normal drive strength

5.2.2 Nonswitching electrical specifications

5.2.2.1 Voltage and current operating requirements

Table 36. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICIO}	IO pin negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-3	—	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins • Negative current injection	 -25	 —	 mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

1. All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than V_{IO_MIN} (= V_{SS}-0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|.
2. Open drain outputs must be pulled to V_{DD}.

5.2.2.2 LVD and POR operating requirements

Table 37. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV = 00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV = 01)	2.72	2.80	2.88	V	
V_{LVW3H}		2.82	2.90	2.98	V	

Table continues on the next page...

Table 37. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVW4H}	• Level 3 falling (LVWV = 10) • Level 4 falling (LVWV = 11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV = 00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV = 01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV = 10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV = 11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low-power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising thresholds are falling threshold + hysteresis voltage

5.2.2.3 Voltage and current operating behaviors

Table 38. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — normal drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –5 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –1.5 mA	V_{DD} – 0.5	—	V	
V_{OH}	Output high voltage — high drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –18 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –6 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — normal drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1.5 mA	—	0.5	V	
V_{OL}	Output low voltage — high drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 18 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 6 mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	

Table continues on the next page...

Table 38. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	2
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	µA	2
I_{IN}	Input leakage current (total all pins) for full temperature range	—	64	µA	2
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
R_{PU}	Internal pullup resistors	20	50	kΩ	3

1. PTB0, PTB1, PTC3, PTC4, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at V_{DD} = 3.6 V
3. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

5.2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- HIRC clock mode

Table 39. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	µs	1
	• VLLS0 → RUN	—	152	166	µs	
	• VLLS1 → RUN	—	152	166	µs	
	• VLLS3 → RUN	—	93	104	µs	
	• LLS → RUN	—	7.5	8	µs	
	• VLPS → RUN	—	7.5	8	µs	
	• STOP → RUN	—	7.5	8	µs	

1. Normal boot (FTFA_FOPT[LPBOOT]=11)

5.2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

NOTE

The while (1) test is executed with flash cache enabled.

Table 40. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUNCO}	Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V					2
	• at 25 °C	—	5.76	6.40	mA	
	• at 105 °C	—	6.04	6.68		
I_{DD_RUNCO}	Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V					
	• at 25 °C	—	3.21	3.85	mA	
	• at 105 °C	—	3.49	4.13		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					2
	• at 25 °C	—	6.45	7.09	mA	
	• at 105 °C	—	6.75	7.39		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V_{DD} = 3.0 V					2
	• at 25 °C	—	3.95	4.59		
	• at 105 °C	—	4.23	4.87	mA	
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, V_{DD} = 3.0 V					2
	• at 25 °C	—	2.68	3.32	mA	
	• at 105 °C	—	2.96	3.60		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					2
	• at 25 °C	—	8.08	8.72	mA	
	• at 105 °C	—	8.39	9.03		

Table continues on the next page...

Table 40. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					
	• at 25 °C	—	3.90	4.54	mA	
	• at 105 °C	—	4.21	4.85		
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, V_{DD} = 3.0 V					
	• at 25 °C	—	2.66	3.30	mA	
	• at 105 °C	—	2.94	3.58		
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, V_{DD} = 3.0 V					
	• at 25 °C	—	2.03	2.67	mA	
	• at 105 °C	—	2.31	2.95		
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					
	• at 25 °C	—	5.52	6.16	mA	
	• at 105 °C	—	5.83	6.47		
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock disable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					
	• at 25 °C	—	5.29	5.93	mA	
	• at 105 °C	—	5.56	6.20		
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock enable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					
	• at 25 °C	—	6.91	7.55	mA	
	• at 105 °C	—	7.19	7.91		
I_{DD_VLPRCO}	Very Low Power Run Core Mark in Flash in Compute Operation mode: Core@4 MHz, Flash @1 MHz, V_{DD} = 3.0 V					
	• at 25 °C	—	826	907	µA	
I_{DD_VLPRCO}	Very-low-power-run While(1) loop in SRAM in compute operation mode— 8 MHz LIRC mode, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V					
	• at 25 °C	—	405	486	µA	
I_{DD_VLPRCO}	Very-low-power run While(1) loop in SRAM in compute operation mode:—2 MHz LIRC mode, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V					
	• at 25 °C	—	154	235	µA	

Table continues on the next page...

Table 40. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	108	189	µA	
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V_{DD} = 3.0 V • at 25 °C	—	39	120	µA	
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	249	330	µA	
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock enable, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	337	418	µA	
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	416	497	µA	
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	494	575	µA	
I_{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	166	247	µA	
I_{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V_{DD} = 3.0 V • at 25 °C	—	50	131	µA	
I_{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	208	289	µA	
I_{DD_WAIT}	Wait mode current—core disabled, 48 MHz system/24 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, V_{DD} = 3.0 V	—	1.81	1.89	mA	
I_{DD_WAIT}	Wait mode current—core disabled, 24 MHz system/12 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, V_{DD} = 3.0 V	—	1.22	1.39	mA	

Table continues on the next page...

Table 40. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 4 MHz system/ 1 MHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V	—	172	182	µA	
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 2 MHz system/ 0.5 MHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V	—	69	76	µA	
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 125 kHz system/ 31.25 kHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V	—	36	40	µA	
I_{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, 12 MHz bus and flash, V_{DD} = 3.0 V	—	1.81	2.06	mA	
I_{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, flash doze enabled, 12 MHz bus, V_{DD} = 3.0 V	—	1.00	1.25	mA	
I_{DD_STOP}	Stop mode current at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	— — — —	161.93 181.45 236.29 390.33	171.82 191.96 271.17 465.58	µA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	— — — —	3.31 10.43 34.14 104.38	5.14 17.68 61.06 164.44	µA	
I_{DD_VLPS}	Very-low-power stop mode current at 1.8 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	— — — —	3.21 10.26 33.49 102.92	5.22 17.62 60.19 162.20	µA	
I_{DD_LLS}	Low-leakage stop mode current, all peripheral disable, at 3.0 V • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C	— — — — —	2.06 4.72 8.13 13.34 41.08	3.33 6.85 13.30 24.70 52.43	µA	
I_{DD_LLS}	Low-leakage stop mode current with RTC current, at 3.0 V	—	2.46	3.73	µA	

Table continues on the next page...

Table 40. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 25 °C and below	—	5.12	7.25		
	• at 50 °C	—	8.53	11.78		
	• at 70 °C	—	13.74	18.91		
	• at 85 °C	—	41.48	52.83		
	• at 105 °C					
I_{DD_LLS}	Low-leakage stop mode current with RTC current, at 1.8 V				μA	3
	• at 25 °C and below	—	2.35	2.70		
	• at 50 °C	—	4.91	6.75		
	• at 70 °C	—	8.32	11.78		
	• at 85 °C	—	13.44	18.21		
	• at 105 °C	—	40.47	51.85		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V				μA	
	• at 25 °C and below	—	1.45	1.85		
	• at 50 °C	—	3.37	4.39		
	• at 70 °C	—	5.76	8.48		
	• at 85 °C	—	9.72	14.30		
	• at 105 °C	—	30.41	37.50		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V				μA	3
	• at 25 °C and below	—	2.05	2.45		
	• at 50 °C	—	3.97	4.99		
	• at 70 °C	—	6.36	9.08		
	• at 85 °C	—	10.32	14.73		
	• at 105 °C	—	31.01	38.10		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V				μA	3
	• at 25 °C and below	—	1.96	2.36		
	• at 50 °C	—	3.86	5.67		
	• at 70 °C	—	6.23	8.53		
	• at 85 °C	—	10.21	13.37		
	• at 105 °C	—	30.25	37.02		
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V					
	• at 25 °C and below	—	0.66	0.80		
	• at 50°C	—	1.78	3.87		
	• at 70°C	—	2.55	4.26	μA	

Table continues on the next page...

Table 40. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 85°C	—	4.83	6.64		
	• at 105 °C	—	16.42	20.49		
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 3.0 V					3
	• at 25 °C and below	—	1.26	1.40		
	• at 50°C	—	2.38	4.47		
	• at 70°C	—	3.15	4.86	µA	
	• at 85°C	—	5.43	7.24		
	• at 105 °C	—	17.02	21.09		
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 1.8 V					3
	• at 25 °C and below	—	1.16	1.30		
	• at 50°C	—	1.96	2.28		
	• at 70°C	—	2.78	3.37	µA	
	• at 85°C	—	4.85	6.88		
	• at 105 °C	—	15.78	18.81		
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V					
	• at 25 °C and below	—	0.35	0.47	µA	
	• at 50 °C	—	1.25	1.44		
	• at 70 °C	—	2.53	3.24		
	• at 85 °C	—	4.40	5.24		
	• at 105 °C	—	16.09	19.29		
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 1) at 3 V					
	• at 25 °C and below	—	0.18	0.28		
	• at 50 °C	—	1.09	1.31	µA	
	• at 70 °C	—	2.25	2.94		
	• at 85 °C	—	4.25	5.10		
	• at 105 °C	—	15.95	19.10		

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG_Lite configured for HIRC mode. CoreMark benchmark compiled using IAR 7.10 with optimization level high, optimized for balanced.
3. RTC uses external 32 kHz crystal as clock source, and the current includes ERCLK32K power consumption.

Table 41. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IRC8MHz}$	8 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 8 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	93	93	93	93	93	93	µA
$I_{IRC2MHz}$	2 MHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 2 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	29	29	29	29	29	29	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	224	230	238	245	253	µA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							
	• VLLS1	440	490	540	560	570	580	
	• VLLS3	440	490	540	560	570	580	
	• LLS	490	490	540	560	570	680	
	• VLPS	510	560	560	560	610	680	nA
	• STOP	510	560	560	560	610	680	
I_{LPTMR}	LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO.	30	30	30	85	100	200	nA
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	µA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							
	• IRC8M (8 MHz internal reference clock)	114	114	114	114	114	114	µA
	• IRC2M (2 MHz internal reference clock)	34	34	34	34	34	34	

Table continues on the next page...

Table 41. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I_{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. • IRC8M (8 MHz internal reference clock) • IRC2M (2 MHz internal reference clock)	147 42	147 42	147 42	147 42	147 42	147 42	µA
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	330	330	330	330	330	330	µA
I_{LCD}	LCD peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the OSC0_CR[EREFSTEN, EREFSTEN] bits. VIREG disabled, resistor bias network enabled, 1/8 duty cycle, 8 x 36 configuration for driving 288 Segments, 32 Hz frame rate, no LCD glass connected. Includes ERCLK32K (32 kHz external crystal) power consumption.	4.5	4.5	4.5	4.5	4.5	4.5	µA

5.2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG-Lite in HIRC for run mode, and LIRC for VLPR mode
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

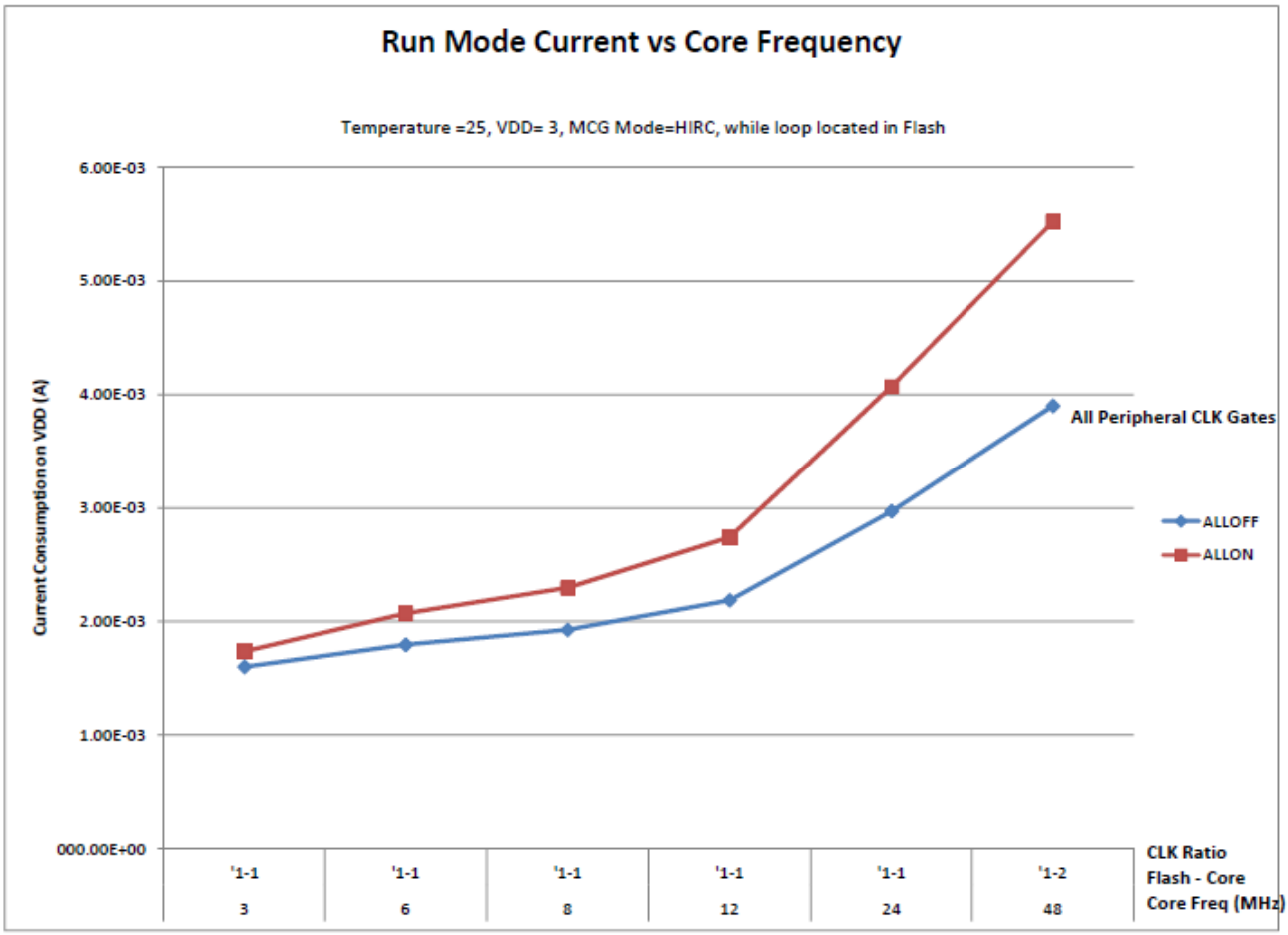
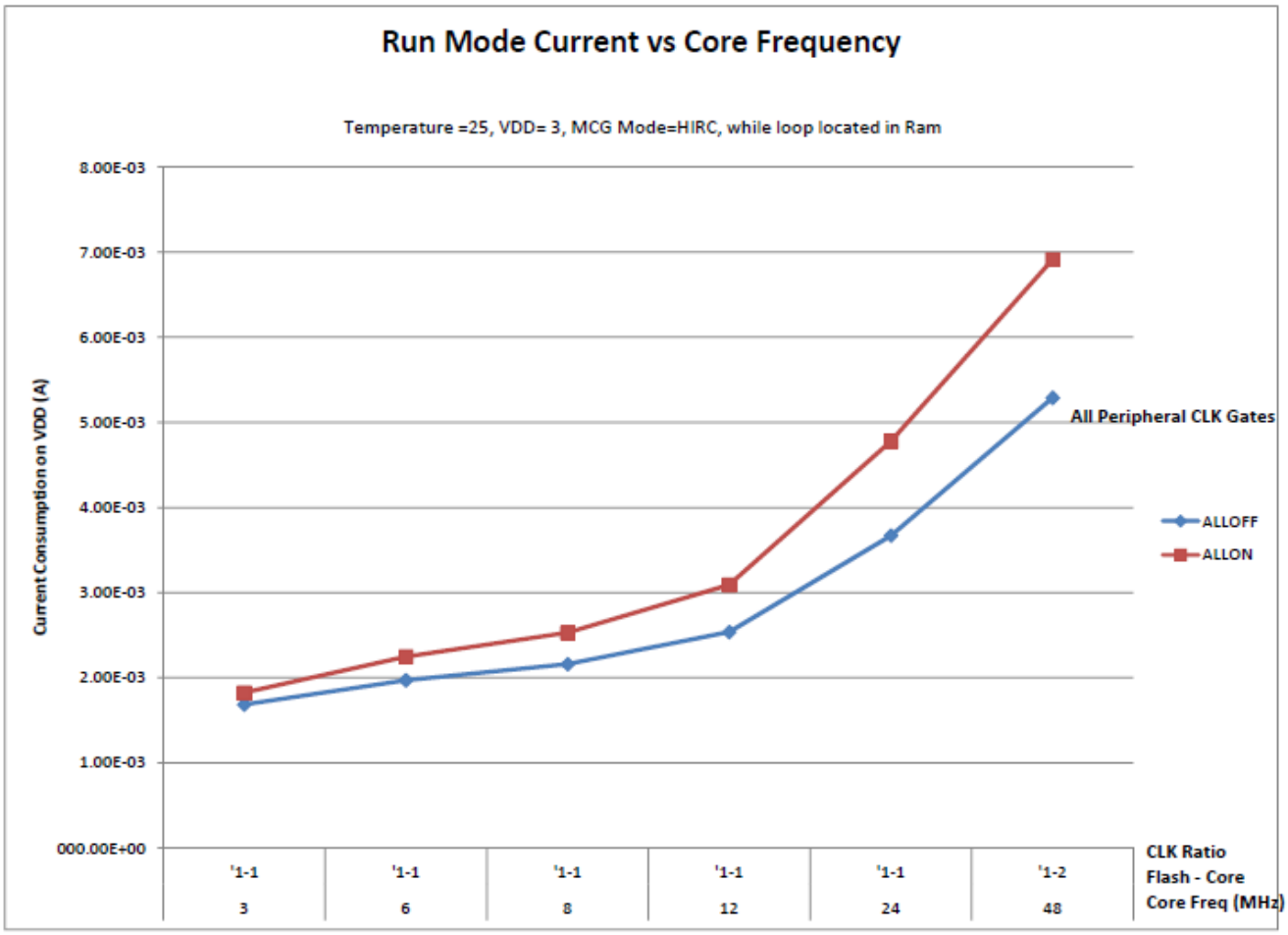


Figure 17. Run mode supply current vs. core frequency


Run Mode Current vs Core Frequency
Temperature =25, VDD= 3, MCG Mode=HIRC, while loop located in Ram
Current Consumption on VDD (A)
8.00E-03
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
000.00E+00
All Peripheral CLK Gates
ALLOFF
ALLON
'1-1
3
'1-1
6
'1-1
8
'1-1
12
'1-1
24
'1-2
48
CLK Ratio
Flash - Core
Core Freq (MHz)

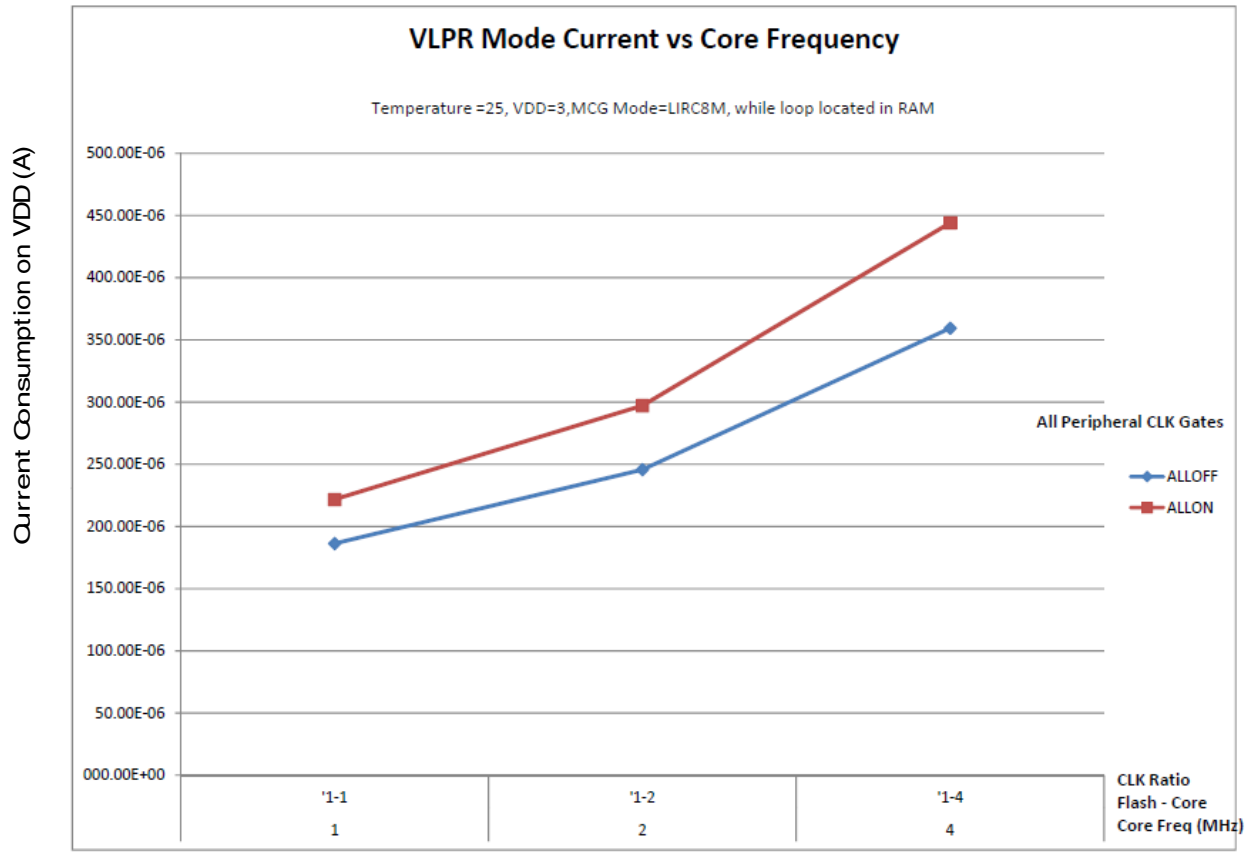


Figure 18. VLPR mode current vs. core frequency

5.2.2.6 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance. The system designer can consult the following NXP applications notes, available on nxp.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers

- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

5.2.2.7 Capacitance attributes

Table 42. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN}	Input capacitance	—	7	pF

5.2.3 Switching specifications

5.2.3.1 Device clock specifications

Table 43. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
f_{SYS}	System and core clock[1]	—	48	MHz
f_{BUS}	Bus clock[1]	—	24	MHz
f_{FLASH}	Flash clock[1]	—	24	MHz
f_{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz
f_{LPTMR}	LPTMR clock	—	24	MHz
VLPR and VLPS modes[2]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	1	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{LPTMR}	LPTMR clock[3]	—	24	MHz
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	—	16	MHz
f_{TPM}	TPM asynchronous clock	—	8	MHz
$f_{LPUART0/1}$	LPUART0/1 asynchronous clock	—	8	MHz

1. The maximum value of system clock, core clock, bus clock, and flash clock under normal run mode can be 3% higher than the specified maximum frequency when IRC 48 MHz is used as the clock source.
2. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
3. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

5.2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 44. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise and fall time	—	36	ns	3

1. The synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

5.2.4 Thermal specifications

5.2.4.1 Thermal operating requirements

Table 45. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.

5.2.4.2 Thermal attributes

Table 46. Thermal attributes

Board type	Symbol	Description	48 QFN	32 QFN	64 LQFP	64 MAPBGA	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	86	101	70	50.3	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	29	33	51	42.9	°C/W	

Table continues on the next page...

Table 46. Thermal attributes (continued)

Board type	Symbol	Description	48 QFN	32 QFN	64 LQFP	64 MAPBGA	Unit	Notes
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	71	84	58	41.4	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	24	28	45	38.0	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	12	13	33	39.6	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	1.7	1.7	20	27.3	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	3	4	0.4	°C/W	4
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom (natural convection)	-	-	-	12.6	°C/W	5

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.
5. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

5.3 Peripheral operating requirements and behaviors

5.3.1 Core modules

5.3.1.1 SWD electricals

Table 47. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

Table continues on the next page...

Table 47. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J1	SWD_CLK frequency of operation • Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

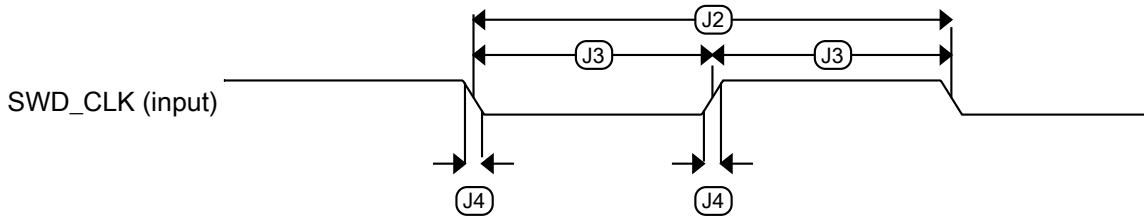


Figure 19. Serial wire clock input timing

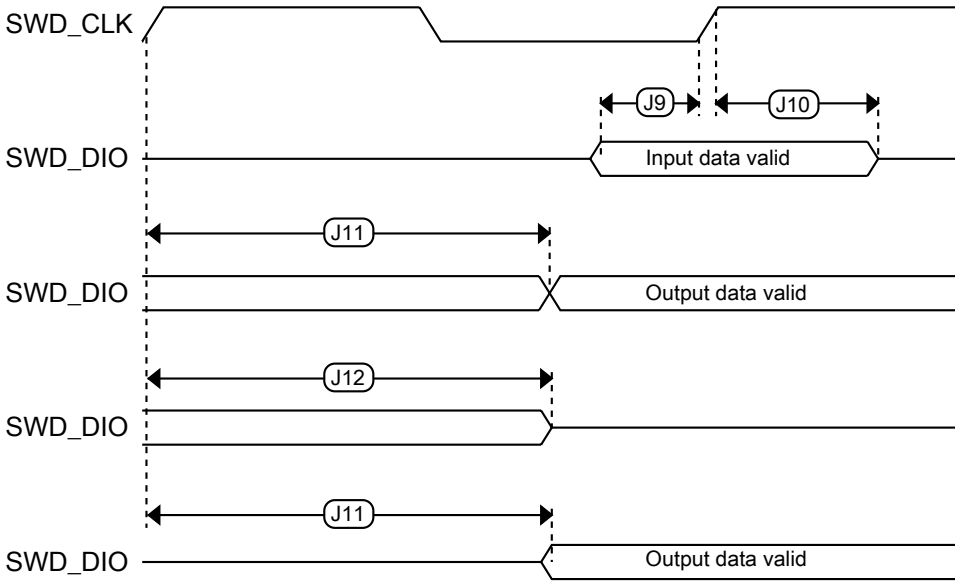


Figure 20. Serial wire data timing

5.3.2 System modules

There are no specifications necessary for the device's system modules.

5.3.3 Clock modules

5.3.3.1 MCG-Lite specifications

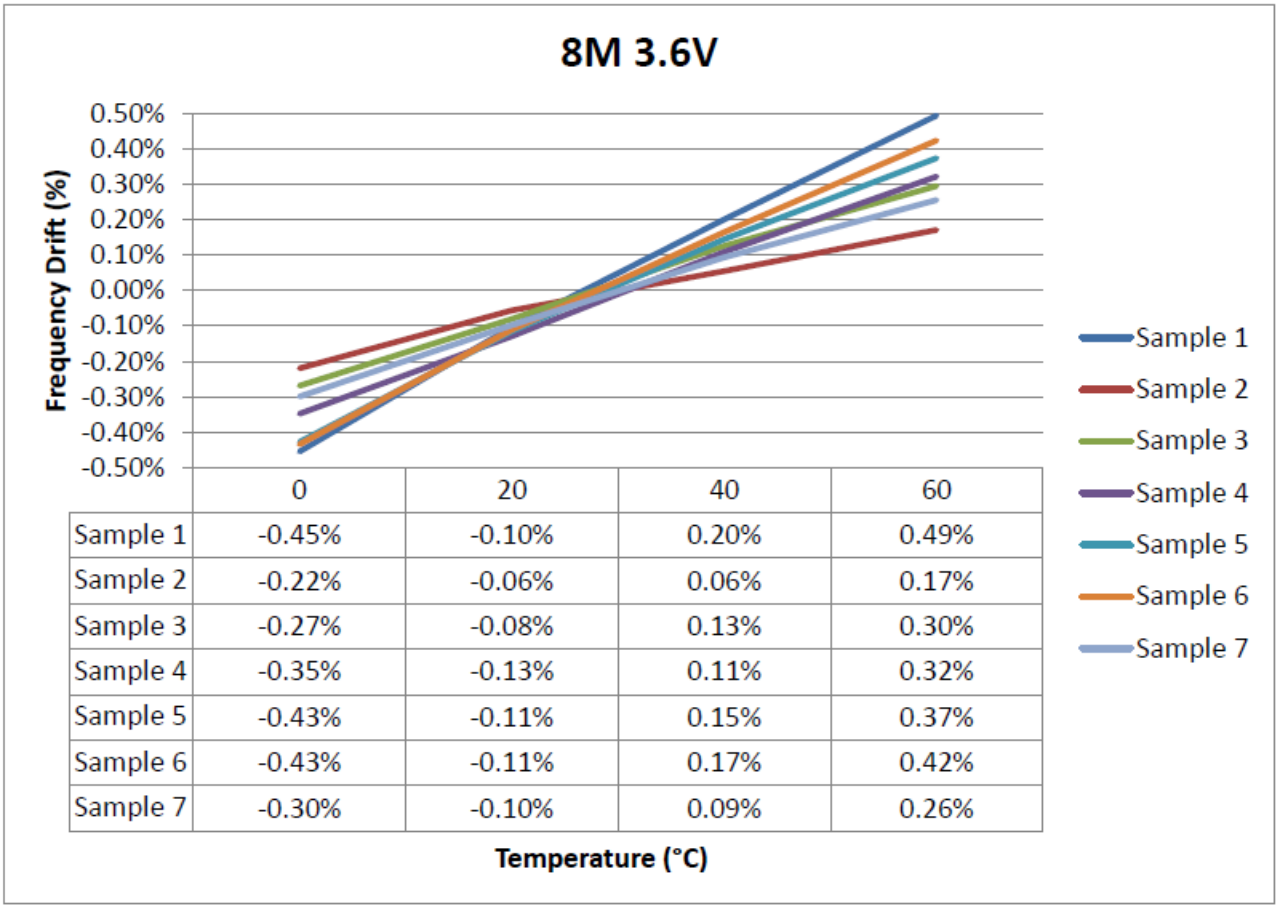
Table 48. IRC48M specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD}	Supply current	—	400	500	µA	—
f_{IRC}	Output frequency	—	48	—	MHz	—
$\Delta f_{irc48m\_ol\_lv}$	Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over temperature	—	± 0.5	± 1.5	$\%f_{irc48m}$	1
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over temperature	—	± 0.5	± 1.0	$\%f_{irc48m}$	1
T_j	Period jitter (RMS)	—	35	150	ps	—
T_{su}	Startup time	—	2	3	µs	—

1. The maximum value represents characterized results equivalent to mean plus or minus three times the standard deviation (mean +/-3sigma).

Table 49. IRC8M/2M specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_2M}	Supply current in 2 MHz mode	—	14	17	µA	—
I_{DD_8M}	Supply current in 8 MHz mode	—	30	35	µA	—
f_{IRC_2M}	Output frequency	—	2	—	MHz	—
f_{IRC_8M}	Output frequency	—	8	—	MHz	—
$f_{IRC\_T\_2M}$	Output frequency range (trimmed)	—	—	±3	$\%f_{IRC}$	—
$f_{IRC\_T\_8M}$	Output frequency range (trimmed)	—	—	±3	$\%f_{IRC}$	—
T_{su_2M}	Startup time	—	—	12.5	µs	—
T_{su_8M}	Startup time	—	—	12.5	µs	—



	0	20	40	60
Sample 1	-0.45%	-0.10%	0.20%	0.49%
Sample 2	-0.22%	-0.06%	0.06%	0.17%
Sample 3	-0.27%	-0.08%	0.13%	0.30%
Sample 4	-0.35%	-0.13%	0.11%	0.32%
Sample 5	-0.43%	-0.11%	0.15%	0.37%
Sample 6	-0.43%	-0.11%	0.17%	0.42%
Sample 7	-0.30%	-0.10%	0.09%	0.26%

Figure 21. IRC8M Frequency Drift vs Temperature curve

5.3.3.2 Oscillator electrical specifications

5.3.3.2.1 Oscillator DC electrical specifications

Table 50. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz (RANGE=01)	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	

Table continues on the next page...

Table 50. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	µA	
	• 4 MHz	—	400	—	µA	
	• 8 MHz (RANGE=01)	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, R_F is integrated and must not be attached externally.

5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

5.3.3.2.2 Oscillator frequency specifications

Table 51. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

5.3.4 Memories and memory interfaces

5.3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

5.3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 52. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk128k}$	Erase Block high-voltage time for 128 KB	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

5.3.4.1.2 Flash timing specifications — commands

Table 53. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk128k}$	Read 1s Block execution time • 128 KB program flash	—	—	1.7	ms	1
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
$t_{ersblk128k}$	Erase Flash Block execution time • 128 KB program flash	—	88	600	ms	2
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	1
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	175	1300	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	175	1300	ms	2

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

5.3.4.1.3 Flash high voltage current behaviors

Table 54. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

5.3.4.1.4 Reliability specifications

Table 55. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 125 °C.

5.3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

5.3.6 Analog

5.3.6.1 ADC electrical specifications

Using differential inputs can achieve better system accuracy than using single-end inputs.

5.3.6.1.1 16-bit ADC operating conditions

Table 56. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	—
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	3
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	3
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 × VREFH VREFH	V	—

Table continues on the next page...

Table 56. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	—
R_{ADIN}	Input series resistance		—	2	5	kΩ	—
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	4
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	24	MHz	5
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	5
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	1200	ksps	6
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	ksps	6

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. VREFH can act as VREF_OUT when VREFV1 module is enabled.
4. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
5. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
6. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

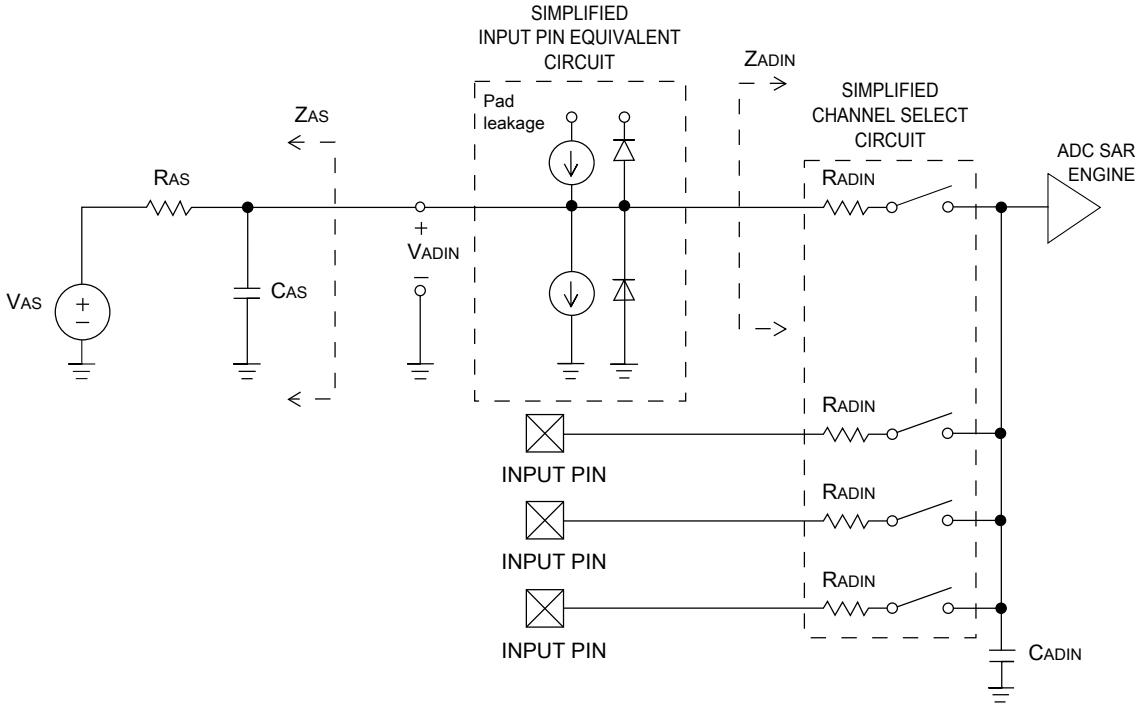


Figure 22. ADC input impedance equivalency diagram

5.3.6.1.2 16-bit ADC electrical characteristics

Table 57. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	t_{ADACK} = 1/ f_{ADACK}
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes	—	±4	±6.8	LSB[4]	5
		• <12-bit modes	—	±1.4	±2.1		
DNL	Differential non-linearity	• 12-bit modes	—	±0.7	–1.1 to +1.9	LSB[4]	5
		• <12-bit modes	—	±0.2	–0.3 to 0.5		
INL	Integral non-linearity	• 12-bit modes	—	±1.0	–2.7 to +1.9	LSB[4]	5
		• <12-bit modes	—	±0.5			

Table continues on the next page...

Table 57. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
					–0.7 to +0.5		
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	V_{ADIN} = V_{DDA}[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 — —	 -94 -85	 — —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 82 78	 95 90	 — —	dB dB	7
E_{IL}	Input leakage error		I_{In} × R_{AS}			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

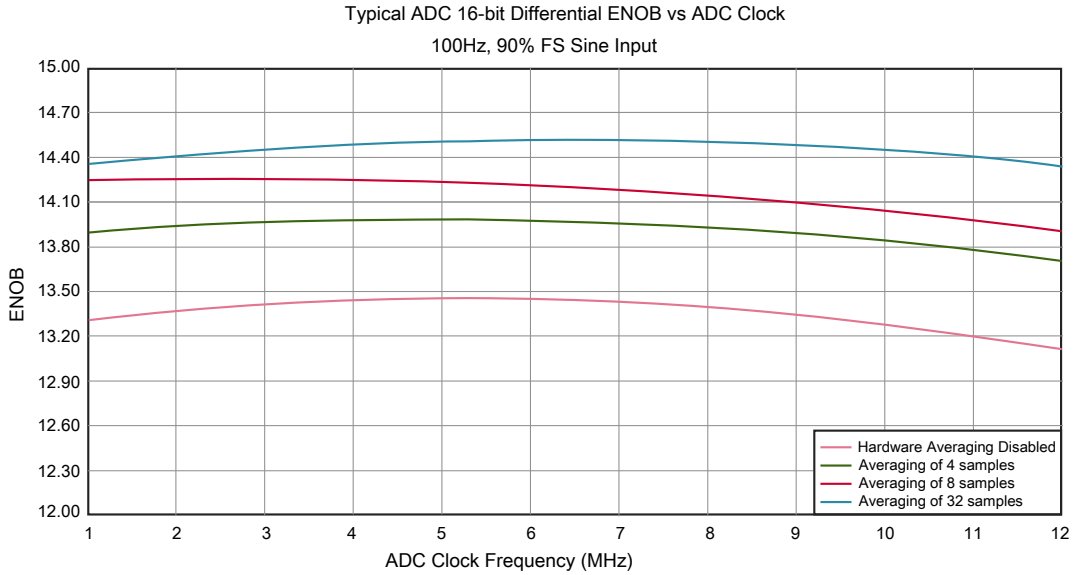


Figure 23. Typical ENOB vs. ADC_CLK for 16-bit differential mode

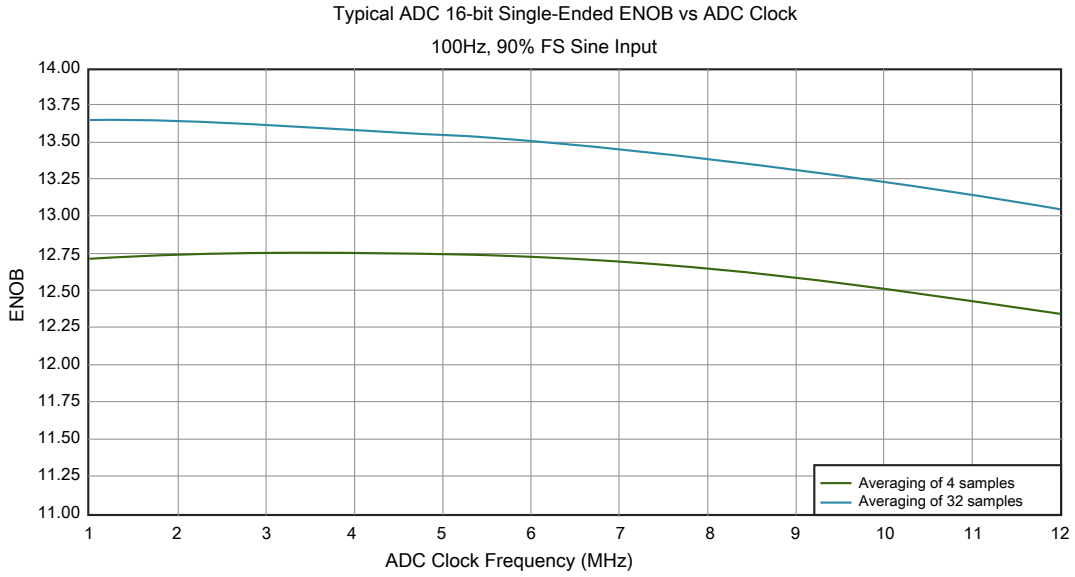


Figure 24. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

5.3.6.2 Voltage reference electrical specifications

Table 58. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage		3.6	V	
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 59 is tested under the condition of setting VREF_TRM[CHOPEN], VREF_SC[REGEN] and VREF_SC[ICOMPEN] bits to 1.

Table 59. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	1
V_{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	1
V_{out}	Voltage reference output — user trim	1.193	—	1.197	V	1
V_{step}	Voltage reference trim step	—	0.5	—	mV	1
V_{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range: 0 to 70°C)	—	—	50	mV	1
I_{bg}	Bandgap only current	—	—	80	µA	1
I_{lp}	Low-power buffer current	—	—	360	uA	1
I_{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	—	200	—	µV	1, 2
T_{stup}	Buffer startup time	—	—	100	µs	
$T_{chop\_osc\_stup}$	Internal bandgap start-up delay with chop oscillator enabled	—	—	35	ms	—
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 60. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	°C	

Table 61. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	

5.3.6.3 CMP and 6-bit DAC electrical specifications

Table 62. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

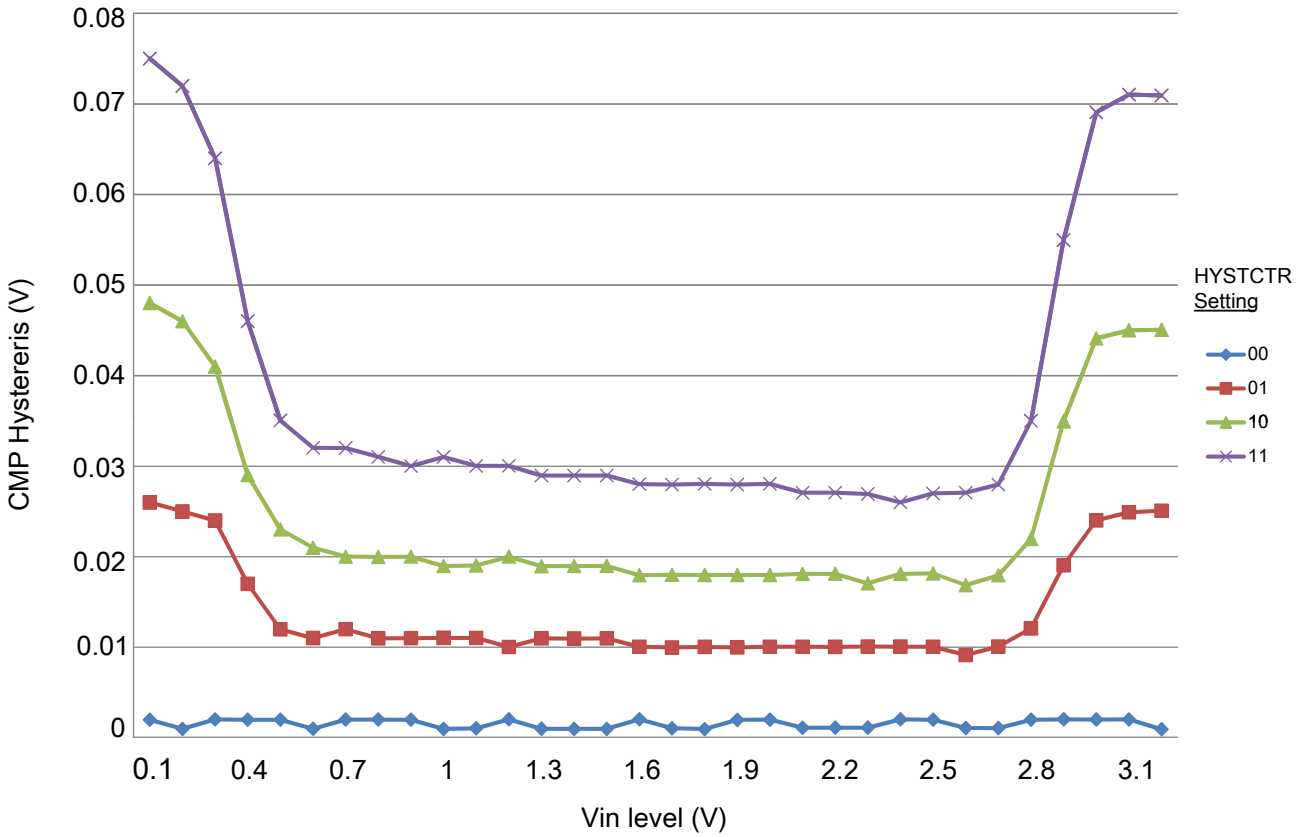


Figure 25. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

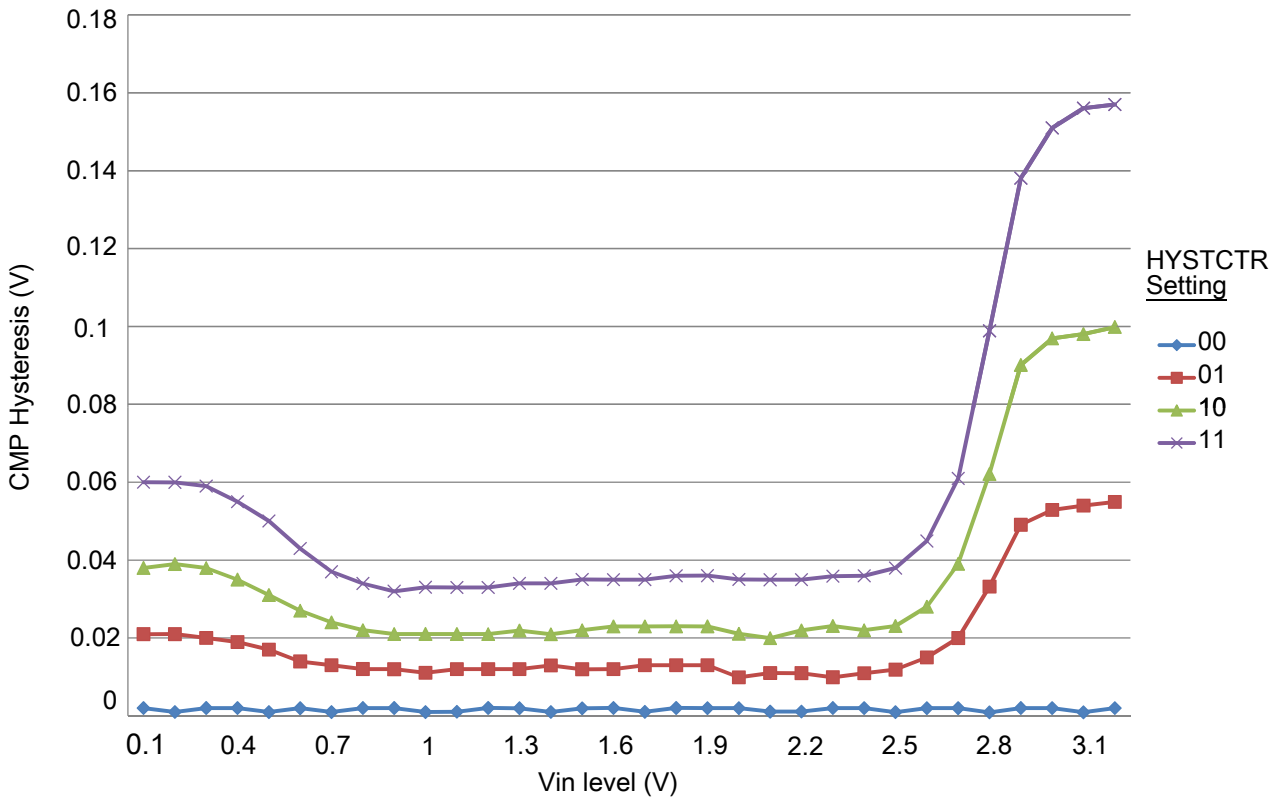


Figure 26. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

5.3.6.4 12-bit DAC electrical characteristics

5.3.6.4.1 12-bit DAC operating requirements

Table 63. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage		3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REF_OUT}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

5.3.6.4.2 12-bit DAC operating behaviors

Table 64. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	250	µA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	900	µA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	µs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	µs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	µV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/µs	
	• High power (SP_{HP})	1.2	1.7	—		
	• Low power (SP_{LP})	0.05	0.12	—		
BW	3dB bandwidth				kHz	
	• High power (SP_{HP})	550	—	—		
	• Low power (SP_{LP})	40	—	—		

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} −100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV
4. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV with V_{DDA} > 2.4 V
5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} − 100 mV
6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

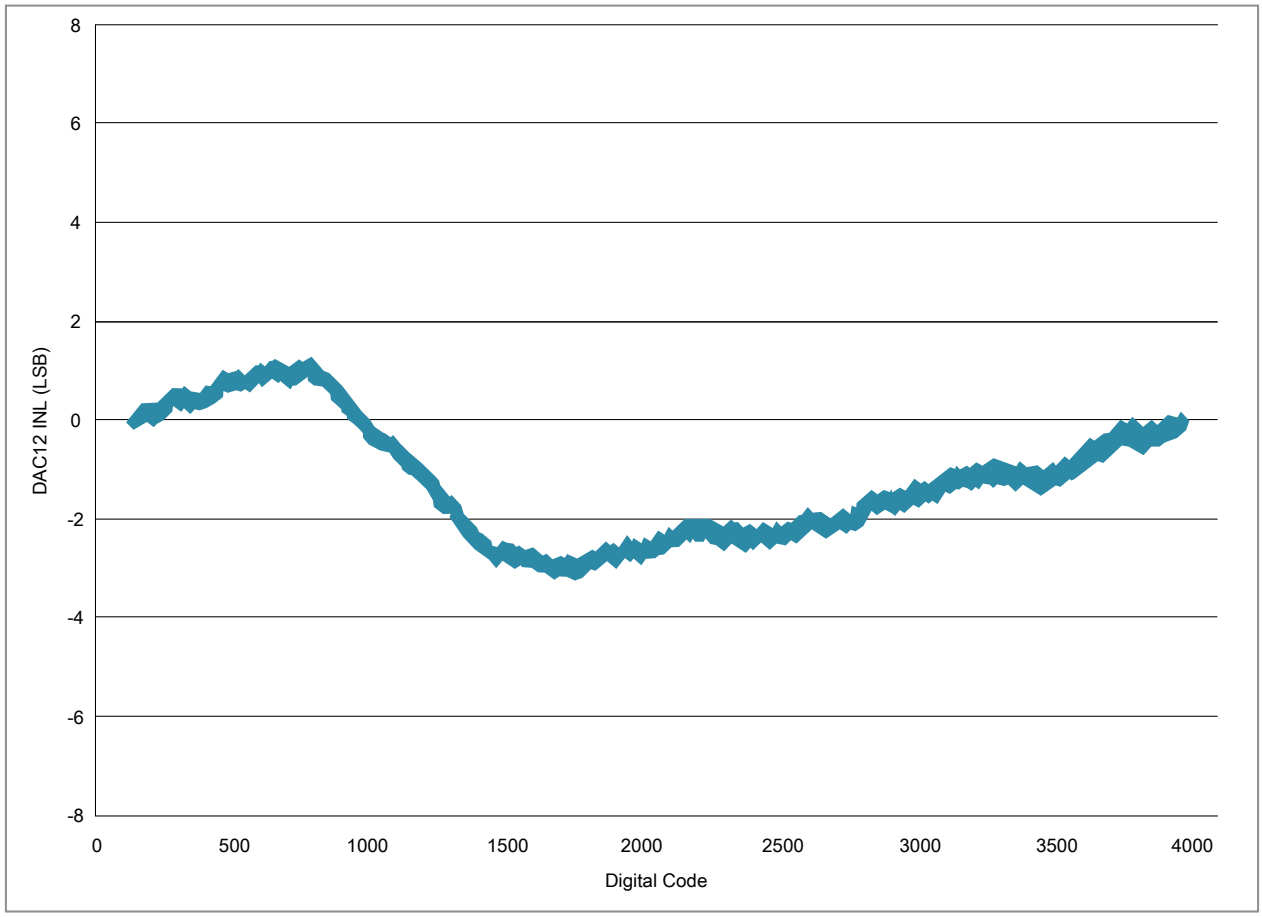


Figure 27. Typical INL error vs. digital code

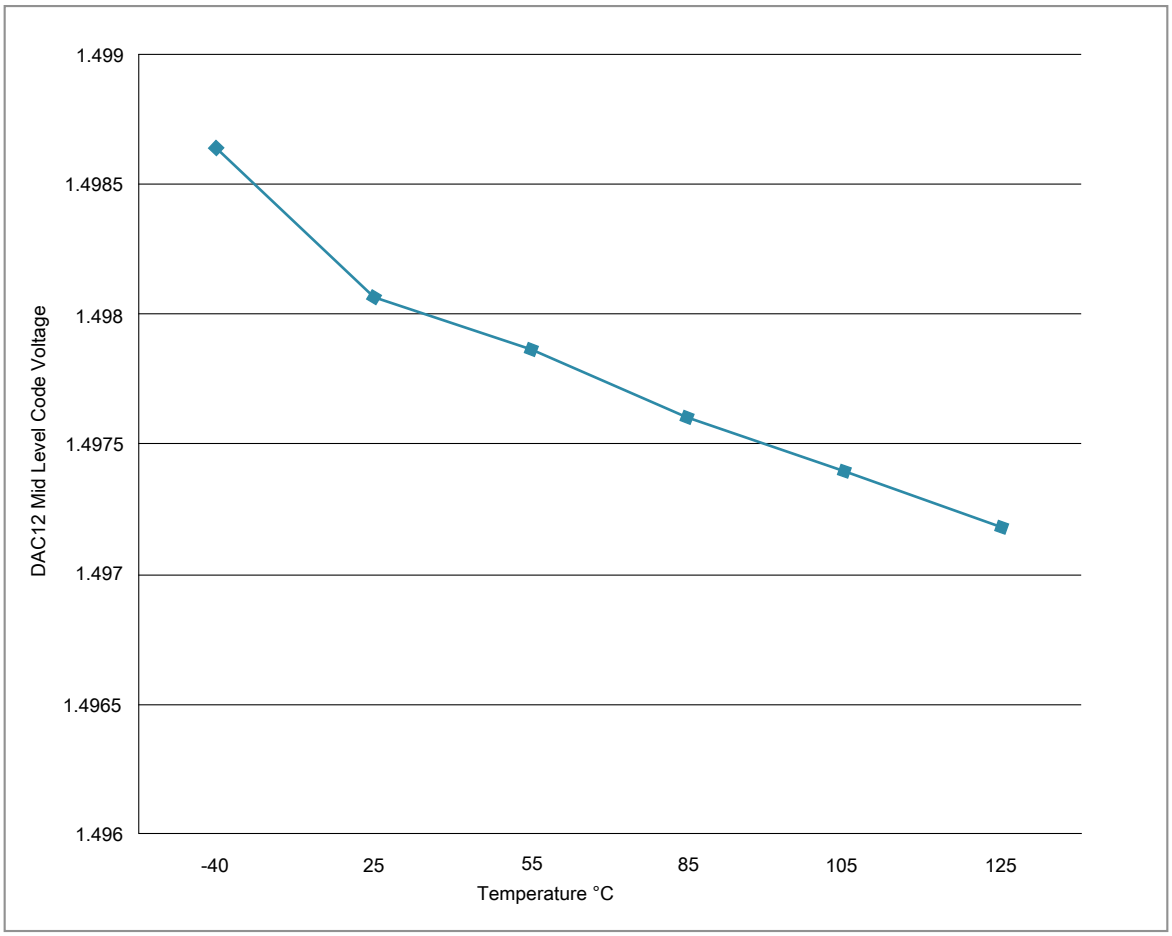


Figure 28. Offset at half scale vs. temperature

5.4 Timers

See General switching specifications.

5.5 Communication interfaces

5.5.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit usb.org .

NOTE

The IRC48M do not meet the USB jitter specifications for certification for Host mode operation.

This device cannot support Host mode operation.

5.5.2 USB VREG electrical specifications

Table 65. USB VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	125	186	µA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	µA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25 °C • Across operating voltage and temperature	— —	650 —	— 4	nA µA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) > 3.6 V • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

5.5.3 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

Table 66. SPI master mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$

Table 67. SPI master mode timing on slew rate enabled pads

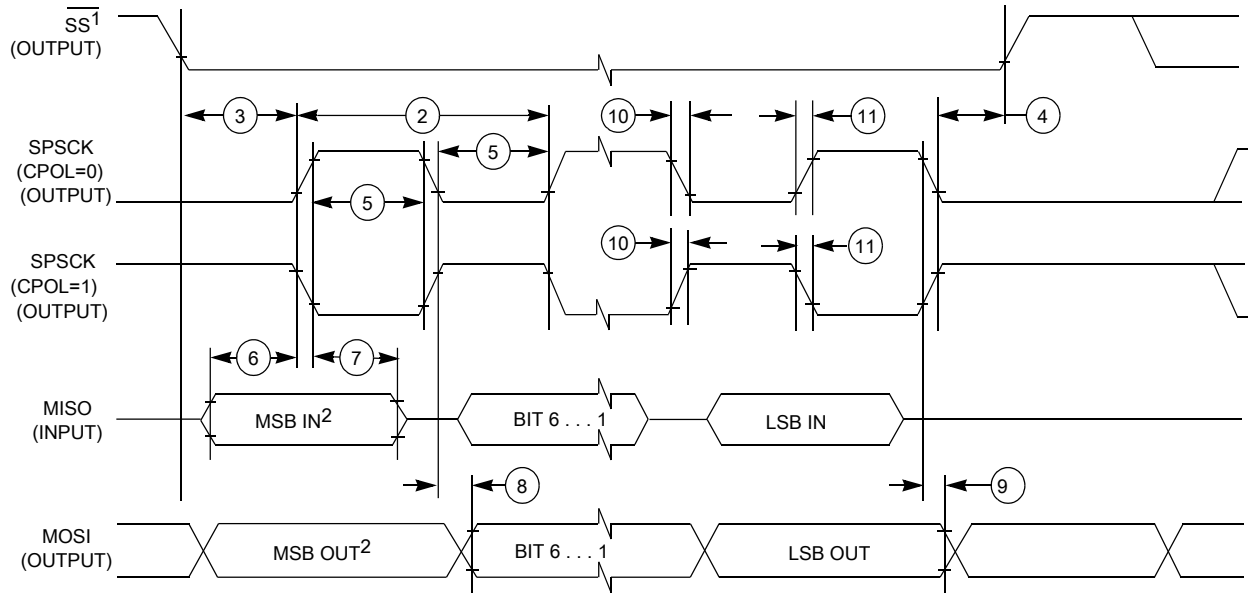
Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—

Table continues on the next page...

Table 67. SPI master mode timing on slew rate enabled pads (continued)

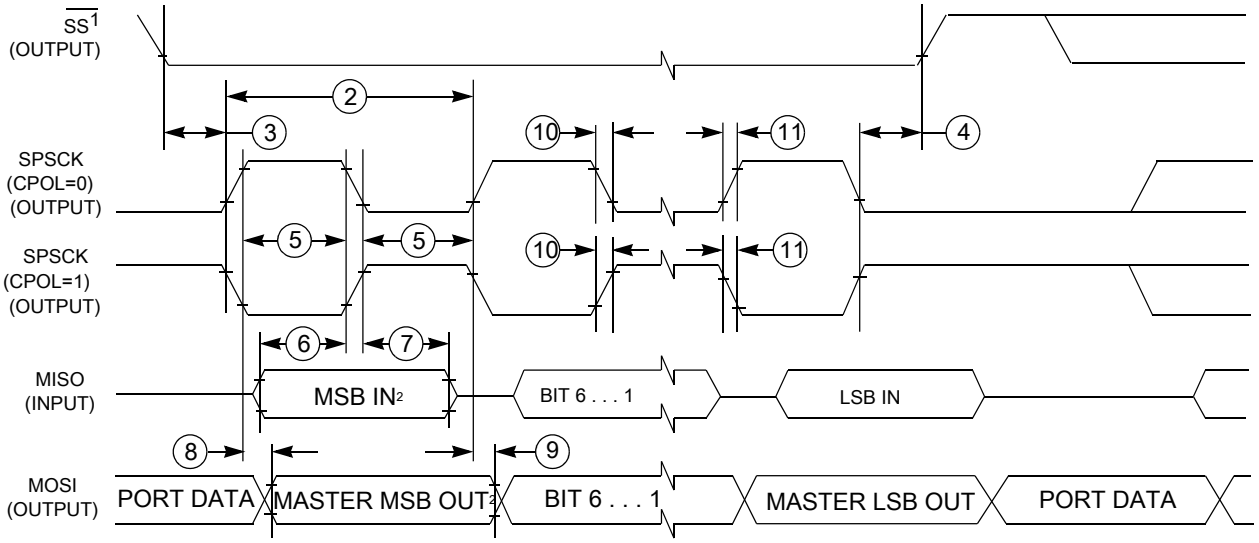
Num.	Symbol	Description	Min.	Max.	Unit	Note
8	t_v	Data valid (after SPSCK edge)	—	52	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 29. SPI master mode timing (CPHA = 0)



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 30. SPI master mode timing (CPHA = 1)

Table 68. SPI slave mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.5	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	31	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

Table 69. SPI slave mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	122	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

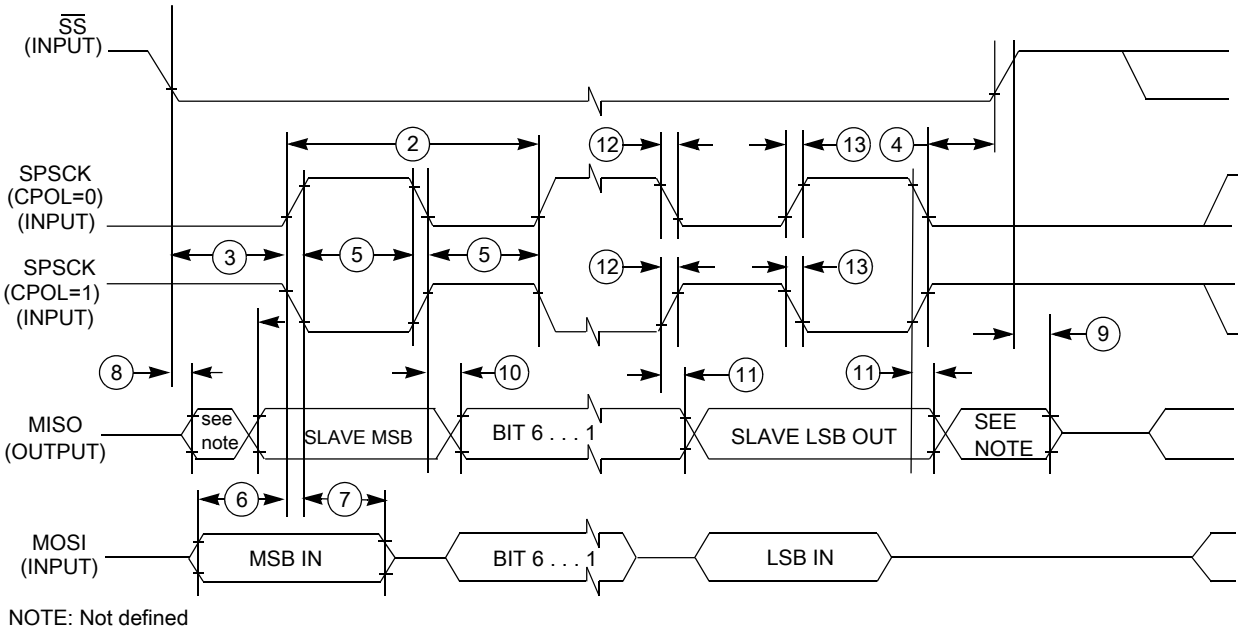
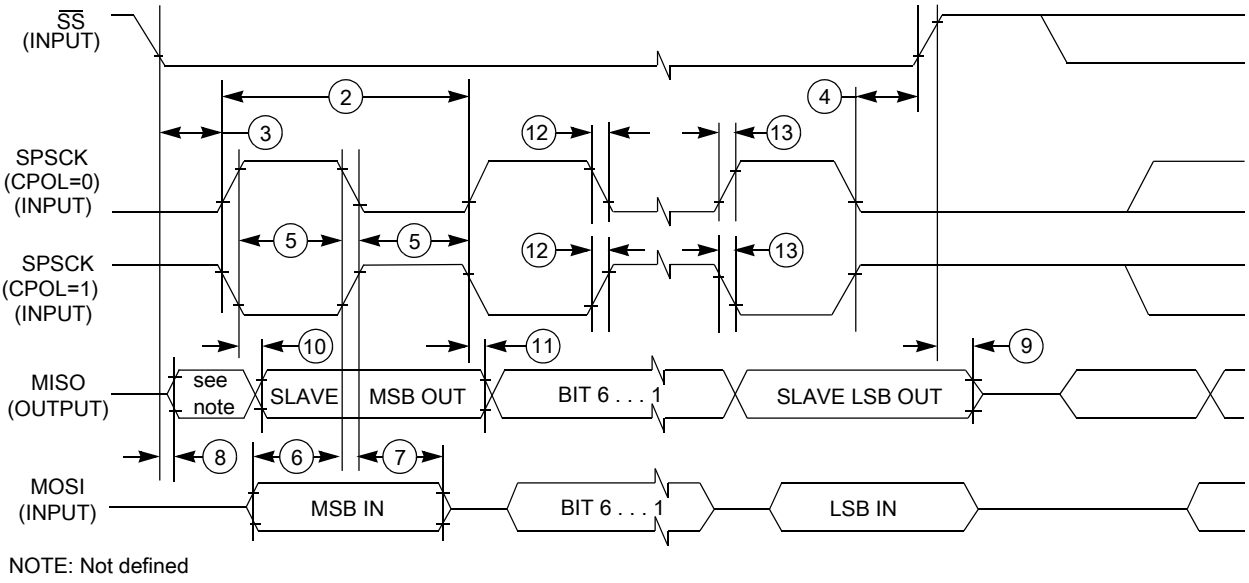


Figure 31. SPI slave mode timing (CPHA = 0)



NOTE: Not defined

Figure 32. SPI slave mode timing (CPHA = 1)

5.5.4 I²C

5.5.4.1 Inter-Integrated Circuit Interface (I2C) timing

Table 70. I2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400[1]	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.25	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I²C bus devices	t_{HD}; DAT	0[2]	3.45[3]	0[4]	0.9[2]	µs
Data set-up time	t_{SU}; DAT	250[5]	—	100[3, 6]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[7]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[6]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can be achieved only when using the high drive pins across the full voltage range and when using the normal drive pins and VDD ≥ 2.7 V.
2. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I^2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
7. C_b = total capacitance of the one bus line in pF.

Table 71. I^2C 1Mbit/s timing

Characteristic	Symbol	Minimum	Maximum	Unit
SCL Clock Frequency	f_{SCL}	0	1[1]	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	0.26	—	µs
LOW period of the SCL clock	t_{LOW}	0.5	—	µs
HIGH period of the SCL clock	t_{HIGH}	0.26	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	0.26	—	µs
Data hold time for I^2C bus devices	t_{HD}; DAT	0	—	µs
Data set-up time	t_{SU}; DAT	50	—	ns
Rise time of SDA and SCL signals	t_r	20 +0.1C_b	120	ns
Fall time of SDA and SCL signals	t_f	20 +0.1C_b[2]	120	ns
Set-up time for STOP condition	t_{SU}; STO	0.26	—	µs
Bus free time between STOP and START condition	t_{BUF}	0.5	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	0	50	ns

1. The maximum SCL clock frequency of 1 Mbit/s can support maximum bus loading when using the high drive pins across the full voltage range.
2. C_b = total capacitance of the one bus line in pF.

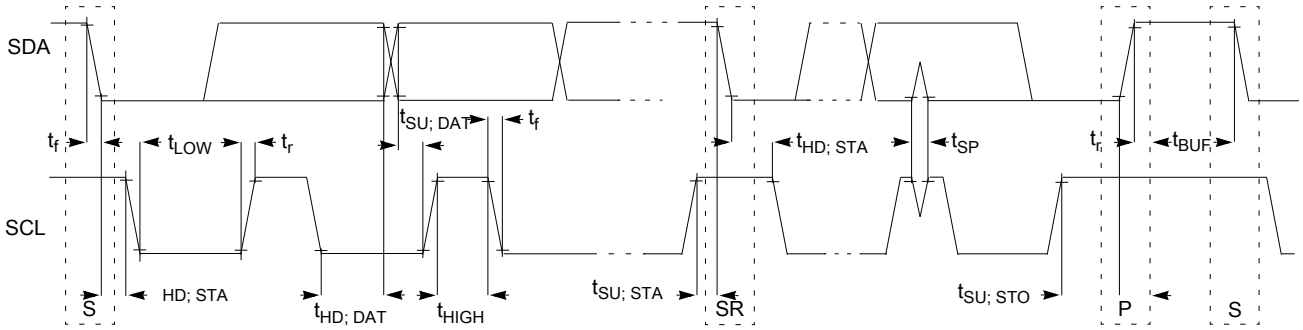


Figure 33. Timing definition for devices on the I^2C bus

5.5.5 UART

See General switching specifications.

5.6 Human-machine interfaces (HMI)

5.6.1 LCD electrical characteristics

Table 72. LCD electricals

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{Frame}	LCD frame frequency					
	• GCR[FFR]=0	23.3	—	73.1	Hz	
	• GCR[FFR]=1	46.6	—	146.2	Hz	
C_{LCD}	LCD charge pump capacitance — nominal value	—	100	—	nF	
C_{BYLCD}	LCD bypass capacitance — nominal value	—	100	—	nF	1
C_{Glass}	LCD glass capacitance	—	2000	8000	pF	2
V_{IREG}	V_{IREG}				V	3
	• RVTRIM=0000	—	0.91	—		
	• RVTRIM=1000	—	0.92	—		
	• RVTRIM=0100	—	0.93	—		
	• RVTRIM=1100	—	0.94	—		
	• RVTRIM=0010	—	0.96	—		
	• RVTRIM=1010	—	0.97	—		
	• RVTRIM=0110	—	0.98	—		
	• RVTRIM=1110	—	0.99	—		
	• RVTRIM=0001	—	1.01	—		
	• RVTRIM=1001	—	1.02	—		
	• RVTRIM=0101	—	1.03	—		
	• RVTRIM=1101	—	1.05	—		
	• RVTRIM=0011	—	1.06	—		
	• RVTRIM=1011	—	1.07	—		
	• RVTRIM=0111	—	1.08	—		
	• RVTRIM=1111	—	1.09	—		
Δ_{RTRIM}	V_{IREG} TRIM resolution	—	—	3.0	% V_{IREG}	
I_{VIREG}	V_{IREG} current adder — RVEN = 1	—	1	—	µA	

Table continues on the next page...

Table 72. LCD electricals (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{RBIAS}	RBIAS current adder					
	• LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF)	—	10	—	µA	
	• LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)	—	1	—	µA	
R_{RBIAS}	RBIAS resistor values					
	• LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF)	—	0.28	—	MΩ	
	• LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)	—	2.98	—	MΩ	
VLL1	VLL1 voltage	—	—	V_{IREG}	V	4
VLL2	VLL2 voltage	—	—	2 x V_{IREG}	V	4
VLL3	VLL3 voltage	—	—	3 x V_{IREG}	V	4
VLL1	VLL1 voltage	—	—	V_{DDA} / 3	V	5
VLL2	VLL2 voltage	—	—	V_{DDA} / 1.5	V	5
VLL3	VLL3 voltage	—	—	V_{DDA}	V	5

1. The actual value used could vary with tolerance.
2. For highest glass capacitance values, LCD_GCR[LADJ] should be configured as specified in the LCD Controller chapter within the device's reference manual.
3. V_{IREG} maximum should never be externally driven to any level other than V_{DD} - 0.15 V
4. VLL1, VLL2 and VLL3 are a function of V_{IREG} only when the regulator is enabled (GCR[RVEN]=1) and the charge pump is enabled (GCR[CPSEL]=1).
5. VLL1, VLL2 and VLL3 are a function of V_{DDA} only under either of the following conditions:
   - The charge pump is enabled (GCR[CPSEL]=1), the regulator is disabled (GCR[RVEN]=0), and VLL3 = V_{DDA} through the internal power switch (GCR[VSUPPLY]=0).
   - The resistor bias string is enabled (GCR[CPSEL]=0), the regulator is disabled (GCR[RVEN]=0), and VLL3 is connected to V_{DDA} externally (GCR[VSUPPLY]=1).

6 Design considerations

6.1 Hardware design considerations

This device contains protective circuitry to guard against damage due to high static voltage or electric fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

6.1.1 Printed circuit board recommendations

- Place connectors or cables on one edge of the board and do not place digital circuits between connectors.
- Drivers and filters for I/O functions must be placed as close to the connectors as possible. Connect TVS devices at the connector to a good ground. Connect filter capacitors at the connector to a good ground. Consider to add ferrite bead or inductor to some sensitive lines.
- Physically isolate analog circuits from digital circuits if possible.
- Place input filter capacitors as close to the MCU as possible.
- For best EMC performance, route signals as transmission lines; use a ground plane directly under LQFP packages; and solder the exposed pad (EP) to ground directly under QFN packages.

6.1.2 Power delivery system

Consider the following items in the power delivery system:

- Use a plane for ground.
- Use a plane for MCU VDD supply if possible.
- Always route ground first, as a plane or continuous surface, and never as sequential segments.
- Always route the power net as star topology, and make each power trace loop as minimum as possible.
- Route power next, as a plane or traces that are parallel to ground traces.
- Place bulk capacitance, 10 µF or more, at the entrance of the power plane.
- Place bypass capacitors for MCU power domain as close as possible to each VDD/VSS pair, including VDDA/VSSA and VREFH/VREFL.
- The minimum bypass requirement is to place 0.1 µF capacitors positioned as near as possible to the package supply pins.
- Take special care to minimize noise levels on the VREFH/VREFL inputs. An option is to use the internal reference voltage (output 1.2 V typically) as the ADC reference.

NOTE

The internally-generated Voltage Reference Output (VREF_OUT) is bonded to the VREFH pin on some packages and to PTE30 on other packages. When VREF_OUT is used, a 0.1 µF capacitor is required as a filter. Do not connect any other supply voltage to the pin that has VREF_OUT activated.

6.1.3 Analog design

Each ADC input must have an RC filter as shown in the following figure. The maximum value of R must be RAS max if fast sampling and high resolution are required. The value of C must be chosen to ensure that the RC time constant is very small compared to the sample period.

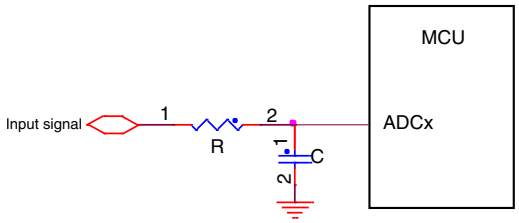


Figure 34. RC circuit for ADC input

High voltage measurement circuits require voltage division, current limiting, and over-voltage protection as shown the following figure. The voltage divider formed by R1 – R4 must yield a voltage less than or equal to VREFH. The current must be limited to less than the injection current limit. Since the ADC pins do not have diodes to VDD, external clamp diodes must be included to protect against transient over-voltages.

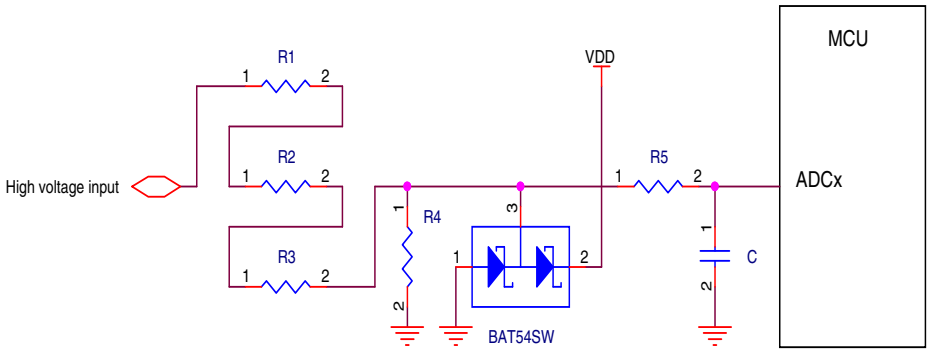


Figure 35. High voltage measurement with an ADC input

NOTE

For more details of ADC related usage, refer to AN5250: How to Increase the Analog-to-Digital Converter Accuracy in an Application.

6.1.4 Digital design

Ensure that all I/O pins cannot get pulled above VDD (Max I/O is VDD+0.3V).

CAUTION

Do not provide power to I/O pins prior to VDD, especially the RESET_b pin.

- RESET_b pin

  The RESET_b pin is an open-drain I/O pin that has an internal pullup resistor. An external RC circuit is recommended to filter noise as shown in the following figure. The resistor value must be in the range of 4.7 kΩ to 10 kΩ; the recommended capacitance value is 0.1 µF. The RESET_b pin also has a selectable digital filter to reject spurious noise.

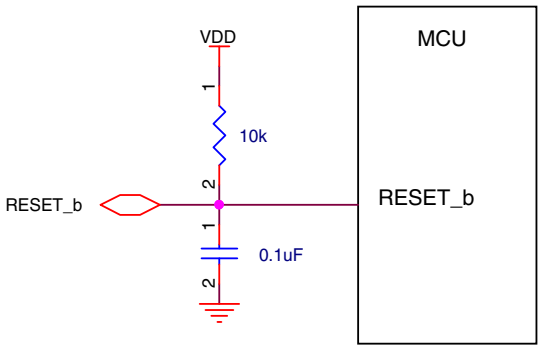


Figure 36. Reset circuit

When an external supervisor chip is connected to the RESET_b pin, a series resistor must be used to avoid damaging the supervisor chip or the RESET_b pin, as shown in the following figure. The series resistor value (RS below) must be in the range of 100 Ω to 1 kΩ depending on the external reset chip drive strength. Select the open-drain output from the supervisor chip.

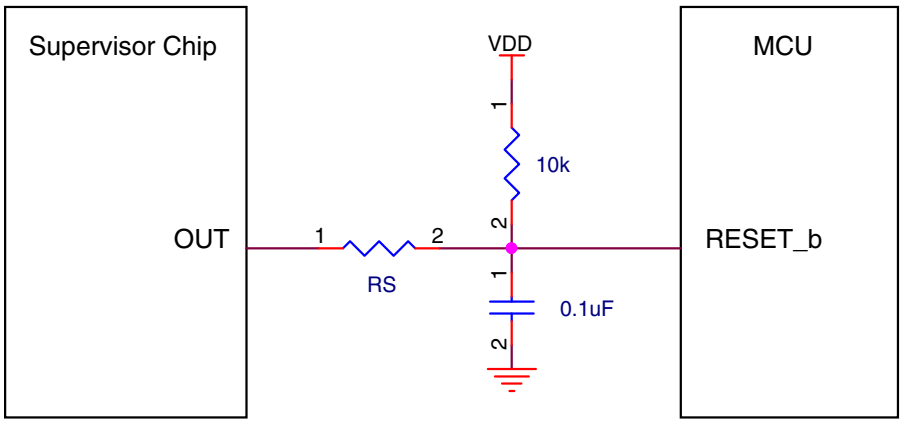


Figure 37. Reset signal connection to external reset chip

- NMI pin

  Do not add a pull-down resistor or capacitor on the NMI_b pin, because a low level on this pin will trigger non-maskable interrupt. When this pin is enabled as the NMI function, an external pull-up resistor (10 kΩ) as shown in the following figure is recommended for robustness.

  If the NMI_b pin is used as an I/O pin, the non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI_DIS] bit to zero.

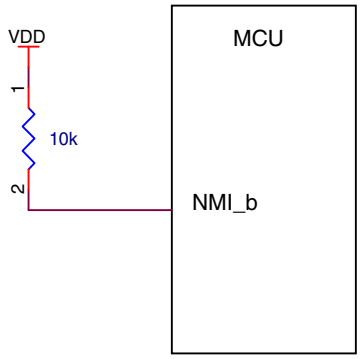


Figure 38. NMI pin biasing

- Debug interface

  This MCU uses the standard Arm SWD interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (SWD_DIO has an internal pull-up and SWD_CLK has an internal pull-down), external 10 kΩ pull resistors are recommended for system robustness. The RESET_b pin recommendations mentioned above must also be considered.

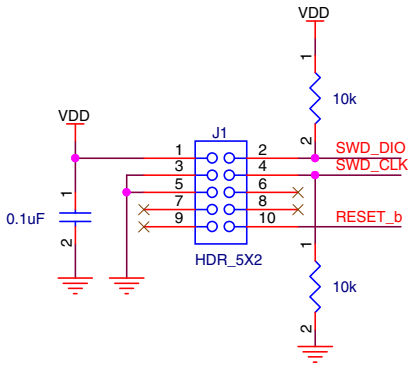


Figure 39. SWD debug interface

- Low leakage stop mode wakeup

  Select low leakage wakeup pins (LLWU_Px) to wake the MCU from one of the low leakage stop modes (LLS/VLLSx). See the pinout table for pin selection.

- Unused pin

  Unused GPIO pins must be left floating (no electrical connections) with the MUX field of the pin's PORTx_PCRn register equal to 0:0:0. This disables the digital input path to the MCU.

  If the USB module is not used, leave the USB data pins (USB0_DP, USB0_DM) floating.

6.1.5 Crystal oscillator

When using an external crystal or ceramic resonator as the frequency reference for the MCU clock system, refer to the following table and diagrams.

The feedback resistor, RF, is incorporated internally with the low power oscillators. An external feedback is required when using high gain (HGO=1) mode.

Internal load capacitors (Cx, Cy) are provided in the low frequency (32.786 kHz) mode. Use the SCxP bits in the OSC0_CR register to adjust the load capacitance for the crystal. Typically, values of 10pf to 16 pF are sufficient for 32.768 kHz crystals that have a 12.5 pF CL specification. The internal load capacitor selection must not be used for high frequency crystals and resonators.

Table 73. External crystal/resonator connections

Oscillator mode	Oscillator mode
Low frequency (32.768 kHz), low power	Diagram 1
Low frequency (32.768 kHz), high gain	Diagram 2, Diagram 4
High frequency (3-32 MHz), low power	Diagram 3
High frequency (3-32 MHz), high gain	Diagram 4

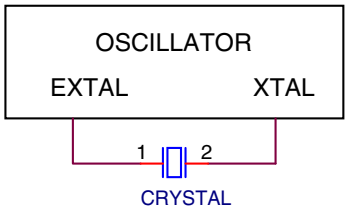


Figure 40. Crystal connection – Diagram 1

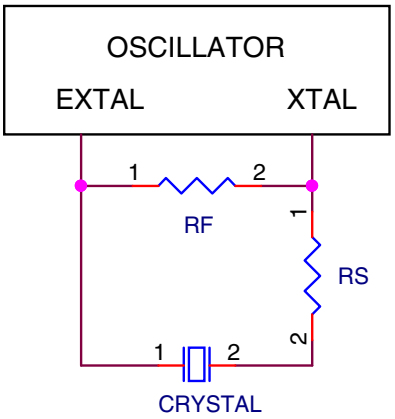


Figure 41. Crystal connection – Diagram 2

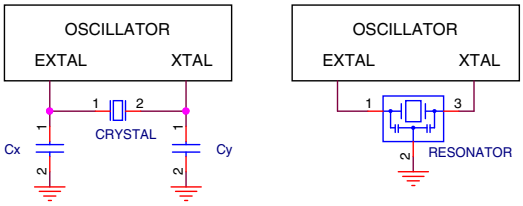


Figure 42. Crystal connection – Diagram 3

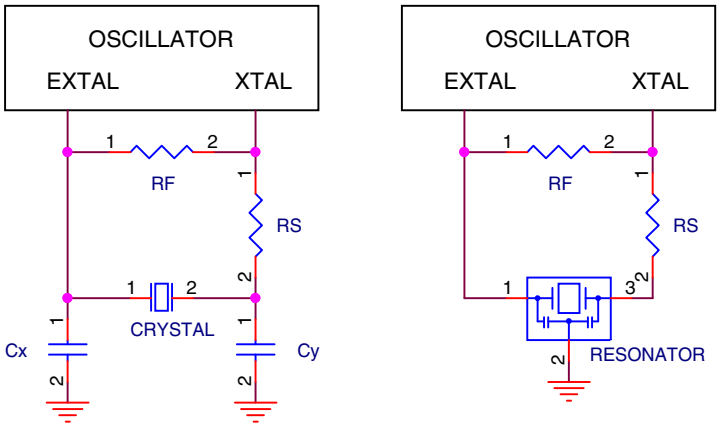


Figure 43. Crystal connection – Diagram 4

6.2 Software considerations

All K32 L-series ultra-low power Microcontrollers (MCUs), optimized for low-leakage applications, are supported by comprehensive NXP and third-party hardware and software enablement solutions, which can reduce development costs and time to market. Featured software and tools are listed below.

Evaluation and Prototyping Hardware

- NXP Freedom Development Platform: http://www.nxp.com/freedom
- Tower System Development Platform: http://www.nxp.com/tower

IDEs for K32 L2B MCUs

- MCUXpresso: https://mcuxpresso.nxp.com

Run-time Software

- K32 L2B SDK: http://mcuxpresso.nxp.com

For all other partner-developed software and tools, visit http://www.nxp.com/partners.

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

B PF S FS SPF T PG FR SR PT

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 74. Part number fields descriptions

Field	Description	Values
B	Brand	• K32
PF	Product Family	• L2
S	Sub-family	• A= Sub-family A • B= Sub-family B
FS	Flash size	• 1 = 64 KB • 2 = 128 KB • 3 = 256 KB • 4 = 512 KB
SPF	Special Feature	• 0 = Dual core • 1 = Single core
T	Temperature range (°C)	• V = -40 to 105
PG	Package	• FM = 32 QFN • FT = 48 QFN • MP = 64 BGA • LH = 64 LQFP
FR	Frequency (MHz)	• 0 = 0 - 50 MHz
SR	Silicon Revision	• A = Initial Mask Set • B = 1st Major Spin
PT	Packaging Type	• R = Std Reel

7.4 Example

This is an example part number:

K32L2B31VLH0A

8 Revision History

The following table provides a revision history for this document.

Table 75. Revision History

Rev. No.	Date	Substantial Changes
2	December 2019	• Added Related Resources table in front page of the Data sheet. • Corrected description of PD/PU in Table 8 Pin Properties section. • Updated values in "Default" column for pins 1, 2, 9, 10, 49-52 in K32 L2B Signal Multiplexing and Pin Assignments (LQFP and MAPBGA). • Added EXTRG_IN signal in TPM signal descriptions and Table 29.
1	September 2019	Initial public release. • Removed support of CRC throughout. • Replaced name of function pin VREFO with VREF_OUT. • Changed the high drive pin number to 6 for 48 QFN in Ordering information. • Updated flash and RAM in Figure 1. System diagram in the Overview section. • Added DAC topic to the "Peripheral Features" section. • Updated memory addresses and peripherals in Memory map. • Updated 32 QFN and 48 QFN pinouts and diagrams to remove usage of USB_VDD pin. • Updated pin names in Pin properties. Split the table into two, each for 64 LQFP/ MAPBGA and 32/48 QFN packages. • Added thermal attributes for 32 QFN and 48 QFN packages in Thermal attributes. • Updated part number format and fields in Format and Fields.
0	July 2019	• Initial release (internal).

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Document Number K32L2B3x
Revision 2, 12/2019