SCH322x

SCH3227/SCH3226/SCH3224/SCH3222
Silicon Errata and Data Sheet Clarifications

TABLE 1: SILICON DEV/REV VALUES

Part Number	STRAPOPT(3)	Device ID(1)	Revision ID for Silicon Revision(2)
			A
SCH3222	--	7Fh	02h
SCH3224	--	7Fh	02h
SCH3226	0 (low)	7Dh	02h
SCH3226	1 (high)	7Fh	02h
SCH3227	0 (low)	7Dh	02h
SCH3227	1 (high)	7Fh	02h

Note 1: The Device ID is visible as an 8-bit number at Plug and Play Configuration Index 20h.

2: The HW Revision Number is visible as an 8-bit number at Plug and Play Configuration Index 21h and Version/Stepping Number Register 3Fh.

3: STRAPOPT is a pin that is present on the SCH3226 and SCH3227 devices only. It affects the pinout and also the Device ID code, as shown above.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A
Serial Port	Reset	1.	Resetting UART 3 and UART 4 with PCI_RST	X

Note 1: If there are multiple revision-letter columns under this one, only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

1. Module: Serial Port

UART 3 and UART 4 do not tri-state their outputs on a PCI_RESET as do UART 1 and UART 2.

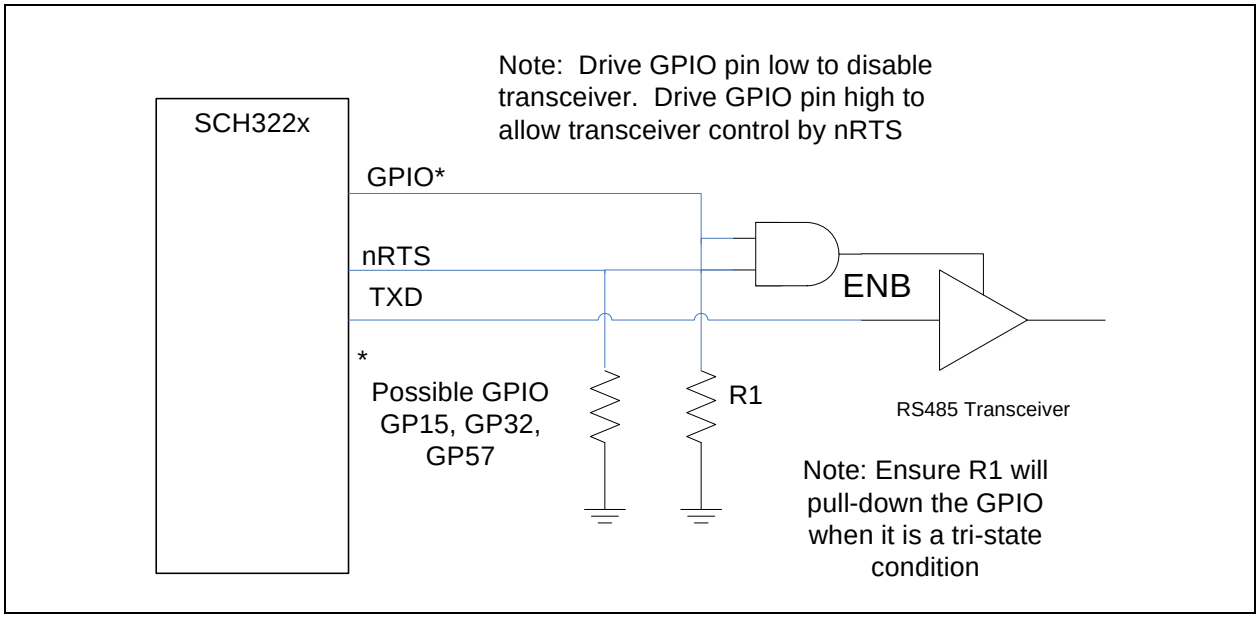
UART 3 and UART 4 outputs are not controlled by the Configuration Register 0x30 ACTIVATE bit.

END USER IMPLICATIONS

UART 3 and UART 4 outputs will drive High when PCI_RESET goes active or when the ACTIVATE bit is cleared, and if the platform uses RTS to control an RS485 transceiver this may interrupt communication.

Work Around

Use GPIO pin to disable RS485 transceiver when ACTIVATE bit is cleared.



Data Sheet Clarifications

Note:	The following typographic corrections and clarifications apply to Data Sheet Document #00002121A, which is at Revision A, and specifies only the family members SCH3222, SCH3224, SCH3226 and SCH3227. Other members of the SCH322x family have separate data sheets, and separate errata sheets.

TABLE 3: DATA SHEET CLARIFICATION SUMMARY

Module	Item Number	Issue Summary
Temp Monitor and Fan Control	1.	Incorrect offset for PME_EN1
Temp Monitor and Fan Control	2.	No Support for HWM SMI Events
Power Control	3.	32KHz Clock Required for PB_IN# and PB_OUT#
8042 Keyboard Controller	4.	Incorrect Register for Keyboard/Mouse Swap
Programmable Clock Output	5.	Misleading Label in Figure
Temp Monitor and Fan Control	6.	Incorrect Values in Table
Temp Monitor and Fan Control	7.	No Hardware Monitor Interrupt Event on SERIRQ
Runtime Registers	8.	Inconsistent Default for Keyboard PWRBTN Runtime Register
Runtime Registers	9.	Inconsistent Default for Runtime Registers
LPC Timing Diagrams	10.	Inconsistent PCI Clock Max Period

1. Module: Temperature Monitoring and Fan Control

The section “Interrupt as a PME Event,” refers to the PME_EN1 register at offset 0Ah. The offset for PME_EN1 is 08h.

2. Module: Temperature Monitoring and Fan Control

The section “Interrupt as an SMI Event,” is incorrect. Hardware monitoring interrupts are not routed to the SMI block and do not generate SMI events. The section will be removed in its entirety.

3. Module: Power Control Features

A clock is required on CLKI32 (pin 99) to clock in and debounce PB_IN# and to assert PB_OUT#. If CLKI32 is either not connected or is not connected to an active clock, PB_OUT# will not be asserted. CLKI32 should be connected to a 32KHz clock. A clock can be provided for PB_IN# by connecting CLKI32 to the SUSCLK output from the core logic south bridge.

4. Module: 8042 Keyboard Controller

The section “Keyboard/Mouse Swap Bit” says that there is a bit in the Keyboard Select configuration register at 0xF1 in logical device 7, used for swapping the keyboard and mouse pins. There is no such register. The keyboard/mouse swap bit is located in bit[6] of Runtime Register 0x5C, which is correctly documented.

5. Module: Programmable Clock Output

In the figure “Reset Generation Circuit”, there is a signal labeled “RESETB”. The figure implies that the signal comes in from an input pin. This is incorrect. The figure should indicate that the signal is an internally generated Power On Reset signal.

6. Module: Temperature Monitoring and Fan Control

The Nominal Voltage and Maximum Voltage numbers in the table "Voltage Limits vs. Register Setting" are incorrect for the row labeled 2.5V. The table indicates the nominal voltage is 5.0V and the maximum voltage is 6.64V. These two values are incorrect.

The correct nominal voltage is 2.5V, matching the signal name. The maximum voltage is 3.32V.

7. Module: Temperature Monitoring and Fan Control

In the subsection titled "Interrupt Event on Serial IRQ", in chapter "Temperature Monitoring and Fan Control", it is stated that the interrupt can be routed to the SERIRQ using configuration register 0x70 in Logical Device A. This is not correct. The Hardware Monitor Interrupt cannot be directly routed to a SERIRQ and there is no configuration register 0x70 in Logical Device A. This subsection will be deleted in subsequent releases of the data sheet.

As described in the subsections that precede this one, the Hardware Monitor interrupt can be routed onto a pin, onto an SMI or onto a PME. If it is required to route the HWM interrupt to a SERIRQ, it can be routed to an SMI, which can in turn be routed on SERIRQ2.

8. Module: Runtime Registers

The Description column of the Keyboard PWRBTN/SPEKEY runtime register specification states that the default value for bits[5:4], Keyboard Power Button Release, is 00b (De-assert KB_PB_STS 0.5sec after it is asserted).
This is inconsistent with the Name column, which states that the VBAT POR default value for bits[5:4] is 10b.

The actual default value is 10b. The system must set bits[5:4] to 00b if that is the desired behavior.

9. Module: Runtime Registers

The default POR values listed in the table "Runtime Register POR Summary" are incorrect in two cases. In addition, the default POR value for an additional register is incorrect in both this Summary table and also in the table "Detailed Runtime Register Description". Also, this Register table incorrectly states that register 0x10, PME_STS7, is reset on VBAT POR. The PME_STS7 register is reset on VTR POR, as stated in Summary table.

The following table shows the correct POR values for the registers in question:

Runtime Register	Description	VTR POR Default, Summary Table	VTR POR Default, Register Table	Actual VTR POR Default
0x10	PME_EN7	0x00	VBAT POR 0x00	0x00
0x13	SP34	0x00	0x44	0x44
0x4E	GP4	0x00	0xF0	0x05
0x6E	GP44	0x00	0x80	0x80

10. Module: LPC Timing Diagrams

In the chapter “Timing Diagrams”, section “LPC Interface Timing”:
In the table underneath the first figure “PCI Clock Timing”, the parameter t1 (Period) is given an incorrect value in the MAX column. It shows 33.3ns, and should instead be 52.6ns, which represents the lowest tested LPC frequency of 19MHz.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level and Date	Section	Description
DS80000694B (09-25-19)	Data Sheet Clarifications, Module #4 - 8042 Keyboard Controller	“Runtime Register 0x5” changed to “Runtime Register 0x5C”.
DS80000694A (04-11-16)	Initial Draft Version	

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