

FEATURES

- Member of the Texas Instruments Widebus+™ Family
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t_{pd} of 2.8 ns at 1.8 V
- Low Power Consumption, 40- μ A Max I_{CC}
- ± 8 -mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

This 32-bit edge-triggered D-type flip-flop is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC32374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as four 8-bit flip-flops, two 16-bit flip-flops, or one 32-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKE	Tape and reel	SN74AUC32374GKER	MM374

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

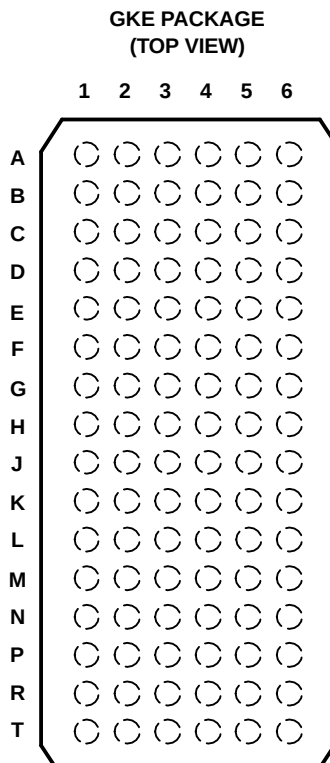


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SN74AUC32374
32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

SCES475–AUGUST 2003–REVISED MAY 2005



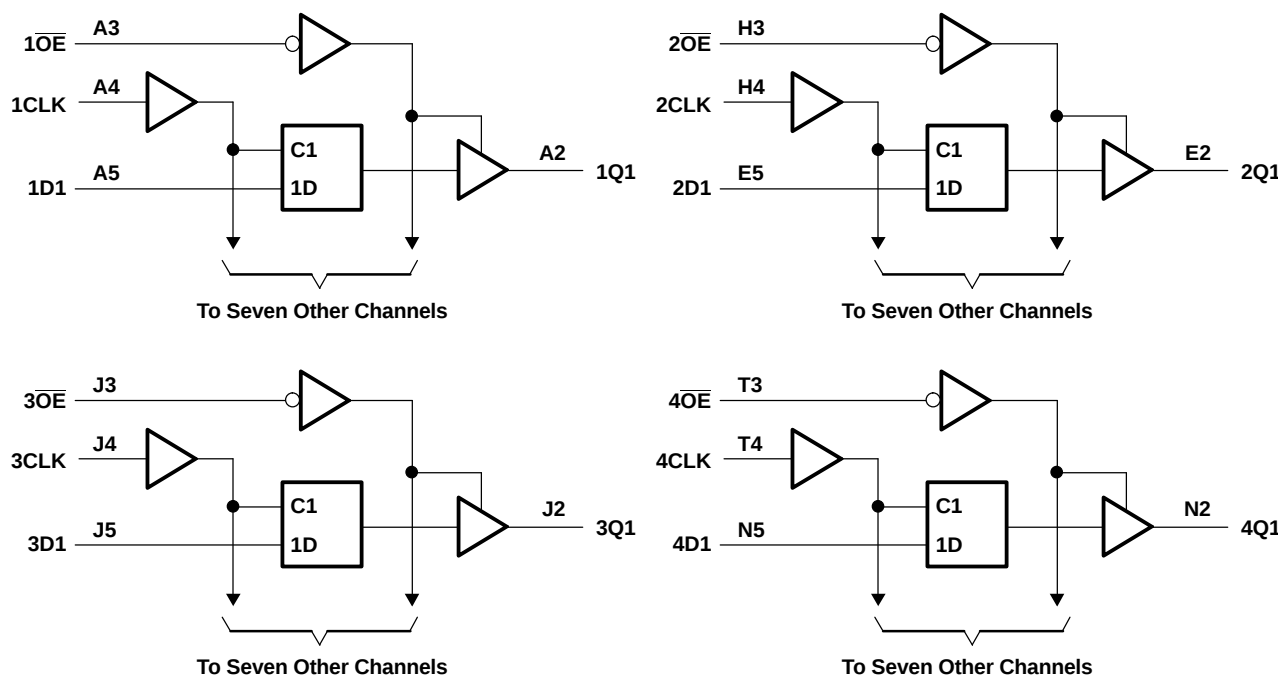
TERMINAL ASSIGNMENTS

	1	2	3	4	5	6
A	1Q2	1Q1	1 $\overline{OE}$	1CLK	1D1	1D2
B	1Q4	1Q3	GND	GND	1D3	1D4
C	1Q6	1Q5	V _{CC}	V _{CC}	1D5	1D6
D	1Q8	1Q7	GND	GND	1D7	1D8
E	2Q2	2Q1	GND	GND	2D1	2D2
F	2Q4	2Q3	V _{CC}	V _{CC}	2D3	2D4
G	2Q6	2Q5	GND	GND	2D5	2D6
H	2Q7	2Q8	2 $\overline{OE}$	2CLK	2D8	2D7
J	3Q2	3Q1	3 $\overline{OE}$	3CLK	3D1	3D2
K	3Q4	3Q3	GND	GND	3D3	3D4
L	3Q6	3Q5	V _{CC}	V _{CC}	3D5	3D6
M	3Q8	3Q7	GND	GND	3D7	3D8
N	4Q2	4Q1	GND	GND	4D1	4D2
P	4Q4	4Q3	V _{CC}	V _{CC}	4D3	4D4
R	4Q6	4Q5	GND	GND	4D5	4D6
T	4Q7	4Q8	4 $\overline{OE}$	4CLK	4D8	4D7

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	H or L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



SN74AUC32374

32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	–0.5	3.6	V
V _I	Input voltage range ⁽²⁾	–0.5	3.6	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	3.6	V
V _O	Output voltage range ⁽²⁾	–0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		–50 mA
I _{OK}	Output clamp current	V _O < 0		–50 mA
I _O	Continuous output current		±20	mA
	Continuous current through V _{CC} or GND		±100	mA
θ _{JA}	Package thermal impedance ⁽³⁾		40	°C/W
T _{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	0.8	2.7	V
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}	V
		V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	1.7	
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V	0	V
		V _{CC} = 1.1 V to 1.95 V	0.35 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	0.7	
V _I	Input voltage	0	3.6	V
V _O	Output voltage	Active state	0	V _{CC}
		3-state	0	3.6
I _{OH}	High-level output current	V _{CC} = 0.8 V	–0.7	mA
		V _{CC} = 1.1 V	–3	
		V _{CC} = 1.4 V	–5	
		V _{CC} = 1.65 V	–8	
		V _{CC} = 2.3 V	–9	
I _{OL}	Low-level output current	V _{CC} = 0.8 V	0.7	mA
		V _{CC} = 1.1 V	3	
		V _{CC} = 1.4 V	5	
		V _{CC} = 1.65 V	8	
		V _{CC} = 2.3 V	9	
Δt/Δv	Input transition rise or fall rate		20	ns/V
T _A	Operating free-air temperature	–40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}		I _{OH} = −100 μA	0.8 V to 2.7 V	V _{CC} − 0.1			V
		I _{OH} = −0.7 mA	0.8 V	0.55			
		I _{OH} = −3 mA	1.1 V	0.8			
		I _{OH} = −5 mA	1.4 V	1			
		I _{OH} = −8 mA	1.65 V	1.2			
		I _{OH} = −9 mA	2.3 V	1.8			
V _{OL}		I _{OL} = 100 μA	0.8 V to 2.7 V	0.2			V
		I _{OL} = 0.7 mA	0.8 V	0.25			
		I _{OL} = 3 mA	1.1 V	0.3			
		I _{OL} = 5 mA	1.4 V	0.4			
		I _{OL} = 8 mA	1.65 V	0.45			
		I _{OL} = 9 mA	2.3 V	0.6			
I _I	All inputs	V _I = V _{CC} or GND	0 to 2.7 V	±5			μA
I _{off}		V _I or V _O = 2.7 V	0	±10			μA
I _{OZ}		V _O = V _{CC} or GND	2.7 V	±10			μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	0.8 V to 2.7 V	40			μA
C _i		V _I = V _{CC} or GND	2.5 V	3			pF
C _o		V _O = V _{CC} or GND	2.5 V	5			pF

(1) All typical values are at T_A = 25°C.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

		V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V		V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		UNIT
		TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	85	250		250		250		250		MHz
t _w	Pulse duration, CLK high or low	5.9	1.9		1.9		1.9		1.9		ns
t _{SU}	Setup time, data before CLK↑	1.4	0.8		0.7		0.6		0.6		ns
t _h	Hold time, data after CLK↑	0.1	0.8		0.6		0.6		0.4		ns

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V		V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
f _{max}			85	250		250		250			250		MHz
t _{pd}	CLK	Q	7.3	1	4.5	0.8	2.9	0.7	1.5	2.8	0.7	2.2	ns
t _{en}	$\overline{\text{OE}}$	Q	7	1.2	5.3	0.8	3.6	0.8	1.5	2.9	0.7	2.2	ns
t _{dis}	$\overline{\text{OE}}$	Q	8.2	2	7.1	1	4.8	1.4	2.7	4.5	0.5	2.2	ns

SN74AUC32374

32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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Operating Characteristics⁽¹⁾

T_A = 25°C

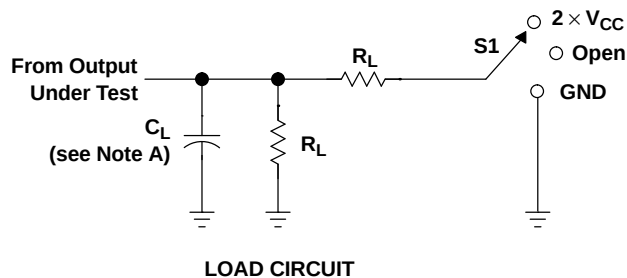
PARAMETER			TEST CONDITIONS	V _{CC} = 0.8 V	V _{CC} = 1.2 V	V _{CC} = 1.5 V	V _{CC} = 1.8 V	V _{CC} = 2.5 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C _{pd} ⁽²⁾ (each output)	Power dissipation capacitance	Outputs enabled, 1 output switching	1 f _{data} = 5 MHz, 1 f _{clk} = 10 MHz, 1 f _{out} = 5 MHz, $\overline{OE}$ = GND, C _L = 0 pF	24	24	24.1	26.2	31.2	pF
C _{pd} (Z)	Power dissipation capacitance	Outputs disabled, 1 clock and 1 data switching	1 f _{data} = 5 MHz, 1 f _{clk} = 10 MHz, f _{out} = not switching, $\overline{OE}$ = V _{CC} , C _L = 0 pF	7.5	7.5	8	9.4	13.2	pF
C _{pd} ⁽³⁾ (each clock)	Power dissipation capacitance	Outputs disabled, clock only switching	1 f _{data} = 0 MHz, 1 f _{clk} = 10 MHz, f _{out} = not switching, $\overline{OE}$ = V _{CC} , C _L = 0 pF	13.8	13.8	14	14.7	17.5	pF

(1) Total device C_{pd} for multiple (n) outputs switching and (y) clocks inputs switching = [n * C_{pd} (each output)] + [y * C_{pd} (each clock)].

(2) C_{pd} (each output) is the C_{pd} for each data bit (input and output circuitry) as it operates at 5 MHz (Note: the clock is operating at 10 MHz in this test, but its I_{CC} component has been subtracted out).

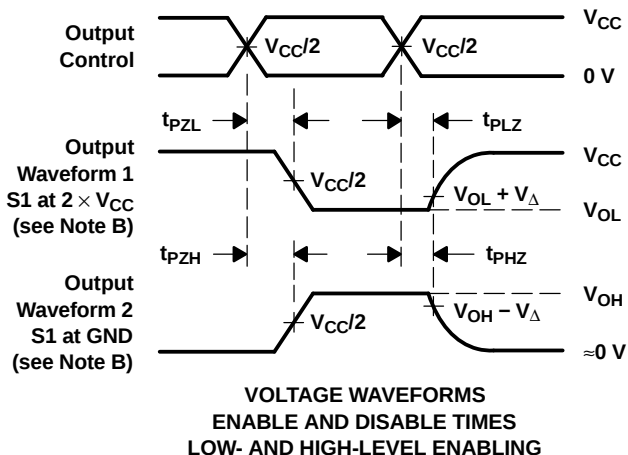
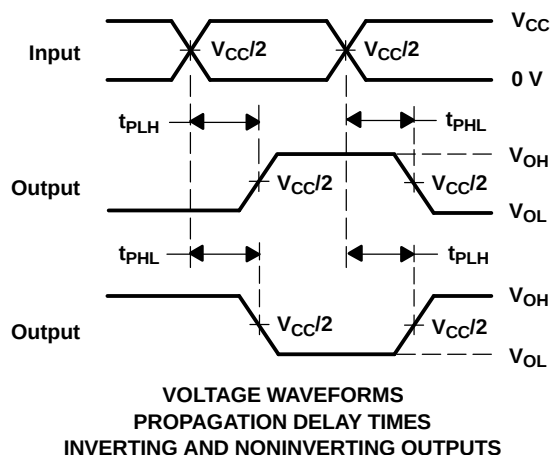
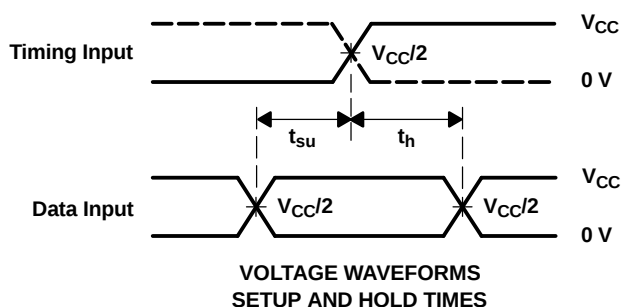
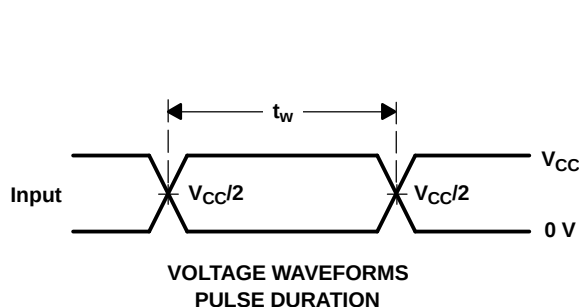
(3) C_{pd} (each clock) is the C_{pd} for the clock circuitry only as it operates at 10 MHz.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_{Δ}
0.8 V	15 pF	2 k Ω	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	2 k Ω	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V $\pm$ 0.15 V	30 pF	1 k Ω	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 Ω	0.15 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, $Z_O = 50 \Omega$, slew rate $\geq$ 1 V/ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUC32374ZKER	NRND	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	MM374	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

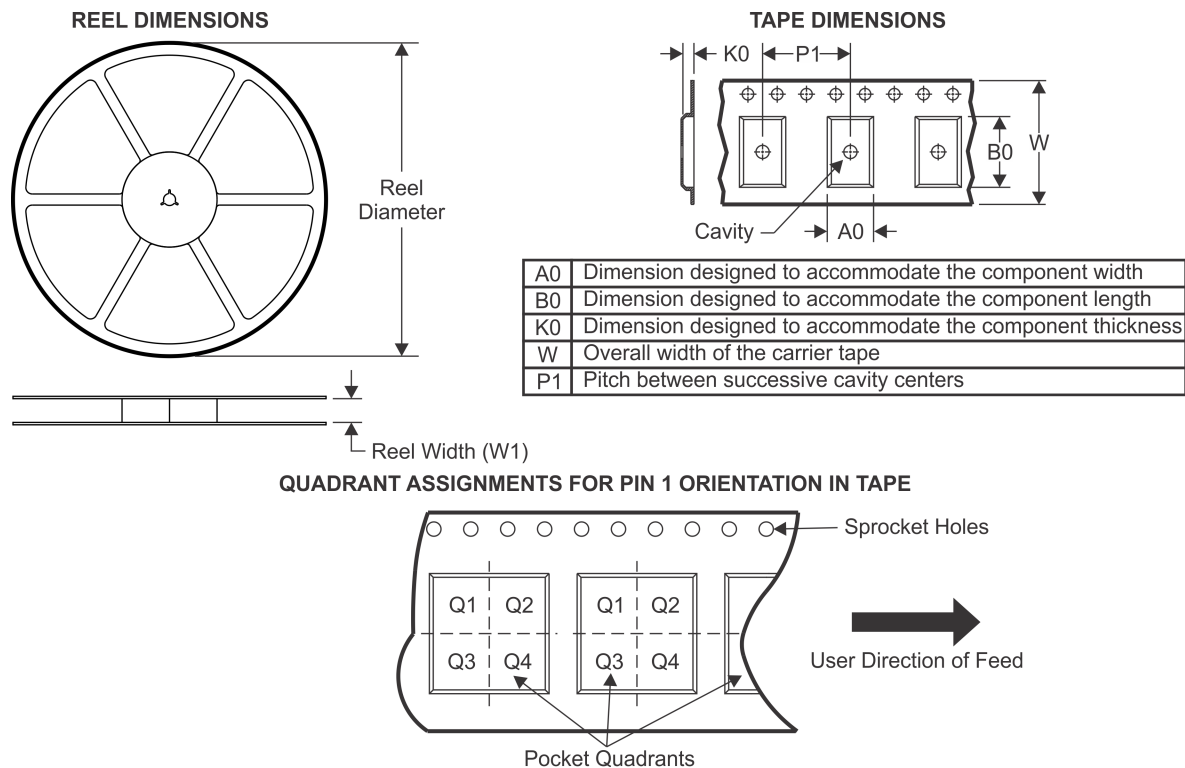
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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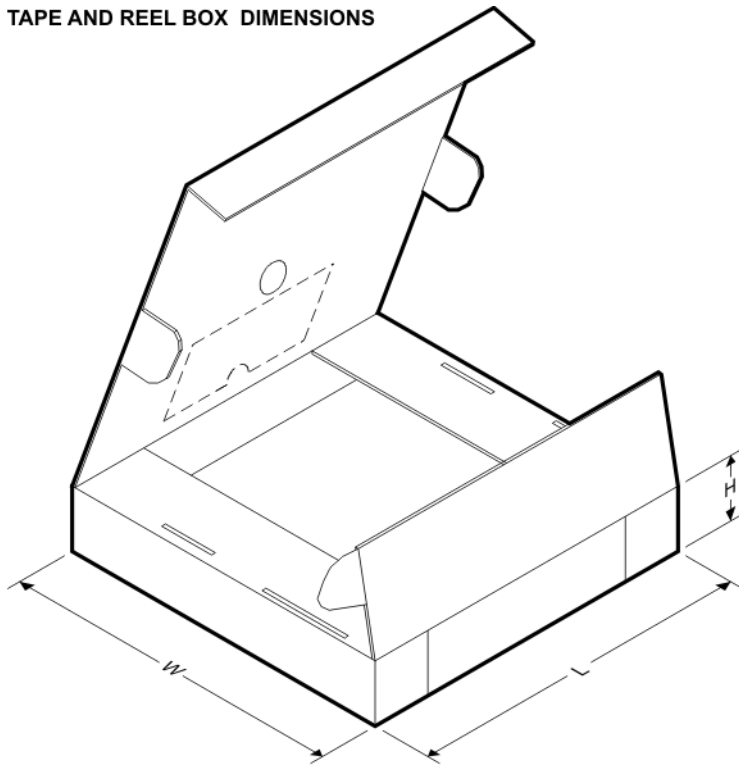
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC32374ZKER	LFBGA	ZKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

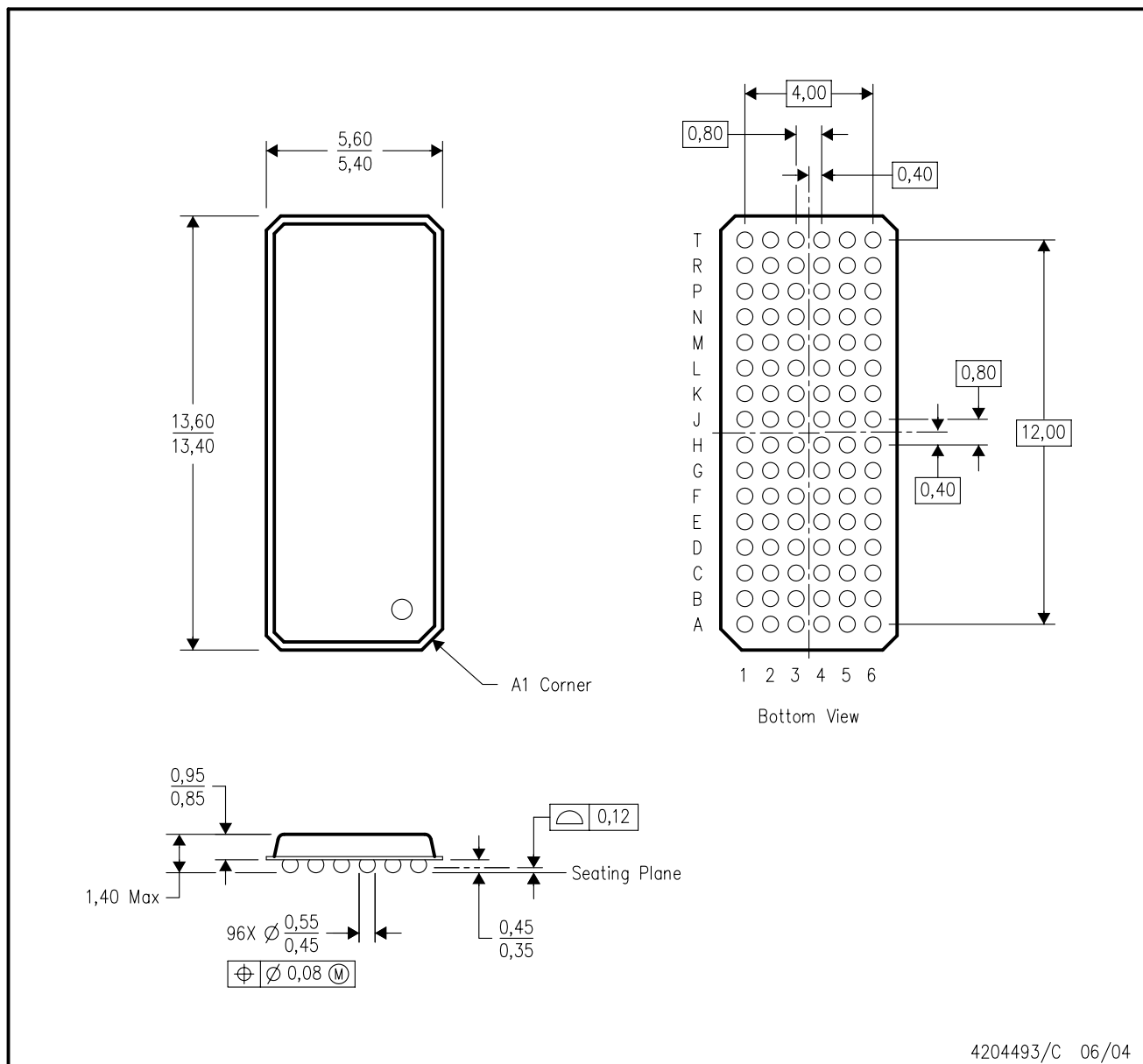


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC32374ZKER	LFBGA	ZKE	96	1000	336.6	336.6	41.3

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation CC.
 - D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

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