# Dual 1.6GHz to 2.7GHz High Dynamic Range Downconverting Mixer

## FEATURES

- **Conversion Gain: 8.3dB at 2.35GHz**
- **IIP3: 27.3dBm at 2.35GHz**
- **Noise Figure: 9.8dB at 2.35GHz**
- **15.3dB NF Under 5dBm Blocking**
- **High Input P1dB**
- **47dB Channel-to-Channel Isolation**
- **3.3V Supply, 1.3W Power Consumption**
- **Low Power Mode for 0.8W Consumption**
- **Independent Channel Shutdown Control**
- **50Ω Single-Ended RF and LO Inputs**
- **LO Input Matched In All Modes**
- **0dBm LO Drive Level**
- **Small Package and Solution Size**
- **–40°C to 105°C Operation**

## APPLICATIONS

- 3G/4G Wireless Infrastructure Diversity Receivers (LTE, W-CDMA, TD-SCDMA, WiMAX, GSM 1800)
- MIMO Infrastructure Diversity Receivers
- High Dynamic Range Downmixer Applications

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## DESCRIPTION

The LTC®5592 is part of a family of dual-channel high dynamic range, high gain downconverting mixers covering the 600MHz to 4.5GHz RF frequency range. **The LTC5592 is optimized for 1.6GHz to 2.7GHz RF applications. The LO frequency must fall within the 1.5GHz to 2.5GHz range for optimum performance.** A typical application is a LTE or WiMAX receiver with a 2.3GHz to 2.7GHz RF input and low side LO.

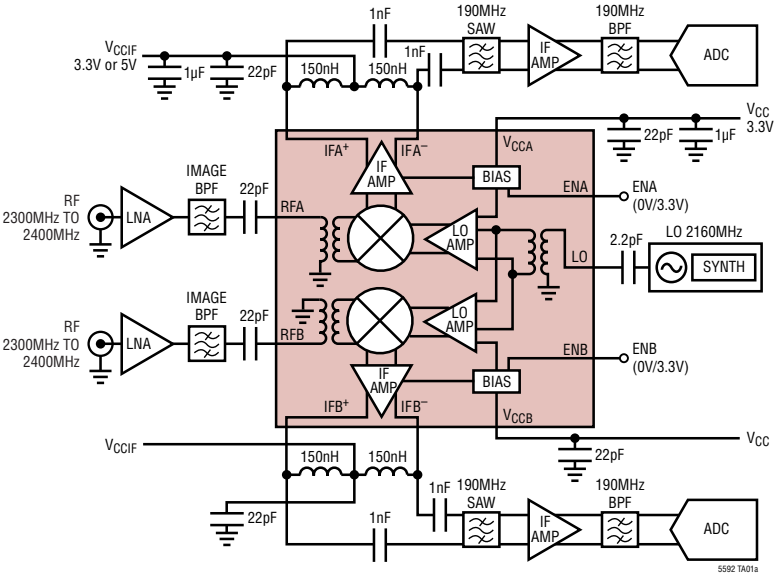
The LTC5592's high conversion gain and high dynamic range enable the use of lossy IF filters in high selectivity receiver designs, while minimizing the total solution cost, board space and system-level variation. A low current mode is provided for additional power savings and each of the mixer channels has independent shutdown control.

**High Dynamic Range Dual Downconverting Mixer Family**

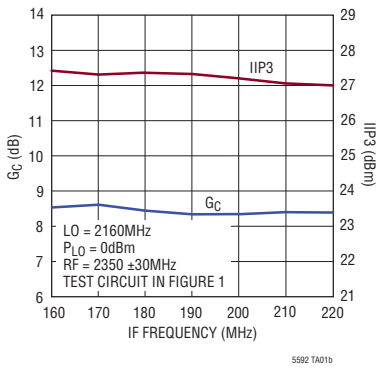
| PART NUMBER | RF RANGE | LO RANGE |
|---|---|---|
| LTC5590 | 600MHz to 1.7GHz | 700MHz to 1.5GHz |
| LTC5591 | 1.3GHz to 2.3GHz | 1.4GHz to 2.1GHz |
| **LTC5592** | **1.6GHz to 2.7GHz** | **1.5GHz to 2.5GHz** |
| LTC5593 | 2.3GHz to 4.5GHz | 2.1GHz to 4.2GHz |

## TYPICAL APPLICATION

**Wideband LTE Receiver**




**Wideband Conversion Gain and IIP3 vs IF Frequency**



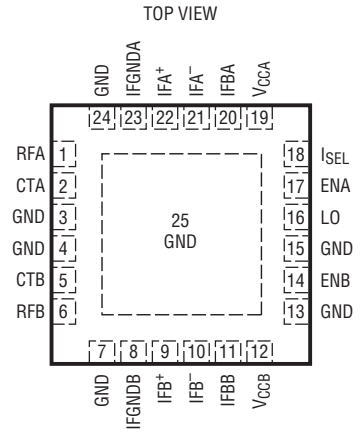

LTC5592 ONLY, MEASURED ON EVALUATION BOARD

## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Supply Voltage ($V_{CC}$) ..... 4.0V
IF Supply Voltage ($V_{CCIF}$) ..... 5.5V
Enable Voltage (ENA, ENB) ..... –0.3V to $V_{CC}$ + 0.3V
Bias Adjust Voltage (IFBA, IFBB) ..... –0.3V to $V_{CC}$ + 0.3V
Power Select Voltage ($I_{SEL}$) ..... –0.3V to $V_{CC}$ + 0.3V
LO Input Power (1GHz to 3GHz) ..... 9dBm
LO Input DC Voltage ..... ±0.1V
RFA, RFB Input Power (1GHz to 3GHz) ..... 15dBm
RFA, RFB Input DC Voltage ..... ±0.1V
Operating Temperature Range ($T_C$) ..... –40°C to 105°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature ($T_J$) ..... 150°C

## PIN CONFIGURATION




UH PACKAGE
24-LEAD (5mm × 5mm) PLASTIC QFN
$T_{JMAX}$ = 150°C, $\theta_{JC}$ = 7°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC5592IUH#PBF | LTC5592IUH#TRPBF | 5592 | 24-Lead (5mm × 5mm) Plastic QFN | –40°C to 105°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## DC ELECTRICAL CHARACTERISTICS

**$V_{CC}$ = 3.3V, $V_{CCIF}$ = 3.3V, ENA = ENB = High, $I_{SEL}$ = Low, $T_C$ = 25°C, unless otherwise noted. Test circuit shown in Figure 1. (Note 2)**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Power Supply Requirements ($V_{CCA}$, $V_{CCB}$, $V_{CCIFA}$, $V_{CCIFB}$)** | | | | | |
| $V_{CCA}$, $V_{CCB}$ Supply Voltage (Pins 12, 19) | | 3.1 | 3.3 | 3.5 | V |
| $V_{CCIFA}$, $V_{CCIFB}$ Supply Voltage (Pins 9, 10, 21, 22) | | 3.1 | 3.3 | 5.3 | V |
| Mixer Supply Current (Pins 12, 19) | Both Channels Enabled | | 199 | 237 | mA |
| IF Amplifier Supply Current (Pins 9, 10, 21, 22) | Both Channels Enabled | | 202 | 252 | mA |
| Total Supply Current (Pins 9, 10, 12, 19, 21, 22) | Both Channels Enabled | | 401 | 489 | mA |
| Total Supply Current – Shutdown | ENA = ENB = Low | | | 500 | µA |
| **Enable Logic Input (ENA, ENB) High = On, Low = Off** | | | | | |
| ENA, ENB Input High Voltage (On) | | 2.5 | | | V |
| ENA, ENB Input Low Voltage (Off) | | | | 0.3 | V |
| ENA, ENB Input Current | –0.3V to $V_{CC}$ + 0.3V | –20 | | 30 | µA |
| Turn On Time | | | 0.9 | | µs |
| Turn Off Time | | | 1 | | µs |

## DC ELECTRICAL CHARACTERISTICS

**$V_{CC}$ = 3.3V, $V_{CCIF}$ = 3.3V, ENA = ENB = High, $I_{SEL}$ = Low, $T_C$ = 25°C, unless otherwise noted. Test circuit shown in Figure 1. (Note 2)**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Low Power Mode Logic Input ($I_{SEL}$) High = Low Power, Low = Normal Power Mode** | | | | | |
| $I_{SEL}$ Input High Voltage | | 2.5 | | | V |
| $I_{SEL}$ Input Low Voltage | | | | 0.3 | V |
| $I_{SEL}$ Input Current | –0.3V to $V_{CC}$ + 0.3V | –20 | | 30 | µA |
| **Low Power Mode Current Consumption ($I_{SEL}$ = High)** | | | | | |
| Mixer Supply Current (Pins 12, 19) | Both Channels Enabled | | 130 | 156 | mA |
| IF Amplifier Supply Current (Pins 9, 10, 21, 22) | Both Channels Enabled | | 122 | 156 | mA |
| Total Supply Current (Pins 9, 10, 12, 19, 21, 22) | Both Channels Enabled | | 252 | 312 | mA |

## AC ELECTRICAL CHARACTERISTICS

**$V_{CC}$ = 3.3V, $V_{CCIF}$ = 3.3V, ENA = ENB = High, $I_{SEL}$ = Low, $T_C$ = 25°C, $P_{LO}$ = 0dBm, $P_{RF}$ = –3dBm (Δf = 2MHz for two tone IIP3 tests), unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3, 4)**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| LO Input Frequency Range | | | 1500 to 2500 | | MHz |
| RF Input Frequency Range | Low Side LO<br>High Side LO | | 1600 to 2700<br>1600 to 2300 | | MHz<br>MHz |
| IF Output Frequency Range | Requires External Matching | | 5 to 500 | | MHz |
| RF Input Return Loss | $Z_O$ = 50Ω, 1600MHz to 2700MHz | | >13 | | dB |
| LO Input Return Loss | $Z_O$ = 50Ω, 1700MHz to 2500MHz | | >17 | | dB |
| IF Output Impedance | Differential at 190MHz | | 379Ω\|\|2.2pF | | R\|\|C |
| LO Input Power | $f_{LO}$ = 1700MHz to 2500MHz | –4 | 0 | 6 | dBm |
| LO to RF Leakage | $f_{LO}$ = 1700MHz to 2500MHz | | <–34 | | dBm |
| LO to IF Leakage | $f_{LO}$ = 1700MHz to 2500MHz | | <–37 | | dBm |
| RF to LO Isolation | $f_{RF}$ = 1600MHz to 2700MHz | | >57 | | dB |
| RF to IF Isolation | $f_{RF}$ = 1600MHz to 2700MHz | | >37 | | dB |
| Channel-to-Channel Isolation | $f_{RF}$ = 1600MHz to 2700MHz | | >47 | | dB |

**Low Side LO Downmixer Application: $I_{SEL}$ = Low, RF = 1900MHz to 2700MHz, IF = 190MHz, $f_{LO} = f_{RF} – f_{IF}$**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Conversion Gain | RF = 1950MHz<br>RF = 2350MHz<br>RF = 2550MHz | 6.8 | 9.5<br>8.3<br>8.1 | | dB<br>dB<br>dB |
| Conversion Gain Flatness | RF = 2350 ±30MHz, LO = 2160MHz, IF = 190 ±30MHz | | ±0.14 | | dB |
| Conversion Gain vs Temperature | $T_C$ = –40°C to 105°C, RF = 2350MHz | | –0.006 | | dB/°C |
| Input 3rd Order Intercept | RF = 1950MHz<br>RF = 2350MHz<br>RF = 2550MHz | 24.0 | 26.3<br>27.3<br>26.3 | | dBm<br>dBm<br>dBm |
| SSB Noise Figure | RF = 1950MHz<br>RF = 2350MHz<br>RF = 2550MHz | | 9.4<br>9.8<br>9.9 | | dB<br>dB<br>dB |

## AC ELECTRICAL CHARACTERISTICS

**$V_{CC}$ = 3.3V, $V_{CCIF}$ = 3.3V, ENA = ENB = High, $T_C$ = 25°C, $P_{LO}$ = 0dBm, $P_{RF}$ = –3dBm (Δf = 2MHz for two tone IIP3 tests), unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3)**

**Low Side LO Downmixer Application: $I_{SEL}$ = Low, RF = 1900MHz to 2700MHz, IF = 190MHz, $f_{LO} = f_{RF} – f_{IF}$**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| SSB Noise Figure Under Blocking | $f_{RF}$ = 2400MHz, $f_{LO}$ = 2210MHz, $f_{BLOCK}$ = 2500MHz<br>$P_{BLOCK}$ = 5dBm<br>$P_{BLOCK}$ = 10dBm | | <br>15.3<br>21.2 | | <br>dB<br>dB |
| 2RF-2LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF}/2$) | $f_{RF}$ = 2255MHz at –10dBm, $f_{LO}$ = 2160MHz, $f_{IF}$ = 190MHz | | –68 | | dBc |
| 3RF-3LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF}/3$) | $f_{RF}$ = 2223.33MHz at –10dBm, $f_{LO}$ = 2160MHz, $f_{IF}$ = 190MHz | | –74 | | dBc |
| Input 1dB Compression | $f_{RF}$ = 2350MHz, $V_{CCIF}$ = 3.3V<br>$f_{RF}$ = 2350MHz, $V_{CCIF}$ = 5V | | 11<br>14.6 | | dBm<br>dBm |

**Low Power Mode, Low Side LO Downmixer Application: $I_{SEL}$ = High, RF = 1900MHz to 2700MHz, IF = 190MHz, $f_{LO} = f_{RF} – f_{IF}$**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Conversion Gain | RF = 2350MHz | | 7.1 | | dB |
| Input 3rd Order Intercept | RF = 2350MHz | | 22.3 | | dBm |
| SSB Noise Figure | RF = 2350MHz | | 10.2 | | dB |
| Input 1dB Compression | RF = 2350MHz, $V_{CCIF}$ = 3.3V<br>RF = 2350MHz, $V_{CCIF}$ = 5V | | 11.3<br>12.6 | | dBm<br>dBm |

**High Side LO Downmixer Application: $I_{SEL}$ = Low, RF = 1600MHz to 2300MHz, IF = 190MHz, $f_{LO} = f_{RF} + f_{IF}$**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Conversion Gain | RF = 1750MHz<br>RF = 1950MHz<br>RF = 2150MHz | | 9.1<br>8.7<br>8.3 | | dB<br>dB<br>dB |
| Conversion Gain Flatness | RF = 1950 ±30MHz, LO = 2140MHz, IF = 190 ±30MHz | | ±0.33 | | dB |
| Conversion Gain vs Temperature | $T_C$ = –40°C to 105°C, RF = 1900MHz | | –0.005 | | dB/°C |
| Input 3rd Order Intercept | RF = 1750MHz<br>RF = 1950MHz<br>RF = 2150MHz | | 25.3<br>25.4<br>25.1 | | dBm<br>dBm<br>dBm |
| SSB Noise Figure | RF = 1750MHz<br>RF = 1950MHz<br>RF = 2150MHz | | 9.2<br>9.8<br>10.4 | | dB<br>dB<br>dB |
| SSB Noise Figure Under Blocking | $f_{RF}$ = 1950MHz, $f_{LO}$ = 2140MHz, $f_{BLOCK}$ = 1850MHz<br>$P_{BLOCK}$ = 5dBm<br>$P_{BLOCK}$ = 10dBm | | <br>16.5<br>22.7 | | <br>dB<br>dB |
| 2LO-2RF Output Spurious Product ($f_{RF} = f_{LO} – f_{IF}/2$) | $f_{RF}$ = 2045MHz at –10dBm, $f_{LO}$ = 2140MHz, $f_{IF}$ = 190MHz | | –68 | | dBc |
| 3LO-3RF Output Spurious Product ($f_{RF} = f_{LO} – f_{IF}/3$) | $f_{RF}$ = 2076.67MHz at –10dBm, $f_{LO}$ = 2140MHz, $f_{IF}$ = 190MHz | | –75 | | dBc |
| Input 1dB Compression | RF = 1950MHz, $V_{CCIF}$ = 3.3V<br>RF = 1950MHz, $V_{CCIF}$ = 5V | | 10.6<br>14.0 | | dBm<br>dBm |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC5592 is guaranteed functional over the case operating temperature range of –40°C to 105°C ($\theta_{JC}$ = 7°C/W).

**Note 3:** SSB Noise Figure measured with a small-signal noise source, bandpass filter and 6dB matching pad on RF input, bandpass filter and 6dB matching pad on the LO input, and no other RF signals applied.

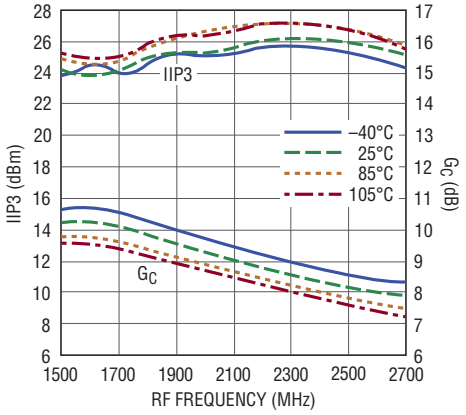
**Note 4:** Channel A to channel B isolation is measured as the relative IF output power of channel B to channel A, with the RF input signal applied to channel A. The RF input of channel B is 50Ω terminated and both mixers are enabled.

# TYPICAL AC PERFORMANCE CHARACTERISTICS

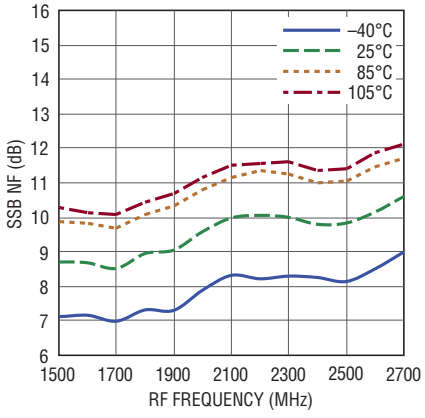
**Low Side LO**

**$V_{CC}$ = 3.3V, $V_{CCIF}$ = 3.3V, ENA = ENB = High, $I_{SEL}$ = Low, $T_C$ = 25°C, $P_{LO}$ = 0dBm, $P_{RF}$ = –3dBm (–3dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 190MHz, unless otherwise noted. Test circuit shown in Figure 1.**

### Conversion Gain and IIP3 vs RF Frequency

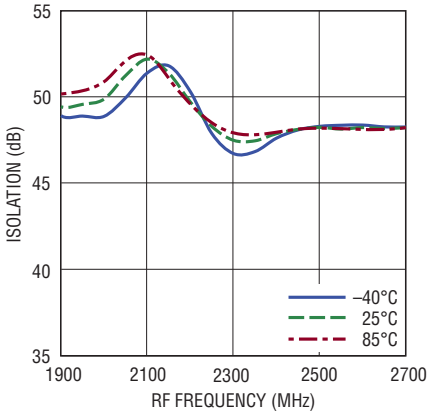



### SSB NF vs RF Frequency



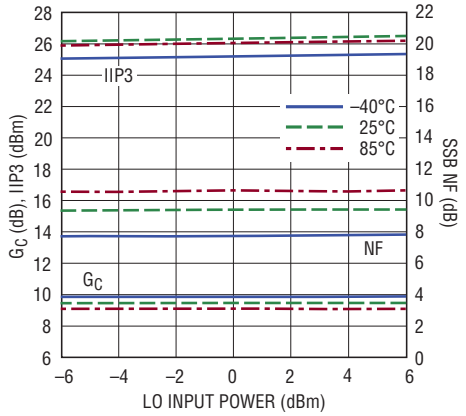

5592 G02

### Channel Isolation vs RF Frequency



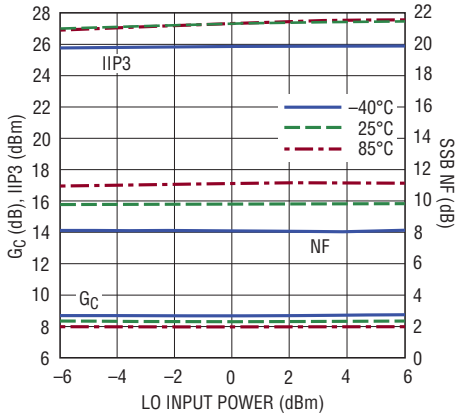

5592 G03

### 1950MHz Conversion Gain, IIP3 and NF vs LO Power



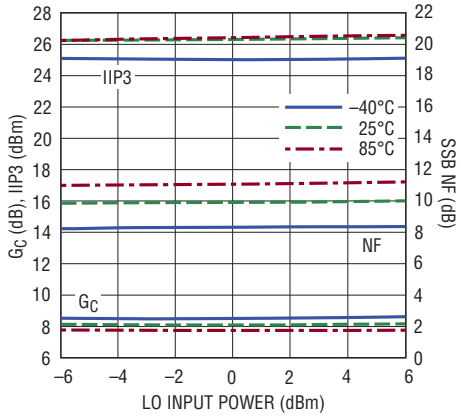

5592 G04

### 2350MHz Conversion Gain, IIP3 and NF vs LO Power



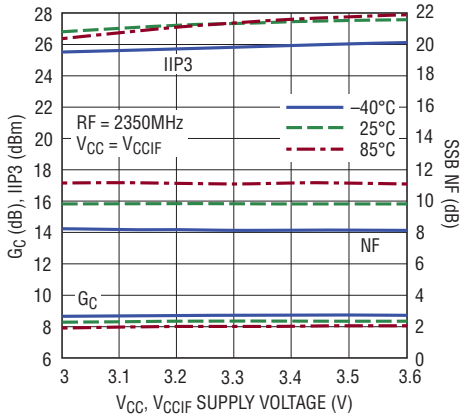

5592 G05

### 2550MHz Conversion Gain, IIP3 and NF vs LO Power



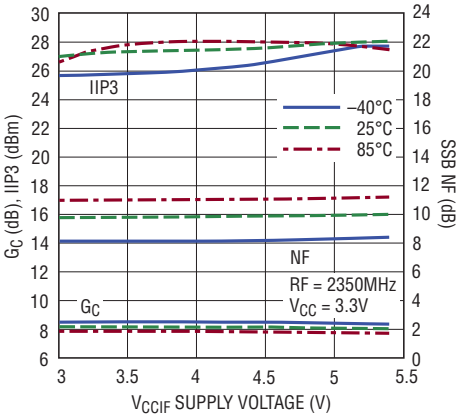

5592 G06

### Conversion Gain, IIP3 and NF vs Supply Voltage (Single Supply)



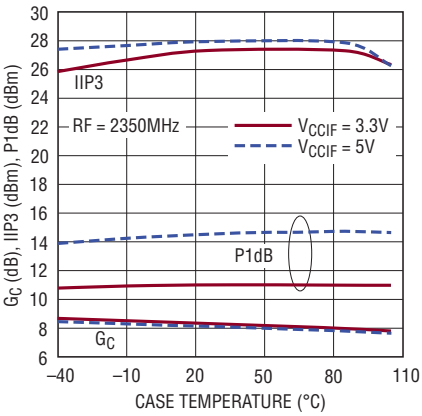

5592 G07

### Conversion Gain, IIP3 and NF vs Supply Voltage (Dual Supply)




5592 G08

### Conversion Gain, IIP3 and RF Input P1dB vs Temperature



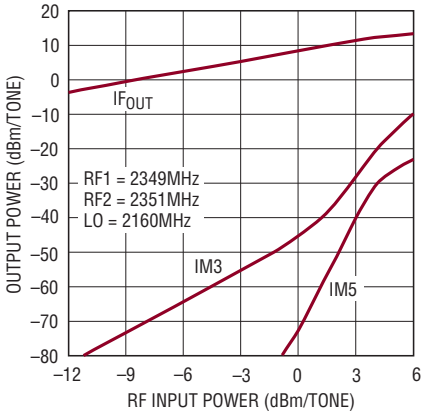

5592 G09

## TYPICAL AC PERFORMANCE CHARACTERISTICS

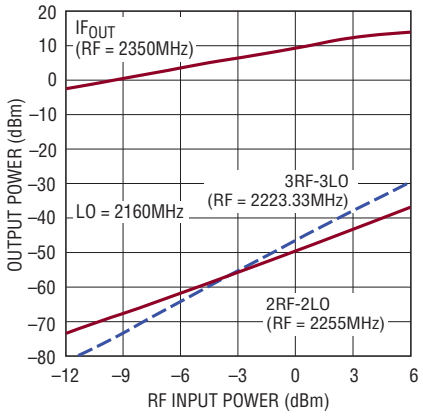
**Low Side LO**

**$V_{CC}$ = 3.3V, $V_{CCIF}$ = 3.3V, ENA = ENB = High, $I_{SEL}$ = Low, $T_C$ = 25°C, $P_{LO}$ = 0dBm, $P_{RF}$ = –3dBm (–3dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 190MHz, unless otherwise noted. Test circuit shown in Figure 1.**

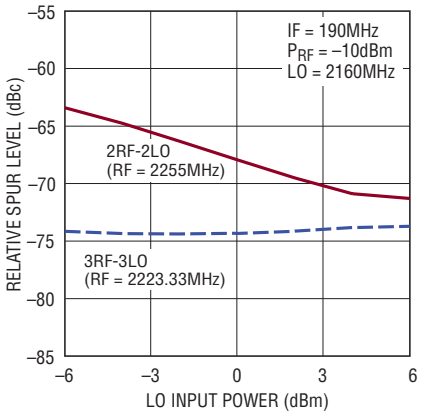
### 2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



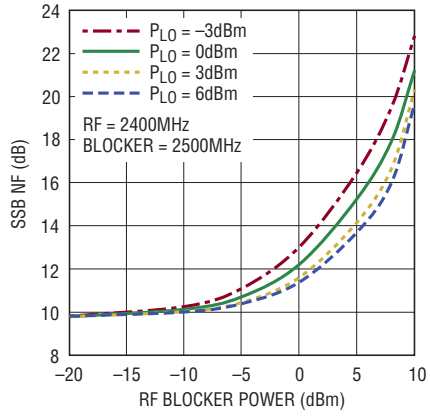

### Single-Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



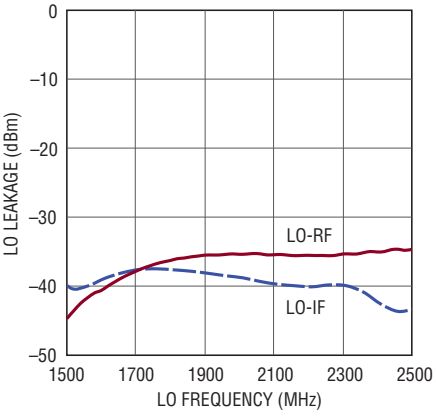

### 2 × 2 and 3 × 3 Spur Suppression vs LO Input Power



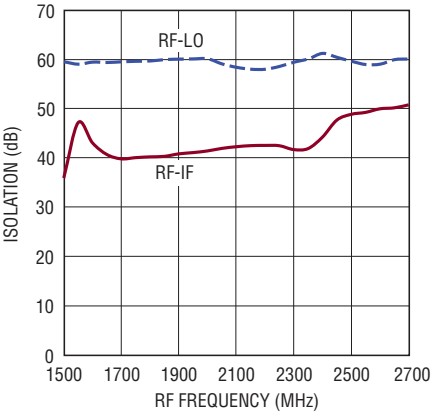

### SSB Noise Figure vs RF Blocker Power



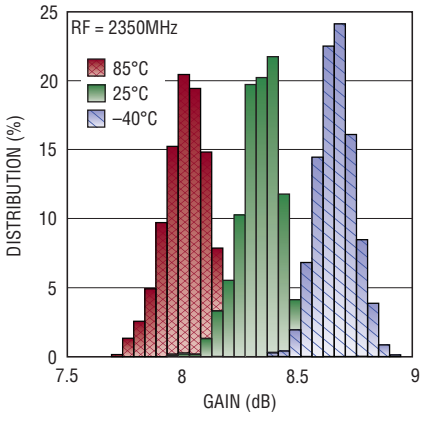

### LO Leakage vs LO Frequency



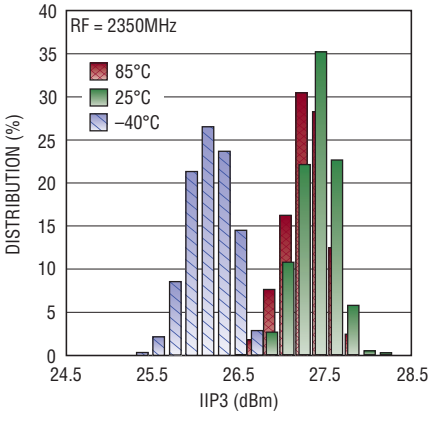

### RF Isolation vs RF Frequency



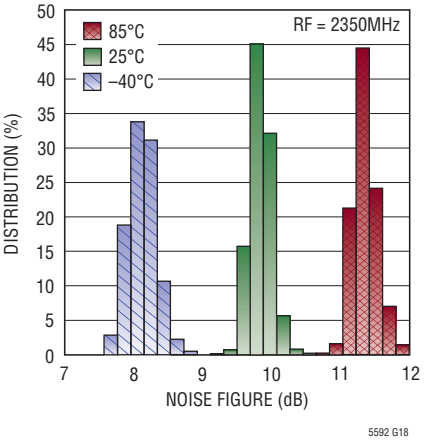

### Conversion Gain Distribution




### IIP3 Distribution




### SSB Noise Figure Distribution

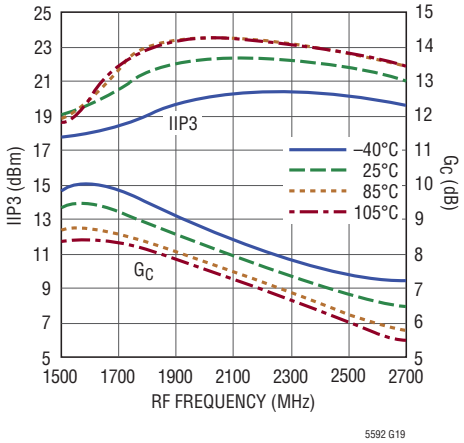


## TYPICAL AC PERFORMANCE CHARACTERISTICS

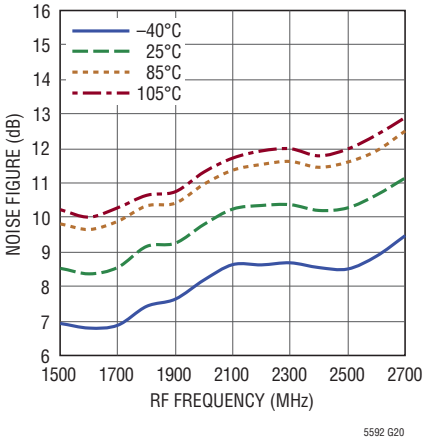
**Low Power Mode, Low Side LO**

**$V_{CC}$ = 3.3V, $V_{CCIF}$ = 3.3V, ENA = ENB = High, $I_{SEL}$ = High, $T_C$ = 25°C, $P_{LO}$ = 0dBm, $P_{RF}$ = –3dBm (–3dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 190MHz, unless otherwise noted. Test circuit shown in Figure 1.**

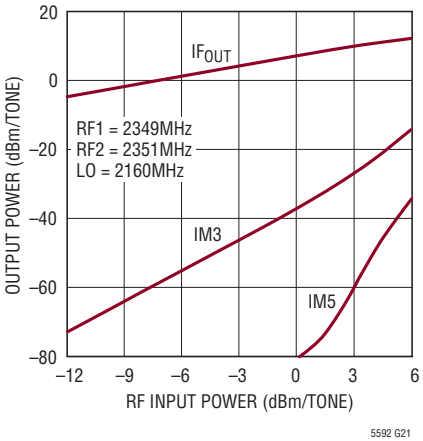
### Conversion Gain and IIP3 vs RF Frequency



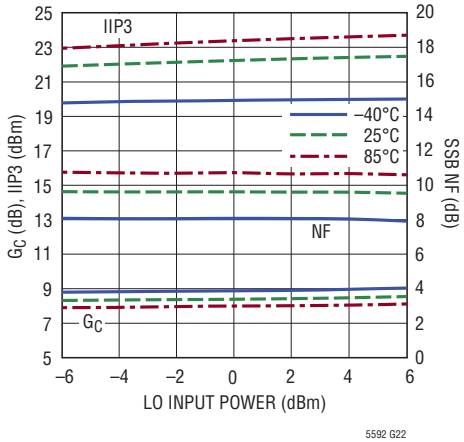

### SSB NF vs RF Frequency



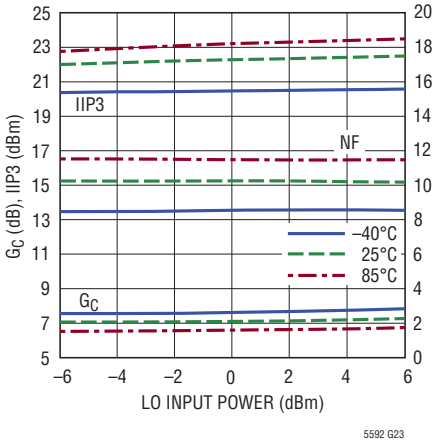

### 2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



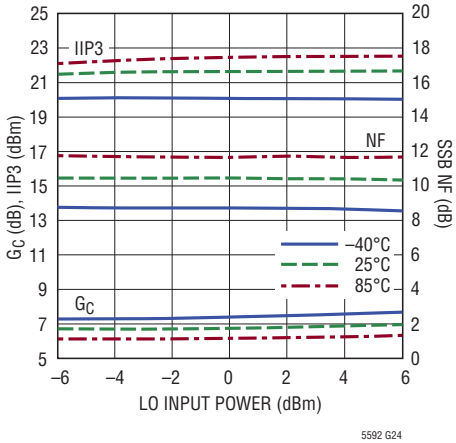

### 1950MHz Conversion Gain, IIP3 and NF vs LO Power



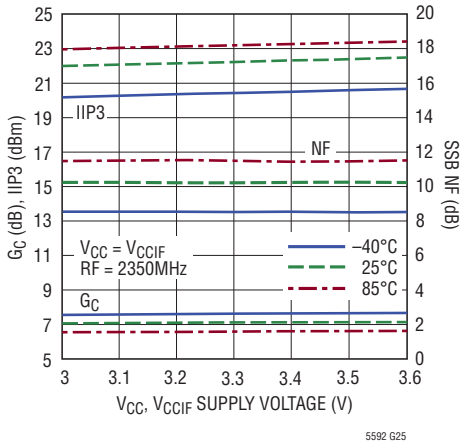

### 2350MHz Conversion Gain, IIP3 and NF vs LO Power



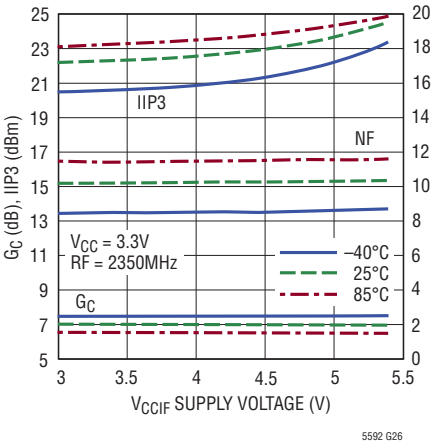

### 2550MHz Conversion Gain, IIP3 and NF vs LO Power



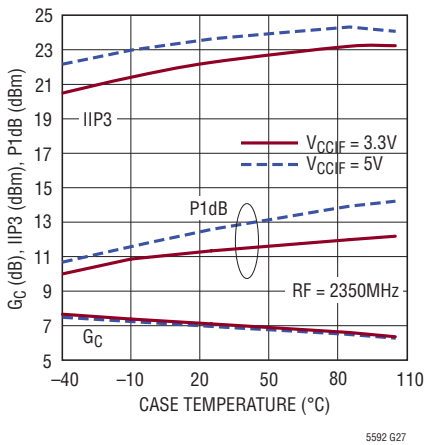

### Conversion Gain, IIP3 and NF vs Supply Voltage (Single Supply)




### Conversion Gain, IIP3 and NF vs Supply Voltage (Dual Supply)




### Conversion Gain, IIP3 and RF Input P1dB vs Temperature

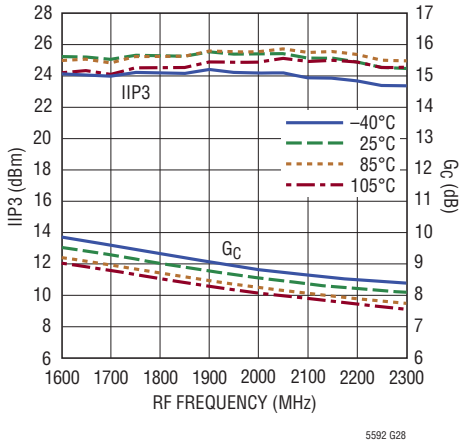


# TYPICAL AC PERFORMANCE CHARACTERISTICS

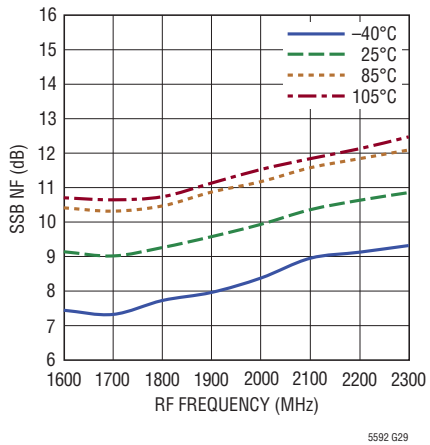
**High Side LO**

**$V_{CC}$ = 3.3V, $V_{CCIF}$ = 3.3V, ENA = ENB = High, $I_{SEL}$ = Low, $T_C$ = 25°C, $P_{LO}$ = 0dBm, $P_{RF}$ = –3dBm (–3dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 190MHz, unless otherwise noted. Test circuit shown in Figure 1.**

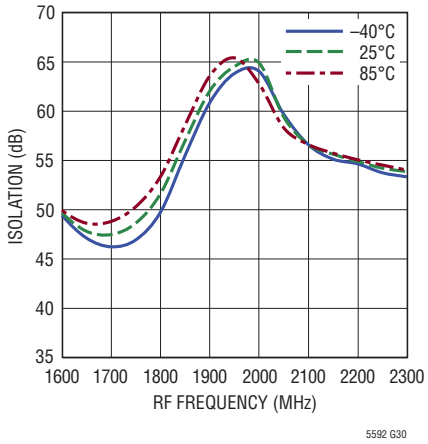
### Conversion Gain and IIP3 vs RF Frequency



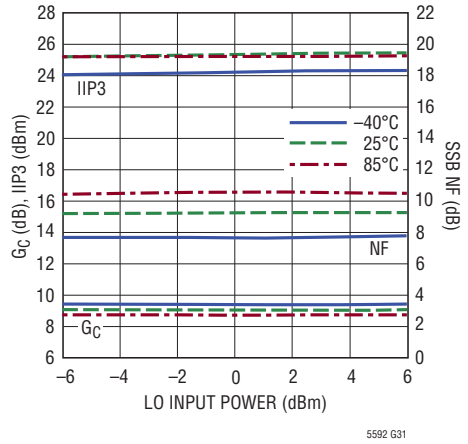

### SSB NF vs RF Frequency



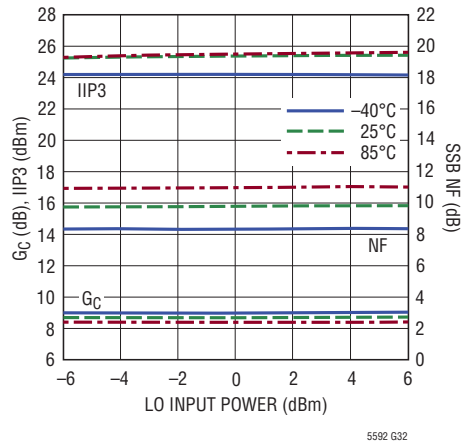

### Channel Isolation vs RF Frequency



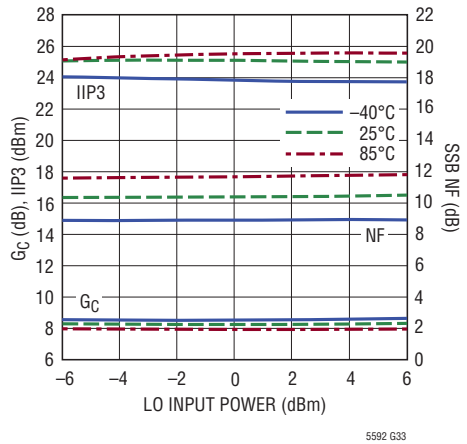

### 1750MHz Conversion Gain, IIP3 and NF vs LO Power



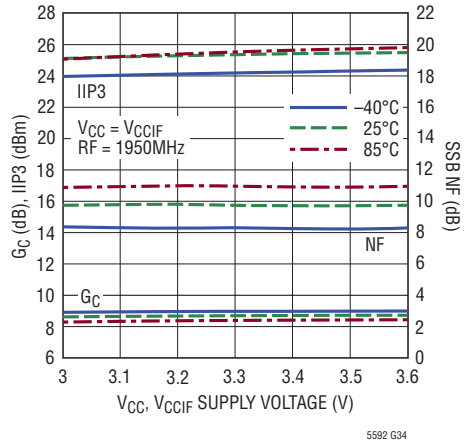

### 1950MHz Conversion Gain, IIP3 and NF vs LO Power



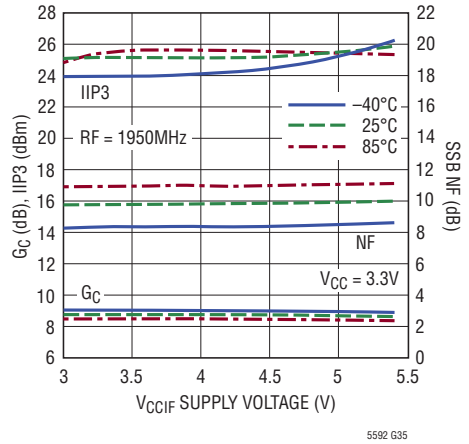

### 2150MHz Conversion Gain, IIP3 and NF vs LO Power



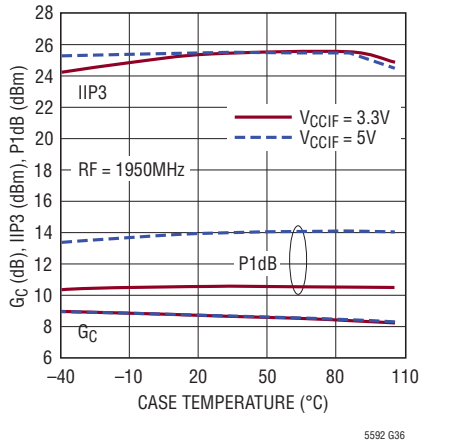

### Conversion Gain, IIP3 and NF vs Supply Voltage (Single Supply)




### Conversion Gain, IIP3 and NF vs Supply Voltage (Dual Supply)



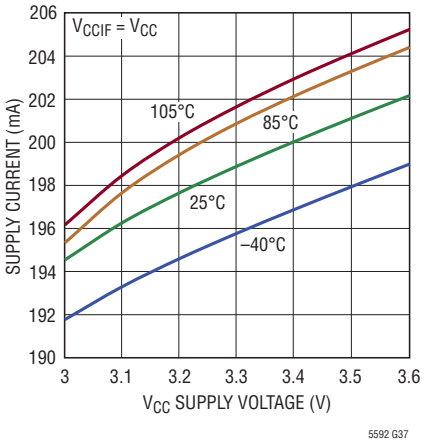

### Conversion Gain, IIP3 and RF Input P1dB vs Temperature



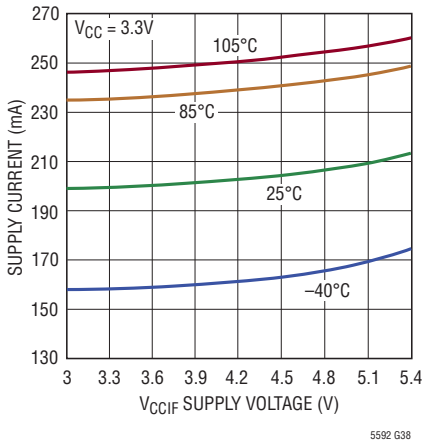
## TYPICAL DC PERFORMANCE CHARACTERISTICS

**$I_{SEL}$ = Low, ENA = ENB = High, test circuit shown in Figure 1.**

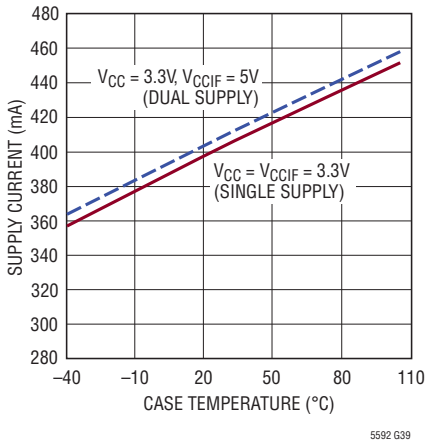
**$V_{CC}$ Supply Current vs Supply Voltage (Mixer + LO Amplifier)**




**$V_{CCIF}$ Supply Current vs Supply Voltage (IF Amplifier)**

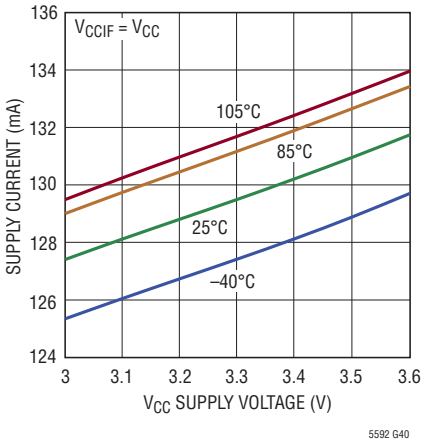



**Total Supply Current vs Temperature ($V_{CC}$ + $V_{CCIF}$)**

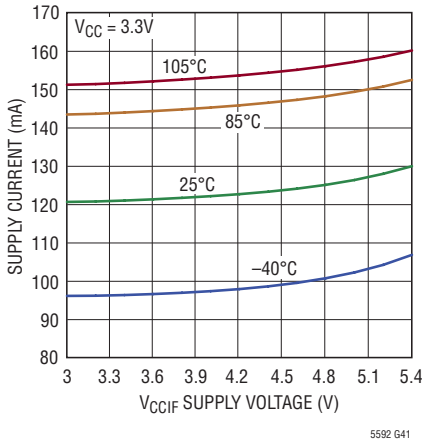



**$I_{SEL}$ = High, ENA = ENB = High, test circuit shown in Figure 1.**

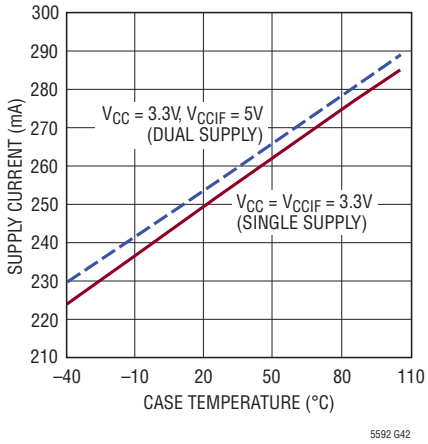
**$V_{CC}$ Supply Current vs Supply Voltage (Mixer + LO Amplifier)**




**$V_{CCIF}$ Supply Current vs Supply Voltage (IF Amplifier)**




**Total Supply Current vs Temperature ($V_{CC}$ + $V_{CCIF}$)**




## PIN FUNCTIONS

**RFA, RFB (Pins 1, 6):** Single-Ended RF Inputs for Channels A and B. These pins are internally connected to the primary sides of the RF input transformers, which have low DC resistance to ground. **Series DC-blocking capacitors should be used to avoid damage to the integrated transformer when DC voltage is present at the RF inputs.** The RF inputs are impedance matched when the LO input is driven with a 0±6dBm source between 1.5GHz and 2.5GHz and the channels are enabled.

**CTA, CTB (Pins 2, 5):** RF Transformer Secondary Center-Tap on Channels A and B. These pins may require bypass capacitors to ground to optimize IIP3 performance. Each pin has an internally generated bias voltage of 1.2V and must be DC-isolated from ground and $V_{CC}$.

**GND (Pins 3, 4, 7, 13, 15, 24, Exposed Pad Pin 25):** Ground. These pins must be soldered to the RF ground plane on the circuit board. The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the printed circuit board.

## PIN FUNCTIONS

**IFGNDB, IFGNDA (Pins 8, 23):** DC Ground Returns for the IF Amplifiers. These pins must be connected to ground to complete the DC current paths for the IF amplifiers. Chip inductors may be used to tune LO-IF and RF-IF leakage. Typical DC current is 101mA for each pin.

**$IFB^+$, $IFB^-$, $IFA^-$, $IFA^+$ (Pins 9, 10, 21, 22):** Open-Collector Differential Outputs for the IF Amplifiers of Channels B and A. These pins must be connected to a DC supply through impedance matching inductors, or transformer center-taps. Typical DC current consumption is 50.5mA into each pin.

**IFBB, IFBA (Pins 11, 20):** Bias Adjust Pins for the IF Amplifiers. These pins allow independent adjustment of the internal IF buffer currents for channels B and A, respectively. The typical DC voltage on these pins is 2.2V. If not used, these pins must be DC isolated from ground and $V_{CC}$.

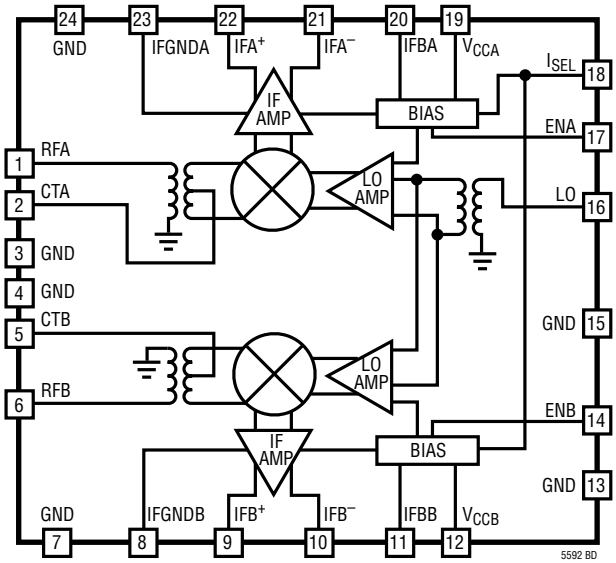
**$V_{CCB}$ and $V_{CCA}$ (Pins 12, 19):** Power Supply Pins for the LO Buffers and Bias Circuits. These pins must be connected to a regulated 3.3V supply with bypass capacitors located close to the pins. Typical current consumption is 99.5mA per pin.

**ENB, ENA (Pins 14, 17):** Enable Pins. These pins allow Channels B and A, respectively, to be independently enabled. An applied voltage of greater than 2.5V activates the associated channel while a voltage of less than 0.3V disables the channel. Typical input current is less than 10µA. These pins must not be allowed to float.

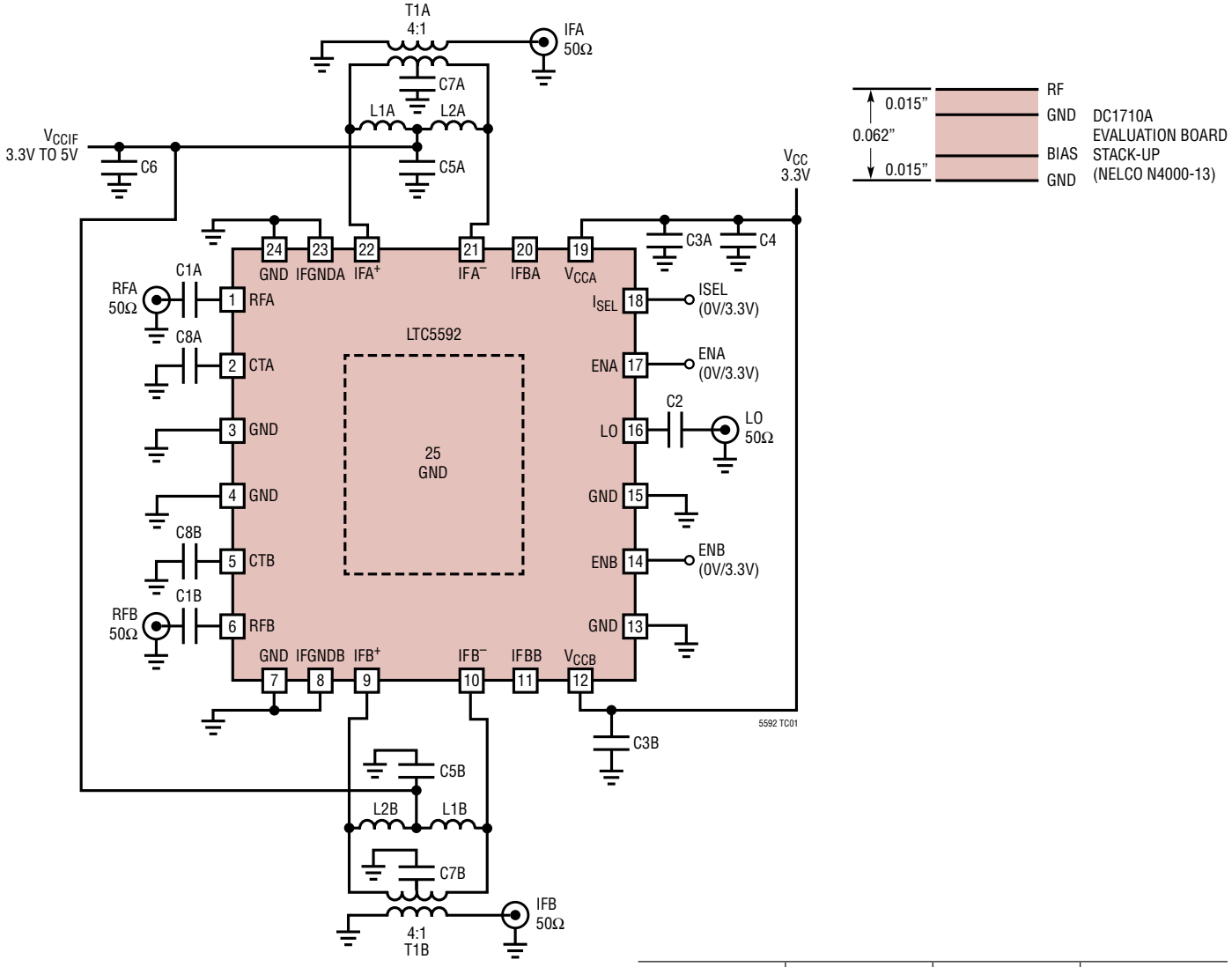
**LO (Pin 16):** Single-Ended Local Oscillator Input. This pin is internally connected to the primary side of the LO input transformer and has a low DC resistance to ground. **Series DC-blocking capacitors should be used to avoid damage to the integrated transformer when DC voltage present at LO input.** The LO input is internally matched to 50Ω for all states of ENA and ENB.

**$I_{SEL}$ (Pin 18):** Low Power Select Pin. When this pin is pulled low (<0.3V), both mixer channels are biased at the normal current level for best RF performance. When greater than 2.5V is applied, both channels operate at reduced current, which provides reasonable performance at lower power consumption. This pin must not be allowed to float.

## BLOCK DIAGRAM



## TEST CIRCUIT




| L1, L2 vs IF FREQUENCIES | |
|---|---|
| **IF (MHz)** | **L1, L2 (nH)** |
| 140 | 270 |
| 190 | 150 |
| 240 | 100 |
| 300 | 56 |
| 380 | 33 |
| 450 | 22 |

| REF DES | VALUE | SIZE | VENDOR |
|---|---|---|---|
| C1A, C1B | 22pF | 0402 | AVX |
| C2 | 2.2pF | 0402 | AVX |
| C3A, C3B C5A, C5B | 22pF | 0402 | AVX |
| C4, C6 | 1µF | 0603 | AVX |
| C7A, C7B | 1000pF | 0402 | AVX |
| C8A, C8B | 4.7pF | 0402 | AVX |
| L1A, L1B L2A, L2B | 150nH | 0603 | Coilcraft |
| T1A, T1B | TC4-1W-7ALN+ | | Mini-Circuits |

**Figure 1. Standard Downmixer Test Circuit Schematic (190MHz IF)**

## APPLICATIONS INFORMATION

### Introduction

The LTC5592 consists of two identical mixer channels driven by a common LO input signal. Each high linearity mixer consists of a passive double-balanced mixer core, IF buffer amplifier, LO buffer amplifier and bias/enable circuits. See the Pin Functions and Block Diagram sections for a description of each pin. Each of the mixers can be shutdown independently to reduce power consumption and low current mode can be selected that allows a trade-off between performance and power consumption. The RF and LO inputs are single-ended and are internally matched to 50Ω. Low side or high side LO injection can be used. The IF outputs are differential. The evaluation circuit, shown in Figure 1, utilizes bandpass IF output matching and an IF transformer to realize a 50Ω single-ended IF output. The evaluation board layout is shown in Figure 2.

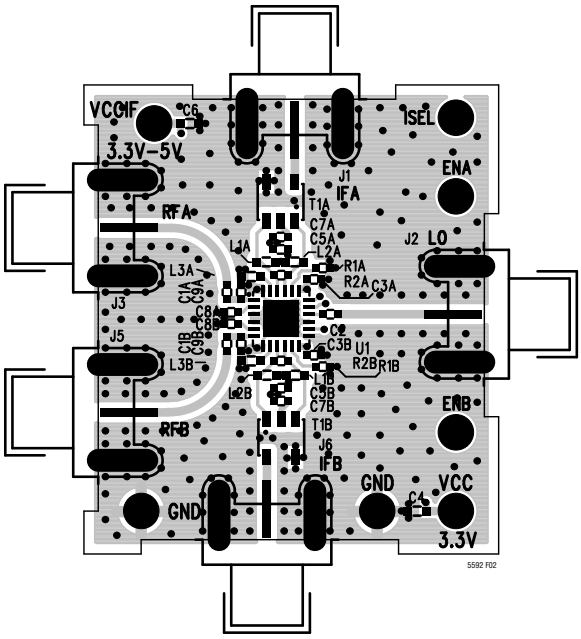



**Figure 2. Evaluation Board Layout (DC1710A)**

### RF Inputs

The RF inputs of channels A and B are identical. The RF input of channel A, shown in Figure 3, is connected to the primary winding of an integrated transformer. A 50Ω match is realized when a series external capacitor, C1A, is connected to the RF input. C1A is also needed for DC blocking if the source has DC voltage present, since the primary side of the RF transformer is internally DC-grounded. The DC resistance of the primary is approximately 3.9Ω.

The secondary winding of the RF transformer is internally connected to the channel A passive mixer core. The center-tap of the transformer secondary is connected to Pin 2 (CTA) to allow the connection of bypass capacitor, C8A. The value of C8A can be adjusted to improve channel isolation at specific RF frequencies with minor impact to conversion gain, linearity and noise performance. When used, it should be located within 2mm of Pin 2 for proper high frequency decoupling. The nominal DC voltage on the CTA pin is 1.2V.

For the RF inputs to be properly matched, the appropriate LO signal must be applied to the LO input. A broadband input match is realized with C1A = 22pF. The measured input return loss is shown in Figure 4 for LO frequencies of 1.7GHz, 2.16GHz and 2.5GHz. As shown in Figure 4, the RF input impedance is dependent on LO frequency, although a single value of C1A is adequate to cover the 1.7GHz to 2.5GHz RF band.

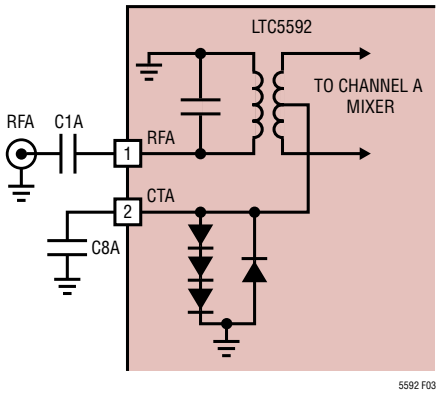



**Figure 3. Channel A RF Input Schematic**

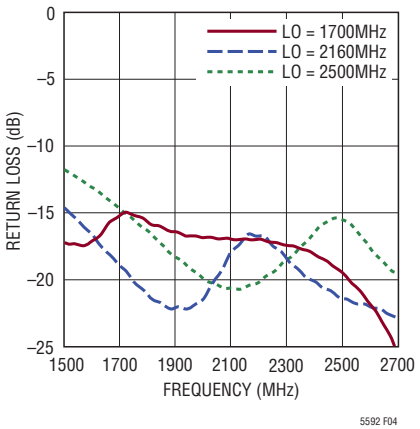



**Figure 4. RF Port Return Loss**

## APPLICATIONS INFORMATION

The RF input impedance and input reflection coefficient, versus RF frequency, are listed in Table 1. The reference plane for this data is Pin 1 of the IC, with no external matching, and the LO is driven at 2.16GHz.

**Table 1. RF Input Impedance and S11 (at Pin 1, No External Matching, $f_{LO}$ = 2.16GHz)**

| FREQUENCY (GHz) | RF INPUT IMPEDANCE | S11 | |
|---|---|---|---|
| | | MAG | ANGLE |
| 1.6 | 66.0 + j6.8 | 0.15 | 20 |
| 1.7 | 62.4 + j0.5 | 0.11 | 2 |
| 1.8 | 57.9 – j3.8 | 0.08 | –24 |
| 1.9 | 53.2 – j6.1 | 0.07 | –59 |
| 2.0 | 48.5 – j8.8 | 0.09 | –95 |
| 2.1 | 40.6 – j9.3 | 0.14 | –130 |
| 2.2 | 35.0 – j0.1 | 0.18 | –180 |
| 2.3 | 39.3 + j3.7 | 0.13 | –201 |
| 2.4 | 41.2 + j3.9 | 0.11 | –207 |
| 2.5 | 41.7 + j4.3 | 0.10 | –211 |
| 2.6 | 42.8 + j4.1 | 0.09 | –212 |
| 2.7 | 44.1 + j3.6 | 0.07 | –213 |

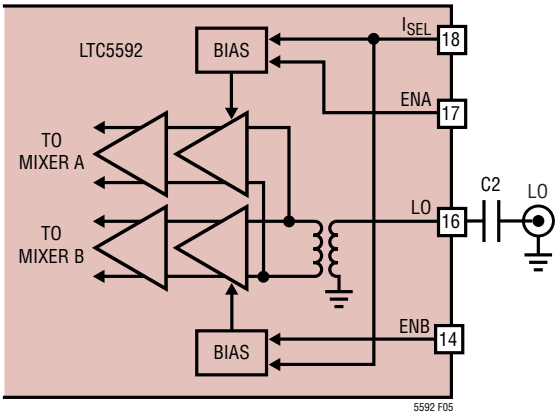



**Figure 5. LO Input Schematic**

### LO Input

The LO input, shown in Figure 5, is connected to the primary winding of an integrated transformer. A 50Ω impedance match is realized at the LO port by adding an external series capacitor, C2. This capacitor is also needed for DC blocking if the LO source has DC voltage present, since the primary side of the LO transformer is DC-grounded internally. The DC resistance of the primary is approximately 1.8Ω.

The secondary of the transformer drives a pair of high speed limiting differential amplifiers for channels A and B. The LTC5592's LO amplifiers are optimized for the 1.7GHz to 2.5GHz LO frequency range; however, LO frequencies outside this frequency range may be used with degraded performance.

The LO port is always 50Ω matched when $V_{CC}$ is applied, even when one or both of the channels is disabled. This helps to reduce frequency pulling of the LO source when the mixer is switched between different operating states. Figure 6 illustrates the LO port return loss for the different operating modes.

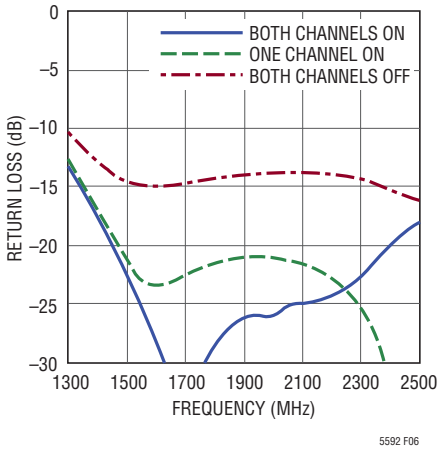



**Figure 6. LO Input Return Loss**

The nominal LO input level is 0dBm, though the limiting amplifiers will deliver excellent performance over a ±6dBm input power range. Table 2 lists the LO input impedance and input reflection coefficient versus frequency.

**Table 2. LO Input Impedance vs Frequency (at Pin 16, No External Matching, ENA = ENB = High)**

| FREQUENCY (GHz) | INPUT IMPEDANCE | S11 | |
|---|---|---|---|
| | | MAG | ANGLE |
| 1.7 | 46.4 + j34.4 | 0.34 | 76 |
| 1.8 | 47.0 + j31.0 | 0.31 | 78 |
| 1.9 | 46.5 + J28.2 | 0.28 | 81 |
| 2.0 | 44.4 + J26.8 | 0.28 | 86 |
| 2.1 | 43.1 + j26.0 | 0.28 | 89 |
| 2.2 | 41.8 + j26.2 | 0.29 | 91 |
| 2.3 | 40.4 + j27.4 | 0.31 | 92 |
| 2.4 | 38.8 + j28.5 | 0.33 | 94 |
| 2.5 | 38.0 + j30.4 | 0.35 | 93 |

## APPLICATIONS INFORMATION

### IF Outputs

The IF amplifiers in channels A and B are identical. The IF amplifier for channel A, shown in Figure 7, has differential open collector outputs (IFA+ and IFA–), a DC ground return pin (IFGNDA), and a pin for adjusting the internal bias (IFBA). The IF outputs must be biased at the supply voltage ($V_{CCIFA}$), which is applied through matching inductors L1A and L2A. Alternatively, the IF outputs can be biased through the center tap of a transformer (T1A). The common node of L1A and L2A can be connected to the center tap of the transformer. Each IF output pin draws approximately 50.5mA of DC supply current (101mA total). An external load resistor, R2A, can be used to improve impedance matching if desired.

IFGNDA (Pin 23) must be grounded or the amplifier will not draw DC current. Inductor L3A may improve LO-IF and RF-IF leakage performance in some applications, but is otherwise not necessary. Inductors should have small resistance for DC. High DC resistance in L3A will reduce the IF amplifier supply current, which will degrade RF performance.

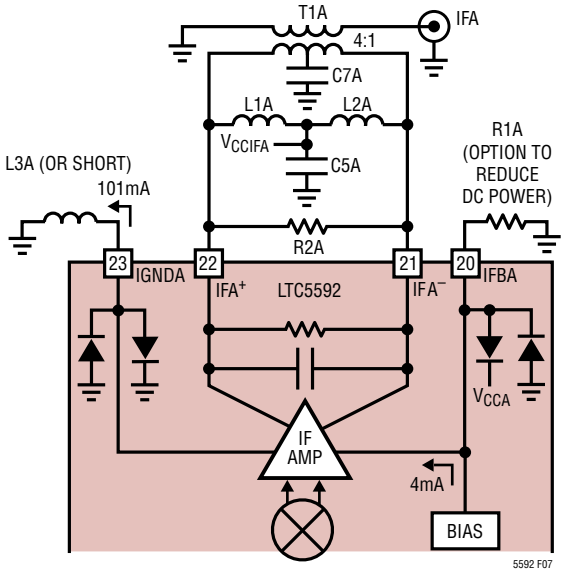



**Figure 7. IF Amplifier Schematic with Bandpass Match**

For optimum single-ended performance, the differential IF output must be combined through an external IF transformer or a discrete IF balun circuit. The evaluation board (see Figures 1 and 2) uses a 4:1 IF transformer for impedance transformation and differential to single-ended conversion. It is also possible to eliminate the IF transformer and drive differential filters or amplifiers directly.

The IF output impedance can be modeled as 379Ω in parallel with 2.2pF. The equivalent small-signal model, including bondwire inductance, is shown in Figure 8. Frequency-dependent differential IF output impedance is listed in Table 3. This data is referenced to the package pins (with no external components) and includes the effects of IC and package parasitics.

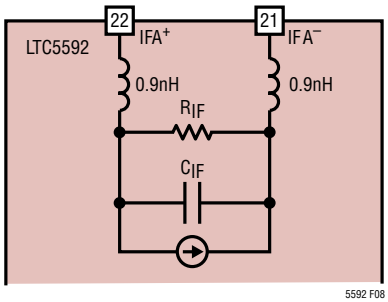



**Figure 8. IF Output Small-Signal Model**

### Bandpass IF Matching

The bandpass IF matching configuration, shown in Figures 1 and 7, is best suited for IF frequencies in the 90MHz to 500MHz range. Resistor R2A may be used to reduce the IF output resistance for greater bandwidth and inductors L1A and L2A resonate with the internal IF output capacitance at the desired IF frequency. The value of L1A, L2A can be estimated as follows:

$$L1A = L2A = \frac{1}{\left[\left(2\pi f_{IF}\right)^2 \bullet 2 \bullet C_{IF}\right]}$$

where $C_{IF}$ is the internal IF capacitance (listed in Table 3).

## APPLICATIONS INFORMATION

Values of L1A and L2A are tabulated in Figure 1 for various IF frequencies. The measured IF output return loss for bandpass IF matching is plotted in Figure 9.

**Table 3. IF Output Impedance vs Frequency**

| FREQUENCY (MHz) | DIFFERENTIAL OUTPUT IMPEDANCE ($R_{IF}$ \|\| $X_{IF}$ ($C_{IF}$)) |
|---|---|
| 90 | 403 \|\| – j610 (2.9pF) |
| 140 | 384 \|\| – j474 (2.4pF) |
| 190 | 379 \|\| – j381 (2.2pF) |
| 240 | 380 \|\| – j316 (2.1pF) |
| 300 | 377 \|\| – j253 (2.1pF) |
| 380 | 376 \|\| – j210 (2.0pF) |
| 450 | 360 \|\| – j177 (2.0pF) |

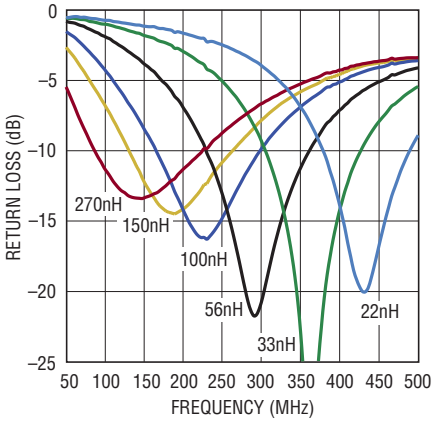



**Figure 9. IF Output Return Loss with Bandpass Matching**

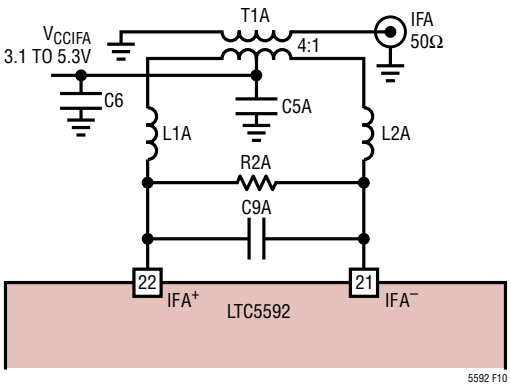



**Figure 10. IF Output with Lowpass Matching**

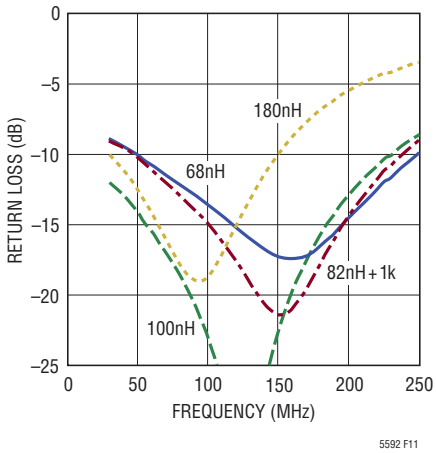



**Figure 11. IF Output Return Loss with Lowpass Matching**

### Lowpass IF Matching

For IF frequencies below 90MHz, the inductance values become unreasonably high and the lowpass topology shown in Figure 10 is preferred. This topology also can provide improved RF to IF and LO to IF isolation. $V_{CCIFA}$ is supplied through the center tap of the 4:1 transformer. A lowpass impedance transformation is realized by shunt elements R2A and C9A (in parallel with the internal RIF and CIF), and series inductors L1A and L2A. Resistor R2A is used to reduce the IF output resistance for greater bandwidth, or it can be omitted for the highest conversion gain. The final impedance transformation to 50Ω is realized by transformer T1A. The measured return loss is shown in Figure 11 for different values of inductance (C9A = open). The case with 82nH inductors and a 1k load resistor (R2A) is also shown. The LTC5592 demo board (see Figure 2) has been laid out to accommodate this matching topology with only minor modifications.

### IF Amplifier Bias

The IF amplifier delivers excellent performance with $V_{CCIF}$ = 3.3V, which allows a single supply to be used for $V_{CC}$ and $V_{CCIF}$. At $V_{CCIF}$ = 3.3V, the RF input P1dB of the mixer is limited by the output voltage swing. For higher P1dB, in this case, resistor R2A (Figure 7) can be used to reduce the output impedance and thus the voltage swing, thus improving P1dB. The trade-off for improved P1dB will be lower conversion gain.

With $V_{CCIF}$ increased to 5V the P1dB increases by over 3dB, at the expense of higher power consumption. Mixer P1dB performance at 1950MHz and 2350MHz is tabulated in Table 4 for $V_{CCIF}$ values of 3.3V and 5V. For the highest conversion gain, high-Q wire-wound chip inductors are recommended for L1A and L2A. Low cost multilayer chip inductors may be substituted, with a slight reduction in conversion gain.

## APPLICATIONS INFORMATION

**Table 4. Performance Comparison with $V_{CCIF}$ = 3.3V and 5V**

**(RF = 1950MHz, High Side LO, IF = 190MHz)**

| $V_{CCIF}$ (V) | R2A (Ω) | $I_{CCIF}$ (mA) | $G_C$ (dB) | P1dB (dBm) | IIP3 (dBm) | NF (dB) |
|---|---|---|---|---|---|---|
| 3.3 | Open | 202 | 8.7 | 10.6 | 25.4 | 9.8 |
| | 1k | 202 | 7.5 | 11.3 | 25.4 | 9.9 |
| 5 | Open | 209 | 8.7 | 14.0 | 25.5 | 9.9 |

**(RF = 2350MHz, Low Side LO, IF = 190MHz)**

| $V_{CCIF}$ (V) | R2A (Ω) | $I_{CCIF}$ (mA) | $G_C$ (dB) | P1dB (dBm) | IIP3 (dBm) | NF (dB) |
|---|---|---|---|---|---|---|
| 3.3 | Open | 202 | 8.3 | 11.0 | 27.3 | 9.8 |
| | 1k | 202 | 7.1 | 11.8 | 27.5 | 9.8 |
| 5 | Open | 209 | 8.1 | 14.6 | 28.0 | 10.0 |

The IFBA pin (Pin 20) is available for reducing the DC current consumption of the IF amplifier, at the expense of IIP3. The nominal DC voltage at Pin 20 is 2.1V, and this pin should be left open-circuited for optimum performance. The internal bias circuit produces a 4mA reference for the IF amplifier, which causes the amplifier to draw approximately 101mA. If resistor R1A is connected to Pin 20 as shown in Figure 7, a portion of the reference current can be shunted to ground, resulting in reduced IF amplifier current. For example, R1A = 1k will shunt away 1.5mA from Pin 20 and the IF amplifier current will be reduced by 25% to approximately 75.5mA. Table 5 summarizes RF performance versus IF amplifier current.

**Table 5. Mixer Performance with Reduced IF Amplifier Current**

**RF = 1950MHz, High Side LO, IF = 190MHz, $V_{CC}$ = $V_{CCIF}$ = 3.3V**

| R1 | $I_{CCIF}$ (mA) | $G_C$ (dB) | IIP3 (dBm) | P1dB (dBm) | NF (dB) |
|---|---|---|---|---|---|
| Open | 202 | 8.7 | 25.4 | 10.6 | 9.8 |
| 4.7kΩ | 184 | 8.5 | 25.2 | 10.8 | 9.8 |
| 2.2kΩ | 170 | 8.4 | 24.8 | 10.9 | 9.7 |
| 1kΩ | 151 | 8.1 | 24.4 | 11.1 | 9.8 |

**RF = 2350MHz, Low Side LO, IF = 190MHz, $V_{CC}$ = $V_{CCIF}$ = 3.3V**

| R1 | $I_{CCIF}$ (mA) | $G_C$ (dB) | IIP3 (dBm) | P1dB (dBm) | NF (dB) |
|---|---|---|---|---|---|
| Open | 202 | 8.3 | 27.3 | 11.0 | 9.8 |
| 4.7kΩ | 184 | 8.1 | 26.8 | 11.2 | 9.8 |
| 2.2kΩ | 170 | 8.0 | 26.2 | 11.2 | 9.8 |
| 1kΩ | 151 | 7.7 | 25.4 | 11.3 | 9.8 |

### Low Power Mode

Both mixer channels can be set to low power mode using the $I_{SEL}$ pin. This allows flexibility to select a reduced current mode of operation when lower RF performance is acceptable, reducing power consumption by 37%. Figure 12 shows a simplified schematic of the $I_{SEL}$ pin interface. When $I_{SEL}$ is set low (<0.3V), both channels operate at nominal DC current. When $I_{SEL}$ is set high (>2.5V), the DC current in both channels is reduced, thus reducing power consumption. The performance in low power mode and normal power mode are compared in Table 6.

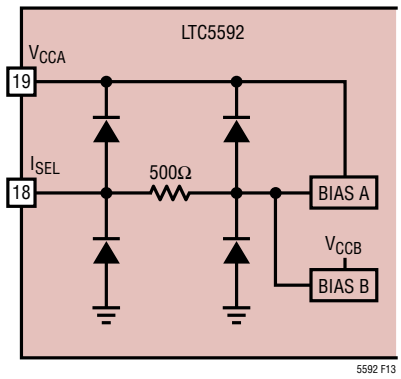



**Figure 12. $I_{SEL}$ Interface Schematic**

**Table 6. Performance Comparison Between Different Power Modes**

**RF = 1950MHz, High Side LO, IF = 190MHz, $V_{CC}$ = $V_{CCIF}$ = 3.3V**

| $I_{SEL}$ | $I_{TOTAL}$ (mA) | $G_C$ (dB) | IIP3 (dBm) | P1dB (dBm) | NF (dB) |
|---|---|---|---|---|---|
| Low | 401 | 8.7 | 25.4 | 10.6 | 9.8 |
| High | 252 | 7.4 | 21.2 | 10.9 | 10.2 |

**RF = 2350MHz, Low Side LO, IF = 190MHz, $V_{CC}$ = $V_{CCIF}$ = 3.3V**

| $I_{SEL}$ | $I_{TOTAL}$ (mA) | $G_C$ (dB) | IIP3 (dBm) | P1dB (dBm) | NF (dB) |
|---|---|---|---|---|---|
| Low | 401 | 8.3 | 27.3 | 11.0 | 9.8 |
| High | 252 | 7.1 | 22.3 | 11.3 | 10.2 |

# APPLICATIONS INFORMATION

## Enable Interface

Figure 13 shows a simplified schematic of the ENA pin interface (ENB is identical). To enable channel A, the ENA voltage must be greater than 2.5V. If the enable function is not required, the enable pin can be connected directly to $V_{CC}$. The voltage at the enable pin should never exceed the power supply voltage ($V_{CC}$) by more than 0.3V. If this should occur, the supply current could be sourced through the ESD diode, potentially damaging the IC.

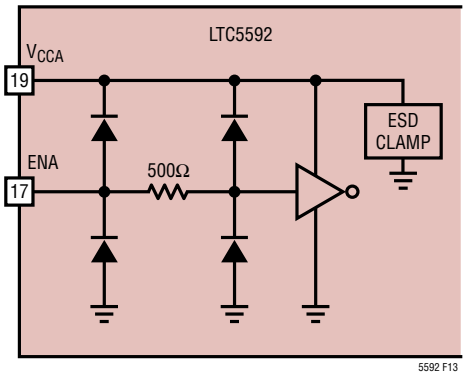



**Figure 13. ENA Interface Schematic**

The Enable pins must be pulled high or low. If left floating, the on/off state of the IC will be indeterminate. If a three-state condition can exist at the enable pins, then a pull-up or pull-down resistor must be used.

## Supply Voltage Ramping

Fast ramping of the supply voltage can cause a current glitch in the internal ESD protection circuits. Depending on the supply inductance, this could result in a supply voltage transient that exceeds the maximum rating. A supply voltage ramp time of greater than 1ms is recommended.

## Spurious Output Levels

Mixer spurious output levels versus harmonics of the RF and LO are tabulated in Tables 7 and 8 for frequencies up to 10GHz. The spur levels were measured on a standard evalution board using the test circuit shown in Figure 1. The spur frequencies can be calculated using the following equation:

$$f_{SPUR} = (M \bullet f_{RF}) - (N \bullet f_{LO})$$

**Table 7. IF Output Spur Levels (dBc), High Side LO**

**(RF = 1950MHz, $P_{RF}$ = –3dBm, $P_{LO}$ = 0dBm, $V_{CC}$ = $V_{CCIF}$ = 3.3V, $T_C$ = 25°C)**

| | | N | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| M | 0 | – | –45.2 | –46.9 | –68.4 | –70.8 | –75.3 | –72.0 | –82.0 | | |
| | 1 | –51.0 | 0 | –64.4 | –54.5 | –68.1 | –66.3 | –74.9 | –72.2 | | |
| | 2 | –80.0 | –80.9 | –60.6 | * | –81.4 | * | * | * | * | |
| | 3 | * | –83.5 | * | –75.8 | * | * | * | * | * | * |
| | 4 | * | * | * | * | * | * | * | * | * | * |
| | 5 | * | * | * | * | * | * | * | * | * | * |
| | 6 | * | * | * | * | * | * | * | * | * | * |
| | 7 | * | * | * | * | * | * | * | * | * | * |
| | 8 | | * | * | * | * | * | * | * | * | * |
| | 9 | | | * | * | * | * | * | * | * | * |
| | 10 | | | | * | * | * | * | * | * | * |

*Less than –90dBc

**Table 8. IF Output Spur Levels (dBc), Low Side LO**

**(RF = 2350MHz, $P_{RF}$ = –3dBm, $P_{LO}$ = 0dBm, $V_{CC}$ = $V_{CCIF}$ = 3.3V, $T_C$ = 25°C)**

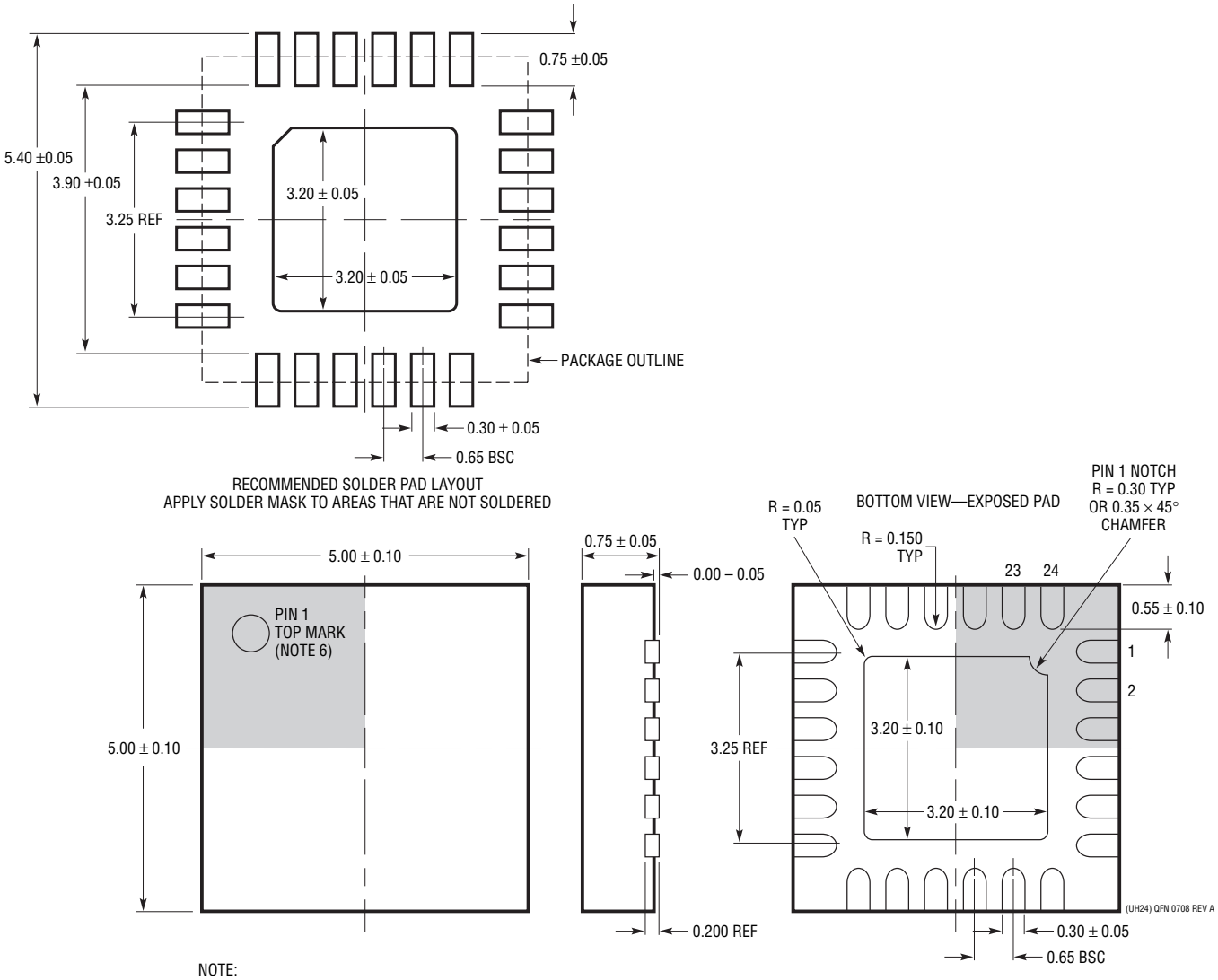
| | | N | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| M | 0 | – | –44.9 | –46.2 | –69.9 | –69.7 | –78.0 | –71.9 | | | |
| | 1 | –50.7 | 0 | –63.1 | –45.7 | –67.0 | –68.9 | –71.1 | –72.2 | * | |
| | 2 | –77.8 | –78.7 | –66.5 | * | –89.1 | * | * | * | * | * |
| | 3 | * | * | * | –70.1 | * | * | * | * | * | * |
| | 4 | * | * | * | * | * | * | * | * | * | * |
| | 5 | * | * | * | * | * | * | * | * | * | * |
| | 6 | * | * | * | * | * | * | * | * | * | * |
| | 7 | | * | * | * | * | * | * | * | * | * |
| | 8 | | | * | * | * | * | * | * | * | * |
| | 9 | | | | * | * | * | * | * | * | * |
| | 10 | | | | | * | * | * | * | * | * |

*Less than –90dBc

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**UH Package**
**24-Lead Plastic QFN (5mm × 5mm)**
(Reference LTC DWG # 05-08-1747 Rev A)




NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 08/13 | Changed LO lower frequency range from 1.7GHz to 1.5GHz. | 1 |
| | | LO Input Frequency Range: changed lower frequency from 1700MHz to 1500MHz. | 3 |
| | | RF Input Frequency Range, Low Side LO: changed lower frequency from 1900MHz to 1600MHz. | 3 |
| | | Updated “Conversion Gain and IIP3 vs RF Frequency” and “SSB NF vs RF Frequency” plots to include 1500MHz frequency characteristics. | 5 |
| | | Updated “LO Leakage vs LO Frequency” plot to include 1500MHz frequency characteristics. | 6 |
| | | Updated “Conversion Gain and IIP3 vs RF Frequency” and “SSB NF vs RF Frequency” plots to include 1500MHz frequency characteristics. | 7 |
| | | Pin Functions section RFA, RFB (Pins 1, 6): Changed LO input source lower frequency from 1.7GHz to 1.5GHz. | 9 |
| | | Right column, last paragraph. Deleted sentence: “These LO frequencies correspond to lower, middle and upper values in the LO range.” | 12 |
| | | Figure 6, updated the LO Input Return Loss plot to include 1300MHz frequency characteristics. | 13 |

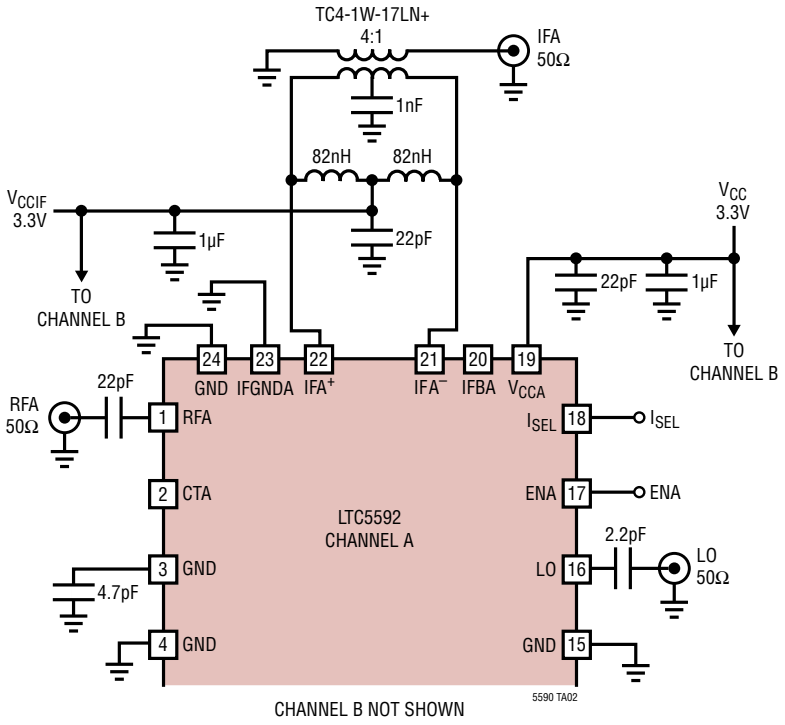


LINEAR TECHNOLOGY

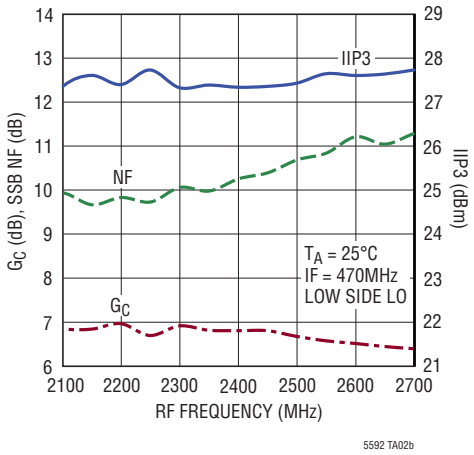
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## TYPICAL APPLICATION

**Downconverting Mixer with 470MHz IF**




**Conversion Gain, NF and IIP3 vs RF Frequency**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| **Infrastructure** | | |
| LTC5569 | 300MHz to 4GHz, 3.3V Dual Active Downconverting Mixer | 2dB Gain, 26.7dBm IIP3 and 11.7dB NF at 1950MHz, 3.3V/180mA Supply |
| LT5557 | 400MHz to 3.8GHz, 3.3V Downconverting Mixer | 2.9dB Gain, 24.7dBm IIP3 and 11.7dB NF at 1950MHz, 3.3V/82mA Supply |
| LTC6416 | 2GHz 16-Bit ADC Buffer | 40.25dBm OIP3 to 300MHz, Programmable Fast Recovery Output Clamping |
| LTC6412 | 31dB Linear Analog VGA | 35dBm OIP3 at 240MHz, Continuous Gain Range –14dB to 17dB |
| LTC554x | 600MHz to 4GHz Downconverting Mixer Family | 8dB Gain, >25dBm IIP3, 10dB NF, 3.3V/200mA Supply |
| LT5554 | Ultralow Distort IF Digital VGA | 48dBm OIP3 at 200MHz, 2dB to 18dB Gain Range, 0.125dB Gain Steps |
| LT5578 | 400MHz to 2.7GHz Upconverting Mixer | 27dBm OIP3 at 900MHz, 24.2dBm at 1.95GHz, Integrated RF Transformer |
| LT5579 | 1.5GHz to 3.8GHz Upconverting Mixer | 27.3dBm OIP3 at 2.14GHz, NF = 9.9dB, 3.3V Supply, Single-Ended LO and RF Ports |
| **RF Power Detectors** | | |
| LT5581 | 6GHz Low Power RMS Detector | 40dB Dynamic Range, ±1dB Accuracy Over Temperature, 1.5mA Supply Current |
| LTC5582 | 10GHz RMS Power Detector | 40MHz to 10GHz, Up to 57dB Dynamic Range, ±0.5dB Accuracy Over Temperature |
| LTC5583 | Dual 6GHz RMS Power Detector | 40MHz to 6GHz, Up to 60dB Dynamic Range, >40dB Channel-to-Channel Isolation |
| **ADCs** | | |
| LTC2285 | 14-Bit, 125Msps Dual ADC | 72.4dB SNR, >88dB SFDR, 790mW Power Consumption |
| LTC2185 | 16-Bit, 125Msps Dual ADC Ultralow Power | 74.8dB SNR, 185mW/Channel Power Consumption |
| LTC2242-12 | 12-Bit, 250Msps ADC | 65.4dB SNR, 78dB SFDR, 740mW Power Consumption |


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LT 0813 REV A • PRINTED IN USA
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