65V, 2A Synchronous Step-Down Regulator with 2.5µA Quiescent Current

FEATURES

- **Wide Input Voltage Range: 3.4V to 65V**
- **Ultralow Quiescent Current Burst Mode® Operation:**
  - **2.5µA I_Q Regulating 12V_{IN} to 3.3V_{OUT}**
  - **Output Ripple < 10mV_{P-P}**
- **High Efficiency Synchronous Operation:**
  - **94% Efficiency at 1A, 12V_{IN} to 5V_{OUT}**
  - **92% Efficiency at 1A, 12V_{IN} to 3.3V_{OUT}**
- **Fast 30ns Minimum Switch-On Time**
- **Low Dropout Under All Conditions: 250mV at 1A**
- **Safely Tolerates Inductor Saturation in Overload**
- Low EMI
- Adjustable and Synchronizable: 200kHz to 2.2MHz
- Accurate 1V Enable Pin Threshold
- Internal Compensation
- Output Soft-Start and Tracking
- Small Thermally Enhanced 16-Lead MSOP and 24-Lead 3mm × 5mm QFN Packages

APPLICATIONS

- Automotive and Industrial Supplies
- General Purpose Step-Down
- GSM Power Supplies

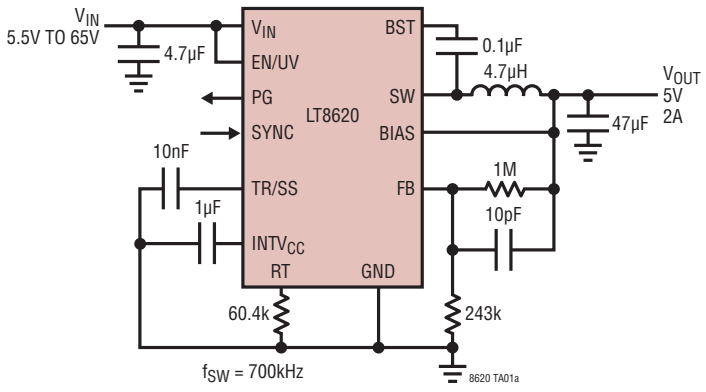
DESCRIPTION

The LT®8620 is a compact, high efficiency, high speed synchronous monolithic step-down switching regulator that accepts a wide input voltage range up to 65V, and consumes only 2.5µA of quiescent current. Top and bottom power switches are included with all necessary circuitry to minimize the need for external components. Low ripple Burst Mode operation enables high efficiency down to very low output currents while keeping the output ripple below 10mV_{P-P}. A SYNC pin allows synchronization to an external clock. Internal compensation with peak current mode topology allows the use of small inductors and results in fast transient response and good loop stability. The EN/UV pin has an accurate 1V threshold and can be used to program V_{IN} undervoltage lockout or to shut down the LT8620 reducing the input supply current to 1µA. A capacitor on the TR/SS pin programs the output voltage ramp rate during start-up. The PG flag signals when V_{OUT} is within ±9% of the programmed output voltage as well as fault conditions. The LT8620 is available in small 16-Lead MSOP and 3mm × 5mm QFN packages with exposed pads for low thermal resistance.

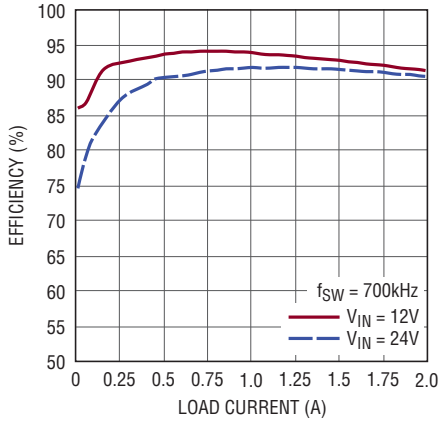
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TYPICAL APPLICATION

5V 2A Step-Down Converter



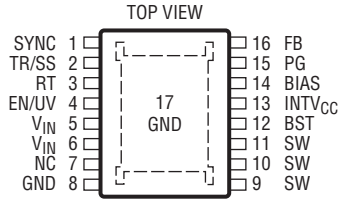
Efficiency at 5V_{OUT}



ABSOLUTE MAXIMUM RATINGS (Note 1)

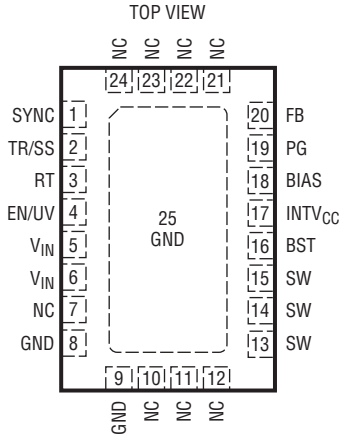
V_{IN}, EN/UV 65V
PG.....42V
BIAS.....25V
BST Pin Above SW Pin.....4V
FB, TR/SS, RT, $INTV_{CC}$ 4V
SYNC Voltage 6V
Operating Junction Temperature Range (Note 2)
LT8620E ..... –40°C to 125°C
LT8620I ..... –40°C to 125°C
LT8620H ..... –40°C to 150°C
LT8620MP ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



MSE PACKAGE
16-LEAD PLASTIC MSOP

θ_{JA} = 40°C/W, $\theta_{JC(PAD)}$ = 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB



UDD PACKAGE
24-LEAD (3mm × 5mm) PLASTIC QFN

θ_{JA} = 46°C/W, $\theta_{JC(PAD)}$ = 5°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8620EMSE#PBF	LT8620EMSE#TRPBF	8620	16-Lead Plastic MSOP	–40°C to 125°C
LT8620IMSE#PBF	LT8620IMSE#TRPBF	8620	16-Lead Plastic MSOP	–40°C to 125°C
LT8620HMSE#PBF	LT8620HMSE#TRPBF	8620	16-Lead Plastic MSOP	–40°C to 150°C
LT8620MPMSE#PBF	LT8620MPMSE#TRPBF	8620	16-Lead Plastic MSOP	–55°C to 150°C
LT8620EUDD#PBF	LT8620EUDD#TRPBF	LGGV	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 125°C
LT8620IUDD#PBF	LT8620IUDD#TRPBF	LGGV	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●		2.9	3.4	V
V_{IN} Quiescent Current	$V_{EN/UV}$ = 0V, V_{SYNC} = 0V	 ●		1.0 1.0	3 8	µA µA
	$V_{EN/UV}$ = 2V, Not Switching, V_{SYNC} = 0V	 ●		1.7 1.7	4 10	µA µA
	$V_{EN/UV}$ = 2V, Not Switching, V_{SYNC} = 2V			0.28	0.5	mA
V_{IN} Current in Regulation	V_{OUT} = 0.97V, V_{IN} = 6V, Output Load = 100µA V_{OUT} = 0.97V, V_{IN} = 6V, Output Load = 1mA	● ●		20 200	50 350	µA µA
Feedback Reference Voltage	V_{IN} = 6V, I_{LOAD} = 0.5A V_{IN} = 6V, I_{LOAD} = 0.5A	 ●	0.964 0.958	0.970 0.970	0.976 0.982	V V
Feedback Voltage Line Regulation	V_{IN} = 4.0V to 42V, I_{LOAD} = 0.5A	●		0.004	0.02	%/V
Feedback Pin Input Current	V_{FB} = 1V		–20		20	nA
$INTV_{CC}$ Voltage	I_{LOAD} = 0mA, V_{BIAS} = 0V I_{LOAD} = 0mA, V_{BIAS} = 3.3V		3.23 3.25	3.4 3.29	3.57 3.35	V V
$INTV_{CC}$ Undervoltage Lockout			2.5	2.6	2.7	V
BIAS Pin Current Consumption	V_{BIAS} = 3.3V, I_{LOAD} = 1A, 2MHz			7.2		mA
Minimum On-Time	I_{LOAD} = 1A, SYNC = 0V I_{LOAD} = 1A, SYNC = 3.3V	● ●		30 30	45 45	ns ns
Minimum Off-Time				90	130	ns
Oscillator Frequency	R_T = 221k, I_{LOAD} = 1A R_T = 60.4k, I_{LOAD} = 1A R_T = 18.2k, I_{LOAD} = 1A	● ● ●	180 665 1.85	210 700 2.00	240 735 2.15	kHz kHz MHz
Top Power NMOS On-Resistance	I_{SW} = 1A			175		mΩ
Top Power NMOS Current Limit		●	2.8	4.1	4.9	A
Bottom Power NMOS On-Resistance	V_{INTVCC} = 3.4V, I_{SW} = 1A			85		mΩ
Bottom Power NMOS Current Limit	V_{INTVCC} = 3.4V		2.9	3.9	4.7	A
SW Leakage Current	V_{IN} = 42V, V_{SW} = 0V, 42V		–1.5		1.5	µA
EN/UV Pin Threshold	EN/UV Rising	●	0.94	1.0	1.06	V
EN/UV Pin Hysteresis				40		mV
EN/UV Pin Current	$V_{EN/UV}$ = 2V		–20		20	nA
PG Upper Threshold Offset from V_{FB}	V_{FB} Falling	●	6	9.0	12	%
PG Lower Threshold Offset from V_{FB}	V_{FB} Rising	●	–6	–9.0	–12	%
PG Hysteresis				1.3		%
PG Leakage	V_{PG} = 3.3V		–40		40	nA
PG Pull-Down Resistance	V_{PG} = 0.1V	●		680	2000	Ω
SYNC Threshold	SYNC Falling SYNC Rising		0.8 1.1	1.0 1.3	1.2 1.5	V V
SYNC Pin Current	V_{SYNC} = 6V		–100		100	nA
TR/SS Source Current		●	1.2	2	2.7	µA
TR/SS Pull-Down Resistance	Fault Condition, TR/SS = 0.1V			220		Ω

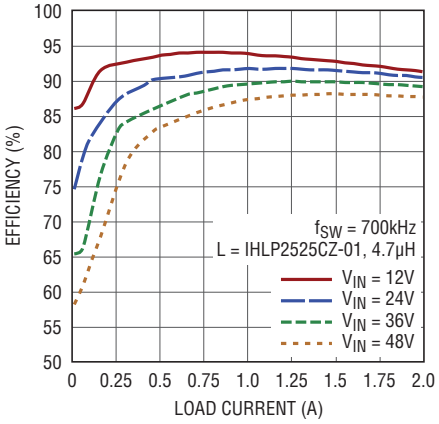
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8620E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LT8620I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT8620H is guaranteed over the full –40°C to 150°C operating junction temperature range. The LT8620MP is 100% tested and guaranteed over the full –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

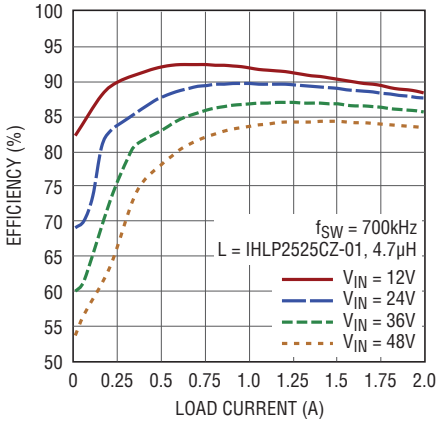
Note 3: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

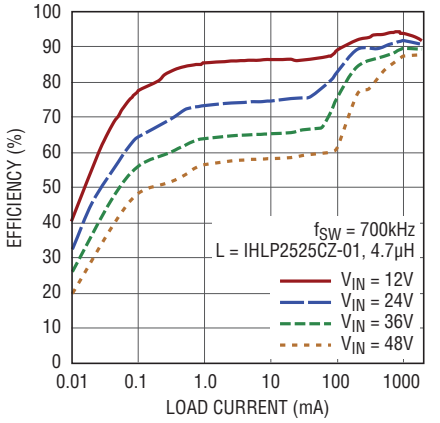
Efficiency at $5V_{OUT}$



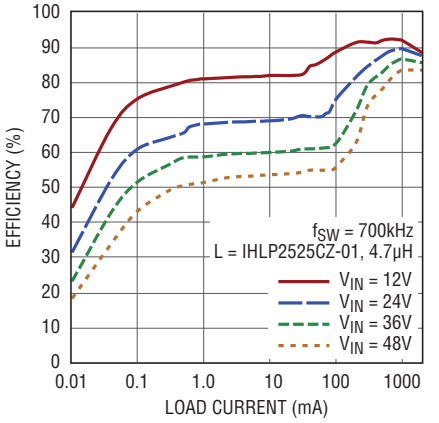
Efficiency at $3.3V_{OUT}$



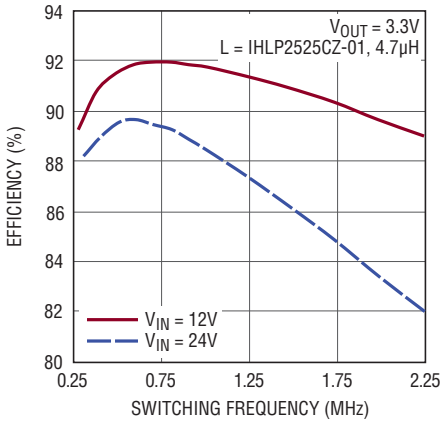
Efficiency at $5V_{OUT}$



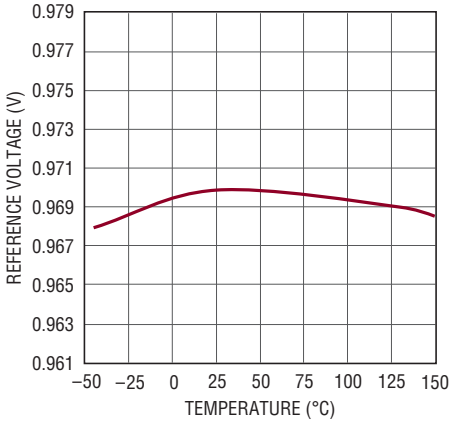
Efficiency at $3.3V_{OUT}$



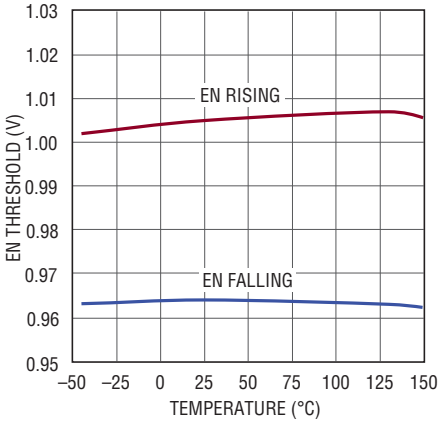
Efficiency vs Frequency at 1A



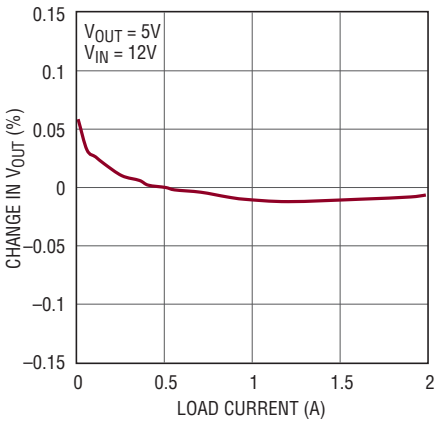
Reference Voltage



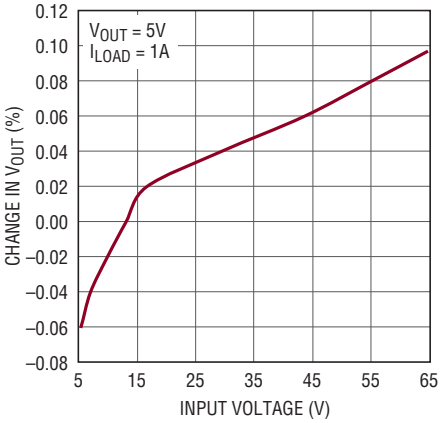
EN Pin Thresholds



Load Regulation

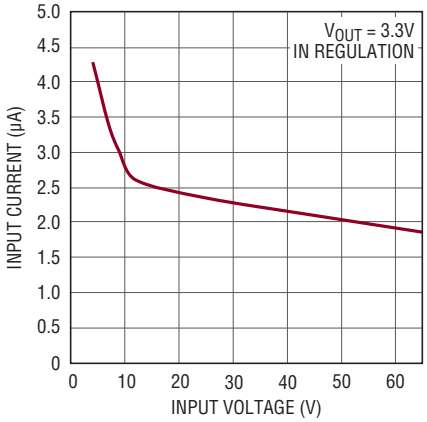


Line Regulation

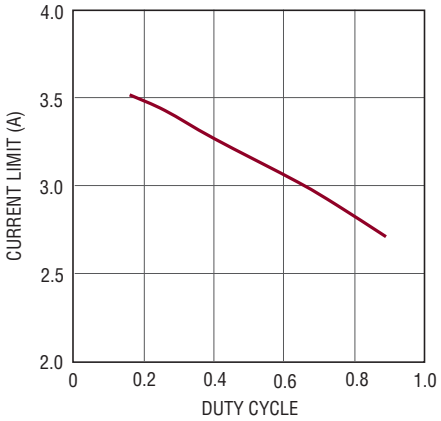


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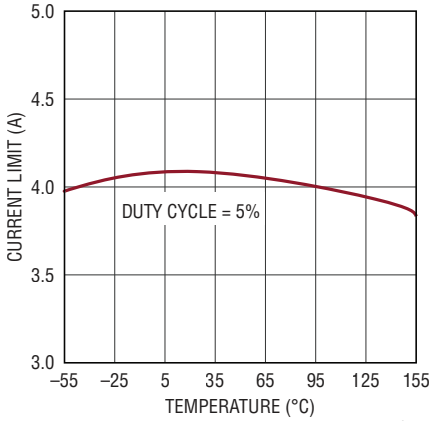
No Load Supply Current



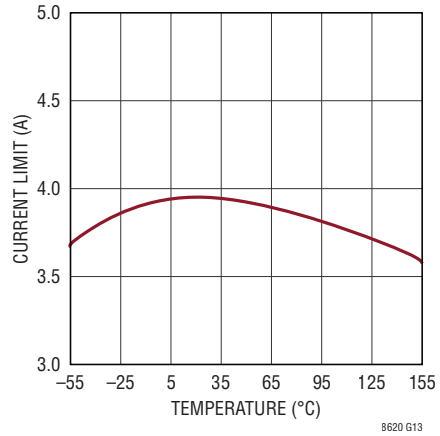
Top FET Current Limit vs Duty Cycle



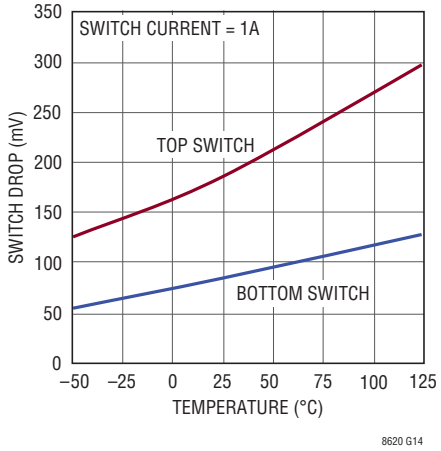
Top FET Current Limit



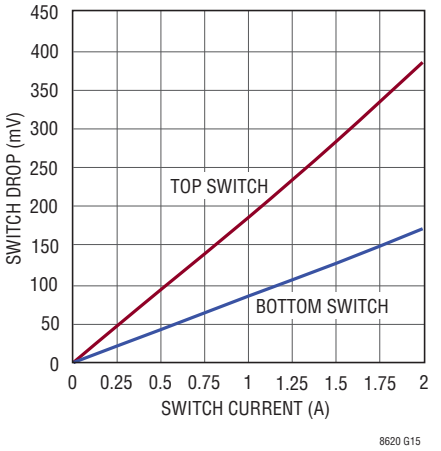
Bottom FET Current Limit



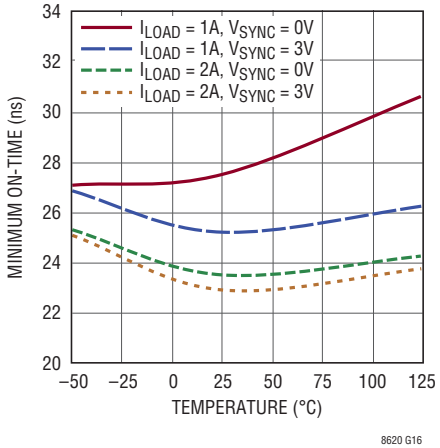
Switch Drop



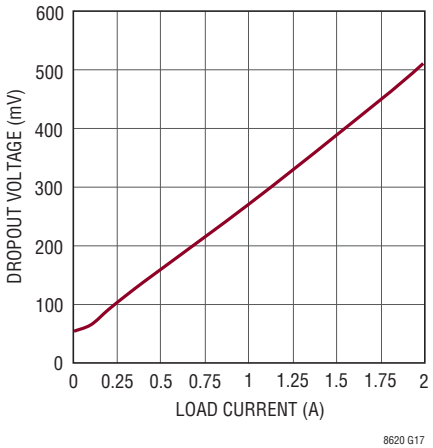
Switch Drop



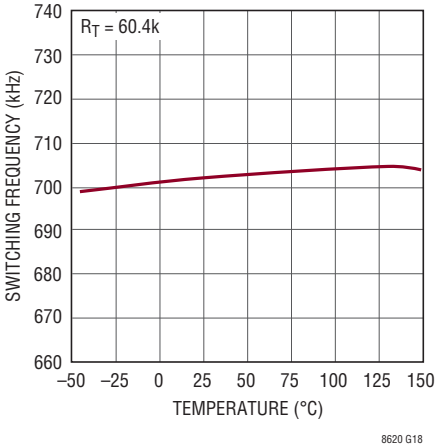
Minimum On-Time



Dropout Voltage

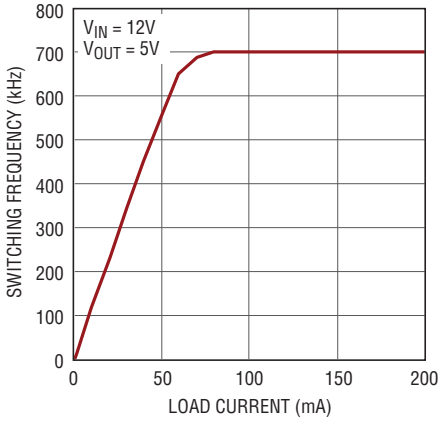


Switching Frequency



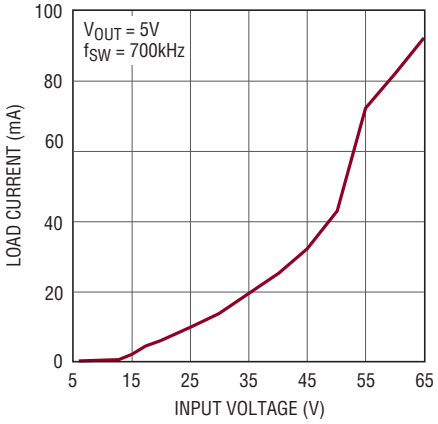
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Burst Frequency



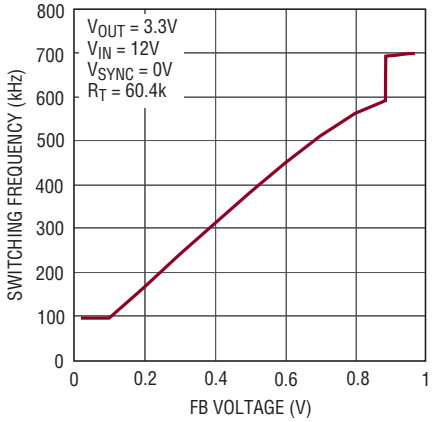
8620 G19

Minimum Load to Full Frequency (SYNC DC High)



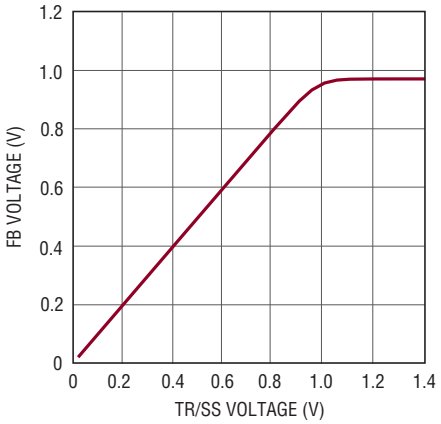
8620 G20

Frequency Foldback



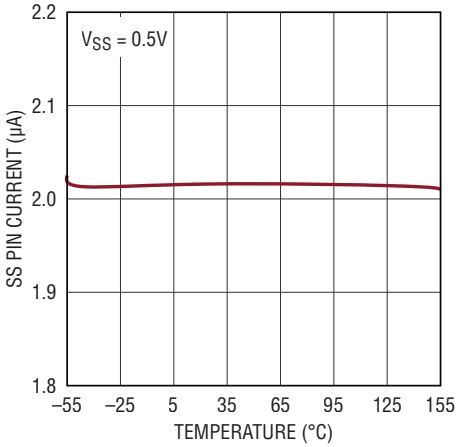
8620 G21

Soft-Start Tracking



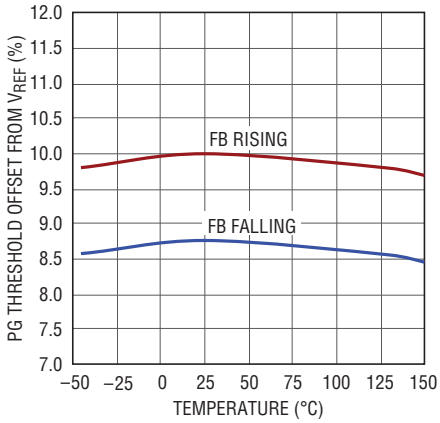
8620 G22

Soft-Start Current



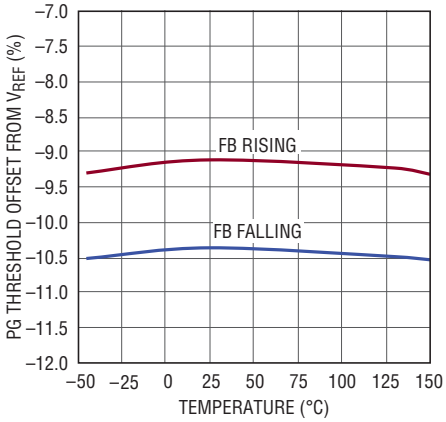
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PG High Thresholds



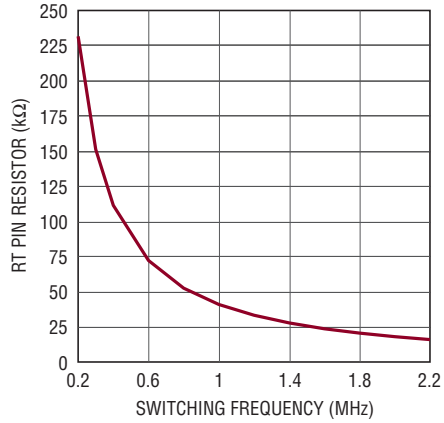
8620 G24

PG Low Thresholds



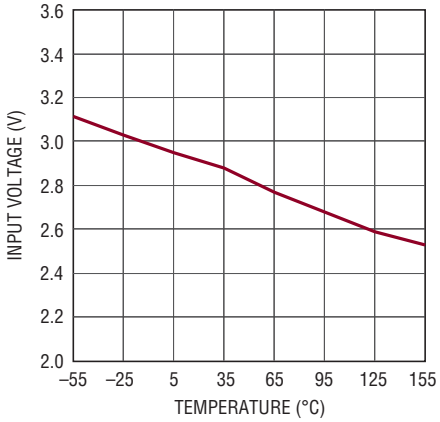
8620 G25

RT Programmed Switching Frequency



8620 G26

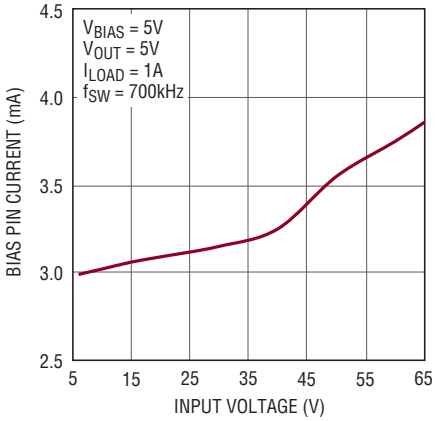
V_{IN} UVLO



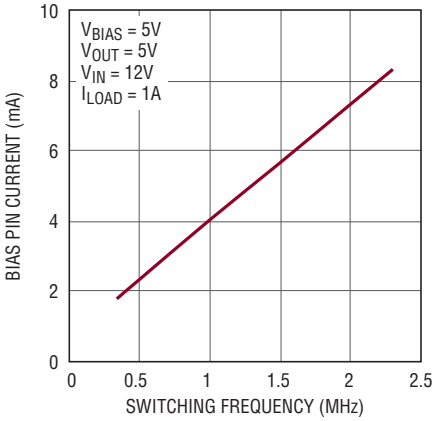
8620 G27

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

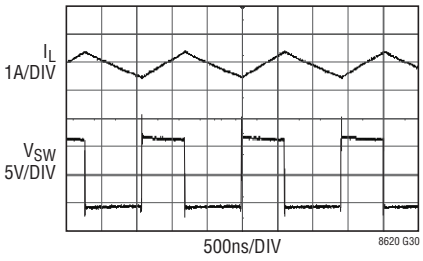
Bias Pin Current



Bias Pin Current

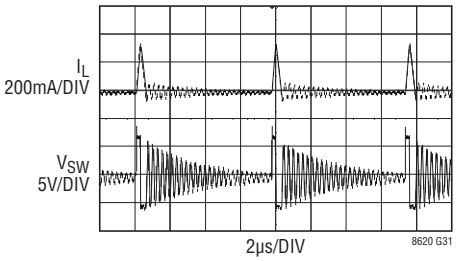


Switching Waveforms, Full Frequency Continuous Operation



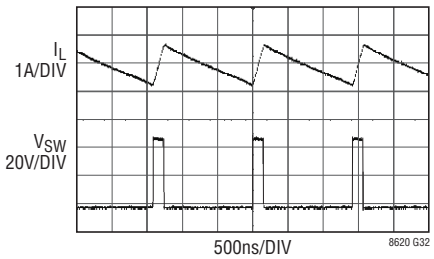
$12V_{IN}$ TO $5V_{OUT}$ AT 1A

Switching Waveforms, Burst Mode Operation



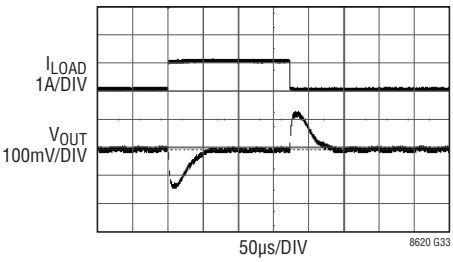
$12V_{IN}$ TO $5V_{OUT}$ AT 10mA
V_{SYNC} = 0V

Switching Waveforms



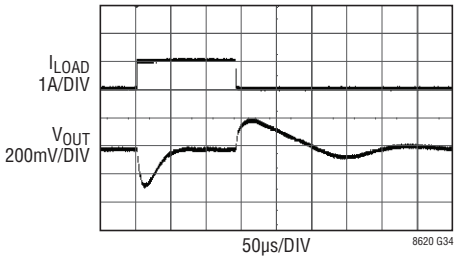
$48V_{IN}$ TO $5V_{OUT}$ AT 1A

Transient Response; Load Current Stepped from 1A to 2A



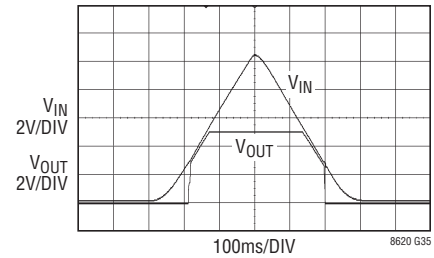
1A TO 2A TRANSIENT
$12V_{IN}$, $5V_{OUT}$
C_{OUT} = 47µF

Transient Response; Load Current Stepped from 50mA (Burst Mode Operation) to 1A



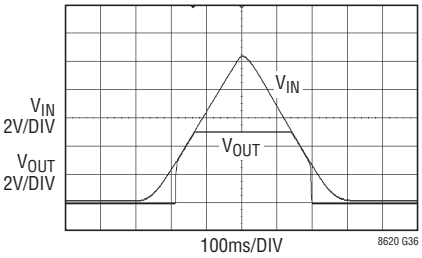
50mA (Burst Mode Operation) TO 1A TRANSIENT
$12V_{IN}$, $5V_{OUT}$
C_{OUT} = 47µF

Start-Up Dropout Performance



2.5Ω LOAD
(2A IN REGULATION)

Start-Up Dropout Performance



20Ω LOAD
(250mA IN REGULATION)

PIN FUNCTIONS

SYNC: External Clock Synchronization Input. Ground this pin for low ripple Burst Mode operation at low output loads. Tie to a clock source for synchronization to an external frequency. Apply a DC voltage of 3V or higher or tie to $INTV_{CC}$ for pulse-skipping mode. When in pulse-skipping mode, the I_Q will increase to several hundred µA. Do not float this pin.

TR/SS: Output Tracking and Soft-Start Pin. This pin allows user control of output voltage ramp rate during start-up. A TR/SS voltage below 0.97V forces the LT8620 to regulate the FB pin to equal the TR/SS pin voltage. When TR/SS is above 0.97V, the tracking function is disabled and the internal reference resumes control of the error amplifier. An internal 2µA pull-up current from $INTV_{CC}$ on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground with an internal 220Ω MOSFET during shutdown and fault conditions; use a series resistor if driving from a low impedance output. This pin may be left floating if the tracking function is not needed.

RT: A resistor is tied between RT and ground to set the switching frequency.

EN/UV: The LT8620 is shut down when this pin is low and active when this pin is high. The hysteretic threshold voltage is 1.00V going up and 0.96V going down. Tie to V_{IN} if the shutdown feature is not used. An external resistor divider from V_{IN} can be used to program a V_{IN} threshold below which the LT8620 will shut down.

V_{IN}: The V_{IN} pins supply current to the LT8620 internal circuitry and to the internal topside power switch. These pins must be tied together and be locally bypassed. Be sure to place the positive terminal of the input capacitor as close as possible to the V_{IN} pins, and the negative capacitor terminal as close as possible to the PGND pins.

NC: No Connect. This pin is not connected to internal circuitry.

SW: The SW pins are the outputs of the internal power switches. Tie these pins together and connect them to the inductor and boost capacitor. This node should be kept small on the PCB for good performance.

BST: This pin is used to provide a drive voltage, higher than the input voltage, to the topside power switch. Place a 0.1µF boost capacitor as close as possible to the IC.

$INTV_{CC}$: Internal 3.4V Regulator Bypass Pin. The internal power drivers and control circuits are powered from this voltage. $INTV_{CC}$ maximum output current is 20mA. Do not load the $INTV_{CC}$ pin with external circuitry. $INTV_{CC}$ current will be supplied from BIAS if V_{BIAS} > 3.1V, otherwise current will be drawn from V_{IN}. Voltage on $INTV_{CC}$ will vary between 2.8V and 3.4V when V_{BIAS} is between 3.0V and 3.6V. Decouple this pin to power ground with at least a 1µF low ESR ceramic capacitor placed close to the IC.

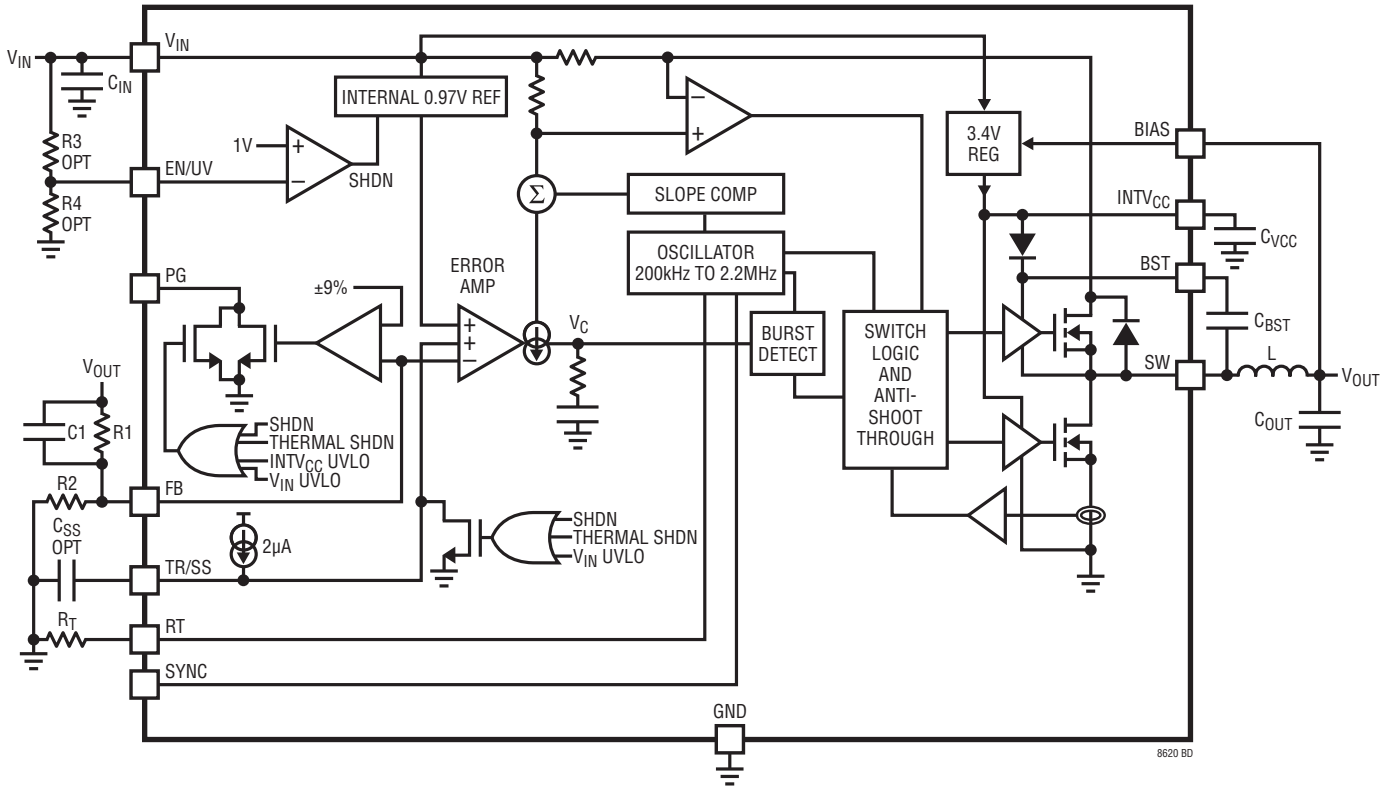
BIAS: The internal regulator will draw current from BIAS instead of V_{IN} when BIAS is tied to a voltage higher than 3.1V. For output voltages of 3.3V to 25V, this pin should be tied to V_{OUT}. If this pin is tied to a supply other than V_{OUT} use a 1µF local bypass capacitor on this pin. If no supply is available, tie to ground.

PG: The PG pin is the open-drain output of an internal comparator. PG remains low until the FB pin is within ±9% of the final regulation voltage, and there are no fault conditions. PG is valid when V_{IN} is above 3.4V, regardless of EN/UV pin state.

FB: The LT8620 regulates the FB pin to 0.970V. Connect the feedback resistor divider tap to this pin. Also, connect a phase lead capacitor between FB and V_{OUT}. Typically, this capacitor is 4.7pF to 10pF.

GND: Ground. The exposed pad must be connected to the negative terminal of the input capacitor and soldered to the PCB in order to lower the thermal resistance.

BLOCK DIAGRAM



OPERATION

The LT8620 is a monolithic, constant frequency, current mode step-down DC/DC converter. An oscillator, with frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the internal VC node. The error amplifier servos the VC node by comparing the voltage on the V_{FB} pin with an internal 0.97V reference. When the load current increases it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the VC voltage until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on until the next clock cycle begins or inductor current falls to zero. If overload conditions result in more than 3.9A flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

If the EN/UV pin is low, the LT8620 is shut down and draws 1µA from the input. When the EN/UV pin is above 1V, the switching regulator will become active.

To optimize efficiency at light loads, the LT8620 operates in Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 1.7µA. In a typical application, 2.5µA will be consumed from the input supply when regulating with no load. The SYNC pin is tied low to use Burst Mode operation and can be tied to a logic high to use pulse-skipping mode. If a clock is applied to the SYNC pin the part will synchronize to an external clock frequency and operate in pulse-skipping mode. While in pulse-skipping mode the oscillator operates continuously and positive SW transitions are aligned to the clock. During light loads, switch pulses are skipped to regulate the output and the quiescent current will be several hundred µA.

To improve efficiency across all loads, supply current to internal circuitry can be sourced from the BIAS pin when biased at 3.3V or above. Else, the internal circuitry will draw current from V_{IN}. The BIAS pin should be connected to V_{OUT} if the LT8620 output is programmed at 3.3V or above.

Comparators monitoring the FB pin voltage will pull the PG pin low if the output voltage varies more than ±9% (typical) from the set point, or if a fault condition is present.

The oscillator reduces the LT8620's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the inductor current when the output voltage is lower than the programmed value which occurs during start-up or overcurrent conditions. When a clock is applied to the SYNC pin or the SYNC pin is held DC high, the frequency foldback is disabled and the switching frequency will slow down only during overcurrent conditions.

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Achieving Ultralow Quiescent Current

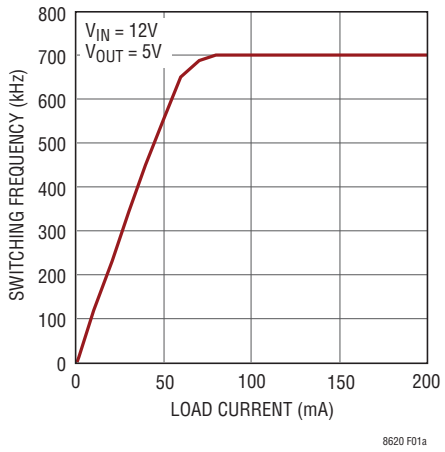
To enhance efficiency at light loads, the LT8620 operates in low ripple Burst Mode operation, which keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and minimizing output voltage ripple. In Burst Mode operation the LT8620 delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode the LT8620 consumes 1.7µA.

As the output load decreases, the frequency of single current pulses decreases (see Figure 1a) and the percentage of time the LT8620 is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. By maximizing the time between pulses, the converter quiescent current approaches 2.5µA for a typical application when there is no output load. Therefore, to optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current.

In order to achieve higher light load efficiency, more energy must be delivered to the output during the single small pulses in Burst Mode operation such that the LT8620 can stay in sleep mode longer between each pulse. This can be achieved by using a larger value inductor (i.e. 4.7µH), and should be considered independent of switching frequency when choosing an inductor. For example, while a lower inductor value would typically be used for a high switching frequency application, if high light load efficiency is desired, a higher inductor value should be chosen.

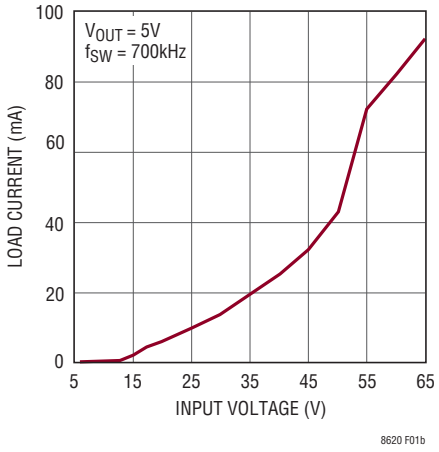
While in Burst Mode operation the current limit of the top switch is approximately 400mA resulting in output voltage ripple shown in Figure 2. Increasing the output capacitance will decrease the output ripple proportionally. As load ramps upward from zero the switching frequency will increase but only up to the switching frequency programmed by the resistor at the RT pin as shown in Figure 1a. The output load at which the LT8620 reaches the programmed frequency varies based on input voltage, output voltage, and inductor choice.

Burst Frequency



(1a)

Minimum Load to Full Frequency (SYNC DC High)



(1b)

Figure 1. SW Frequency vs Load Information in Burst Mode Operation (1a) and Pulse-Skipping Mode (1b)

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For some applications it is desirable for the LT8620 to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. First is the clock stays awake at all times and all switching cycles are aligned to the clock. In this mode much of the internal circuitry is awake at all times, increasing quiescent current to several hundred µA. Second is that full switching frequency is reached at lower output load than in Burst Mode operation (see Figure 1b). To enable pulse-skipping mode, the SYNC pin is tied high either to a logic output or to the $INTV_{CC}$ pin. When a clock is applied to the SYNC pin the LT8620 will also operate in pulse-skipping mode.

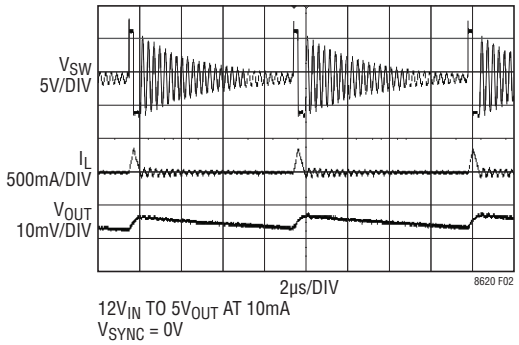


Figure 2. Burst Mode Operation

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to:

$$R1 = R2\left(\frac{V_{OUT}}{0.970V} - 1\right) \quad (1)$$

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

If low input quiescent current and good light-load efficiency are desired, use large resistor values for the FB resistor divider. The current flowing in the divider acts as a load current, and will increase the no-load input current to the converter, which is approximately:

$$I_Q = 1.7\mu A + \left(\frac{V_{OUT}}{R1+R2}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{1}{n}\right) \quad (2)$$

where 1.7µA is the quiescent current of the LT8620 and the second term is the current in the feedback divider reflected to the input of the buck operating at its light load efficiency n. For a 3.3V application with R1 = 1M and R2 = 412k, the feedback divider draws 2.3µA. With V_{IN} = 12V and n = 80%, this adds 0.8µA to the 1.7µA quiescent current resulting in 2.5µA no-load current from the 12V supply. Note that this equation implies that the no-load current is a function of V_{IN}; this is plotted in the Typical Performance Characteristics section.

When using large FB resistors, a 4.7pF to 10pF phase-lead capacitor should be connected from V_{OUT} to FB.

Setting the Switching Frequency

The LT8620 uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 2.2MHz by using a resistor tied from the RT pin to ground. A table showing the necessary R_T value for a desired switching frequency is in Table 1.

The R_T resistor required for a desired switching frequency can be calculated using:

$$R_T = \frac{46.5}{f_{SW}} - 5.2 \quad (3)$$

where R_T is in kΩ and f_{SW} is the desired switching frequency in MHz.

Table 1. SW Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.2	232
0.3	150
0.4	110
0.5	88.7
0.6	71.5
0.7	60.4
0.8	52.3
1.0	41.2
1.2	33.2
14	28.0
1.6	23.7
1.8	20.5
2.0	18.2
2.2	15.8

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Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency and a smaller input voltage range.

The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)}\left(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)}\right)} \quad (4)$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.3V, ~0.15V, respectively at maximum load) and $t_{ON(MIN)}$ is the minimum top switch on-time (see the Electrical Characteristics). This equation shows that a slower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio.

For transient operation, V_{IN} may go as high as the absolute maximum rating of 65V regardless of the R_T value, however the LT8620 will reduce switching frequency as necessary to maintain control of inductor current to assure safe operation.

The LT8620 is capable of a maximum duty cycle of approximately 99%, and the V_{IN}-to-V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch. In this mode the LT8620 skips switch cycles, resulting in a lower switching frequency than programmed by RT.

For applications that cannot allow deviation from the programmed switching frequency at low V_{IN}/V_{OUT} ratios use the following formula to set switching frequency:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{SW(BOT)}}{1 - f_{SW} \bullet t_{OFF(MIN)}} - V_{SW(BOT)} + V_{SW(TOP)} \quad (5)$$

where $V_{IN(MIN)}$ is the minimum input voltage without skipped cycles, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.3V, ~0.15V, respectively at maximum load), f_{SW} is the switching frequency (set by RT), and $t_{OFF(MIN)}$ is the minimum switch off-time. Note that higher switching frequency will increase the minimum input voltage below which cycles will be dropped to achieve higher duty cycle.

Inductor Selection and Maximum Output Current

The LT8620 is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short-circuit conditions the LT8620 safely tolerates operation with a saturated inductor through the use of a high speed peak-current mode architecture.

A good first choice for the inductor value is:

$$L = \frac{V_{OUT} + V_{SW(BOT)}}{f_{SW}} \quad (6)$$

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, $V_{SW(BOT)}$ is the bottom switch drop (~0.15V) and L is the inductor value in µH.

To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of in inductor ripple current:

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L \quad (7)$$

where ΔI_L is the inductor ripple current as calculated in Equation 9 and $I_{LOAD(MAX)}$ is the maximum output load for a given application.

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As a quick example, an application requiring 1A output should use an inductor with an RMS rating of greater than 1A and an I_{SAT} of greater than 1.3A. During long duration overload or short-circuit conditions, the inductor RMS routing requirement is greater to avoid overheating of the inductor. To keep the efficiency high, the series resistance (DCR) should be less than 0.04Ω, and the core material should be intended for high frequency applications.

The LT8620 limits the peak switch current in order to protect the switches and the system from overload faults. The top switch current limit (I_{LIM}) is at least 3.8A at low duty cycles and decreases linearly to 2.8A at DC = 0.8. The inductor value must then be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current.

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2} \quad (8)$$

The peak-to-peak ripple current in the inductor can be calculated as follows:

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (9)$$

where f_{SW} is the switching frequency of the LT8620, and L is the value of the inductor. Therefore, the maximum output current that the LT8620 will deliver depends on the switch current limit, the inductor value, and the input and output voltages. The inductor value may have to be increased if the inductor ripple current does not allow sufficient maximum output current ($I_{OUT(MAX)}$) given the switching frequency, and maximum input voltage used in the desired application.

In order to achieve higher light load efficiency, more energy must be delivered to the output during the single small pulses in Burst Mode operation such that the LT8620 can stay in sleep mode longer between each pulse. This can be achieved by using a larger value inductor (i.e. 4.7µH), and should be considered independent of switching frequency when choosing an inductor. For example, while a lower inductor value would typically be used for a high switching frequency application, if high light load efficiency is desired, a higher inductor value should be chosen.

The optimum inductor for a given application may differ from the one indicated by this design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. For applications requiring smaller load currents, the value of the inductor may be lower and the LT8620 may operate with higher ripple current. This allows use of a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Be aware that low inductance may result in discontinuous mode operation, which further reduces maximum load current.

For more information about maximum output current and discontinuous operation, see Linear Technology's Application Note 44.

Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid sub-harmonic oscillation. See Application Note 19.

Input Capacitor

Bypass the input of the LT8620 circuit with a ceramic capacitor of X7R or X5R type placed as close as possible to the V_{IN} and PGND pins. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 4.7µF to 10µF ceramic capacitor is adequate to bypass the LT8620 and will easily handle the ripple current. Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT8620 and to force this very high frequency switching current into a tight local loop, minimizing EMI. A 4.7µF capacitor is capable of this task, but only if it is placed close to the LT8620 (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT8620. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped)

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tank circuit. If the LT8620 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8620's voltage rating. This situation is easily avoided (see Linear Technology Application Note 88).

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT8620 to produce the DC output. In this role it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT8620's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. For good starting values, see the Typical Applications section.

Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value output capacitor and the addition of a feedforward capacitor placed between V_{OUT} and FB. Increasing the output capacitance will also decrease the output voltage ripple. A lower value of output capacitor can be used to save space and cost but transient performance will suffer and may cause loop instability. See the Typical Applications in this data sheet for suggested capacitor values.

When choosing a capacitor, special attention should be given to the data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

Ceramic Capacitors

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8620 due to their piezoelectric nature. When in Burst Mode operation, the LT8620's switching frequency depends on the load current, and at very light loads the LT8620 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8620 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LT8620. As previously mentioned, a ceramic input capacitor combined with trace or cable inductance forms a high quality (underdamped) tank circuit. If the LT8620 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8620's rating. This situation is easily avoided (see Linear Technology Application Note 88).

Enable Pin

The LT8620 is in shutdown when the EN pin is low and active when the pin is high. The rising threshold of the EN comparator is 1.0V, with 40mV of hysteresis. The EN pin can be tied to V_{IN} if the shutdown feature is not used, or tied to a logic level if shutdown control is required.

Adding a resistor divider from V_{IN} to EN programs the LT8620 to regulate the output only when V_{IN} is above a desired voltage (see the Block Diagram). Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values R3 and R4 such that they satisfy the following equation:

$$V_{IN(EN)} = \left(\frac{R3}{R4} + 1\right) \bullet 1.0V \qquad (10)$$

where the LT8620 will remain off until V_{IN} is above $V_{IN(EN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(EN)}$.

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When operating in Burst Mode operation for light load currents, the current through the $V_{IN(EN)}$ resistor network can easily be greater than the supply current consumed by the LT8620. Therefore, the $V_{IN(EN)}$ resistors should be large to minimize their effect on efficiency at low loads.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 3.4V supply from V_{IN} that powers the drivers and the internal bias circuitry. The $INTV_{CC}$ can supply enough current for the LT8620's circuitry and must be bypassed to ground with a minimum of 1µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. To improve efficiency the internal LDO can also draw current from the BIAS pin when the BIAS pin is at 3.1V or higher. Typically the BIAS pin can be tied to the output of the LT8620, or can be tied to an external supply of 3.3V or above. If BIAS is connected to a supply other than V_{OUT}, be sure to bypass with a local ceramic capacitor. If the BIAS pin is below 3.0V, the internal LDO will consume current from V_{IN}. Applications with high input voltage and high switching frequency where the internal LDO pulls current from V_{IN} will increase die temperature because of the higher power dissipation across the LDO. Do not connect an external load to the $INTV_{CC}$ pin.

Output Voltage Tracking and Soft-Start

The LT8620 allows the user to program its output voltage ramp rate by means of the TR/SS pin. An internal 2µA pulls up the TR/SS pin to $INTV_{CC}$. Putting an external capacitor on TR/SS enables soft starting the output to prevent current surge on the input supply. During the soft-start ramp the output voltage will proportionally track the TR/SS pin voltage. For output tracking applications, TR/SS can be externally driven by another voltage source. From 0V to 0.97V, the TR/SS voltage will override the internal 0.97V reference input to the error amplifier, thus regulating the FB pin voltage to that of TR/SS pin. When TR/SS is above 0.97V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage. The TR/SS pin may be left floating if the function is not needed.

An active pull-down circuit is connected to the TR/SS pin which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the EN/UV pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Output Power Good

When the LT8620's output voltage is within the ±9% window of the regulation point, which is a V_{FB} voltage in the range of 0.883V to 1.057V (typical), the output voltage is considered good and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal pull-down device will pull the PG pin low. To prevent glitching both the upper and lower thresholds include 1.3% of hysteresis.

The PG pin is also actively pulled low during several fault conditions: EN/UV pin is below 1V, $INTV_{CC}$ has fallen too low, V_{IN} is too low, or thermal shutdown.

Synchronization

To select low ripple Burst Mode operation, tie the SYNC pin below 0.4V (this can be ground or a logic low output). To synchronize the LT8620 oscillator to an external frequency connect a square wave (with 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.5V (up to 6V).

The LT8620 will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will pulse skip to maintain regulation. The LT8620 may be synchronized over a 200kHz to 2.2MHz range. The R_T resistor should be chosen to set the LT8620 switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the R_T should be selected for 500kHz. The slope compensation is set by the R_T value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage, and output voltage. Since the synchronization frequency will not change the slopes of the inductor current waveform, if the inductor is large enough to avoid

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subharmonic oscillations at the frequency set by R_T, then the slope compensation will be sufficient for all synchronization frequencies.

For some applications it is desirable for the LT8620 to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. First is the clock stays awake at all times and all switching cycles are aligned to the clock. Second is that full switching frequency is reached at lower output load than in Burst Mode operation. These two differences come at the expense of increased quiescent current. To enable pulse-skipping mode, the SYNC pin is tied high either to a logic output or to the INTVCC pin.

The LT8620 does not operate in forced continuous mode regardless of SYNC signal. Never leave the SYNC pin floating.

Shorted and Reversed Input Protection

The LT8620 will tolerate a shorted output. Several features are used for protection during output short-circuit and brownout conditions. The first is the switching frequency will be folded back while the output is lower than the set point to maintain inductor current control. Second, the bottom switch current is monitored such that if inductor current is beyond safe levels switching of the top switch will be delayed until such time as the inductor current falls to safe levels.

Frequency foldback behavior depends on the state of the SYNC pin: If the SYNC pin is low the switching frequency will slow while the output voltage is lower than the programmed level. If the SYNC pin is connected to a clock source or tied high, the LT8620 will stay at the programmed frequency without foldback and only slow switching if the inductor current exceeds safe levels.

There is another situation to consider in systems where the output will be held high when the input to the LT8620 is absent. This may occur in battery charging applications or in battery-backup systems where a battery or some other supply is diode ORed with the LT8620's output. If the V_{IN} pin is allowed to float and the EN pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT8620's internal circuitry will pull its quiescent current through its SW pin. This is acceptable if the system can tolerate several µA in this state. If the EN pin is grounded the SW pin current will drop to near 1µA. However, if the V_{IN} pin is grounded while the output is held high, regardless of EN, parasitic body diodes inside the LT8620 can pull current from the output through the SW pin and the V_{IN} pin. Figure 3 shows a connection of the V_{IN} and EN/UV pins that will allow the LT8620 to run only when the input voltage is present and that protects against a shorted or reversed input.

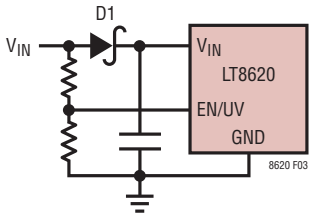


Figure 3. Reverse V_{IN} Protection

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 4 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT8620's V_{IN} pins, GND pins, and the input capacitor. The loop formed by the input capacitor should be as small as possible by placing the capacitor adjacent to the V_{IN} and GND pins. When using a physically large input capacitor the resulting loop may become too large in which case using a small case/value capacitor placed close to the V_{IN} and GND pins plus a larger capacitor further away is preferred. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BOOST nodes should be as small as possible. Finally, keep the FB and RT nodes

APPLICATIONS INFORMATION

small so that the ground traces will shield them from the SW and BOOST nodes. The exposed pad on the bottom of the package must be soldered to ground so that the pad is connected to ground electrically and also acts as a heat sink thermally. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT8620 to additional ground planes within the circuit board and on the bottom side.

High Temperature Considerations

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT8620. The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT8620. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LT8620 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is calculated by multiplying the LT8620 power dissipation by the thermal resistance from junction to ambient. The LT8620 will stop switching and indicate a fault condition if safe junction temperature is exceeded.

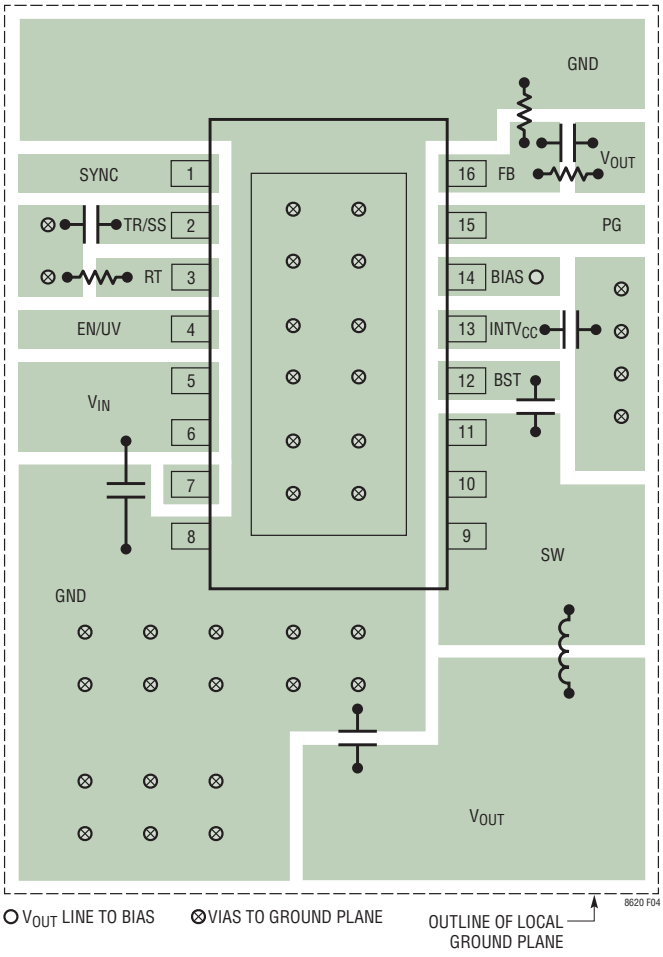


Figure 4a. Recommended PCB Layout for the LT8620 MSOP Package

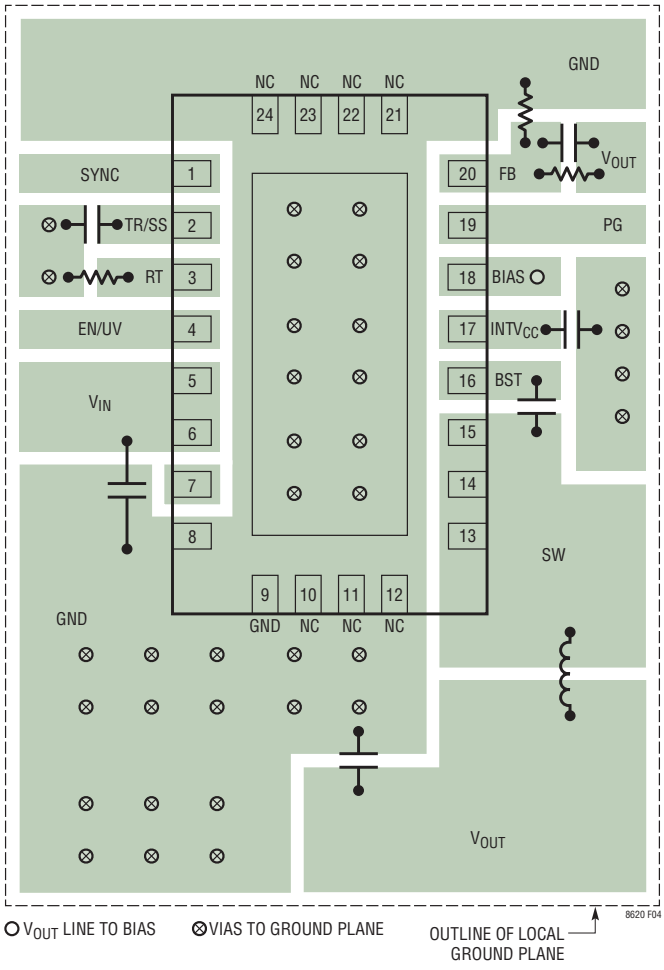
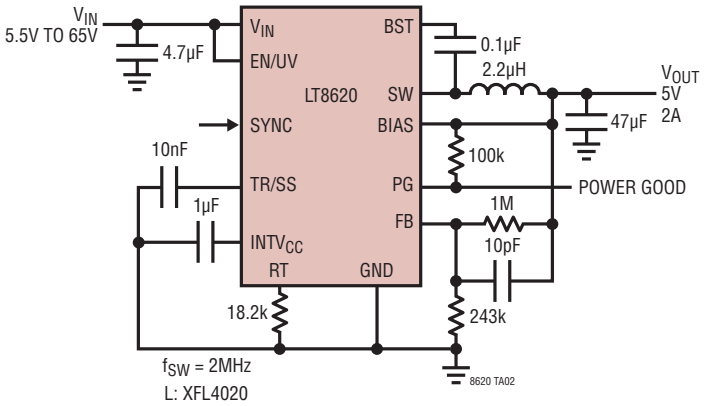


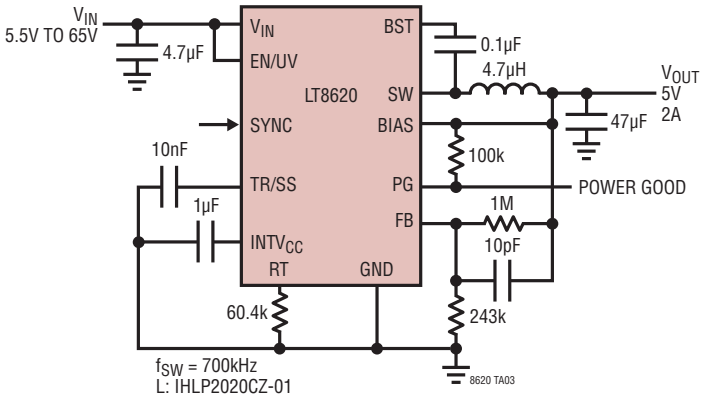
Figure 4b. Recommended PCB Layout for the LT8620 QFN Package

TYPICAL APPLICATIONS

5V 2MHz Step-Down Converter

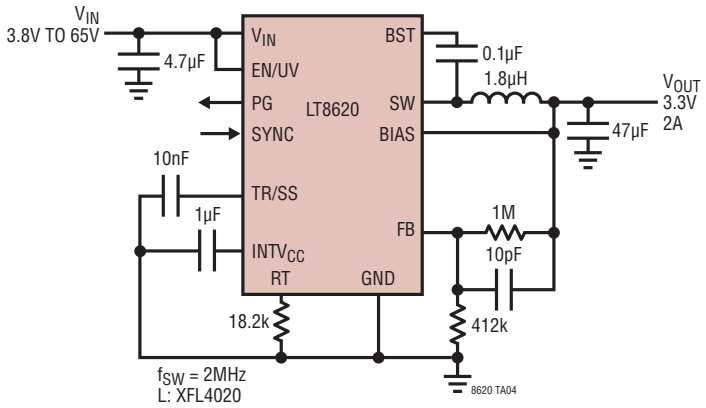


5V Step-Down Converter

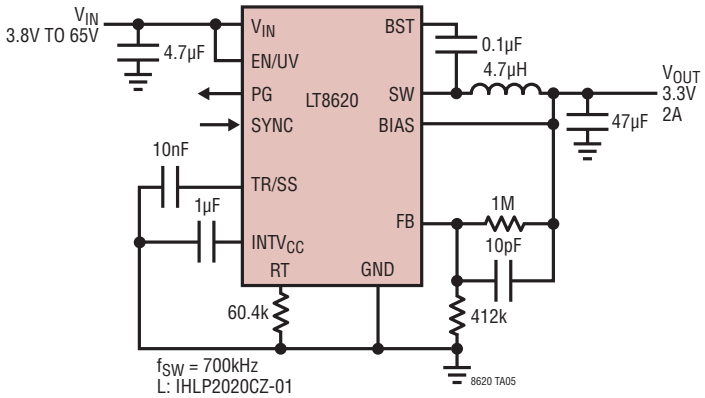


TYPICAL APPLICATIONS

3.3V 2MHz Step-Down Converter

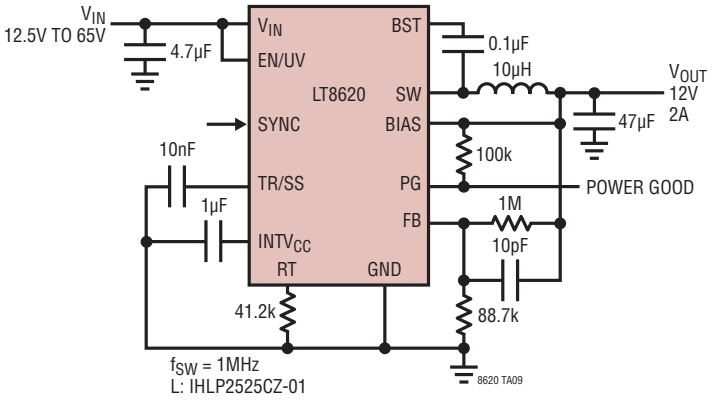


3.3V Step-Down Converter

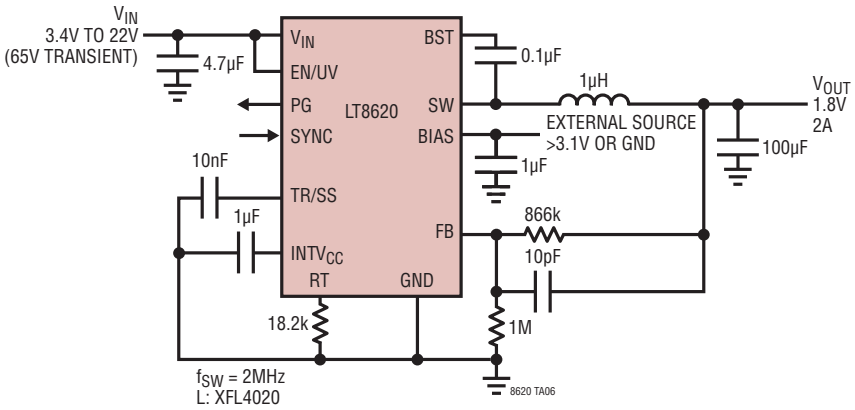


TYPICAL APPLICATIONS

12V Step-Down Converter

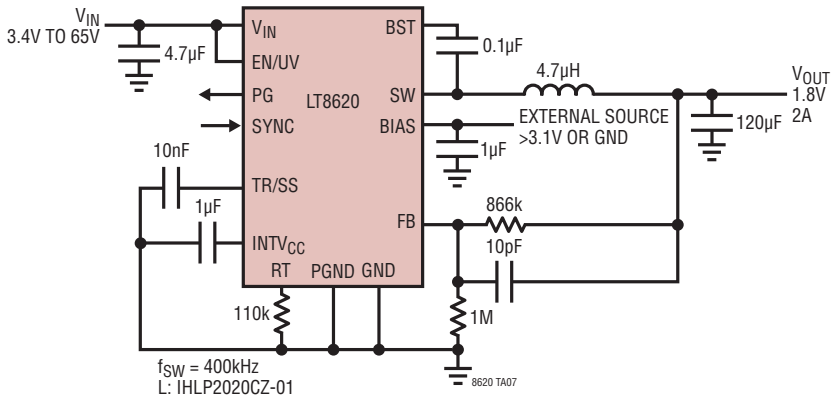


1.8V 2MHz Step-Down Converter

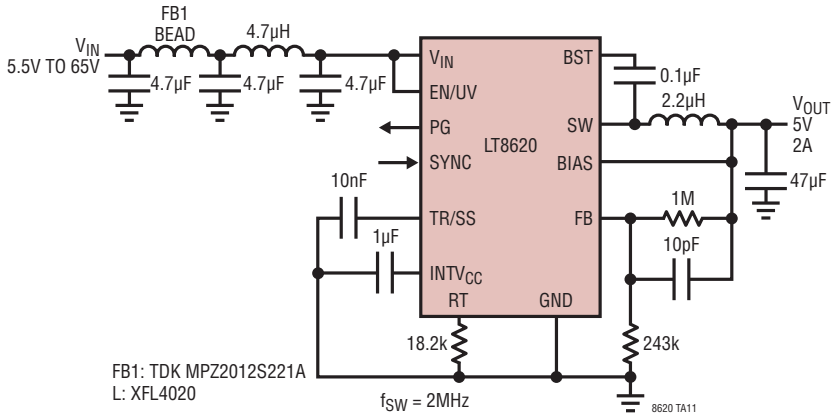


TYPICAL APPLICATIONS

1.8V Step-Down Converter



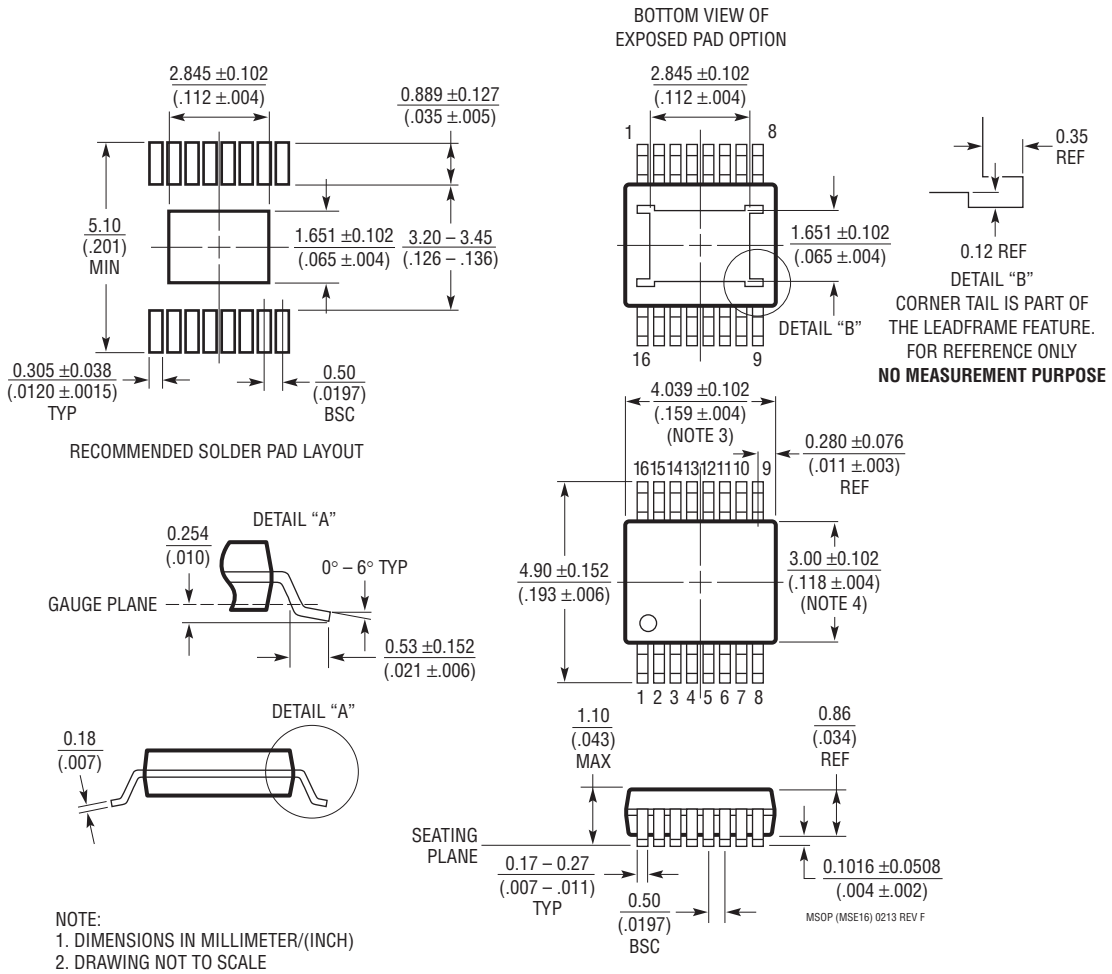
Ultralow EMI 5V 2A Step-Down Converter



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)

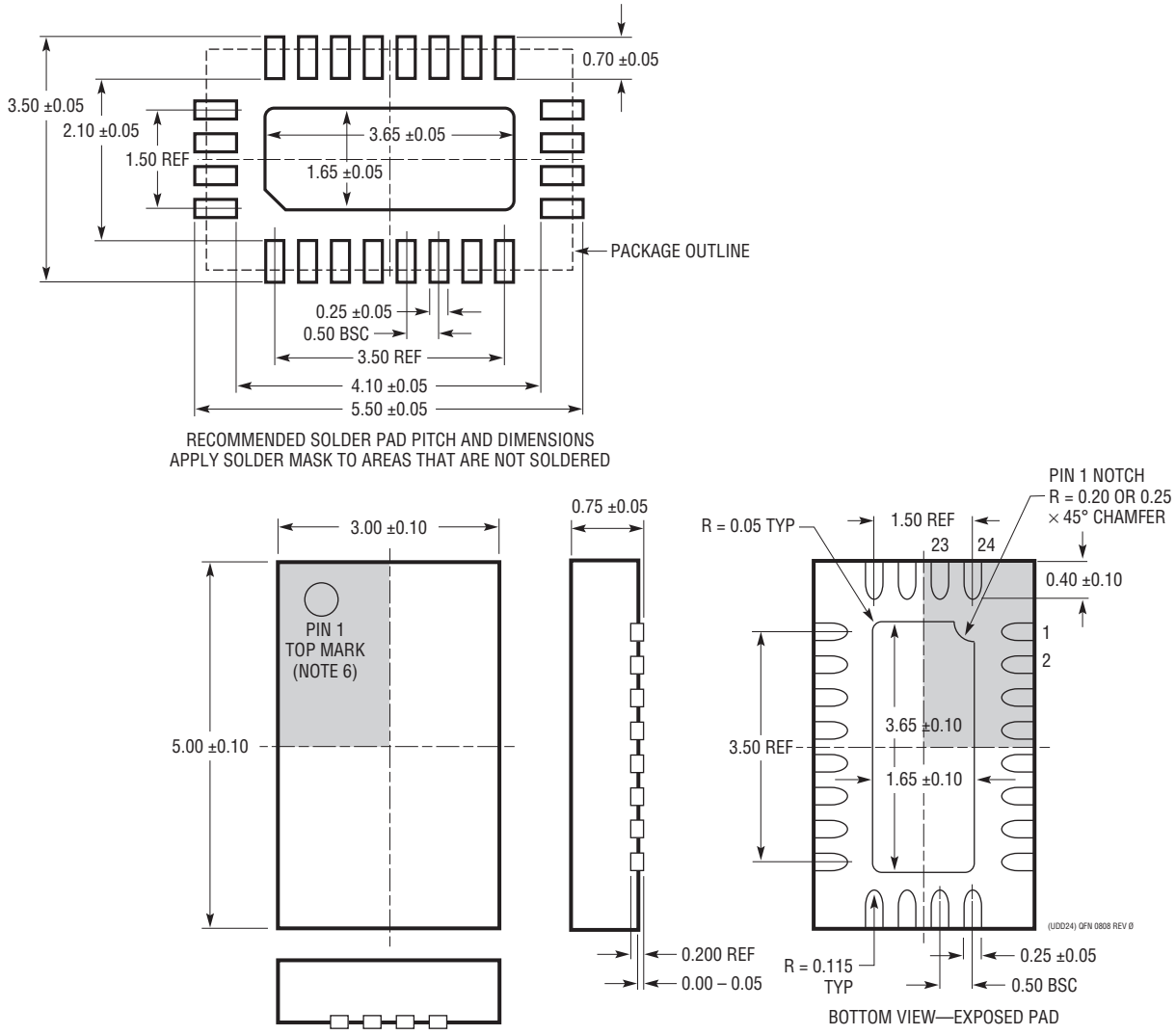


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UDD Package
24-Lead Plastic QFN (3mm × 5mm)
(Reference LTC DWG # 05-08-1833 Rev Ø)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

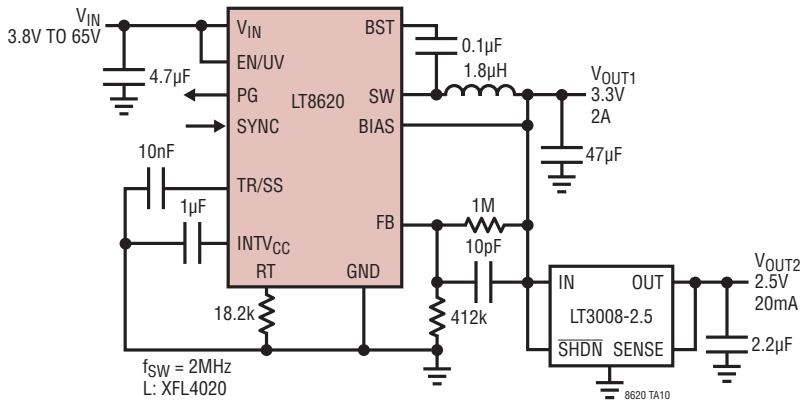
REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/15	Added H- and MP-Grade Versions ABS Max Table, Order Information	2
		Clarified Specifications to 150°C and Note 2	3
		Clarified Current Limit Graphs	5
		Clarified RT Programmed Switching Frequency, Soft-Start Current	6
		Clarified TR/SS and BIAS Pin Function Description	8
		Clarified Overload Conditions from 3.8A to 3.9A	10

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Ultralow I_Q 2.5V, 3.3V Step-Down with LDO



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8610	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN}: 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E Package
LT8610A/ LT8610AB	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN}: 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E Package
LT8611	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA and Input/Output Current Limit/Monitor	V_{IN}: 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 5mm QFN-24 Package
LT8612	42V, 6A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN}: 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 3µA, I_{SD} < 1µA, 3mm × 6mm QFN-28 Package
LT8614	42V, 4A, 96% Efficiency, 2.2MHz Silent Switcher Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN}: 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 4mm QFN-20 Package
LT3690	36V with 60V Transient Protection, 4A, 92% Efficiency, 1.5MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 70µA	V_{IN}: 3.9V to 36V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 70µA, I_{SD} < 1µA, 4mm × 6mm QFN-26 Package
LT3991	55V, 1.2A, 2.2MHz High Efficiency Micropower Step-Down DC/DC Converter with I_Q = 2.8µA	V_{IN}: 4.2V to 62V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 2.8µA, I_{SD} < 1µA, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT3990	62V, 350mA, 2.2MHz High Efficiency Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN}: 4.2V to 65V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 3mm DFN-10 and MSOP-6E Packages
LT3980	58V with Transient Protection to 80V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN}: 3.6V to 58V, Transient to 80V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 85µA, I_{SD} < 1µA, 3mm × 4mm DFN-16 and MSOP-16E Packages

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