MP5403B

Mini PMIC with Dual 4A/5A Peak Bucks, One 2A Load Switch, and Input Power Supervisory

DESCRIPTION

The MP5403B is a monolithic power management unit containing two high-efficiency, step-down, switching converters and a load switch. The two regulators supply peak currents up to 5A and 4A separately, and the load switch supplies up to 3A of load current with an extremely low $R_{DS(ON)}$. With an input range of up to 6V, the MP5403B is ideal for powering ASIC and SOC for solid-state drives (SSD) and other compact power systems.

The peak-current-mode control scheme with pulse-skip mode operation provides the two switchers with fast transient response, high light-load efficiency, and a minimal number of capacitors by using an interleaving PWM clock between the two switchers. The 3A load switch with a low 20mΩ on resistance provides flexible system configuration.

A full set of enable control pins and power good open-drain indicators allow for easy implementation of the start-up and shutdown sequences.

Full protection features include over-current protection (OCP) and thermal shutdown.

The MP5403B requires a minimal number of readily available, standard, external components and is available in a small UTQFN-20 (2.5mmx3mm) package.

FEATURES

- Up to 6V Operating Input Range
- Low I_Q: 85μA for Two Switchers Total
- Two Buck Converters
  - Peak 5A with 55mΩ/20mΩ $R_{DS(ON)}$
  - Peak 4A with 65mΩ/22mΩ $R_{DS(ON)}$
  - 1.5MHz Switching Frequency
  - 180° Interleaving Operation
  - 100% Duty Cycle
  - Load Switch Mode by Pulling FB Low
  - Latch-Off Short-Circuit Protection (SCP)
  - Internal Soft Start (SS) and Output Discharge
  - Optimized Light-Load Efficiency
- One Load Switch with 20mΩ $R_{DS(ON)}$
  - 3A with 20mΩ $R_{DS(ON)}$
  - Soft Start (SS) and Output Discharge
  - Over-Current Protection (OCP)
- EN and Power Good (PG) for Power Sequencing
- Input Power Good (PG) Indicator with Adjustable Threshold and Delay
- Thermal Shutdown
- Available in a UTQFN-20 (2.5mmx3mm) Package

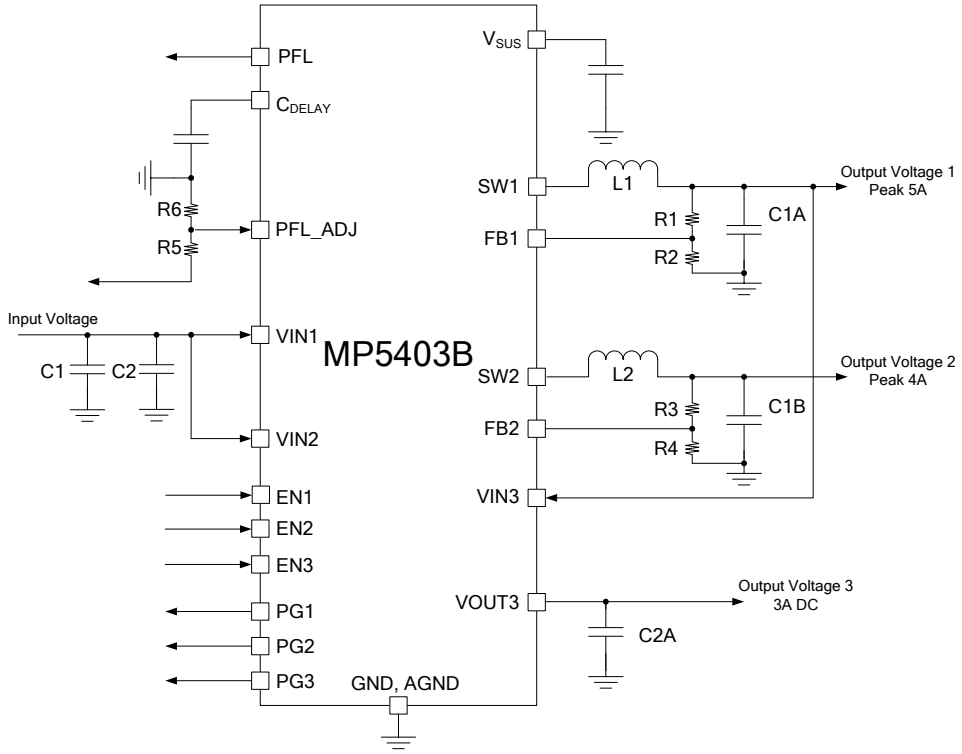
APPLICATIONS

- Solid-State Drives (SSD)
- Portable Instruments
- Battery-Powered Devices

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5403BGQBU	UTQFN-20 (2.5mmx3mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP5403BGQBU–Z)

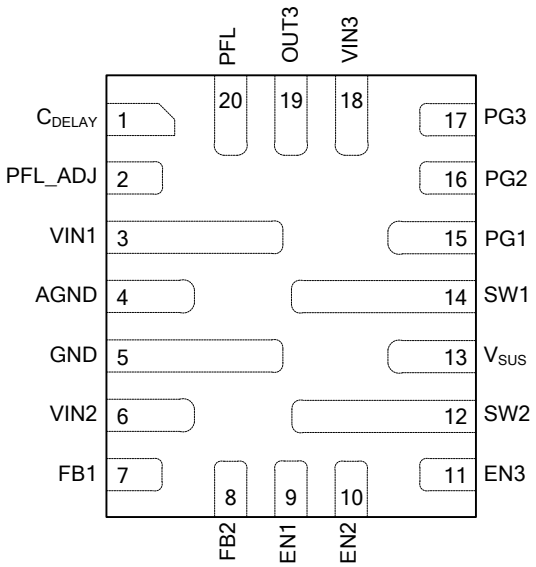
TOP MARKING

AWF
YWW
LLL

AWF: Product code of MP5403BGQBU
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



UTQFN-20 (2.5mmx3mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage ($V_{IN1/2/3}$) 6.5V
$V_{SW1/2}$ ..... -0.3V (-5V for <10ns) to 6.5V (10V for <10ns)
All other pins ..... -0.3V to 6.5V
Continuous power dissipation (T_A = +25°C) ..... 3.5W **(2)(4)**
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN1}) ..... 2.7V to 6V
Supply voltage (V_{IN2}) (if V_{IN1} > UVLO) ..... 2.0V to 6V
Supply voltage (V_{IN3}) (if V_{IN1} > UVLO) ..... 0.5V to 6V
Supply voltage (V_{IN3}) (If V_{IN1} < UVLO) ..... 2.7V to 6V
Output voltage ($V_{OUT1/2}$) ..... 0.6V to $V_{IN1/2}$
Output voltage (V_{OUT3}) ..... V_{IN3}
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance	***θ_{JA}***	***θ_{JC}***	
UTQFN-20 (2.5mmx3mm)			
EV5403-QB-02A **(4)**	35	7	°C/W
JESD51-7 **(5)**	60	13	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV5403-QB-02A, 4-layer PCB.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

$V_{IN1/2}$ = 3.6V, V_{IN3} = 3.6V, T_J = -40°C to 125°C(7), typical value tested at T_J = 25°C unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
For Buck Regulators (V_{IN1} provides control voltage if V_{IN3} is lower than 2.7V)						
Input voltage range	V_{IN1}	For V_{IN1}	2.7		6	V
Under-voltage lockout threshold rising	$V_{IN1_UVLO_R}$	For V_{IN1}	2.3	2.5	2.65	V
Under-voltage lockout threshold hysteresis	$V_{IN1_UVLO_H}$	For V_{IN1}		250		mV
Input voltage range for rail 2	V_{IN2}	$V_{IN1} > V_{IN1_UVLO_R}$	2		6	V
V_{IN2} under-voltage lockout threshold rising	$V_{IN2_UVLO_R}$	For V_{IN2}		1.8	1.85	V
V_{IN2} under-voltage lockout threshold hysteresis	$V_{IN2_UVLO_H}$	For V_{IN2}		300		mV
Supply current (shutdown)	I_{SD}	$V_{EN1/2/3}$ = 0V, T_J = 25°C			1	µA
Supply current (quiescent)	I_{Q1+Q2}	$V_{EN1/2}$ = 2V, V_{EN3} = 0V, $V_{FB1/2}$ =1V		85	110	µA
High-side switch on resistance for peak 5A switcher	R_{DSON1_H}			55		mΩ
Low-side switch on resistance for peak 5A switcher	R_{DSON1_L}			20		mΩ
High-side switch on resistance for peak 4A switcher	R_{DSON2_H}			65		mΩ
Low-side switch on resistance for peak 4A switcher	R_{DSON2_L}			22		mΩ
Switch leakage current	$I_{LK_SW1/2}$	$V_{EN1/2}$ = 0V, $V_{IN1/2}$ = 6V, $V_{SW1/2}$ = 0V and 6V, T_J = 25°C		0	1	µA
High-side current limit for peak 5A switcher	I_{LIM1_H}		6.2	8.5		A
High-side current limit for peak 4A switcher	I_{LIM2_H}		5	7		A
Low-side zero crossing current	$I_{ZCD1/2}$	For both channels		0.1		A
Oscillator frequency	$F_{SW1/2}$	CCM	1.2	1.5	1.8	MHz
Phase shift	PhS	CCM		180		degree
Minimum on time (6)	T_{MIN_ON}			70		ns
Minimum off time (6)	T_{MIN_OFF}			100		ns
Maximum duty cycle (6)	D_{MAX}			100		%
Feedback voltage	$V_{FB1/2}$	T_J = 25°C	594	600	606	mV
		T_J = -40°C to 125°C (7)	591	600	609	mV
Feedback currents	$I_{FB1/2}$	FB1/2 = 0.65V		10	50	nA
Internal soft-start time	$T_{SS1/2}$	For both channels		0.35		ms

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ELECTRICAL CHARACTERISTICS *(continued)*

$V_{IN1/2}$ = 3.6V, V_{IN3} = 3.6V, T_J = -40°C to 125°C(7), typical value tested at T_J = 25°C unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Output discharge resistor	$I_{ssres1/2}$	For both channels		13		Ω
EN high logic	$EN_{1/2_H}$		1.05	1.3	1.5	V
EN low hysteresis	$EN_{1/2_L_HYS}$			150		mV
EN1/2 input current	$I_{EN1/2}$	V_{EN} = 2V		1		μA
		V_{EN} = 0V		0		
EN1 turn-on delay	EN_{TD_1}	For channel 1		100		μs
EN2 turn-on delay	EN_{TD_2}	For channel 2, V_{IN1} > $V_{IN1_UVLO_R}$		100		μs
Power good upper trip threshold	$PG_{1/2_H}$	FB with respect to the regulation		+30		%
Power good lower trip threshold	$PG_{1/2_L}$	FB with respect to the regulation		-10		%
Power good hysteresis	PG_{HY}			5		%
Power good delay for rising	$PD_{TD_1/2\ H}$			20		μs
Power good delay for falling	$PD_{TD_1/2\ L}$			60		μs
Power good sink current capability	$V_{PG_LO_1/2}$	Sink 1mA			0.4	V
Power good leakage current	$PG_{LK_1/2}$	V_{PGBUS} = 1.8V		1		μA
Load Switch						
Input voltage range	V_{IN3}	V_{IN1} > $V_{IN1_UVLO_R}$	0.6		6	V
		V_{IN1} < $V_{IN1_UVLO_R}$	2.7		6	V
Under voltage lockout threshold rising	$V_{IN3_UVLO_R}$	For V_{IN3}	2.3	2.5	2.65	V
Under voltage lockout threshold hysteresis	$V_{IN3_UVLO_H}$	For V_{IN3}		200		mV
Supply current (quiescent)	I_{Q3}	From V_{IN3}, $V_{EN1/2}$ = 0V, V_{EN3} = 3.6V		160	250	μA
On resistor	R_{DSON}			20		mΩ
EN3 high logic threshold	EN_{3_H}		1.05	1.3	1.5	V
EN3 low hysteresis	$EN_{3_L_HYS}$			150		mV
EN3 turn on delay	EN_{TD_3}	V_{IN1} > $V_{IN1_UVLO_R}$		70		μs
		V_{IN1} < $V_{IN1_UVLO_R}$		70		
EN3 input current	I_{EN3}	V_{EN3} = 2V		1		μA
		V_{EN3} = 0V		0		
PG3 high logic threshold	PG_{3_H}	VIN3 - VOUT3 is smaller than the range	150	200		mV
PG3 low logic threshold	PG_{3_L}	VIN3 - VOUT3 is larger than the range		250		mV
Power good delay for rising	PD_{TD_3}			40		μs
Power good sink current capability	$V_{PG_LO_3}$	Sink 1mA			0.4	V
Power good leakage current	PG_{LK_3}	V_{PGBUS} = 1.8V		1		μA

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ELECTRICAL CHARACTERISTICS *(continued)*

$V_{IN1/2}$ = 3.6V, V_{IN3} = 3.6V, T_J = -40°C to 125°C(7), typical value tested at T_J = 25°C unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Current limit	I_{LIM3}			6.2		A
Internal soft-start time	T_{ss3}			0.35		ms
Output resistor	I_{ssres}			13		Ω
Power Failure Circuitry						
V_{SUS} voltage	V_{SUS}			3.6		V
V_{SUS} leakage current	I_{SUS_LK}	V_{SUS} = 3.6V, V_{IN1} = V_{IN3} = 0V, T_J = 25°C		0	1	μA
PFL_ADJ reference	PFL_ADJ	T_A = 25°C	0.594	0.6	0.606	V
		T_J = -40°C to 125°C (7)	0.591	0.6	0.609	V
PFL hysteresis				3		%
PFL high-to-low delay	T_{PFL_HL}			1		μs
C_{DELAY} internal current source	I_{DELAY}			3.1		μA
Power good sink current capability	V_{PFL_LO}	Sink 1mA			0.4	V
Power good leakage current	PFL_{LK}	V_{PGBUS} = 1.8V		1		μA
Thermal shutdown (6)	T_{SD}			160		°C
Thermal hysteresis (6)	T_{HYS}			30		°C

NOTES:

6) Guaranteed by engineering sample characterization, not tested in production.

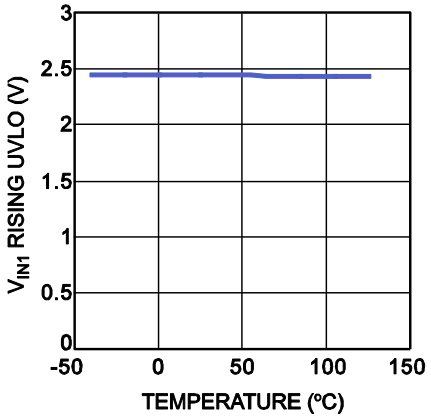
7) Guaranteed by characterization test, not tested in production.

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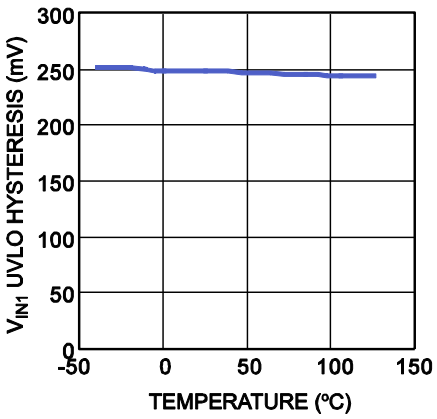
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = 0.47µH, L2 = 0.47µH, T_A = +25°C, unless otherwise noted.

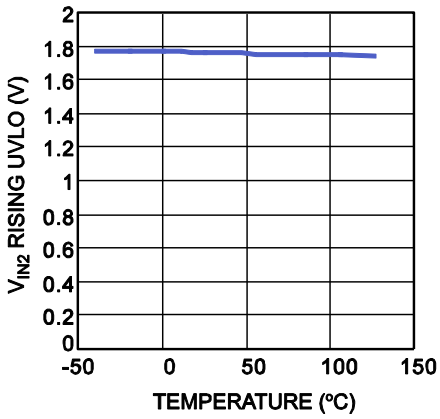
V_{IN1} Rising UVLO



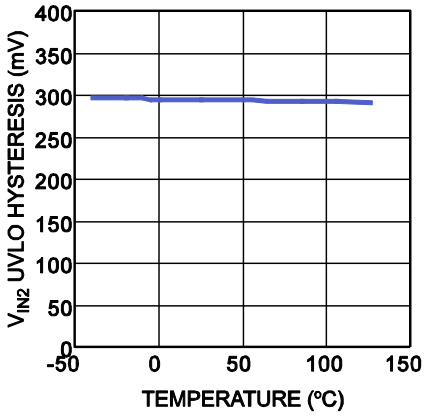
V_{IN1} UVLO Hysteresis



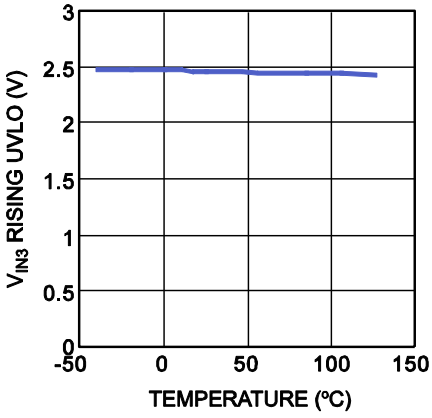
V_{IN2} Rising UVLO



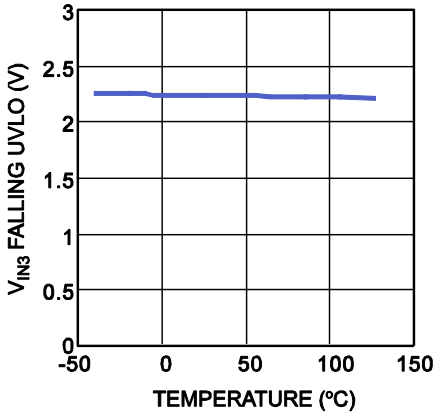
V_{IN2} UVLO Hysteresis



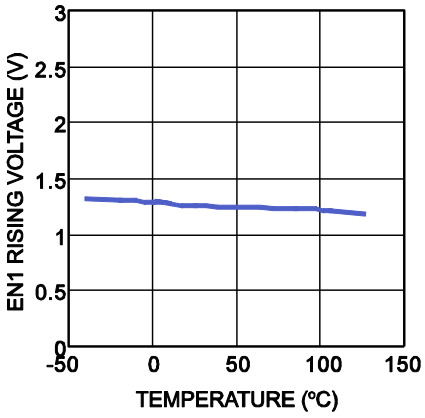
V_{IN3} Rising UVLO



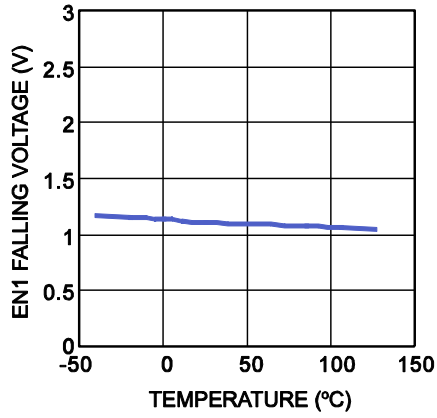
V_{IN3} Falling UVLO



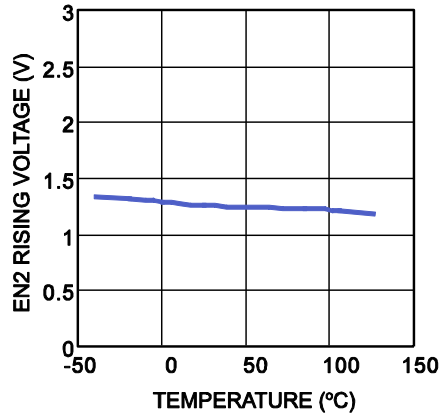
EN1 Rising Voltage



EN1 Falling Voltage



EN2 Rising Voltage

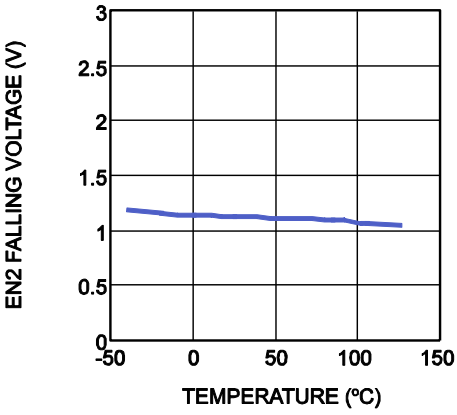


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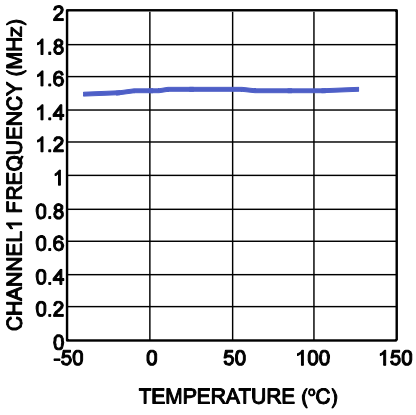
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = 0.47µH, L2 = 0.47µH, T_A = +25°C, unless otherwise noted.

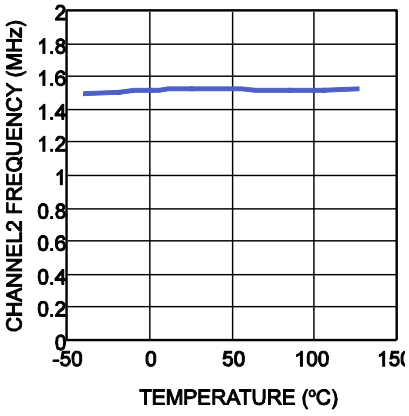
EN2 Falling Voltage



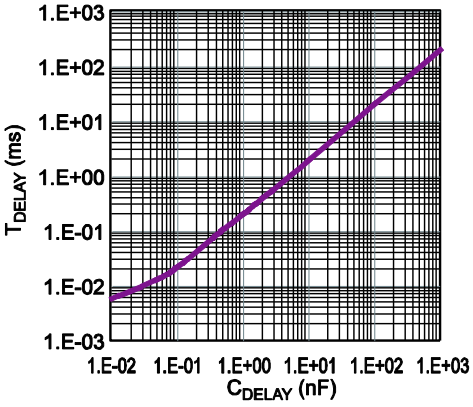
Channel1 Frequency



Channel2 Frequency

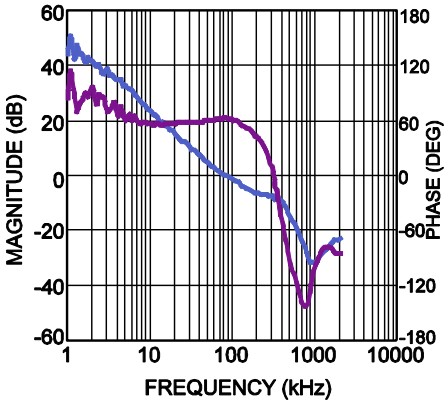


C_{DELAY} vs. T_{DELAY}



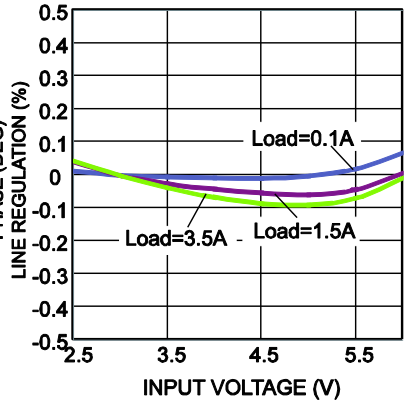
Bode Plot

V_{OUT}=3.3V



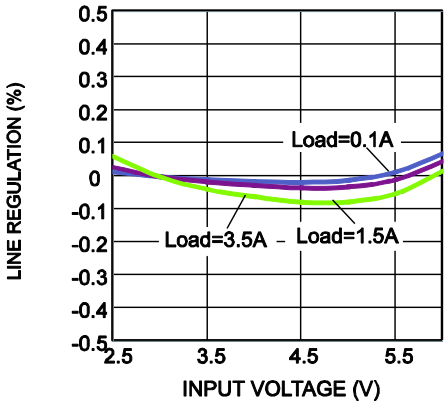
Line Regulation

CH1



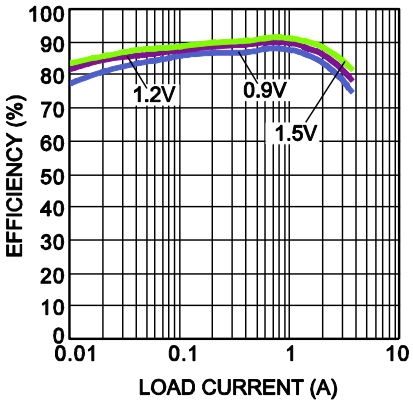
Line Regulation

CH2



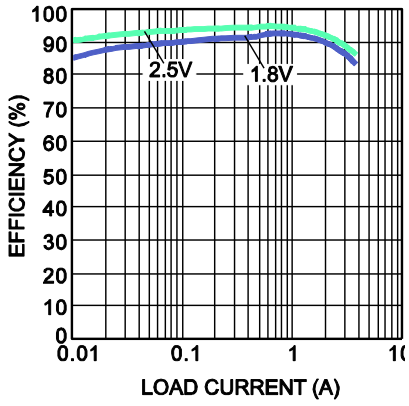
Efficiency

CH1, V_{IN} =3.3V



Efficiency

CH1, V_{IN} =3.3V

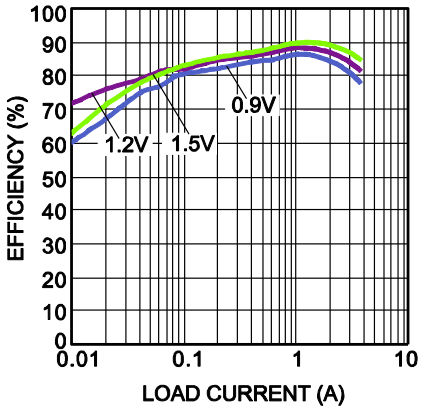


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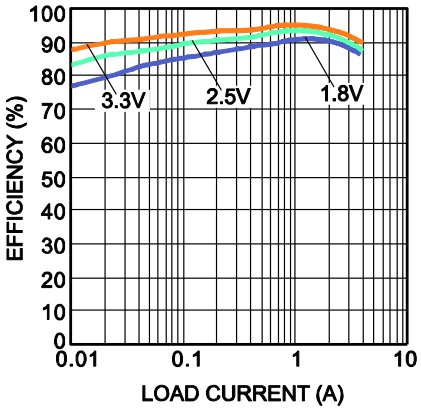
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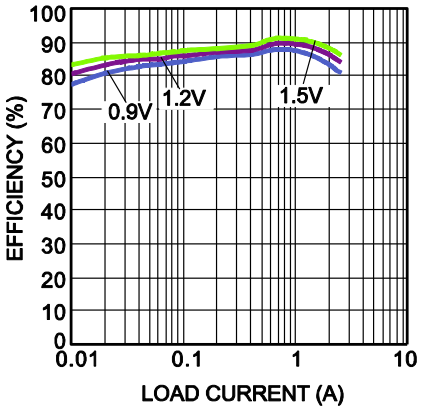
Efficiency
CH1



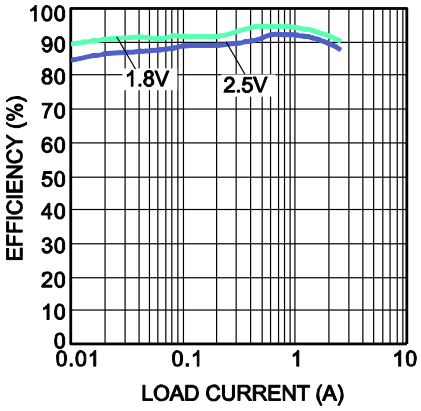
Efficiency
CH1



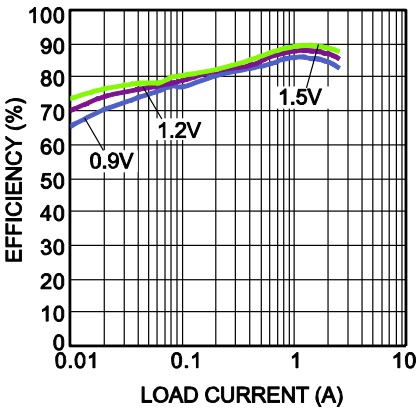
Efficiency
CH2, V_{IN}=3.3V



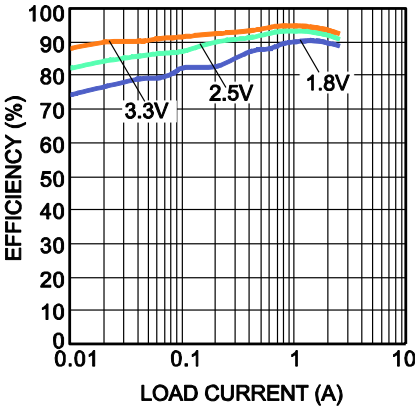
Efficiency
CH2, V_{IN}=3.3V



Efficiency
CH2



Efficiency
CH2

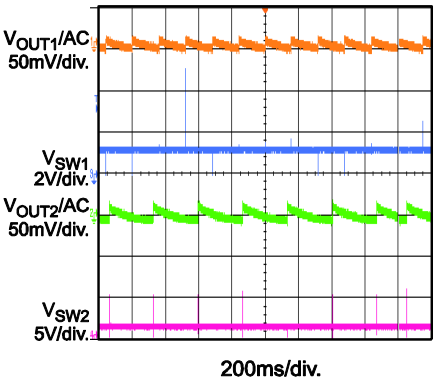


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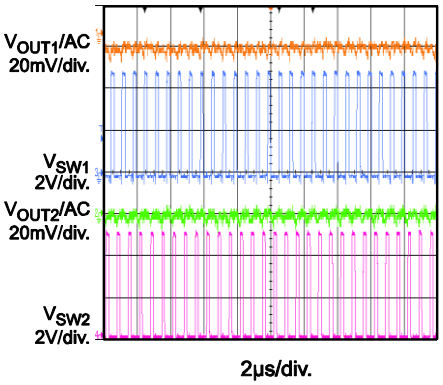
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.2V, V_{OUT2} = 1.2V, L1 = 0.47µH, L2 = 0.47µH, T_A = +25°C, unless otherwise noted.

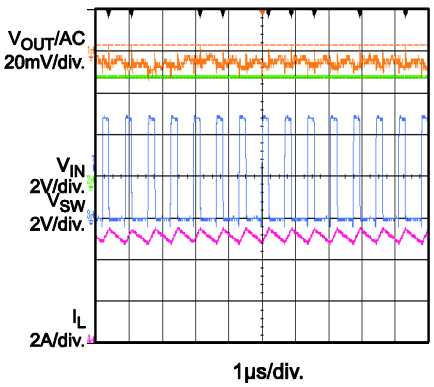
Output Ripple
I_{OUT1}=0A



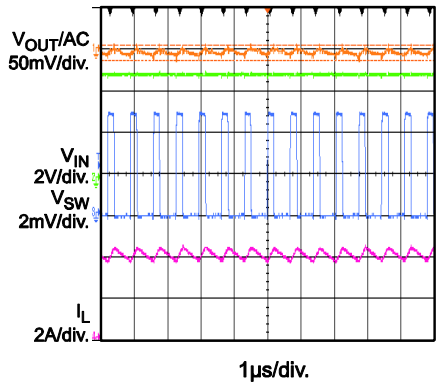
Output Ripple
I_{OUT1}=3.5A, I_{OUT2}=2.5A



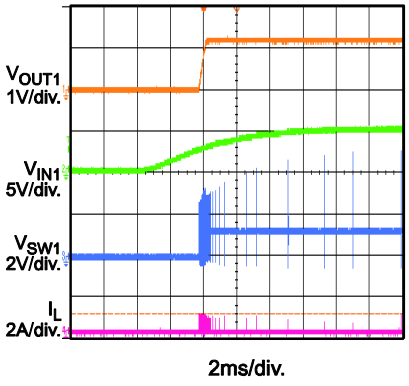
Output Ripple (CH1)
I_{OUT}=5A



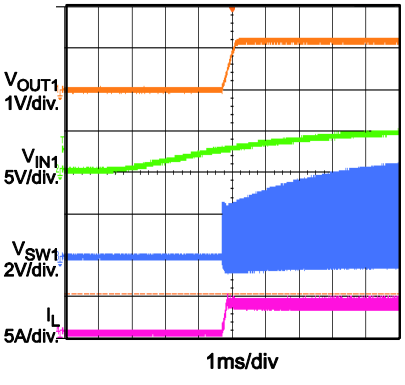
Output Ripple (CH2)
I_{OUT}=4A



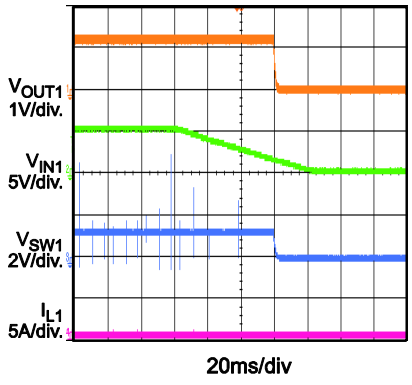
VIN Power-Up without Load (CH1)
I_{OUT}=0A



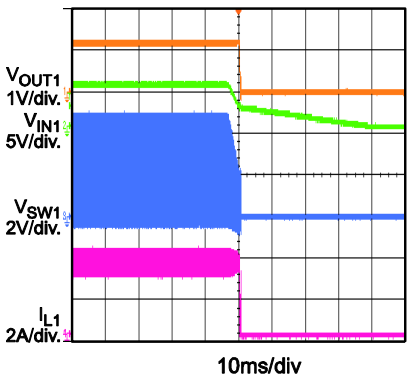
VIN Power-Up with 3.5A Load (CH1)
I_{OUT1}=3.5A



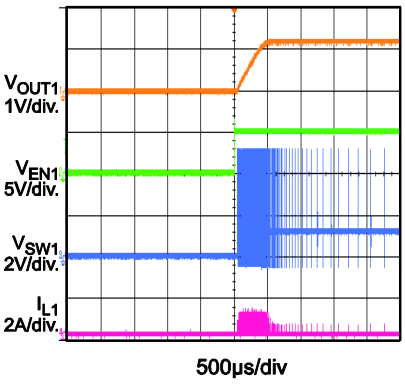
VIN Power-Down without Load (CH1)
I_{OUT1}=0A



VIN Power-Down with 3.5A Load (CH1)
I_{OUT1}=3.5A



EN On without Load (CH1)
I_{OUT1}=0A

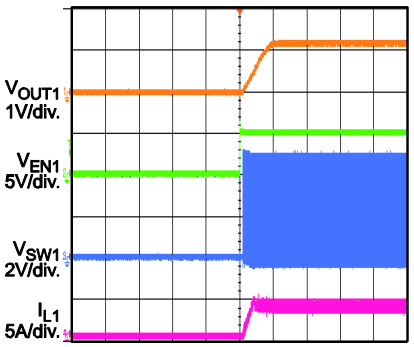


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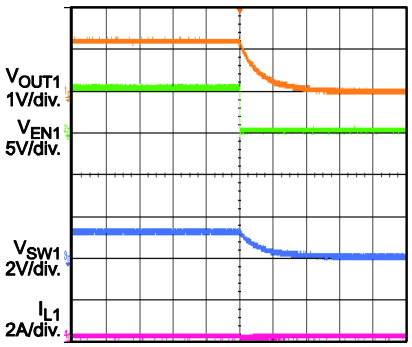
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.2V, V_{OUT2} = 1.2V, L1 = 0.47µH, L2 = 0.47µH, T_A = +25°C, unless otherwise noted.

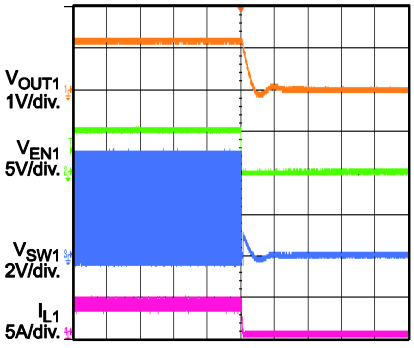
EN On with 3.5A Load (CH1)
I_{OUT1}=3.5A



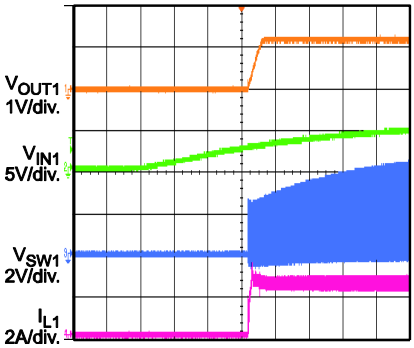
EN Down without Load (CH1)
I_{OUT1}=0A



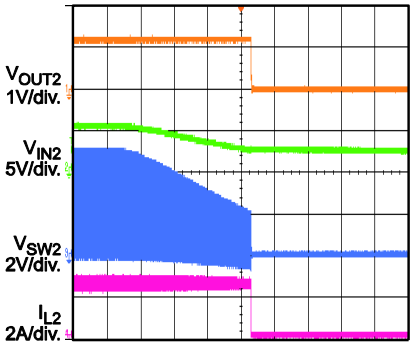
EN Down with 3.5A Load (CH1)
V_{IN}=5V, V_{OUT1}=1.2V, I_{OUT1}=3.5A



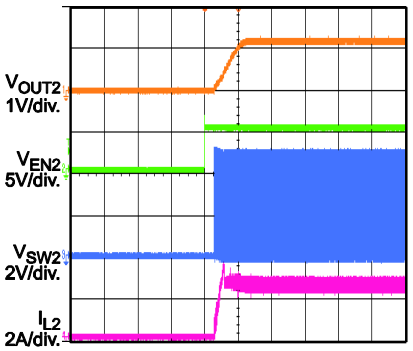
VIN Power-On with 2.5A Load (CH2)
V_{IN}=5V, V_{OUT2}=1.2V, I_{OUT2}=2.5A



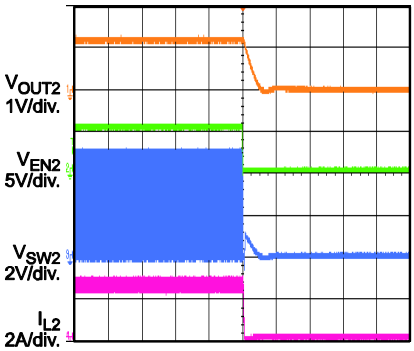
VIN Power-Down with 2.5A Load (CH2)
V_{IN}=5V, V_{OUT2}=1.2V, I_{OUT2}=2.5A



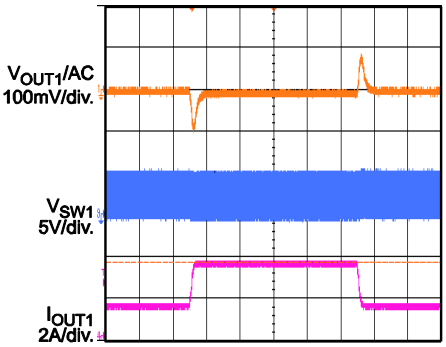
Enable On with 2.5A Load (CH2)
V_{IN}=5V, V_{OUT2}=1.2V, I_{OUT2}=2.5A



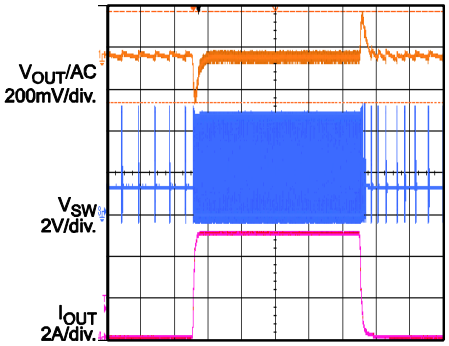
Enable Down with 2.5A Load (CH2)
V_{IN}=5V, V_{OUT2}=1.2V, I_{OUT2}=2.5A



CH1 Transient
V_{IN}=5V, V_{OUT1}=1.2V, 1A Transient to 3.5A, 2.5A/µs Speed



CH1 Transient
V_{IN}=5V, V_{OUT1}=1.2V, 1A Transient to 5A, 2.5A/µs Speed



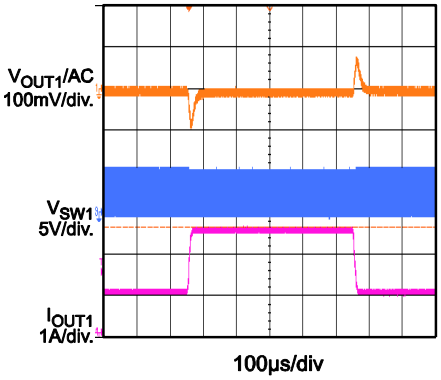
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.2V, V_{OUT2} = 1.2V, L1 = 0.47µH, L2 = 0.47µH, T_A = +25°C, unless otherwise noted.

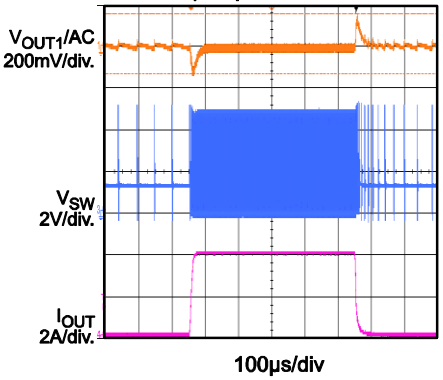
CH2 Transient

V_{IN}=5V, V_{OUT2}=1.2V, 1A Transient to 2.5A, 2.5A/µs Speed



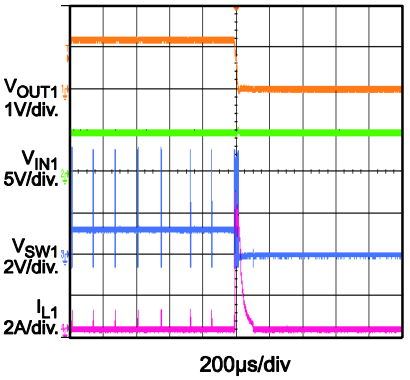
CH2 Transient

V_{IN}=5V, V_{OUT2}=1.2V, 1A Transient to 4A, 2.5A/µs Speed



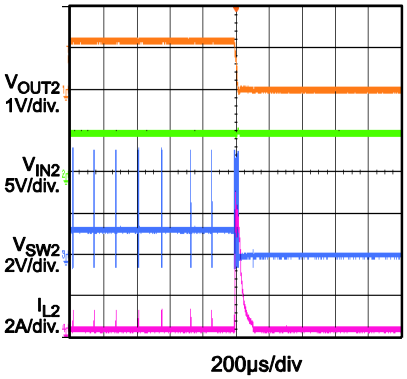
CH1 Short Enter

V_{IN}=5V, V_{OUT1}=1.2V, I_{OUT1}=0A



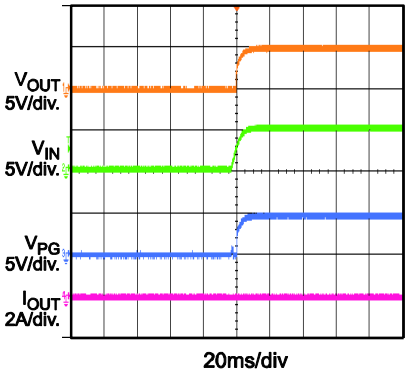
CH2 Short Enter

V_{IN}=5V, V_{OUT2}=1.2V, I_{OUT2}=0A



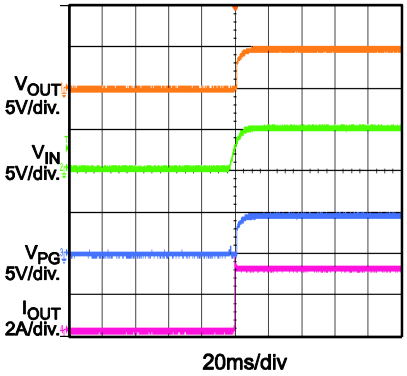
VIN Start-Up (Load Switch)

V_{IN}=5V, V_{OUT}=5V, I_{OUT}=0A



VIN Start-Up (Load Switch)

V_{IN}=5V, V_{OUT}=5V, I_{OUT}=3A

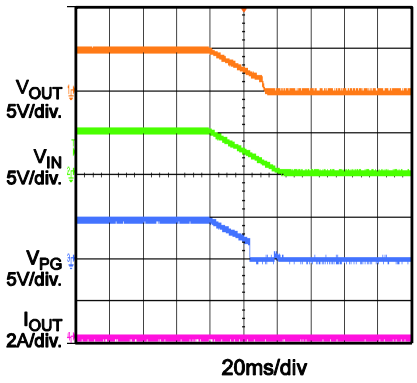


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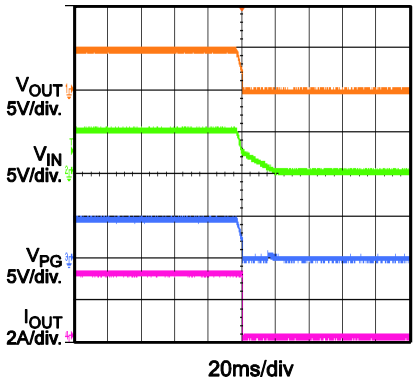
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.2V, V_{OUT2} = 1.2V, L1 = 0.47µH, L2 = 0.47µH, T_A = +25°C, unless otherwise noted.

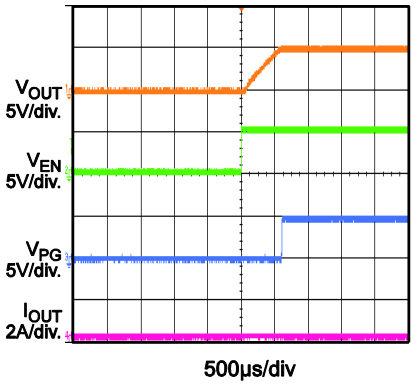
VIN Shutdown (Load Switch)
V_{IN}=5V, V_{OUT}=5V, I_{OUT}=0A



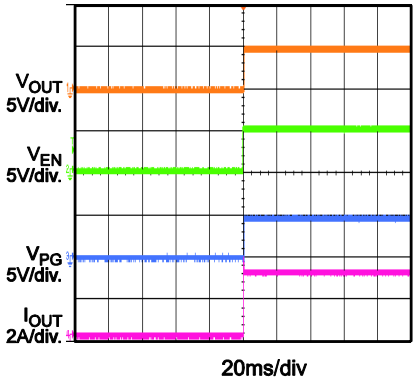
VIN Shutdown (Load Switch)
V_{IN}=5V, V_{OUT}=5V, I_{OUT}=3A



EN Startup (Load Switch)
V_{IN}=5V, V_{OUT}=5V, I_{OUT}=0A



EN Startup (Load Switch)
V_{IN}=5V, V_{OUT}=5V, I_{OUT}=3A



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PIN FUNCTIONS

Pin #	Name	Description
1	C_{DELAY}	**Programmable PFL low-to-high delay time.** When C_{DELAY} is floated, the delay time is minimized.
2	PFL_ADJ	**Power failure threshold adjust.** A resistor divider connected to the voltage rails is used to program the power failure threshold. The resistor divider must be monitored.
3	VIN1	**Input supply voltage to the peak 5A switching regulators.** Place a small decoupling capacitor as close as possible to VIN1 and GND as possible.
4	AGND	**Analog ground.**
5	GND	**Ground.**
6	VIN2	**Input supply voltage to the peak 4A switching regulators.** Place a small decoupling capacitor as close to VIN2 and GND as possible.
7	FB1	**Feedback voltage sense for the peak 5A regulator.** Connect the output voltage of the peak 5A regulator through a resistor divider to FB1 to achieve voltage regulation. Pull FB1 to ground to operate the peak 5A regulator in 100% duty cycle on mode.
8	FB2	**Feedback voltage sense for the peak 4A regulator.** Connect the output voltage of the peak 4A regulator through a resistor divider to FB2 to achieve output voltage regulation. Pull FB2 to ground to operate the peak 4A regulator in 100% duty cycle on mode.
9	EN1	**Enable on/off control for the peak 5A regulator.** There is a 2MΩ resistor from EN1 to GND internally. Float or ground EN1 to turn off the peak 5A regulator.
10	EN2	**Enable on/off control for the peak 4A regulator.** There is a 2MΩ resistor from EN2 to GND internally. Float or ground EN2 to turn off the peak 4A regulator.
11	EN3	**Enable on/off control for the load switch.** There is a 2MΩ resistor from EN3 to GND internally. Float or ground EN3 to turn off the load switch.
12	SW2	**Switch output for the peak 4A regulator.** A thick, wide power routing trace is recommended for SW2 to conduct current.
13	V_{SUS}	**Sustain voltage.** Place a small decoupling capacitor as close to V_{SUS} and GND as possible.
14	SW1	**Switch output for the peak 5A regulator.** A thick and wide power routing trace is recommended for SW1 to conduct current.
15	PG1	**Power good for the peak 5A regulator.** PG1 is an open-drain output. When the output voltage is between -10% to +30% of the regulation windows, PG1 is pulled high externally. When there is no supply, PG1 is pulled low internally.
16	PG2	**Power good for peak 4A regulator.** PG2 is an open-drain output. When the output voltage is between -10% to +30% of the regulation windows, PG2 is pulled high externally. When there is no supply, PG2 is pulled low internally.
17	PG3	**Power good for the load switch.** PG3 is an open-drain output. When the output voltage is below 200mV compared with the input voltage, PG3 is pulled high externally.
18	VIN3	**Input supply voltage for the load switch.**
19	OUT3	**Output voltage for the load switch.**
20	PFL	**Power failure indicator.** PFL is an open-drain output. When the PFL_ADJ voltage is less than 0.6V, PFL is pulled low immediately.

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BLOCK DIAGRAM

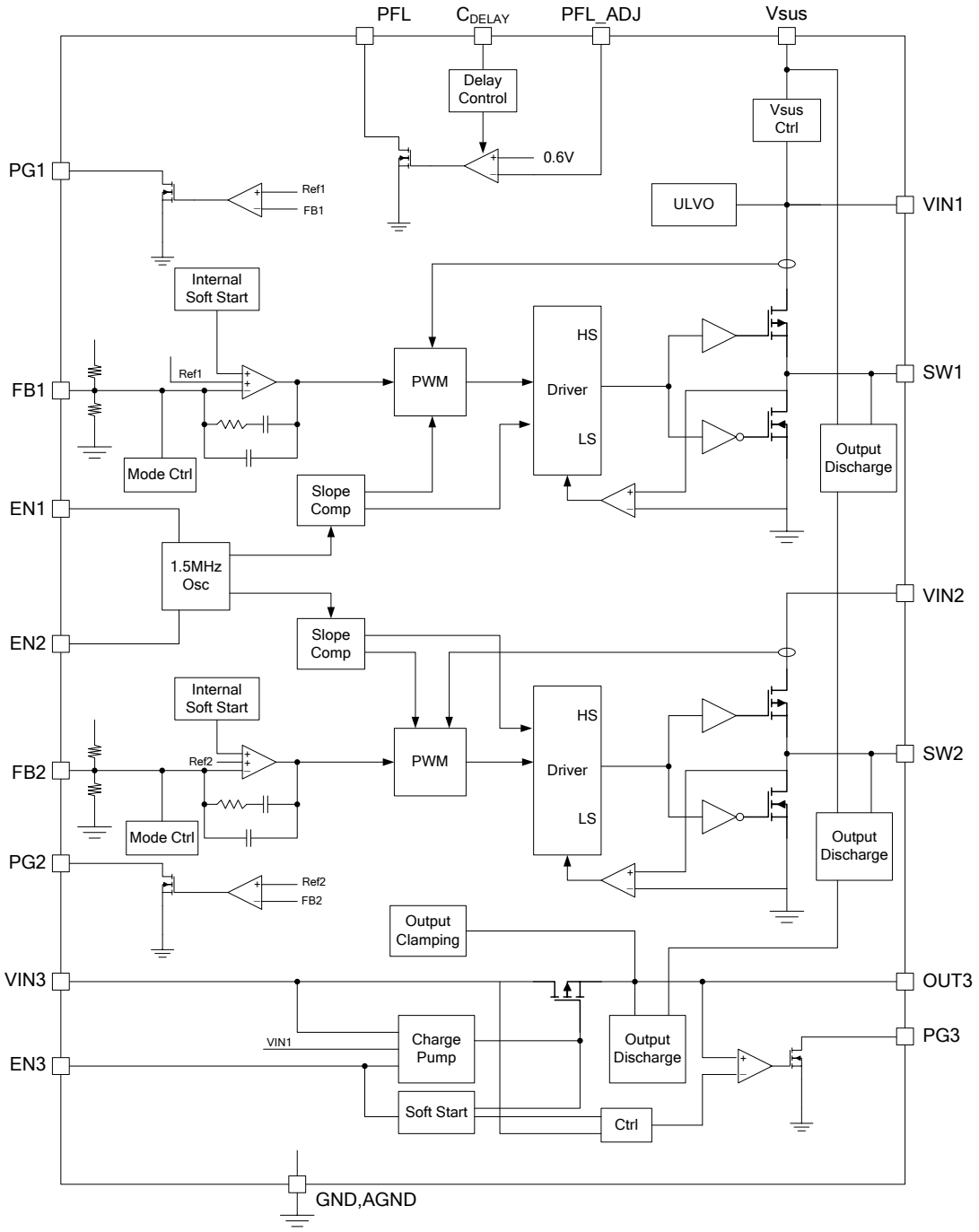


Figure 1: Functional Block Diagram

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OPERATION

The MP5403B has two step-down regulators and one load switch integrated into an ultra-small UTQFN-20 package. The two buck regulators are able to run up to a peak 5A and peak 4A load current, respectively. With a peak-current-mode control scheme and an interleaving PWM clock, the MP5403B minimizes the input voltage ripple and achieves a fast dynamic load response. A 3A load switch with only 20mΩ of $R_{DS(ON)}$ can achieve extremely small conduction loss and provide tight regulation with a high load current. The load switch can also clamp VOUT to 5.5V. The MP5403B can be used in compact solid-state drives (SSD), portable instruments, and battery-powered devices.

Peak-Current-Mode Control

The two buck regulators of the MP5403B operate at an 180° phase shift to reduce the input current ripple and the required input capacitor. In continuous conduction mode (CCM), two internal clocks control the switching behavior. The high-side MOSFET (HS-FET) turns on at the corresponding clock's rising edge. Two clocks are at an 180° phase shift. With the high-side switch current increases and reaches the internal compensation voltage, the high-side switch is turned off, and the low-side switch is turned on to conduct current.

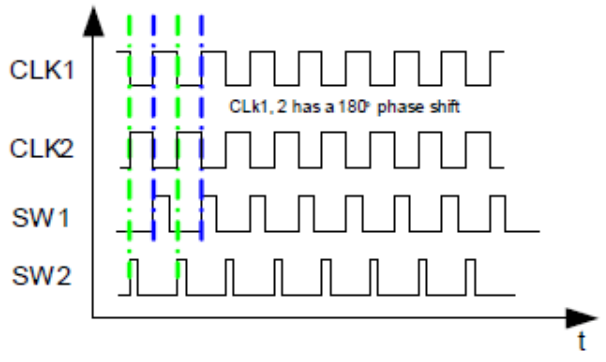


Figure 2: Phase Shift

The switching frequency is 1.5MHz, typically, running in CCM. With a lower input voltage, the switching frequency falls and works with a large duty cycle and a fixed off-time mode.

Light-Load Operation

In light-load mode, the MP5403B uses a proprietary control scheme to save power and improve efficiency. The MP5403B turns off the low-side switch when the inductor current begins reversing. Then MP5403B works in discontinuous conduction mode (DCM) operation. With light-load mode control, the switching loss can be reduced greatly due to the lower switching frequency.

A zero-current cross detection (ZCD) circuit is used to detect if the inductor current begins reversing. Considering the internal circuit propagation time, the typical delay is 50ns. This means that the inductor current continues falling after ZCD is triggered in this delay. If the inductor current falling slew rate is fast (V_{OUT} is high or close to VIN), the low-side MOSFET (LS-FET) is turned off, and the inductor current may be negative. This prevents the MP5403B from entering DCM operation. If DCM operation is required, the off time of the LS-FET in CCM should be longer than 100ns. For example, if V_{IN} is 3.6V and V_{OUT} is 3.4V, then the off time in CCM is 37ns. It is difficult to enter DCM at light load. Using a smaller inductor can improve this and make it easier to enter DCM.

Enable (EN)

When VIN1 is greater than the under-voltage lockout (UVLO) threshold (typically 2.7V), the regulators or the load switch can be enabled by pulling its EN pins above the EN UVLO threshold. Leave the EN pins floating or pull the EN pins down to ground to disable the corresponding channel. There is an internal 2MΩ resistor from the EN pins to ground. There is a delay of about 100µs for VIN1 and VIN2 enable start-up. The VIN3 enable start-up delay is shorter (around 70µs).

Soft Start (SS) and Output Discharge

The MP5403B has a built-in soft start (SS) that ramps up the output voltage at a controlled slew rate to prevent overshooting at start-up for both step-down regulators and the load switch. The soft-start time is set to around 0.35ms. When the regulators are disabled, the internal discharge resistor discharges V_{OUT}. The discharge resistor is biased by V_{SUS} (see Table 1).

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Table 1: Output Discharge Conditions

Output Discharge	VIN	EN
No	>UVLO	High
Yes	>UVLO	Low
Yes	<UVLO	High
Yes	<UVLO	Low

Power Good (PG) Indicators

The MP5403B has three separate power good (PG), open-drain, output indicators for the regulators and load switch. For the two step-down regulators, when FB is in the regulation window (between 90% to 130% of the reference voltage, 0.6V), PG1 and PG2 pins are pulled up to the external bus voltage through certain external resistors. The pull-up resistors are recommend not to be too low to ensure that the leakage current is small when the PG pins are low and not too high if they are used to drive downstream signals. Normally, pull-up resistors between 10kΩ to 400kΩ are sufficient. The PG rising delay is around 20μs. If the FB voltage drops below 90% or rises above 130% of the reference voltage, the PG pins are pulled down to ground by an internal MOSFET. The MOSFET has a maximum $R_{DS(ON)}$ of less than 400Ω. There is also a 60μs delay for the PG falling threshold trigger.

The power good pin for the load switch (PG3) is pulled high when the input voltage of the load switch (VIN3) is higher than its UVLO threshold, the output voltage (VOUT3) is less than 200mV compared with the input voltage of the load switch, and there is around 40μs of rising delay for the PG3 indicator. If any of these three conditions are not met, PG3 is pulled low.

The PG indicators are pulled low when VIN1 is below UVLO. In this condition, the PG pins are self-driven low (around 0.6V).

Power Failure Indicator (PFL)

The power failure indicator (PFL) senses the external voltage rails. When the input voltage is below the programmed threshold, the PFL open-drain output is pulled low immediately to indicate the monitored power failure. PFL_ADJ is used to adjust the power failure threshold voltage. A resistor divider is used to monitor the voltage rail. When the PFL_ADJ voltage is lower than 0.6V, PFL is pulled down to indicate the sense power failure. When the PFL_ADJ voltage is higher than the 0.6V reference voltage, PFL is pulled high with the delay, which is set by C_{DELAY}.

Choose C_{DELAY} using Equation (1):

$$T_{DELAY}(\mu s) = \frac{C_{DELAY}(pF) \times 0.62}{I_{DELAY}(\mu A)} + 3.5\mu s \quad (1)$$

Where T_{DELAY} is the PFL delay time, and I_{DELAY} is the C_{DELAY} internal current source (typically 3.1μA).

Current Limit

The MP5403B has a high-side 6.2A current limit for the first regulator and a 5A current limit for the second regulator. When the high-side switch reaches the current-limit threshold, the regulators shut down the high-side switch and force the low-side switch on until the low-side current drops to the low-side valley current threshold (peak 5A and peak 4A for the two regulators). After the low-side current reaches the valley current threshold, the high-side switch can turn on again. If the high load current persists, the high-side turns on again, and the current-limit mechanism repeats until the output voltage drops to the short-circuit threshold. If the high-load current does not persist, then the regulator resumes normal conditions.

For the load switch, the current limit begins working when the load switch current reaches the current-limit threshold. The gate is pulled low to regulate the load switch current to the current limit. The output voltage drops until thermal shutdown occurs.

Short Circuit and Recovery

When CH1 or CH2 is in buck mode, the MP5403B enters short-circuit protection (SCP) mode when the inductor current reaches the current limit for 300μs continuously or the output voltage drops below 50% of the regulation voltage. In SCP mode, the MP5403B disables the output power stage, discharges the soft-start capacitor, and enters latch-off protection mode. The MP5403B restarts by recycling the power.

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Load Switch Mode of Buck 1/2

By pulling FB1 or FB2 to ground, the step-down regulator 1 or 2 can enter load-switch mode without having to install an inductor. The MP5403B pulses a smaller current to the FB pins before the system starts up. If a low impedance is connected to the FB pins, the MP5403B enters load-switch mode, where the high-side switch is turned on gradually to achieve a soft start, and SCP is equipped.

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APPLICATION INFORMATION

Output Voltage Setting

The output voltage of the two switchers can be adjusted with the external resistor dividers (see Figure 3). The typical reference voltage of both FB1 and FB2 is 600mV. The maximum allowed voltage for the outputs is close to the input voltage minus the voltage drop when the high-side switch is 100% turned on.

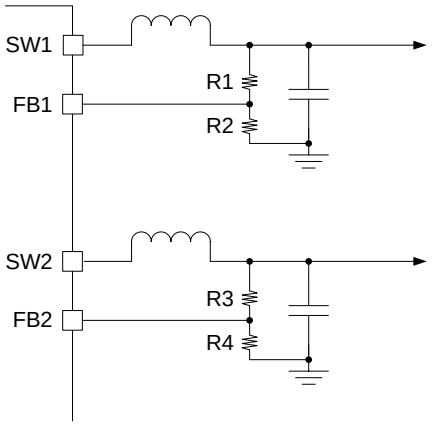


Figure 3: Feedback Resistor Dividers to Set the Output Voltages

The divider current is recommended to be higher than 500nA to avoid influence from the feedback node leakage current (which is in the 10nA level). Considering control loop optimization, the pull-high resistor is recommended to be between 100 - 500kΩ. Then, the pull-down resistor can be calculated with Equation (2):

$$R2(orR4) = \frac{R1(orR3)}{\frac{V_{OUT}}{0.6V} - 1} \quad (2)$$

Table 2 shows some typical output voltages and their corresponding recommended resistor divider values.

Table 2: Output Voltage vs. Resistor Values

V_{OUT}	R1	R2
1.2V	300kΩ	300kΩ
1.5V	300kΩ	200kΩ
1.8V	300kΩ	150kΩ
2.5V	300kΩ	95.3kΩ
3.3V	300kΩ	66.5kΩ

NOTE: C_{OUT} is 22µF for each channel.

Selecting the Inductor

The inductor has a great impact on several key performances for the step-down switcher, such as inductor current ripple, output voltage ripple, efficiency, and load transient response.

Calculate the inductor current ripple with Equation (3):

$$\Delta I_L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \cdot L \cdot f_{SW}} \quad (3)$$

Calculate the inductor peak current with Equation (4):

$$I_{Lpk} = I_{Load} + \frac{\Delta I_L}{2} \quad (4)$$

Choosing the inductance is a trade-off between the output ripple, efficiency, and transient response. The larger the inductance is, the smaller the output ripple, but the slower the response. Choose an inductance that makes the ripple current 30 - 40% of the max load current.

The inductor saturation current must be higher than the inductor peak current.

The inductor also impacts the solution efficiency in terms of conduction loss and frequency- and coil-related loss. Generally, the DC resistance provides DC conduction loss information. For AC conduction loss and coil-related loss, refer to the vendor's datasheet for more detailed information.

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and the switching noise from the device. Select an input capacitor with switching frequency impedance that is less than the input source impedance to prevent high-frequency switching current from passing to the input source. Use low ESR ceramic capacitors with X5R or X7R dielectrics with small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

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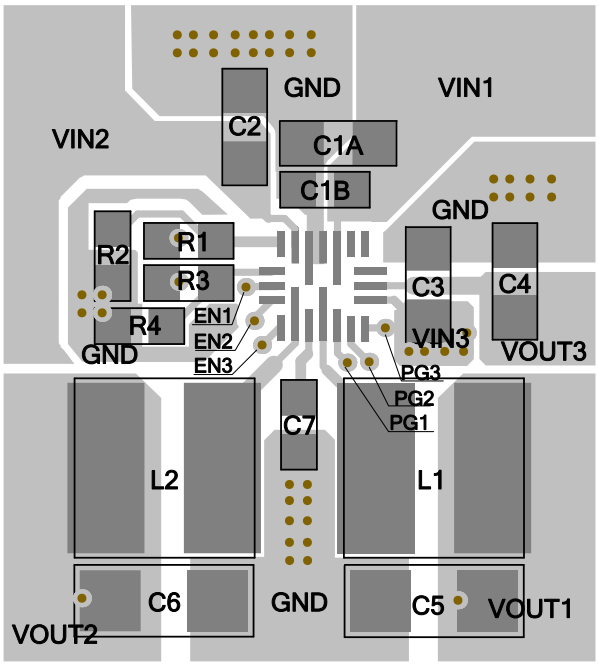
Output Capacitor Selection

The output capacitor limits the output voltage ripple and ensures a stable regulation loop. Select an output capacitor with low impedance at the switching frequency. Use ceramic capacitors with X5R or X7R dielectrics. Using an electrolytic capacitor may result in additional output voltage ripple, thermal issues, and require additional care in selecting the feedback resistor (R1) due to the large ESR. For most applications, a 22µF capacitor is sufficient.

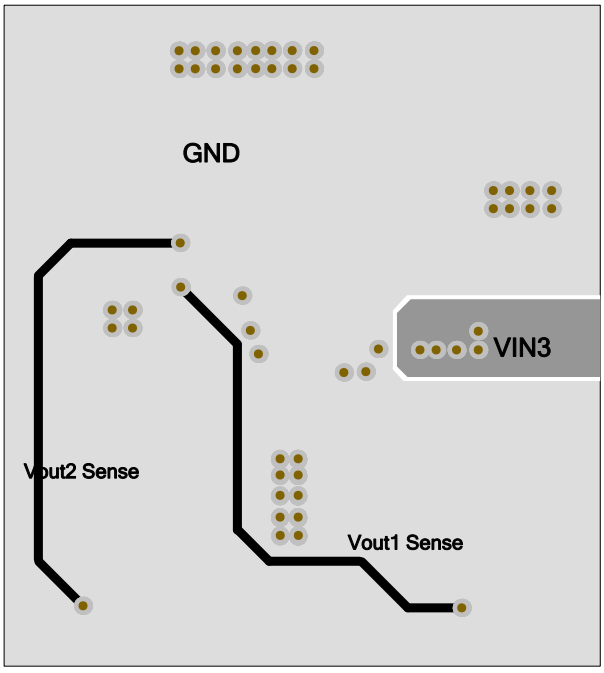
PCB Layout Guidelines

Efficient PCB layout of the switching power supplies is critical for stable operation. If the layout is not done carefully, for the high switching frequency converter especially, the regulator could show poor line or load regulation and stability issues. For best results, refer to Figure 4 and follow the guideline below.

1. Place the input capacitor as close to the IC pins as possible for the high-speed step-down regulator to provide clean control voltage.



Top Layer



Bottom Layer

Figure 4: Recommended Layout

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TYPICAL APPLICATION CIRCUIT

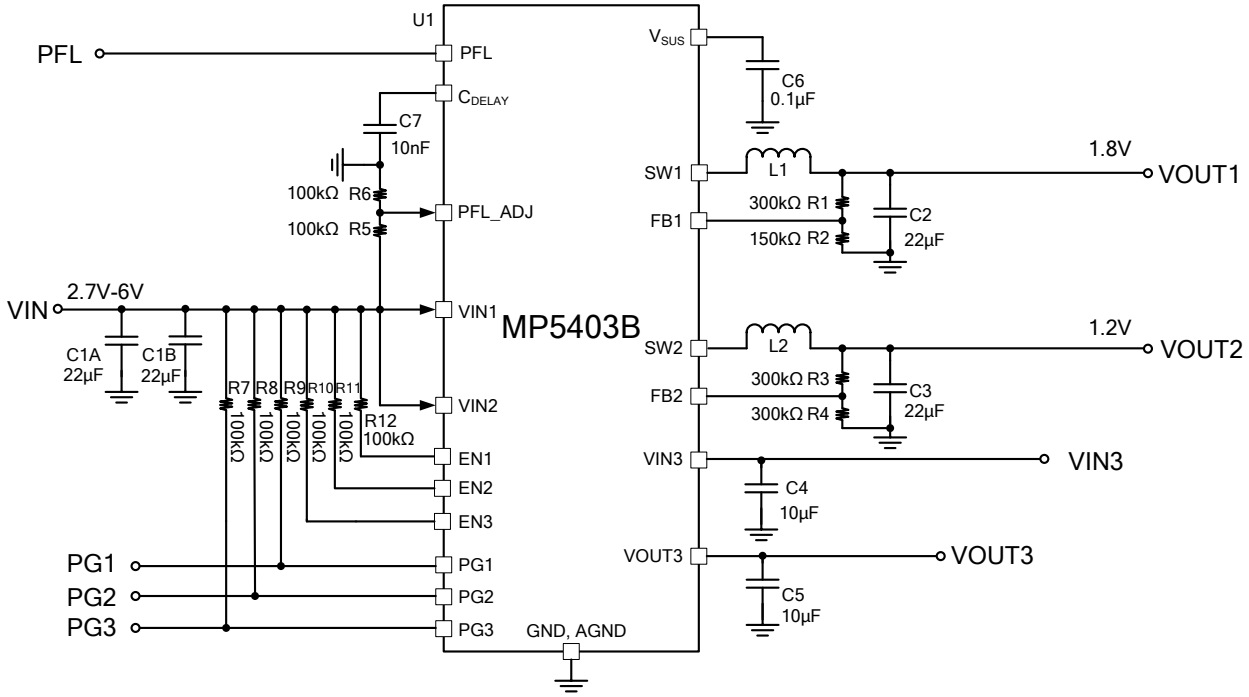
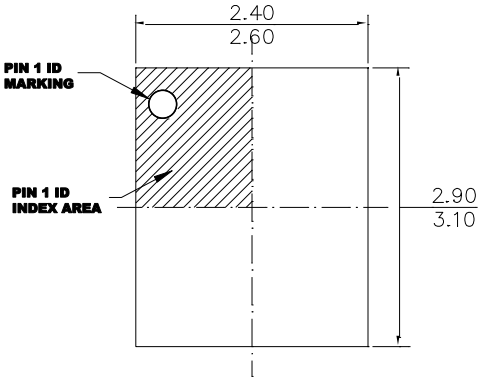


Figure 6: Typical System Architecture by Using Two Units

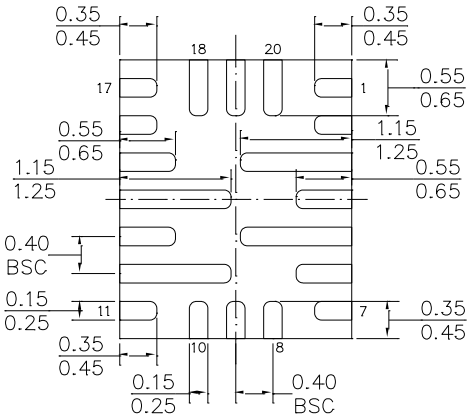
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PACKAGE INFORMATION

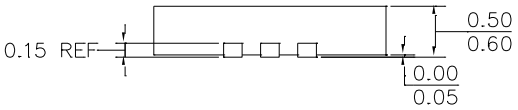
UTQFN-20 (2.5mmX3mm)



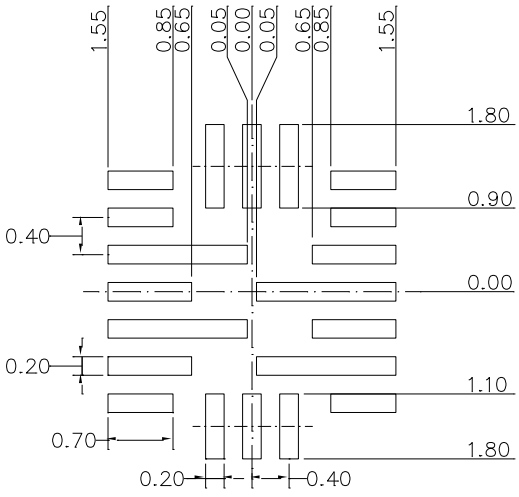
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERN OF PIN3,5,12 AND 14 HAVE THE SAME LENGTH AND WIDTH.
2) LAND PATTERN OF PIN4,6,13 AND 15 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
5) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
6) DRAWING CONFIRMS TO JEDEC MO-220.
7) DRAWING IS NOT TO SCALE.

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