10-Bit, 4× Oversampled SDTV Video Decoder with Differential Inputs and Deinterlacer

Data Sheet

ADV7283

FEATURES

- Worldwide NTSC/PAL/SECAM color demodulation support
- One 10-bit analog-to-digital converter (ADC), 4× oversampling per channel for CVBS, Y/C, and YPrPb modes
- 6 analog video input channels with on-chip antialiasing filters
- Video input support for CVBS (composite), Y/C (S-Video), and YPrPb (component)
- Fully differential, pseudo differential, and single-ended CVBS video input support
- NTSC/PAL/SECAM autodetection
- Up to 4 V common-mode input range solution
- Excellent common-mode noise rejection capabilities
- 5-line adaptive 2D comb filter and CTI video enhancement
- Adaptive Digital Line Length Tracking (ADLLT), signal processing, and enhanced FIFO management provide time-base correction (TBC) functionality
- Integrated automatic gain control (AGC) with adaptive peak white mode
- Fast switching capability
- Integrated interlaced-to-progressive (I2P) video output converter (deinterlacer)
- Adaptive contrast enhancement (ACE)
- Down dither (8-bit to 6-bit)
- Rovi® (Macrovision) copy protection detection
- 8-bit ITU-R BT.656 YCrCb 4:2:2 output
- Full featured vertical blanking interval (VBI) data slicer with world system teletext (WST) support
- Power-down mode available
- 2-wire, I²C-compatible serial interface
- Qualified for automotive applications
- −40°C to +105°C automotive temperature grade
- −40°C to +85°C industrial qualified temperature grade
- 32-lead, 5 mm × 5 mm, RoHS-compliant LFCSP

APPLICATIONS

- Automotive infotainment
- Smartphone/multimedia handsets
- DVRs for video security
- Media players

GENERAL DESCRIPTION

The ADV7283 is a versatile one-chip, multiformat video decoder that automatically detects standard analog baseband video signals compatible with worldwide NTSC, PAL, and SECAM standards in the form of composite, S-Video, and component video.

The ADV7283 converts the analog video signals into a YCrCb 4:2:2 video data stream that is compatible with the 8-bit ITU-R BT.656 interface standard.

The six analog video inputs of the ADV7283 can accept single-ended, pseudo differential, and fully differential signals. The ADV7283 contains a deinterlacer (I2P converter) that allows the device to output video in a progressive format.

The ADV7283 is programmed via a 2-wire, serial bidirectional port (I²C compatible) and is fabricated in a 1.8 V CMOS process.

The ADV7283 is provided in a space-saving LFCSP surface-mount, RoHS-compliant package.

The ADV7283 is available in an automotive grade rated over the −40°C to +105°C temperature range, as well as a −40°C to +85°C temperature range, making the device ideal for both automotive and industrial applications.

Rev. A
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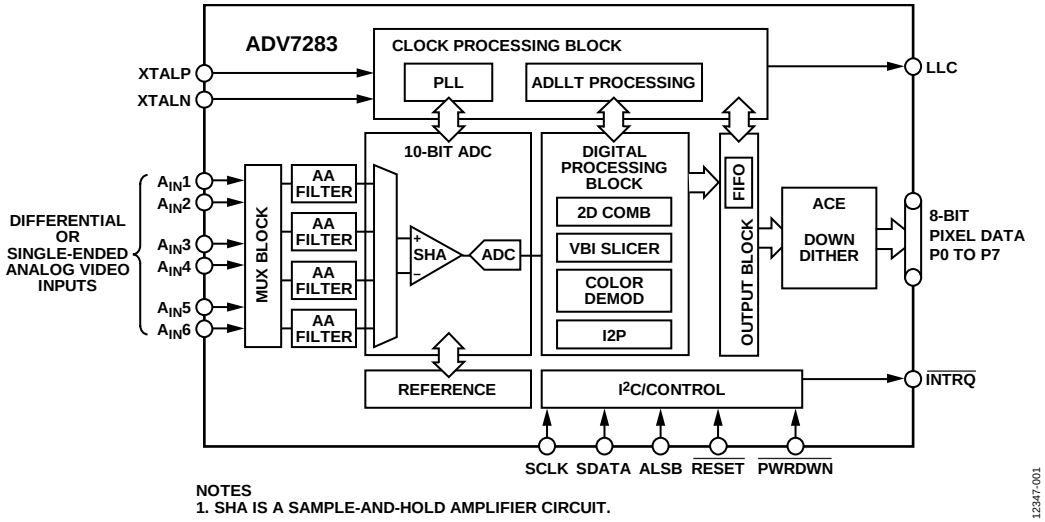
REVISION HISTORY

10/2016—Rev. 0 to Rev. A

Changes to Ordering Guide 21

5/2014—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. SHA IS A SAMPLE-AND-HOLD AMPLIFIER CIRCUIT.

Figure 1.

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE						
ADC Resolution	N				10	Bits
Integral Nonlinearity	INL	CVBS mode		2		LSB
Differential Nonlinearity	DNL	CVBS mode		±0.6		LSB
DIGITAL INPUTS						
Input High Voltage	V_{IH}	D_{VDDIO} = 3.3 V	2			V
		D_{VDDIO} = 1.8 V	1.2			V
Input Low Voltage	V_{IL}	D_{VDDIO} = 3.3 V			0.8	V
		D_{VDDIO} = 1.8 V			0.4	V
Input Leakage Current	I_{IN}	$\overline{\text{RESET}}$ pin	−10		+10	µA
		SDATA, SCLK pins	−10		+15	µA
		$\overline{\text{PWRDWN}}$, ALSB pins	−10		+50	µA
Input Capacitance	C_{IN}				10	pF
CRYSTAL INPUT						
Input High Voltage	V_{IH}	XTALN pin	1.2			V
Input Low Voltage	V_{IL}	XTALN pin			0.4	V
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	D_{VDDIO} = 3.3 V, I_{SOURCE} = 0.4 mA	2.4			V
		D_{VDDIO} = 1.8 V, I_{SOURCE} = 0.4 mA	1.4			V
Output Low Voltage	V_{OL}	D_{VDDIO} = 3.3 V, I_{SINK} = 3.2 mA			0.4	V
		D_{VDDIO} = 1.8 V, I_{SINK} = 1.6 mA			0.2	V
High Impedance Leakage Current	I_{LEAK}				10	µA
Output Capacitance	C_{OUT}				20	pF
POWER REQUIREMENTS[1, 2, 3]						
Digital I/O Power Supply	D_{VDDIO}		1.62	3.3	3.63	V
PLL Power Supply	P_{VDD}		1.71	1.8	1.89	V
Analog Power Supply	A_{VDD}		1.71	1.8	1.89	V
Digital Power Supply	D_{VDD}		1.71	1.8	1.89	V
Digital I/O Supply Current	I_{DVDDIO}			5		mA
PLL Supply Current	I_{PVDD}			12		mA
Analog Supply Current	I_{AVDD}					
Single-Ended CVBS Input				47		mA
Differential CVBS Input		Fully differential and pseudo differential CVBS		69		mA
Y/C Input				60		mA
YPrPb Input				75		mA
Digital Supply Current	I_{DVDD}					
Single-Ended CVBS Input				70		mA
Differential CVBS Input		Fully differential and pseudo differential CVBS		70		mA
Y/C Input				70		mA
YPrPb Input				70		mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER-DOWN CURRENTS[1]						
Digital I/O Supply Power-Down Current	I_{DVDDIO_PD}			73		µA
PLL Supply Power-Down Current	I_{PVDD_PD}			46		µA
Analog Supply Power-Down Current	I_{AVDD_PD}			0.2		µA
Digital Supply Power-Down Current	I_{DVDD_PD}			420		µA
Total Power Dissipation in Power-Down Mode				1		mW

[1] Guaranteed by characterization.
[2] Typical current consumption values are measured with nominal voltage supply levels and an SMPTE bar test pattern.
[3] All specifications apply when the I2P core is activated, unless otherwise stated.

VIDEO SPECIFICATIONS

A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS[1]						
Differential Phase	DP	CVBS input, modulated five-step		0.9		Degrees
Differential Gain	DG	CVBS input, modulated five-step		0.5		%
Luma Nonlinearity	LNL	CVBS input, five-step		2.0		%
NOISE SPECIFICATIONS						
Signal-to-Noise Ratio (SNR), Unweighted	SNR	Luma ramp		57.1		dB
		Luma flat field		58		dB
Analog Front-End Crosstalk				60		dB
Common-Mode Rejection Ratio[2]	CMRR			73		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			−5		+5	%
Vertical Lock Range			40		70	Hz
Subcarrier Lock Range	f_{SC}			±1.3		kHz
Color Lock-In Time				60		Lines
Synchronization Depth Range			20		200	%
Color Burst Range			5		200	%
Fast Switch Speed[3]				100		ms

[1] These specifications apply for all CVBS input types (NTSC, PAL, and SECAM), as well as for single-ended and differential CVBS inputs.
[2] The CMRR of this circuit design is critically dependent on the external resistor matching on the circuit inputs (see the Input Networks section). The CMRR measurement was performed with 0.1% tolerant resistors, a common-mode voltage of 1 V, and a common-mode frequency of 10 kHz.
[3] Fast switch speed is the time required for the ADV7283 to switch from one analog input (single-ended or differential) to another, for example, switching from $A_{IN}1$ to $A_{IN}2$.

ANALOG SPECIFICATIONS

A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLAMP CIRCUITRY					
External Clamp Capacitor			0.1		µF
Input Impedance	Clamps switched off		10		MΩ
Large Clamp Source Current			0.4		mA
Large Clamp Sink Current			0.4		mA
Fine Clamp Source Current			10		µA
Fine Clamp Sink Current			10		µA

CLOCK AND I²C TIMING SPECIFICATIONS

A_{VDD}, D_{VDD}, and P_{VDD}= 1.71 V to 1.89 V, D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL					
Nominal Frequency			28.63636		MHz
Frequency Stability				±50	ppm
I²C PORT					
SCLK Frequency				400	kHz
SCLK Minimum Pulse Width High	t_1	0.6			µs
SCLK Minimum Pulse Width Low	t_2	1.3			µs
Hold Time (Start Condition)	t_3	0.6			µs
Setup Time (Start Condition)	t_4	0.6			µs
SDATA Setup Time	t_5	100			ns
SCLK and SDATA Rise Times	t_6			300	ns
SCLK and SDATA Fall Times	t_7			300	ns
Setup Time (Stop Condition)	t_8		0.6		µs
$\overline{\text{RESET}}$ INPUT					
$\overline{\text{RESET}}$ Pulse Width		5			ms

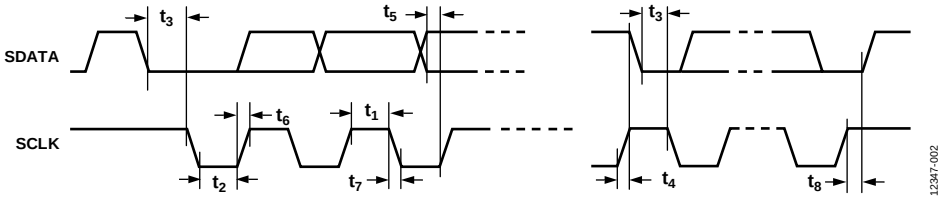


Figure 2. I²C Timing Diagram

PIXEL PORT TIMING SPECIFICATIONS

A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK OUTPUTS						
LLC Output Frequency				27		MHz
LLC Mark Space Ratio	t_{16}:t_{17}		45:55		55:45	% duty cycle
DATA AND CONTROL OUTPUTS						
Data Output Transitional Time	t_{18}	Negative clock edge to start of valid data ($t_{SETUP} = t_{17} - t_{18}$)			3.8	ns
	t_{19}	End of valid data to negative clock edge ($t_{HOLD} = t_{16} - t_{19}$)			6.9	ns

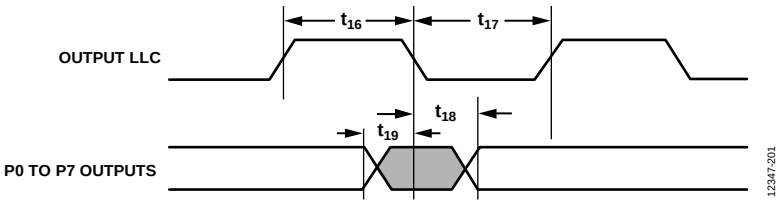


Figure 3. Pixel Port and Control Output Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter[1]	Rating
A_{VDD} to GND	2.2 V
D_{VDD} to GND	2.2 V
P_{VDD} to GND	2.2 V
D_{VDDIO} to GND	4 V
P_{VDD} to D_{VDD}	−0.9 V to +0.9 V
A_{VDD} to D_{VDD}	−0.9 V to +0.9 V
Digital Inputs ($\overline{RESET}$, ALSB, SDATA, SCLK, $\overline{PWRDWN}$) Voltage	GND − 0.3 V to D_{VDDIO} + 0.3 V
Digital Outputs (P7 to P0, $\overline{INTRQ}$, LLC) Voltage	GND − 0.3 V to D_{VDDIO} + 0.3 V
Analog Inputs (XTALN, $A_{IN}1$ to $A_{IN}6$) to Ground	GND − 0.3 V to A_{VDD} + 0.3 V
Maximum Junction Temperature (T_J max)	140°C
Storage Temperature Range	−65°C to +150°C

[1] The absolute maximum ratings assume that the DGND pins and the exposed pad of the ADV7283 are connected together to a common ground plane (GND). This is part of the recommended layout scheme. See the PCB Layout Recommendations section for more information. The absolute maximum ratings are stated in relation to this common ground plane.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

The thermal resistance values in Table 7 are specified for the device soldered onto a 4-layer printed circuit board (PCB) with a common ground plane (GND) and with the exposed pad of the device connected to DGND. The values in Table 7 are maximum values.

Table 7. Thermal Resistance for the 32-Lead LFCSP

Thermal Characteristic	Symbol	Value	Unit
Junction to Ambient Thermal Resistance (Still Air)	θ_{JA}	32.5	°C/W
Junction to Case Thermal Resistance	θ_{JC}	2.3	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

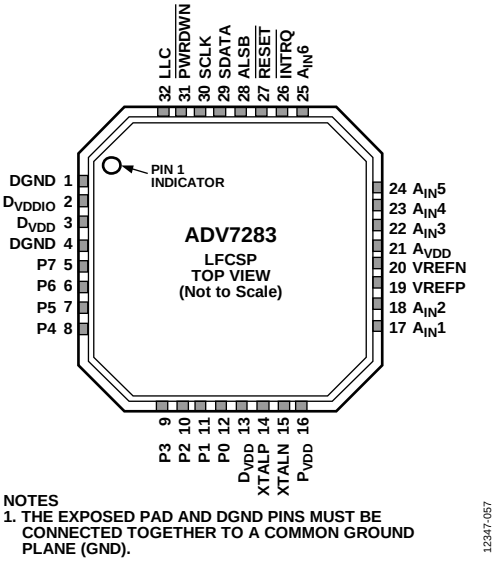


Figure 4. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 4	DGND	Ground	Ground for Digital Supply. The exposed pad and DGND pins must be connected together to a common ground plane (GND).
2	D_{VDDIO}	Power	Digital Input/Output Power Supply (1.8 V or 3.3 V).
3, 13	D_{VDD}	Power	Digital Power Supply (1.8 V).
5 to 12	P7 to P0	Output	Video Pixel Output Ports.
14	XTALP	Output	Output for the External 28.63636 MHz Crystal. Connect this pin to the external 28.63636 MHz crystal, or leave it unconnected if an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the ADV7283. The crystal used with the ADV7283 must be a fundamental crystal.
15	XTALN	Input	Input Pin for the External 28.63636 MHz Crystal. The crystal used with the ADV7283 must be a fundamental crystal. If an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the ADV7283, the output of the oscillator is fed into the XTALN pin.
16	P_{VDD}	Power	PLL Power Supply (1.8 V).
17,18, 22 to 25	$A_{IN}1$ to $A_{IN}6$	Input	Analog Video Input Channels.
19	VREFP	Output	Internal Voltage Reference Output.
20	VREFN	Output	Internal Voltage Reference Output.
21	A_{VDD}	Power	Analog Power Supply (1.8 V).
26	$\overline{\text{INTRQ}}$	Output	Interrupt Request Output. An interrupt occurs when certain signals are detected on the input video.
27	$\overline{\text{RESET}}$	Input	System Reset Input (Active Low). A minimum low reset pulse width of 5 ms is required to reset the ADV7283 circuitry.
28	ALSB	Input	Selector for the I²C Write Address. When ALSB is set to Logic 0, the write address is 0x40; when ALSB is set to Logic 1, the write address is 0x42.
29	SDATA	Input/output	I²C Port Serial Data Input/Output.
30	SCLK	Input	I²C Port Serial Clock Input. The maximum clock rate is 400 kHz.
31	$\overline{\text{PWRDWN}}$	Input	Power-Down Pin. A logic low on this pin places the ADV7283 in power-down mode.
32	LLC	Output	Line-Locked Output Clock for Output Pixel Data. The clock output is typically 27 MHz, but it increases or decreases according to the video line length.
	EPAD (EP)		Exposed Pad. The exposed pad and DGND pins must be connected together to a common ground plane (GND).

THEORY OF OPERATION

The ADV7283 is a versatile one-chip, multiformat video decoder. The device automatically detects standard analog baseband video signals compatible with worldwide NTSC, PAL, and SECAM standards in the form of composite, S-Video, and component video.

The ADV7283 converts the analog video signals into an 8-bit YCrCb 4:2:2 video data stream that is compatible with the 8-bit ITU-R BT.656 interface standard.

The analog video inputs of the ADV7283 accept single-ended, pseudo differential, and fully differential composite video signals, as well as S-Video and YPrPb video signals, supporting a wide range of consumer and automotive video sources.

In differential CVBS mode, the ADV7283, along with an external resistor divider, provides a common-mode input range of up to 4 V, enabling the removal of large signal, common-mode transients present on the video lines.

The advanced I2P function allows the ADV7283 to convert an interlaced video input into a progressive video output. This function is performed without the need for external memory. The ADV7283 uses edge adaptive technology to minimize video defects on low angle lines.

The AGC and clamp restore circuitry allow an input video signal peak-to-peak range of 1.0 V p-p at the analog video input pins of the ADV7283. Alternatively, the AGC and clamp restore circuitry can be bypassed for manual settings.

The external ac coupling capacitors protect the ADV7283 from short-to-battery (STB) events on the analog video input pins.

The ADV7283 supports a number of other functions, including 8-bit to 6-bit down dither mode and ACE.

The ADV7283 is programmed via a 2-wire, serial bidirectional port (I^2C compatible) and is fabricated in a 1.8 V CMOS process. The monolithic CMOS construction of the ADV7283 ensures greater functionality with lower power dissipation.

The ADV7283 is provided in a space-saving LFCSP surface-mount, RoHS-compliant package.

The ADV7283 is available in an automotive grade that is rated over the −40°C to +105°C temperature range, making the device ideal for automotive applications.

The ADV7283 is also available in a −40°C to +85°C temperature range, making it ideal for industrial applications.

ANALOG FRONT END

The analog front end (AFE) of the ADV7283 comprises a single high speed, 10-bit ADC that digitizes the analog video signal before applying it to the standard definition processor (SDP). The AFE uses differential channels to the ADC to ensure high performance in mixed-signal applications and to enable differential CVBS inputs to connect directly to the ADV7283.

The AFE also includes an input mux that enables the application of multiple video signals to the ADV7283. The input mux allows the application of up to six composite video signals to the ADV7283.

Current clamps are positioned in front of the ADC to ensure that the video signal remains within the range of the converter.

A resistor divider network is required before each analog input channel to ensure that the input signal is kept within the range of the ADC (see the Input Networks section). Fine clamping of the video signal is performed downstream by digital fine clamping within the ADV7283.

Table 9 lists the three ADC clock rates that are determined by the video input format to be processed. These clock rates ensure 4× oversampling per channel for CVBS, Y/C, and YPrPb modes.

Table 9. ADC Clock Rates

Input Format	ADC Clock Rate (MHz)[1]	Oversampling Rate per Channel
CVBS (Composite)	57.27	4×
Y/C (S-Video)	114	4×
YPrPb (Component)	172	4×

[1] Based on a 28.63636 MHz crystal between the XTALP and XTALN pins.

The fully differential AFE of the ADV7283 provides inherent small and large signal noise rejection, improved electromagnetic interference (EMI) protection, and the ability to absorb ground bounce. Support is provided for both true differential and pseudo differential signals.

STANDARD DEFINITION PROCESSOR

The ADV7283 can decode a large selection of baseband video signals in composite (both single-ended and differential), S-Video, and component formats. The video processor supports the following standards:

- PAL B, PAL D, PAL G, PAL H, PAL I, PAL M, PAL N, PAL Nc, PAL 60
- NTSC J, NTSC M, NTSC 4.43
- SECAM B, SECAM D, SECAM G, SECAM K, SECAM L

Using the SDP, the ADV7283 can automatically detect the video standard and process it accordingly.

The ADV7283 has a five-line adaptive 2D comb filter that provides superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to the video standard and signal quality without user intervention. Video user controls such as brightness, contrast, saturation, and hue are also available with the ADV7283.

The ADV7283 implements the patented Adaptive Digital Line Length Tracking (ADLLT™) algorithm to track varying video line lengths from sources such as VCRs. ADLLT enables the ADV7283 to track and decode poor quality video sources such as VCRs and noisy sources from tuner outputs and camcorders.

The ADV7283 contains a chroma transient improvement (CTI) processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

The ACE feature of the ADV7283 offers improved visual detail using an algorithm that automatically varies contrast levels to enhance picture detail. ACE increases the contrast in dark areas of an image without saturating the bright areas of the image. This feature is particularly useful in automotive applications, where it can be important to discern objects in shaded areas.

Down dithering converts the output of the ADV7283 from an 8-bit to a 6-bit output, enabling ease of design for standard LCD panels.

The I2P block converts the interlaced video input into a progressive video output without the need for external memory.

The SDP can process a variety of VBI data services, such as closed captioning (CCAP), wide screen signaling (WSS), copy generation management systems (CGMS), and teletext data slicing for world system teletext (WST).

The ADV7283 is fully Rovi® (Macrovision) compliant; detection circuitry enables Type I, Type II, and Type III protection levels to be identified and reported to the user. The decoder is also fully robust to all Rovi signal inputs.

POWER SUPPLY SEQUENCING

OPTIMAL POWER-UP SEQUENCE

The optimal power-up sequence for the ADV7283 is to first power up the 3.3 V D_{VDDIO} supply, followed by the 1.8 V supplies (D_{VDD}, P_{VDD}, and A_{VDD}).

When powering up the ADV7283, follow these steps (during power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section):

1. Assert the $\overline{\text{PWRDWN}}$ and $\overline{\text{RESET}}$ pins (pull the pins low).
2. Power up the D_{VDDIO} supply.
3. After D_{VDDIO} is fully asserted, power up the 1.8 V supplies.
4. After the 1.8 V supplies are fully asserted, pull the $\overline{\text{PWRDWN}}$ pin high.
5. Wait 5 ms and then pull the $\overline{\text{RESET}}$ pin high.
6. After all power supplies and the $\overline{\text{PWRDWN}}$ and $\overline{\text{RESET}}$ pins are powered up and stable, wait an additional 5 ms before initiating I^2C communication with the ADV7283.

SIMPLIFIED POWER-UP SEQUENCE

Alternatively, the ADV7283 can be powered up by asserting all supplies and the $\overline{\text{PWRDWN}}$ and $\overline{\text{RESET}}$ pins simultaneously. After this operation, perform a software reset, then wait 10 ms before initiating I^2C communication with the ADV7283.

While the supplies are being established, ensure that a lower rated supply does not go above a higher rated supply level. During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

POWER-DOWN SEQUENCE

The ADV7283 supplies can be deasserted simultaneously as long as D_{VDDIO} does not go below a lower rated supply.

D_{VDDIO} SUPPLY VOLTAGE

Under normal operating conditions, the ADV7283 operates with a nominal D_{VDDIO} voltage of 3.3 V. The device can also operate with a nominal D_{VDDIO} voltage of 1.8 V. When operating with a nominal voltage of 1.8 V, apply the power-up sequences described in the Optimal Power-Up Sequence and Simplified Power-Up Sequence sections. The only changes are that D_{VDDIO} is powered up to 1.8 V instead of 3.3 V, and the $\overline{\text{PWRDWN}}$ and $\overline{\text{RESET}}$ pins of the ADV7283 are powered up to 1.8 V instead of 3.3 V.

Note that when the ADV7283 operates with a nominal D_{VDDIO} voltage of 1.8 V, then set the drive strength of all digital outputs to a maximum.

Note that when D_{VDDIO} is set to a nominal voltage of 1.8 V, no pins can be pulled up to 3.3 V. For example, pull the I^2C pins of the ADV7283 (SCLK and SDATA) up to 1.8 V instead of 3.3 V.

POWER SUPPLY REQUIREMENTS

Table 10 shows the current rating recommendations for power supply design. Use these values when designing a power supply section to ensure that an adequate current is supplied to the ADV7283.

Table 10. Current Rating Recommendations for Power Supply Design

Current	Rating
I_{DVDDIO}	20 mA
I_{DVDD}	110 mA
I_{AVDD}	100 mA
I_{PVDD}	20 mA

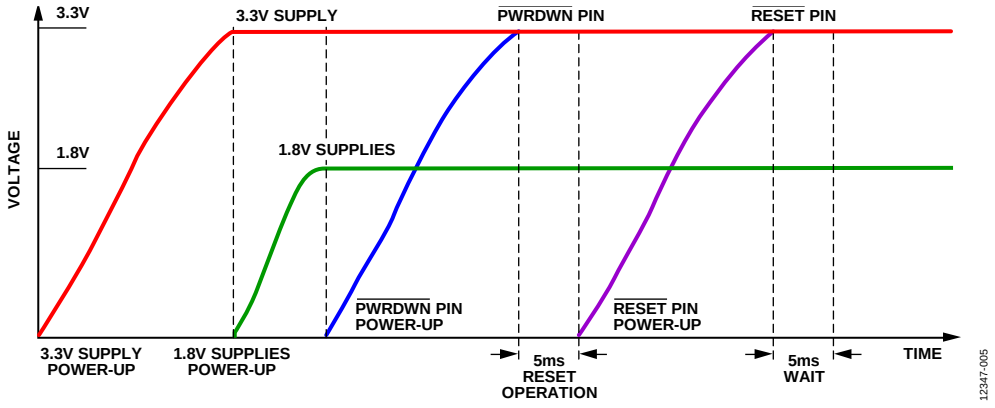


Figure 5. Optimal Power-Up Sequence

INPUT NETWORKS

An input network (external resistor and capacitor circuit) is required on the $A_{IN}x$ input pins of the ADV7283. The components of the input network depend on the video format selected for the analog input.

SINGLE-ENDED INPUT NETWORK

Figure 6 shows the input network to use on each $A_{IN}x$ input pin of the ADV7283 when any of the following video input formats are used:

- Single-ended CVBS
- Y/C (S-Video)
- YPrPb

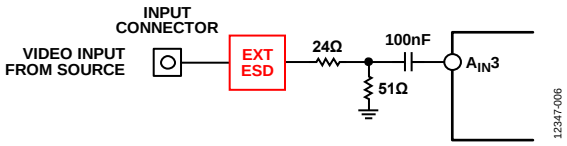


Figure 6. Single-Ended Input Network

The 24 Ω and 51 Ω resistors supply the 75 Ω end termination required for the analog video input. These resistors also create a resistor divider with a gain of 0.68. The resistor divider attenuates the amplitude of the input analog video and scales the input to the ADC range of the ADV7283. This allows an input range of up to 1.47 V p-p. Note that amplifiers within the ADC restore the amplitude of the input signal so SNR performance is maintained.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into the $A_{IN}x$ pins of the ADV7283. The clamping circuitry within the ADV7283 restores the dc bias of the input signal to the optimal level before it is fed into the ADC of the ADV7283.

DIFFERENTIAL INPUT NETWORK

Figure 7 shows the input network to use when differential CVBS video is input on the $A_{IN}x$ input pins of the ADV7283.

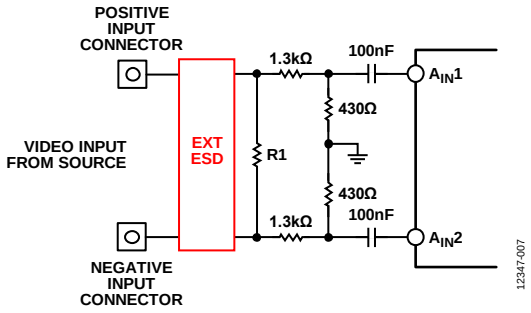


Figure 7. Differential Input Network

Fully differential video transmission involves transmitting two complementary CVBS signals. Pseudo differential video transmission involves transmitting a CVBS signal and a source ground signal.

Differential video transmission has several key advantages over single-ended transmission, including

- Inherent small signal and large signal noise rejection
- Improved EMI performance
- An ability to absorb ground bounce

Resistor R1 provides the RF end termination for the differential CVBS input lines. For a pseudo differential CVBS input, a value of 75 Ω is recommended for R1. For a fully differential CVBS input, a value of 150 Ω is recommended for R1.

The 1.3 kΩ and 430 Ω resistors create a resistor divider with a gain of 0.25. The resistor divider attenuates the amplitude of the input analog video, but increases the input common-mode range of the ADV7283 to 4 V p-p. Note that amplifiers within the ADC restore the amplitude of the input signal so that SNR performance is maintained.

The 100 nF ac coupling capacitors remove the dc bias of the analog input video before it is fed into the $A_{IN}x$ pins of the ADV7283. The clamping circuitry within the ADV7283 restores the dc bias of the input signal to the optimal level before it is fed into the ADC of the ADV7283.

The combination of the 1.3 kΩ and 430 Ω resistors and the 100 nF ac coupling capacitors limits the current flow into the ADV7283 during STB events (see the Short-to-Battery Protection section).

To achieve optimal performance, the 1.3 kΩ and 430 Ω resistors must be closely matched; that is, all 1.3 kΩ and 430 Ω resistors must have the same resistance tolerance, and this tolerance must be as low as possible.

SHORT-TO-BATTERY PROTECTION

In differential mode, the ADV7283 is protected against STB events by the external 100 nF ac coupling capacitors (see Figure 7). The external input network resistors are sized to be large enough to reduce the current flow during an STB event, but small enough to avoid affecting the operation of the ADV7283.

The power rating of the input network resistors must be chosen withstand the high voltages of STB events. Similarly, ensure that the breakdown voltage of the ac coupling capacitors is robust enough to handle STB events.

The R1 resistor is protected because no current or limited current flows through it during an STB event.

APPLICATIONS INFORMATION

INPUT CONFIGURATION

The input format of the ADV7283 is specified using the INSEL[4:0] bits (see Table 11). These bits also configure the SDP core to process CVBS, differential CVBS, Y/C (S-Video), or component (YPrPb) format. The INSEL[4:0] bits are located in the user sub map of the register space at Address 0x00[4:0]. For more information about the registers, see the Register Maps section.

The INSEL[4:0] bits specify predefined analog input routing schemes, eliminating the need for manual mux programming and allowing the user to route the various video signal types to the decoder. For example, if the CVBS input is selected, the remaining channels are powered down.

Table 11. Input Format Specified by the INSEL[4:0] Bits

INSEL[4:0] Bit Value	Video Format	Analog Inputs
00000	CVBS	CVBS input on $A_{IN}1$
00001	CVBS	CVBS input on $A_{IN}2$
00010	CVBS	CVBS input on $A_{IN}3$
00011	CVBS	CVBS input on $A_{IN}4$
00100	Reserved	Reserved
00101	Reserved	Reserved
00110	CVBS	CVBS input on $A_{IN}5$
00111	CVBS	CVBS input on $A_{IN}6$
01000	Y/C (S-Video)	Y input on $A_{IN}1$ C input on $A_{IN}2$
01001	Y/C (S-Video)	Y input on $A_{IN}3$ C input on $A_{IN}4$
01010	Reserved	Reserved
01011	Y/C (S-Video)	Y input on $A_{IN}5$ C input on $A_{IN}6$
01100	YPrPb	Y input on $A_{IN}1$ Pb input on $A_{IN}2$ Pr input on $A_{IN}3$
01101	Reserved	Reserved
01110	Differential CVBS	Positive input on $A_{IN}1$ Negative input on $A_{IN}2$
01111	Differential CVBS	Positive input on $A_{IN}3$ Negative input on $A_{IN}4$
10000	Reserved	Reserved
10001	Differential CVBS	Positive input on $A_{IN}5$ Negative input on $A_{IN}6$
10010 to 11111	Reserved	Reserved

ADAPTIVE CONTRAST ENHANCEMENT

The ADV7283 can increase the contrast of an image depending on the content of the picture, making bright areas brighter and dark areas darker. The optional ACE feature increases the contrast within dark areas without significantly affecting the bright areas. The ACE feature is particularly useful in automotive applications, where it is important to discern objects in shaded areas.

The ACE function is disabled by default. To enable the ACE function, execute the following register writes:

1. Write 0x40 to Register 0x0E in User Sub Map (0x40 or 0x42). This enters User Sub Map 2.
2. Write 0x80 to Register 0x80 in User Sub Map 2 (0x40 or 0x42). This enables ACE.
3. Write 0x00 to Register 0x0E in User Sub Map 2 (0x40 or 0x42). This reenters User Sub Map.

To disable the ACE function, execute the following register writes:

1. Write 0x40 to Register 0x0E in User Sub Map (0x40 or 0x42). This enters User Sub Map 2.
2. Write 0x00 to Register 0x80 in User Sub Map 2 (0x40 or 0x42). This disables ACE.
3. Write 0x00 to Register 0x0E in User Sub Map 2 (0x40 or 0x42). This reenters User Sub Map.

I2P FUNCTION

The I2P function of the ADV7283 allows the device to convert an interlaced video input into a progressive video output. This function is performed without the need for external memory. The ADV7283 use edge adaptive technology to minimize video defects on low angle lines.

The I2P function is disabled by default. To enable the I2P function, use the recommended scripts from Analog Devices, Inc.

ITU-R BT.656 TRANSMITTER CONFIGURATION

The ADV7283 receives analog video and outputs digital video according to the ITU-R BT.656 specification. The ADV7283 outputs the ITU-R BT.656 video data stream over the P0 to P7 data pins, and has a line-locked clock (LLC) pin.

Video data is output over the P0 to P7 pins in YCrCb 4:2:2 format. Synchronization signals are automatically embedded in the video data signal in accordance with the ITU-R BT.656 specification.

The LLC output clocks the output data on the P0 to P7 pins at a nominal frequency of 27 MHz.

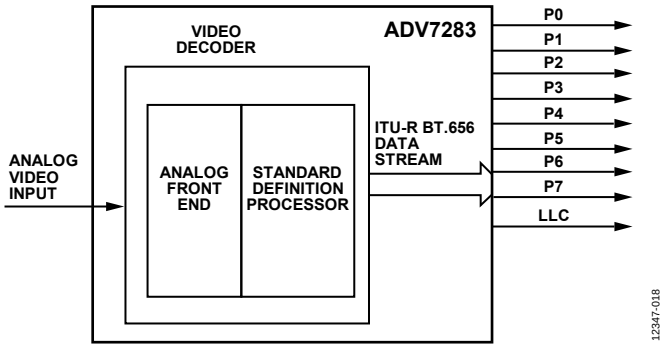


Figure 8. ITU-R BT.656 Output Stage

I²C PORT DESCRIPTION

The ADV7283 supports a 2-wire, I²C-compatible serial interface. Two inputs, serial data (SDATA) and serial clock (SCLK), carry information between the ADV7283 and the system I²C master controller. The I²C port of the ADV7283 allows the user to set up and configure the decoder and to read back captured VBI data.

The ADV7283 has a number of possible I²C slave addresses and subaddresses (see the Register Maps section). The main map of the ADV7283 has four possible slave addresses for read and write operations, depending on the logic level of the ALSB pin (see Table 12).

Table 12. Main Map I²C Address

ALSB Pin	R/$\overline{W}$ Bit	Slave Address
0	0	0x40 (write)
0	1	0x41 (read)
1	0	0x42 (write)
1	1	0x43 (read)

The ALSB pin controls Bit 1 of the slave address. By changing the logic level of the ALSB pin, it is possible to control two ADV7283 devices in an application without using the same I²C slave address. The LSB (Bit 0) specifies either a read or write operation: Logic 1 corresponds to a read operation, and Logic 0 corresponds to a write operation.

To control the device on the bus, a specific protocol is followed.

1. The master initiates a data transfer by establishing a start condition, which is defined as a high to low transition on SDATA while SCLK remains high, and indicates that an address/data stream follows.
2. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address plus the R/$\overline{W}$ bit). The bits are transferred from MSB to LSB.
3. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse; this is known as an acknowledge (ACK) bit.
4. All other devices withdraw from the bus and maintain an idle condition. In the idle condition, the device monitors the SDATA and SCLK lines for the start condition and the correct transmitted address.

The R/$\overline{W}$ bit determines the direction of the data. Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADV7283 acts as a standard I²C slave device on the bus. The data on the SDATA pin is eight bits long, supporting the 7-bit address plus the R/$\overline{W}$ bit. The device has subaddresses to enable access to the internal registers; therefore, it interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto-increment, allowing data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register individually without updating all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCLK high period, issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If the user issues an invalid subaddress, the ADV7283 does not issue an acknowledge and returns to the idle condition.

If the highest subaddress is exceeded in auto-increment mode, one of the following actions is taken:

- In read mode, the register contents of the highest subaddress continue to be output until the master device issues a no acknowledge, which indicates the end of a read. A no acknowledge condition occurs when the SDATA line is not pulled low on the ninth pulse.
- In write mode, the data for the invalid byte is not loaded into a subaddress register. The ADV7283 issues a no acknowledge, and the device returns to the idle condition.

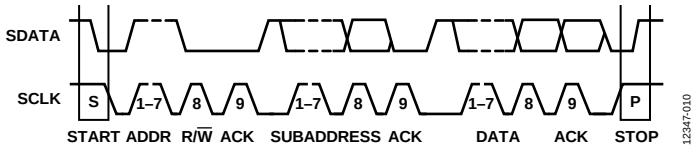


Figure 9. Bus Data Transfer

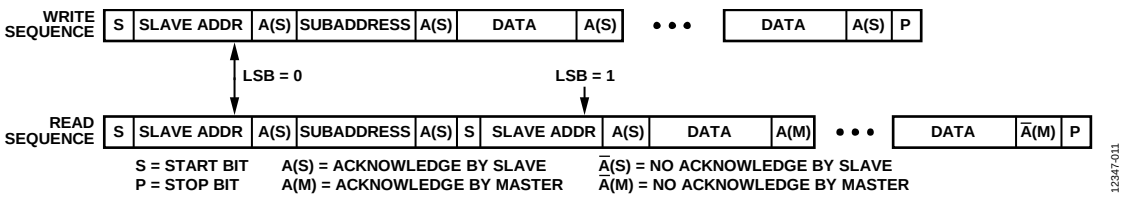


Figure 10. Read and Write Sequence

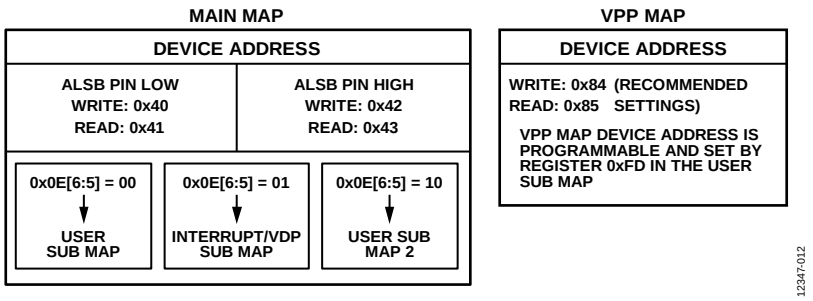


Figure 11. Register Map and Sub Map Access

REGISTER MAPS

The ADV7283 contains two register maps: the main register map and the VPP register map.

Note that the main map of the ADV7283 contains three sub maps: the user sub map, the interrupt/VDP map, and User Sub Map 2.

Main Map

The ALSB pin sets the I²C slave address of the main map of the ADV7283 (see Table 12). The main map allows the user to program the I²C slave addresses of the VPP map. The main map contains three sub maps: the user sub map, the interrupt/VDP sub map, and User Sub Map 2. These three sub maps are accessed by writing to the SUB_USR_EN bits (Address 0x0E[6:5]) within the main map (see Figure 11 and Table 13).

User Sub Map

The user sub map contains registers that program the analog front end and digital core of the ADV7283. The user sub map has the same I²C slave address as the main map. To access the user sub map, set the SUB_USR_EN bits in the main map (Address 0x0E[6:5]) to 00.

Interrupt/VDP Sub Map

The interrupt/VDP sub map contains registers that can be used to program internal interrupts, control the INTRQ pin, and decode VBI data.

The interrupt/VDP sub map has the same I²C slave address as the main map. To access the interrupt/VDP sub map, set the SUB_USR_EN bits in the main map (Address 0x0E[6:5]) to 01.

User Sub Map 2

User Sub Map 2 contains registers that control the ACE, down dither, and fast lock functions. It also contains controls that set the acceptable input luma and chroma limits before the ADV7283 enters free run and color kill modes.

User Sub Map 2 has the same I²C slave address as the main map. To access User Sub Map 2, set the SUB_USR_EN bits in the main map (Address 0x0E[6:5]) to 10.

VPP Map

The video postprocessor (VPP) map contains registers that control the I2P core (interlaced-to-progressive converter).

The VPP map has a programmable I²C slave address, which is programmed using Register 0xFD in the user sub map of the main map. The default value for the VPP map address is 0x00; however, the VPP map cannot be accessed until the I²C slave address is set. The recommended I²C slave address for the VPP map is 0x84.

To set the I²C slave address of the VPP map, write to the VPP_SLAVE_ADDRESS[7:1] bits of the user sub map (Address 0xFD[7:1]).

It is recommended to set the VPP_SLAVE_ADDRESS[7:1] bits to a value of 0x84. This sets the VPP map I²C write address to 0x84 and the I²C read address to 0x85.

SUB_USR_EN Bits, Address 0x0E[6:5]

The ADV7283 main map contains three sub maps: the user sub map, the interrupt/VDP sub map, and User Sub Map 2 (see Figure 11). The user sub map is available by default. The other two sub maps are accessed using the SUB_USR_EN bits. When programming of the interrupt/VDP map or User Sub Map 2 is completed, write to the SUB_USR_EN bits to return to the user sub map.

Table 13. I²C Register Map and Sub Map Addresses

ALSB Pin	R/$\overline{W}$ Bit	Slave Address	SUB_USR_EN Bits (Address 0x0E[6:5])	Register Map or Sub Map
0	0 (write)	0x40	00	User sub map
0	1 (read)	0x41	00	User sub map
0	0 (write)	0x40	01	Interrupt/VDP sub map
0	1 (read)	0x41	01	Interrupt/VDP sub map
0	0 (write)	0x40	10	User Sub Map 2
0	1 (read)	0x41	10	User Sub Map 2
1	0 (write)	0x42	00	User sub map
1	1 (read)	0x43	00	User sub map
1	0 (write)	0x42	01	Interrupt/VDP sub map
1	1 (read)	0x43	01	Interrupt/VDP sub map
1	0 (write)	0x42	10	User Sub Map 2
1	1 (read)	0x43	10	User Sub Map 2
X[1]	0 (write)	0x84	XX[1]	VPP map
X[1]	1 (read)	0x85	XX[1]	VPP map

[1] X and XX mean don't care.

PCB LAYOUT RECOMMENDATIONS

The ADV7283 is a high precision, high speed, mixed-signal device. To achieve maximum performance from the device, it is important to use a well designed PCB. This section provides guidelines for designing a PCB for use with the ADV7283.

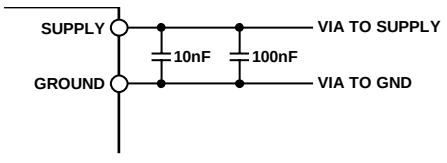
Analog Interface Inputs

When routing the analog interface inputs on the PCB, keep track lengths to a minimum. Use 75 Ω trace impedances when possible; trace impedances other than 75 Ω increase the chance of reflections.

Power Supply Decoupling

It is recommended that each power supply pin be decoupled with 100 nF and 10 nF capacitors. The basic principle is to place a decoupling capacitor within approximately 0.5 cm of each power pin. Avoid placing the decoupling capacitors on the opposite side of the PCB from the ADV7283 because doing so introduces inductive vias in the path.

Place the decoupling capacitors between the power plane and the power pin. Current must flow from the power plane to the capacitor and then to the power pin. Do not apply the power connection between the capacitor and the power pin. The best approach is to place a via close to or beneath the decoupling capacitor pads down to the power plane (see Figure 12).



NOTES
1. GND REFERS TO THE COMMON GROUND PLANE OF THE PCB.

Figure 12. Recommended Power Supply Decoupling

It is especially important to maintain low noise and good stability for the P_{VDD} pin. Pay careful attention to regulation, filtering, and decoupling. It is highly desirable to provide separate regulated supplies for each circuit group (A_{VDD}, D_{VDD}, D_{VDDIO}, and P_{VDD}).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This disparity can result in a measurable change in the voltage supplied to the analog supply regulator, which can, in turn, produce changes in the regulated analog supply voltage. To mitigate this problem, regulate the analog supply, or at least the P_{VDD} supply, from a different, cleaner power source, for example, from a 12 V supply.

Using a single ground plane for the entire board is recommended. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and can result in long ground loops. Therefore, using a single ground plane can improve noise performance.

VREFN and VREFP Pins

Place the circuit associated with the VREFN and VREFP pins as close as possible to the ADV7283 and on the same side of the PCB as the device.

Digital Outputs

The ADV7283 digital outputs are $\overline{\text{INTRQ}}$, LLC, and P0 to P7.

Minimize the trace length that the digital outputs must drive. Longer traces have higher capacitance, requiring more current and, in turn, causing more internal digital noise. Shorter traces reduce the possibility of reflections.

Adding a 30 Ω to 50 Ω series resistor can suppress reflections, reduce EMI, and reduce current spikes inside the ADV7283. If series resistors are used, place them as close as possible to the

pins of the ADV7283. However, do not add vias or extra length to the output trace in an attempt to place the resistors closer.

If possible, limit the capacitance that each digital output must drive to less than 15 pF. This recommendation can be easily accommodated by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside the ADV7283, creating more digital noise on the power supplies.

Exposed Metal Pad

The ADV7283 has an exposed metal pad on the bottom of the package. This pad must be soldered to ground. The exposed pad is used for proper heat dissipation, noise suppression, and mechanical strength.

Digital Inputs

The digital inputs of the ADV7283 are designed to work with 1.8 V signals (3.3 V for D_{VDDIO}) and are not tolerant of 5 V signals. Extra components are required if 5 V logic signals must be applied to the decoder.

TYPICAL CIRCUIT CONNECTION

Figure 13 provides an example of how to connect ADV7283. For detailed schematics of the ADV7283 evaluation board, contact a local Analog Devices field applications engineer or an Analog Devices distributor.

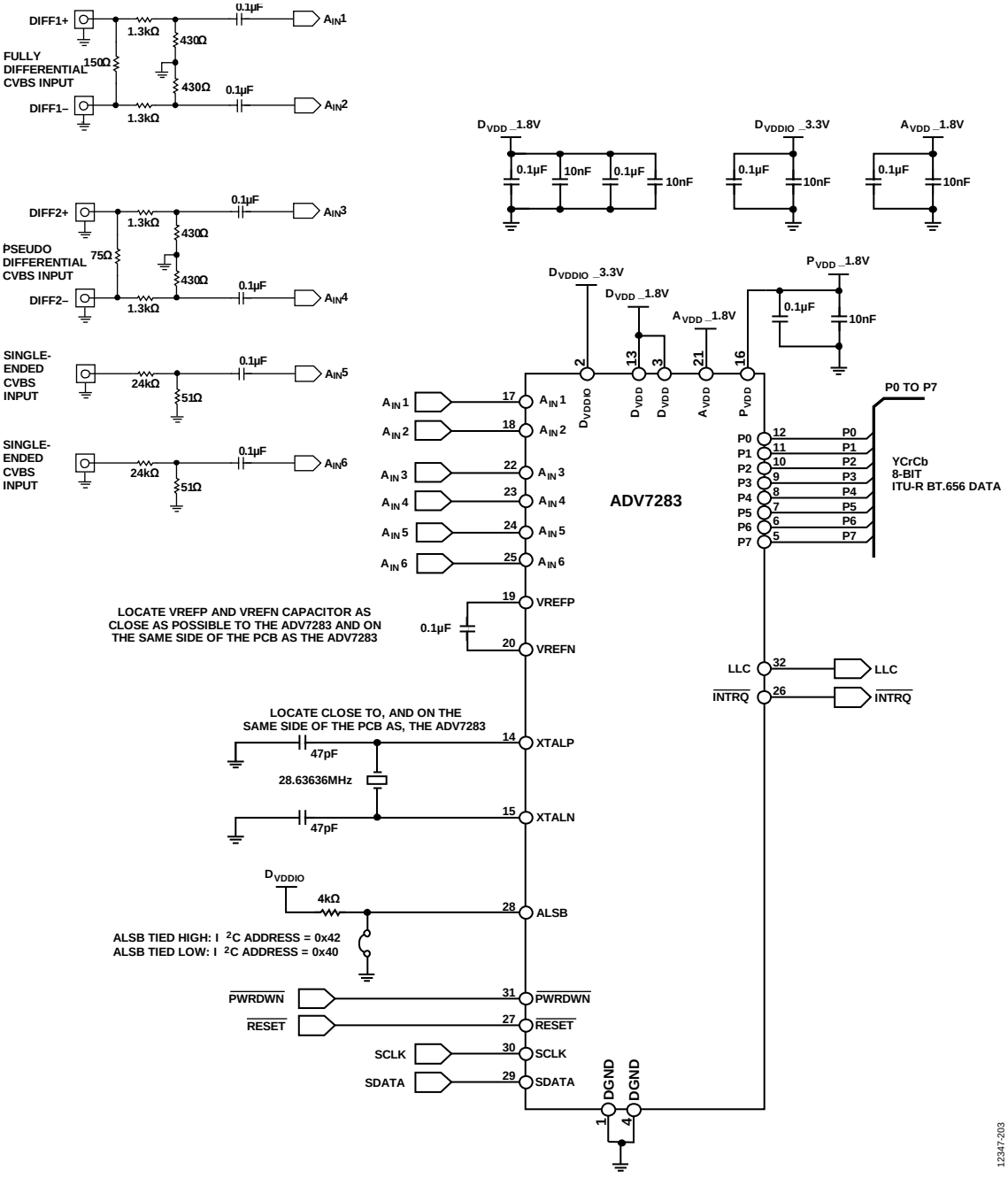


Figure 13. Typical Connection Diagram

OUTLINE DIMENSIONS

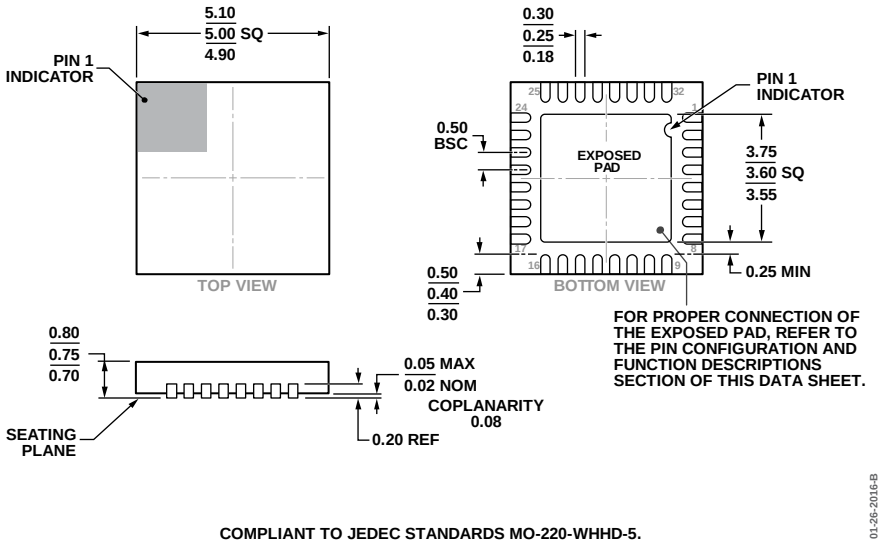


Figure 14. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADV7283BCPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7283BCPZ-RL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7283WBCPZ	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7283WBCPZ-RL	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
EVAL-ADV7283EBZ		Evaluation Board for the ADV7283	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADV7283W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for this model.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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