NSBC115TPDP6

Complementary Bias Resistor Transistors R1 = 100 kΩ, R2 = ∞ kΩ

NPN and PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

Features

- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

(T_A = 25°C both polarities Q1 (PNP) and Q2 (NPN), unless otherwise noted)

Rating	Symbol	Max	Unit
Collector−Base Voltage	V_{CBO}	50	Vdc
Collector−Emitter Voltage	V_{CEO}	50	Vdc
Collector Current − Continuous	I_C	100	mAdc
Input Forward Voltage	$V_{IN(fwd)}$	40	Vdc
Input Reverse Voltage −NPN −PNP	$V_{IN(rev)}$	 6 5	Vdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

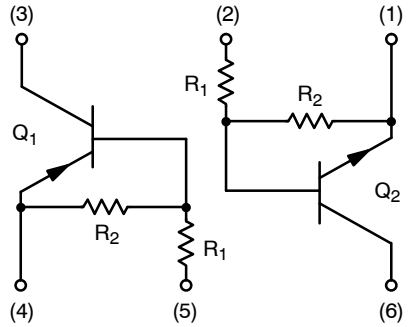
Device	Package	Shipping†
NSBC115TPDP6T5G	SOT−963	8,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

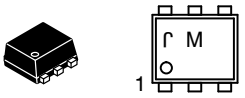
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PIN CONNECTIONS



MARKING DIAGRAMS



SOT−963
CASE 527AD

J = Specific Device Code
M = Date Code*

*Date Code orientation may vary depending upon manufacturing location.

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THERMAL CHARACTERISTICS

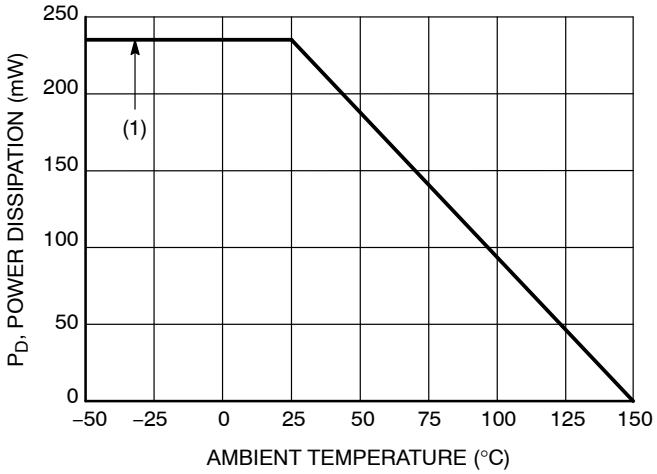
Characteristic	Symbol	Max	Unit
NSBC115TPDP6 (SOT−963) One Junction Heated			
Total Device Dissipation T_A = 25°C (Note 1) (Note 2) Derate above 25°C (Note 1) (Note 2)	P_D	 231 269 1.9 2.2	 mW mW/°C
Thermal Resistance, (Note 1) Junction to Ambient (Note 2)	$R_{\theta JA}$	540 464	°C/W
NSBC115TPDP6 (SOT−963) Both Junction Heated (Note 3)			
Total Device Dissipation T_A = 25°C (Note 1) (Note 2) Derate above 25°C (Note 1) (Note 2)	P_D	 339 408 2.7 3.3	 mW mW/°C
Thermal Resistance, (Note 1) Junction to Ambient (Note 2)	$R_{\theta JA}$	369 306	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

1. FR−4 @ 100 mm^2, 1 oz. copper traces, still air.
2. FR−4 @ 500 mm^2, 1 oz. copper traces, still air.
3. Both junction heated values assume total power is sum of two equally powered channels.

ELECTRICAL CHARACTERISTICS (T_A = 25°C both polarities Q_1 (PNP) and Q_2 (NPN), unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Base Cutoff Current (V_{CB} = 50 V, I_E = 0)	I_{CBO}	–	–	100	nAdc
Collector−Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)	I_{CEO}	–	–	500	nAdc
Emitter−Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	I_{EBO}	–	–	0.1	mAdc
Collector−Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	$V_{(BR)CBO}$	50	–	–	Vdc
Collector−Emitter Breakdown Voltage (Note 4) (I_C = 2.0 mA, I_B = 0)	$V_{(BR)CEO}$	50	–	–	Vdc
ON CHARACTERISTICS					
DC Current Gain (Note 4) (I_C = 5.0 mA, V_{CE} = 10 V)	h_{FE}	160	350	–	
Collector−Emitter Saturation Voltage (Note 4) (I_C = 10 mA, I_B = 1.0 mA)	$V_{CE(sat)}$	–	–	0.25	Vdc
Input Voltage (off) (V_{CE} = 5.0 V, I_C = 100 μA) (NPN) (V_{CE} = 5.0 V, I_C = 100 μA) (PNP)	$V_{i(off)}$	– –	0.6 0.62	– –	Vdc
Input Voltage (on) (V_{CE} = 0.2 V, I_C = 1.0 mA) (NPN) (V_{CE} = 0.2 V, I_C = 1.0 mA) (PNP)	$V_{i(on)}$	– –	1.0 1.0	– –	Vdc
Output Voltage (on) (V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ)	V_{OL}	–	–	0.2	Vdc
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)	V_{OH}	4.9	–	–	Vdc
Input Resistor	R1	70	100	130	kΩ
Resistor Ratio	R_1/R_2	–	–	–	

4. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle ≤ 2%.



(1) SOT−963; 100 mm^2, 1 oz. copper trace

Figure 1. Derating Curve

TYPICAL CHARACTERISTICS – NPN TRANSISTOR
NSBC115TPDP6

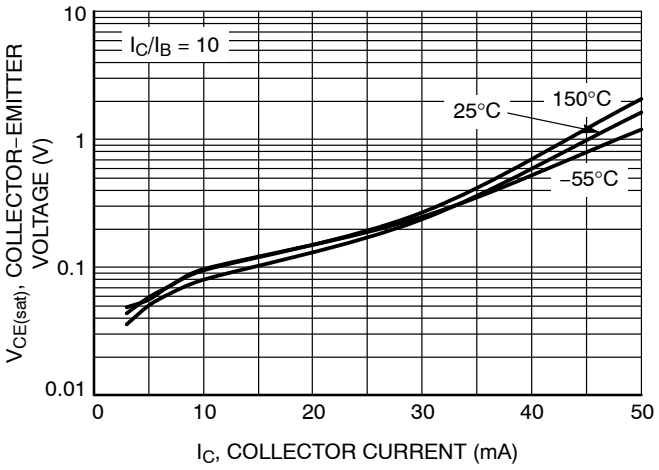


Figure 2. $V_{CE(sat)}$ vs. I_C

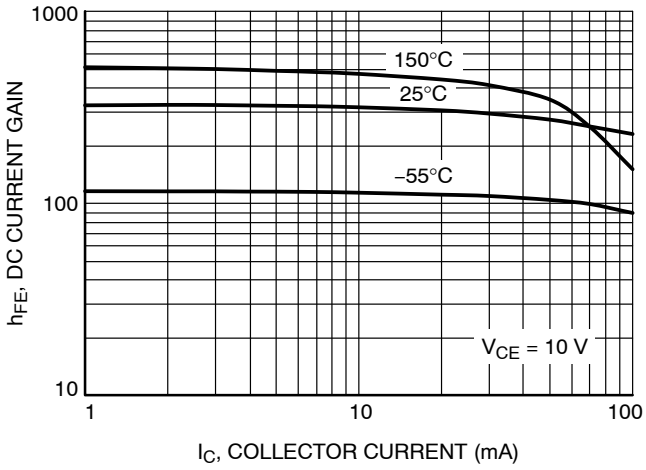


Figure 3. DC Current Gain

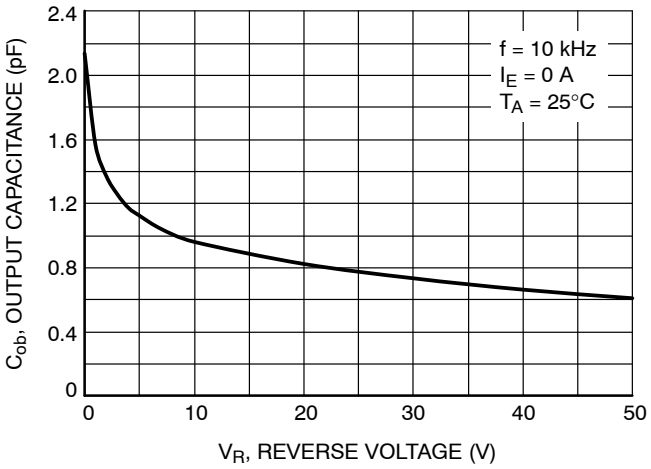


Figure 4. Output Capacitance

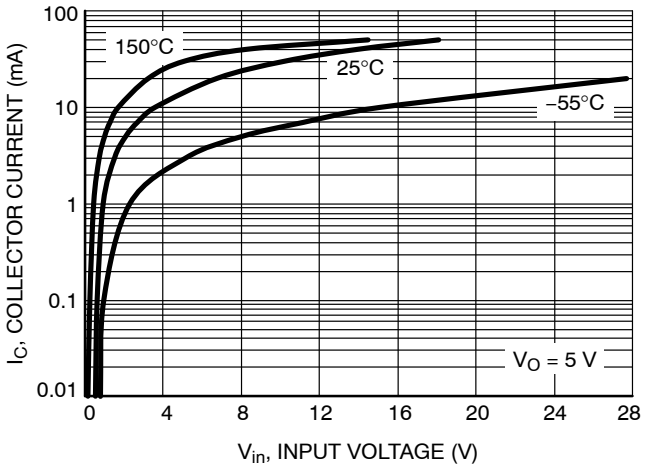


Figure 5. Output Current vs. Input Voltage

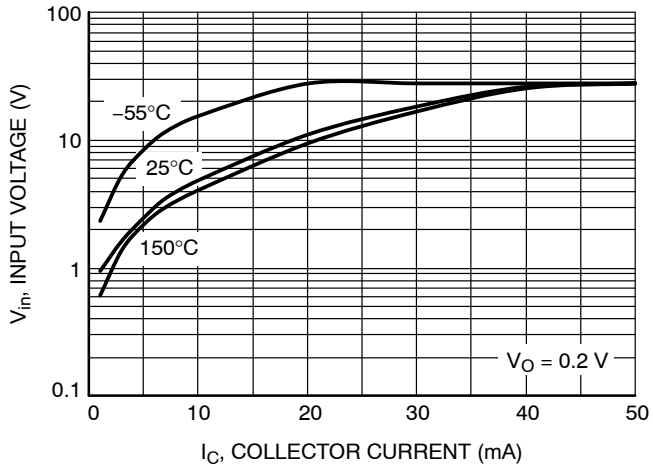


Figure 6. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS – PNP TRANSISTOR
NSBC115TPDP6

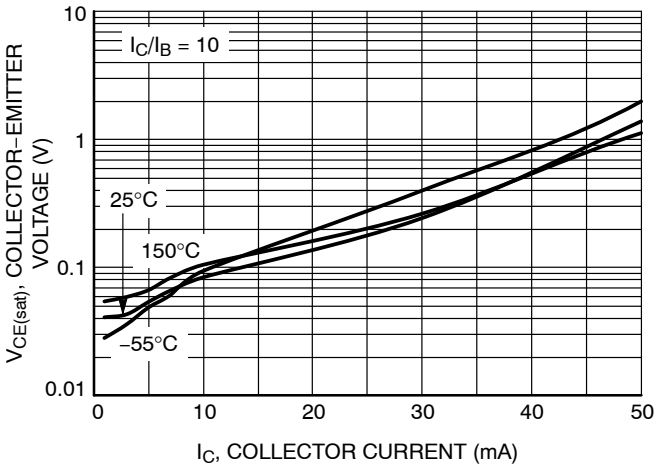


Figure 7. $V_{CE(sat)}$ vs. I_C

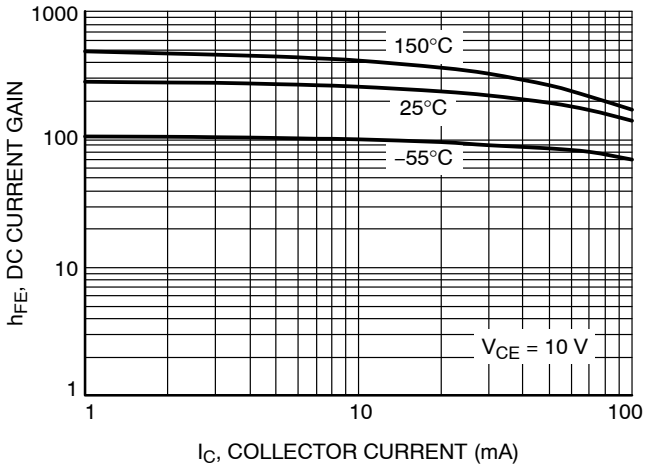


Figure 8. DC Current Gain

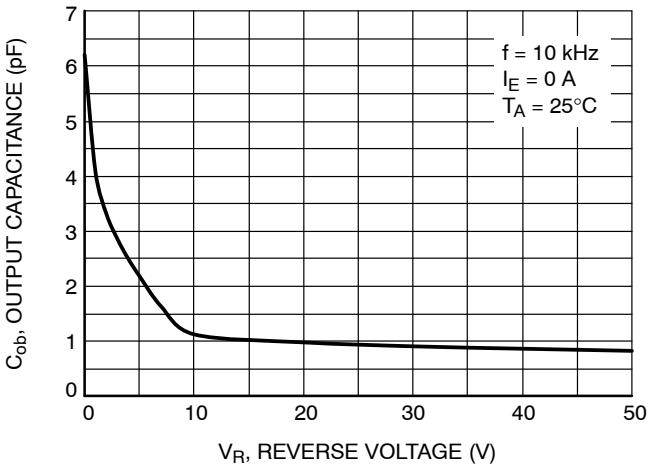


Figure 9. Output Capacitance

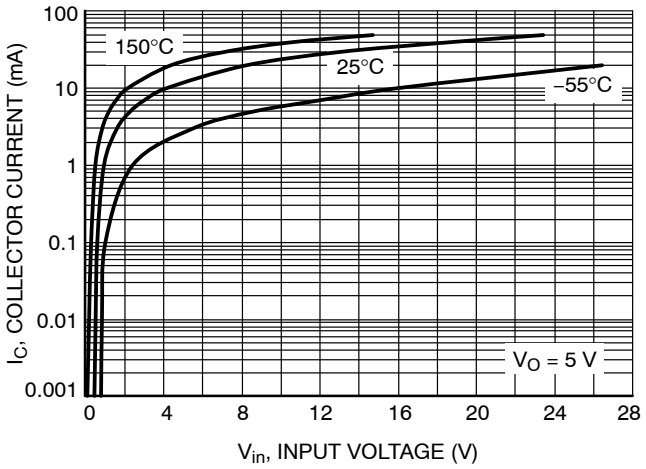


Figure 10. Output Current vs. Input Voltage

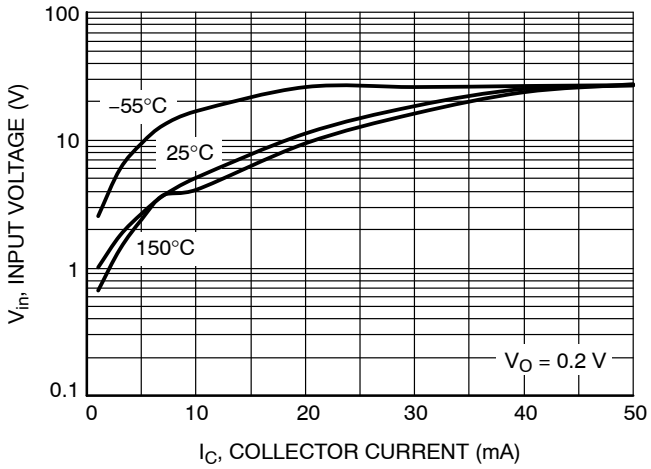
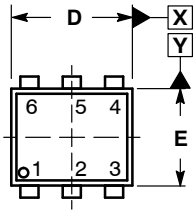


Figure 11. Input Voltage vs. Output Current

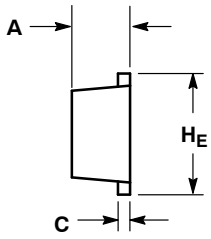
NSBC115TPDP6

PACKAGE DIMENSIONS

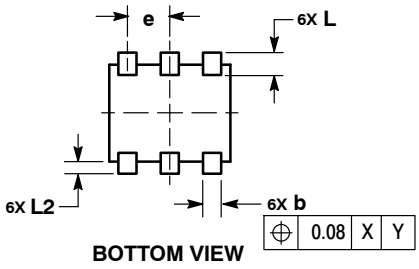
SOT−963
CASE 527AD
ISSUE E



TOP VIEW



SIDE VIEW

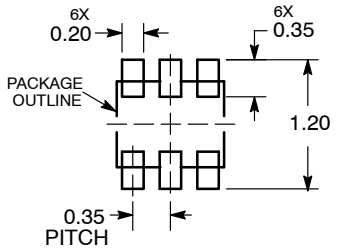


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H_E	0.95	1.00	1.05
L	0.19 REF		
L2	0.05	0.10	0.15

RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

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