



OPA2210 2.2-nV/ $\sqrt{\text{Hz}}$ Precision, Low-Power, 36-V Operational Amplifier

1 Features

- Precision super beta input performance:
 - Low offset voltage: 5 μV (typical)
 - Ultra-low drift: 0.1 $\mu\text{V}/^\circ\text{C}$ (typical)
 - Low input bias current: 0.3 nA (typical)
- Ultra-low noise:
 - Low 0.1-Hz to 10-Hz noise: 90 nV_{PP}
 - Low voltage noise: 2.2 nV/ $\sqrt{\text{Hz}}$ at 1 kHz
- High CMRR: 132 dB (minimum)
- Gain bandwidth product: 18 MHz
- Slew rate: 6.4 V/ μs
- Low quiescent current: 2.5 mA/channel (maximum)
- Short-circuit current: ± 65 mA
- Wide supply range: ± 2.25 V to ± 18 V
- No phase reversal
- Rail-to-rail output

2 Applications

- [Ultrasound scanner](#)
- [Multiparameter patient monitor](#)
- [Merchant network and server PSU](#)
- [Semiconductor test](#)
- [Spectrum analyzer](#)
- [Lab and field instrumentation](#)
- [Data acquisition \(DAQ\)](#)
- [Professional microphone and wireless systems](#)

3 Description

The OPA2210 is the next generation of OPA2209 operational amplifier (op amp). The OPA2210 precision operational amplifier is built on TI's precision super beta complementary bipolar semiconductor process, which offers ultra-low flicker noise, low offset voltage, and low offset voltage temperature drift.

The OPA2210 achieves very low voltage noise density (2.2 nV/ $\sqrt{\text{Hz}}$) while consuming only 2.5 mA (maximum) per amplifier. This device also offers rail-to-rail output swing, which helps to maximize dynamic range.

In precision data acquisition applications, the OPA2210 provides fast settling time to 16-bit accuracy, even for 10-V output swings. Excellent ac performance, combined with only 35 μV (maximum) of offset and 0.6 $\mu\text{V}/^\circ\text{C}$ (maximum) drift over temperature, makes the OPA2210 very suitable for high-speed, high-precision applications.

The OPA2210 is specified over a wide dual power-supply range of ± 2.25 V to ± 18 V, or single-supply operation from 4.5 V to 36 V and is specified from -40°C to 125°C .

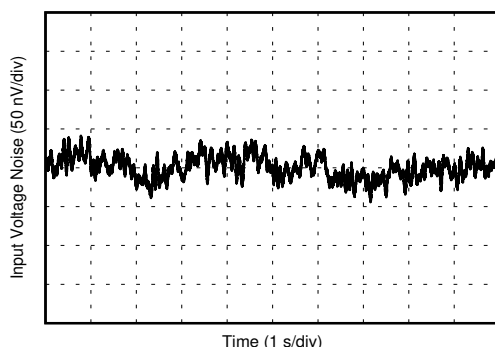
The OPA2210 comes in 8-pin SOIC, VSSOP, and WSON packages.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA2210	SOIC (8)	4.90 mm $\times$ 3.91 mm
	VSSOP (8)	3.00 mm $\times$ 3.00 mm
	WSON (8) (preview)	3.00 mm $\times$ 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

OPA2210 0.1-Hz to 10-Hz Noise



OPA2210 Offset Voltage Drift Distribution

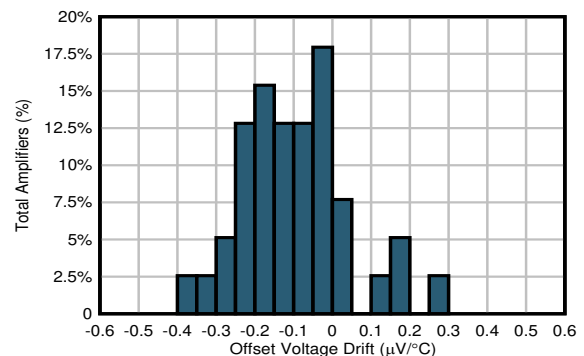


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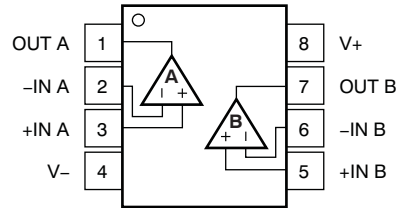
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 2019) to Revision D	Page
• Added OPA2210 DRG package to data sheet as advanced information (preview)	1
Changes from Revision B (March 2019) to Revision C	Page
• Changed super-β to super beta for easier searching	1
• Added SOIC package	1
Changes from Revision A (December 2018) to Revision B	Page
• Changed "OPAx145" to "OPA2210"	18
• Fixed link to TIDA-01427	21
Changes from Original (September 2018) to Revision A	Page
• First release of production-data data sheet	1

5 Pin Configuration and Functions

**D, DGK, and DRG⁽¹⁾ Packages
8-Pin SOIC, VSSOP, and WSON
Top View**



(1) DRG package is preview.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
Voltage	Supply voltage, $V_S = (V+) - (V-)$		40		V
	Signal input pins ⁽²⁾		(V-) – 0.5	(V+) + 0.5	
	Signal input pins	Differential	1		
Current	Signal input pins ⁽²⁾		–10	10	mA
	Output short circuit ⁽³⁾		Continuous		
Temperature	Junction, T_J		150		°C
	Storage temperature, T_{stg}		–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) For input voltages beyond the power-supply rails, voltage or current must be limited.
- (3) Short circuit to ground, one amplifier per package.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Specified voltage, V_S	±2.25	±18	V
Specified temperature	–40	125	°C
Operating temperature, T_A	–55	150	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		OPA2210		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.1	132.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.7	38.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.5	52.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.4	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	68.9	52.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at $V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage	V _S = ±15 V, V _{CM} = 0 V			±5	±35	μV
dV _{OS} /dT	Input offset voltage drift	T _A = −40°C to 125°C			±0.1	±0.5	μV/°C
V _{OS-matching}	Input offset voltage matching				±5	±35	μV
PSRR	vs power supply	V _S = ±2.25 V to ±18 V	T _A = 25°C		0.05	0.5	μV/V
			T _A = −40°C to 125°C			±1	
	Channel separation	DC			±0.1		μV/V
INPUT BIAS OPERATION							
I _B	Input bias current	V _{CM} = 0 V	T _A = 25°C		±0.3	±2	nA
			T _A = −40°C to 85°C			±4	
			T _A = −40°C to 125°C			±7	
I _{OS}	Input offset current	V _{CM} = 0 V	T _A = 25°C		±0.1	±2	nA
			T _A = −40°C to 85°C			±4	
			T _A = −40°C to 125°C			±7	
NOISE							
e _{n p-p}	Input voltage noise	f = 0.1 Hz to 10 Hz			0.09		μV _{PP}
e _n	Noise density	f = 10 Hz			2.5		nV/√Hz
		f = 100 Hz			2.25		
		f = 1 kHz			2.2		
I _n	Input current noise density	f = 1 kHz			400		fA/√Hz
INPUT VOLTAGE RANGE							
V _{CM}	Common-mode voltage range			(V−) + 1.5		(V+) − 1.5	V
CMRR	Common-mode rejection ratio	(V−) + 1.5 V < V _{CM} < (V+) − 1.5 V		132	140		dB
		(V−) + 1.5 V < V _{CM} < (V+) − 1.5 V, T _A = −40°C to 125°C		120	130		
INPUT IMPEDANCE							
	Differential				400 9		kΩ pF
	Common-mode				10 ⁹ 0.5		Ω pF
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	(V−) + 0.2 V < V _O < (V+) − 0.2 V, R _L = 10 kΩ	T _A = 25°C	126	132		dB
			T _A = −40°C to 125°C	120			
		(V−) + 0.6 V < V _O < (V+) − 0.6 V, R _L = 600 Ω ⁽¹⁾	T _A = 25°C	114	120		
			T _A = −40°C to 85°C	110			
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				18		MHz
SR	Slew rate				6.4		V/μs
	Phase margin (ϕ _m)	R _L = 10 kΩ, C _L = 25 pF			80		degrees
t _S	Settling time	0.1%, G = −1, 10-V step, C _L = 100 pF			2.1		μs
		0.0015% (16-bit), G = −1, 10-V step, C _L = 100 pF			2.6		
	Overload recovery time	G = −10			0.5		μs
	Total harmonic distortion + noise (THD+N)	G = +1, f = 1 kHz, V _O = 20 V _{PP} , 600 Ω			0.000025		%

(1) Temperature range limited by thermal performance of the package.

Electrical Characteristics (continued)

at $V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing	R _L = 10 kΩ, A _{OL} > 130 dB		(V−) + 0.2	(V+) − 0.2		V
		R _L = 600 Ω, A _{OL} > 114 dB		(V−) + 0.6	(V+) − 0.6		
		R _L = 10 kΩ, A _{OL} > 120 dB, T _A = −40°C to 125°C		(V−) + 0.2	(V+) − 0.2		
I _{SC}	Short-circuit current	V _S = ±18 V		±65			mA
C _{LOAD}	Capacitive load drive (stable operation)			See <i>Typical Characteristics</i>			
Z _O	Open-loop output impedance			See <i>Typical Characteristics</i>			
POWER SUPPLY							
I _Q	Quiescent current (per amplifier)	I _O = 0 A	T _A = 25°C	2.2		2.5	mA
			T _A = −40°C to 125°C	3.25			

6.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)

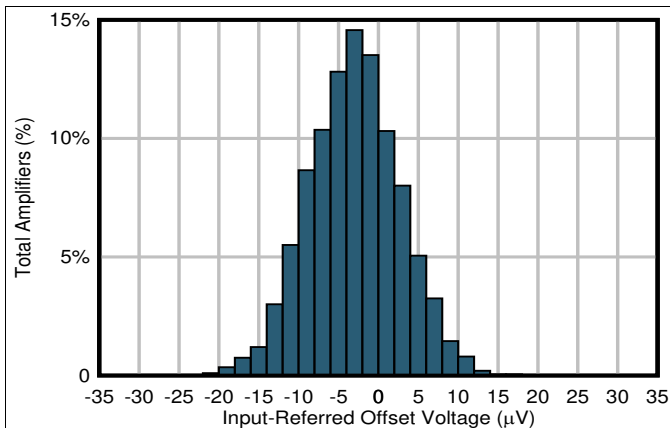


Figure 1. Offset Voltage Production Distribution

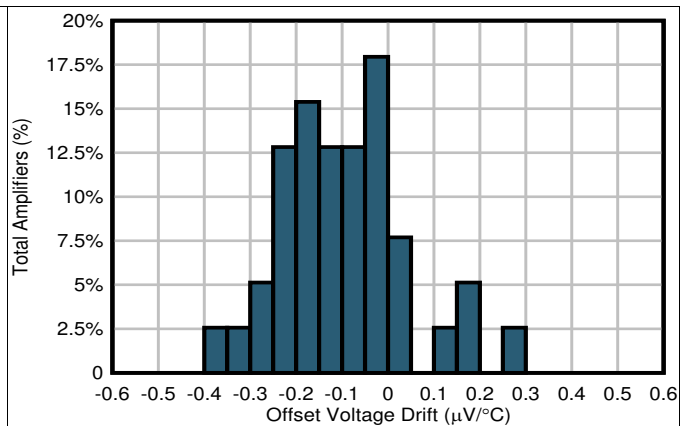


Figure 2. Offset Voltage Drift Distribution

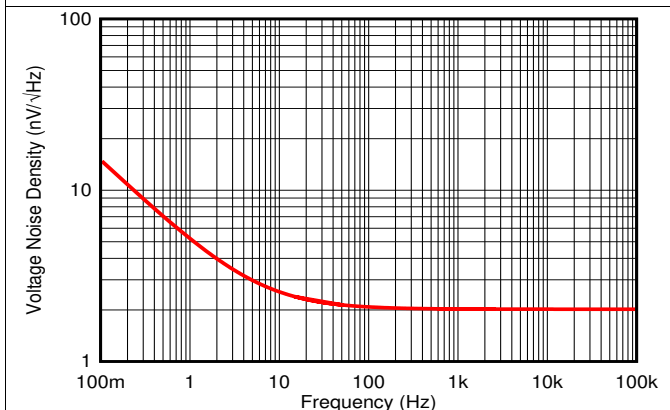


Figure 3. Input Voltage Noise Spectral Density vs Frequency

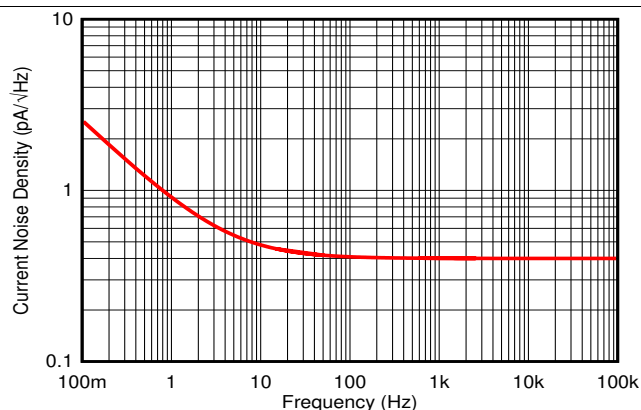


Figure 4. Input Current Noise Spectral Density vs Frequency

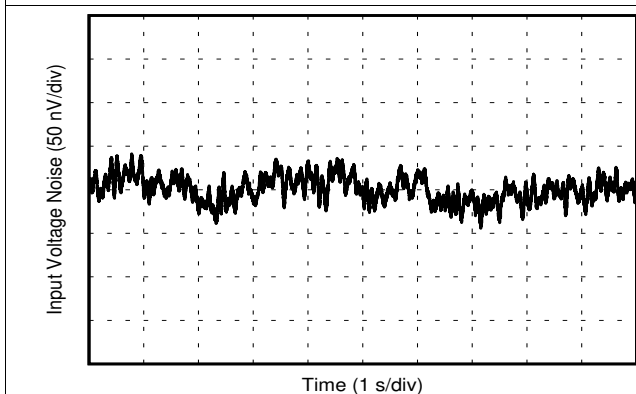


Figure 5. 0.1-Hz to 10-Hz Voltage Noise

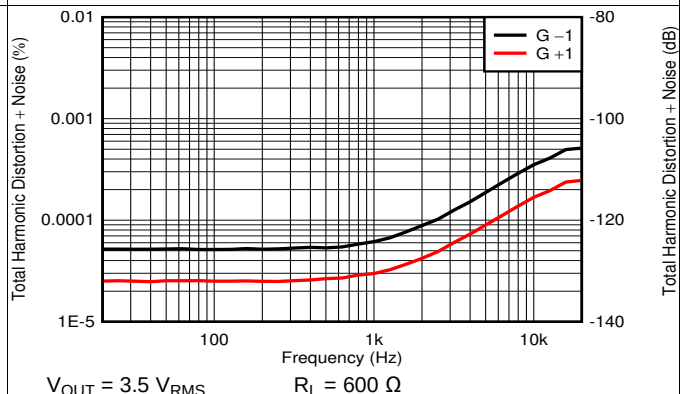


Figure 6. THD+N Ratio vs Frequency

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)

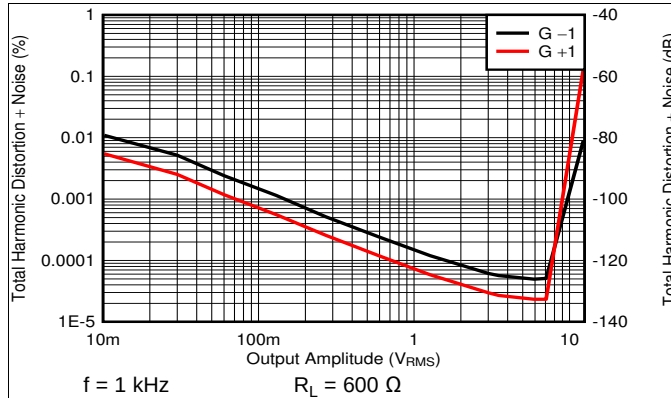
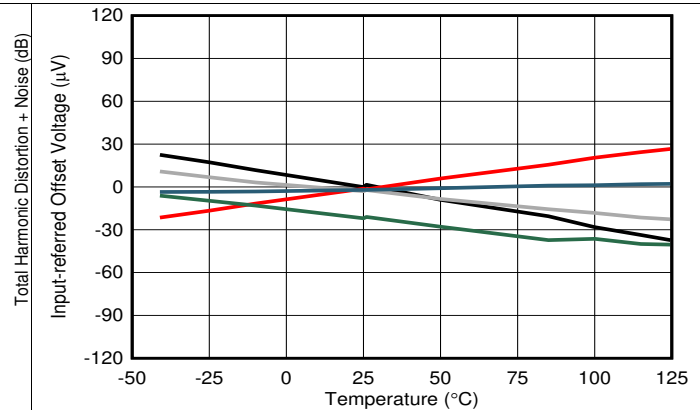
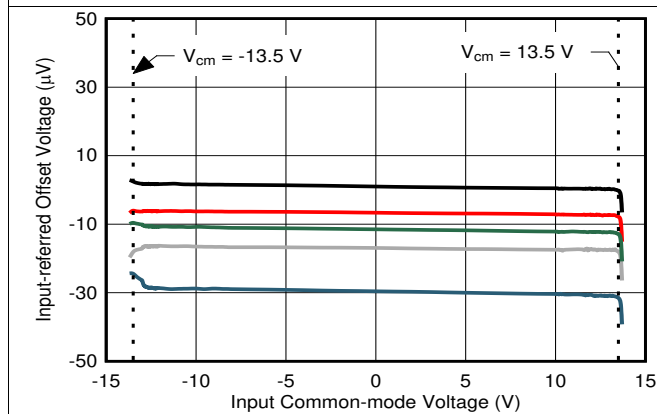


Figure 7. THD+N vs Output Amplitude



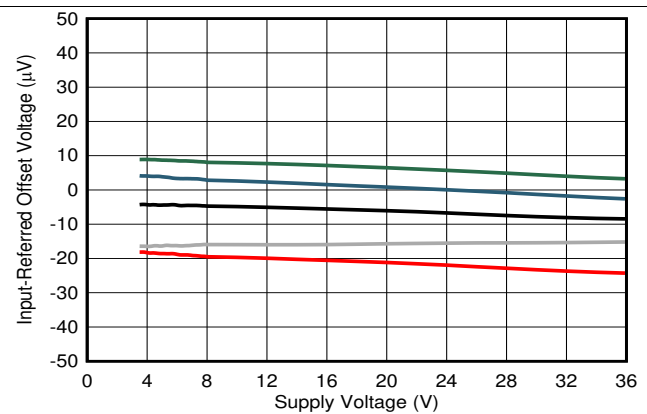
5 typical units

Figure 8. Input Offset Voltage vs Temperature



5 typical units

Figure 9. Offset Voltage vs Common-Mode Voltage



5 typical units

Figure 10. Offset Voltage vs Supply Voltage

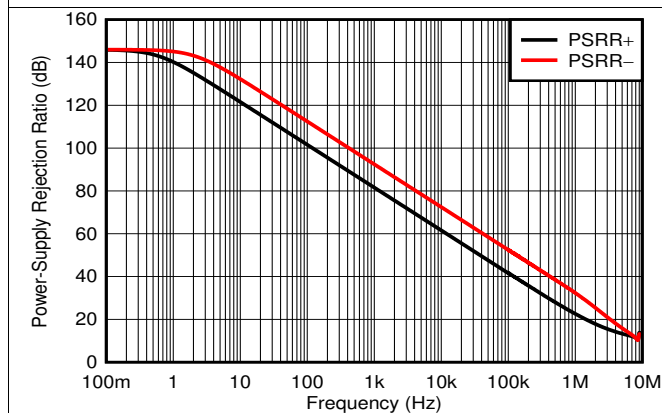


Figure 11. PSRR vs Frequency

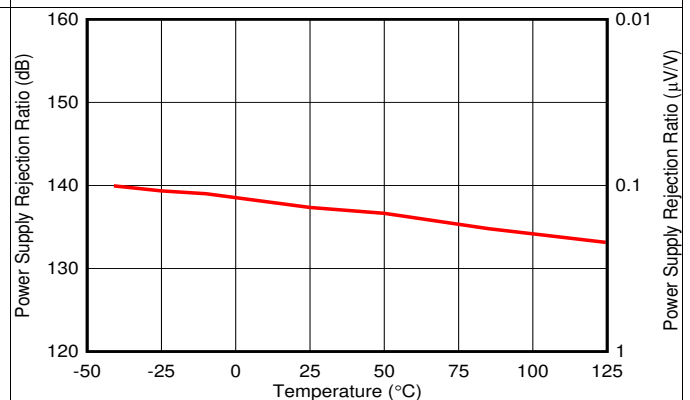


Figure 12. PSRR vs Temperature

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)

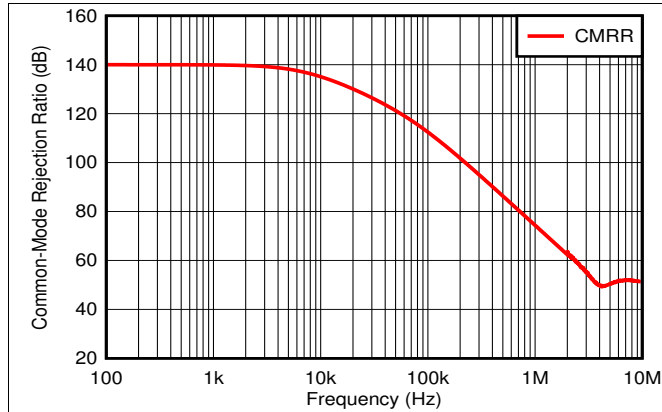


Figure 13. CMRR vs Frequency

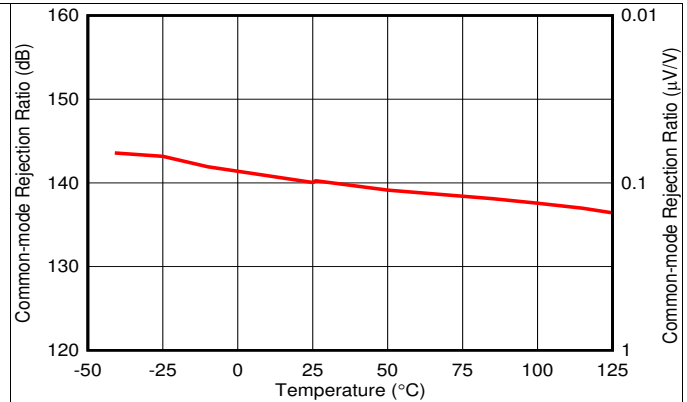


Figure 14. CMRR vs Temperature

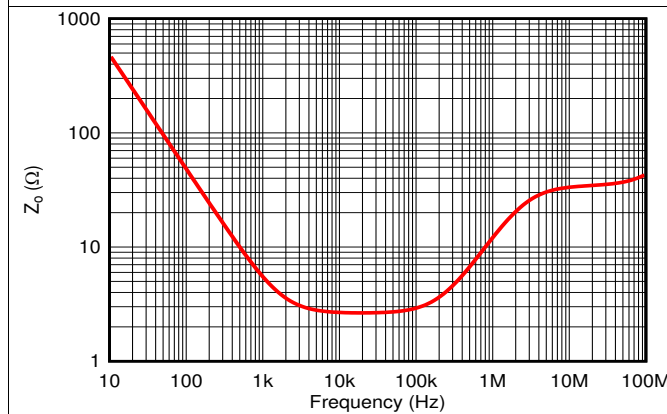


Figure 15. Open-Loop Output Impedance vs Frequency

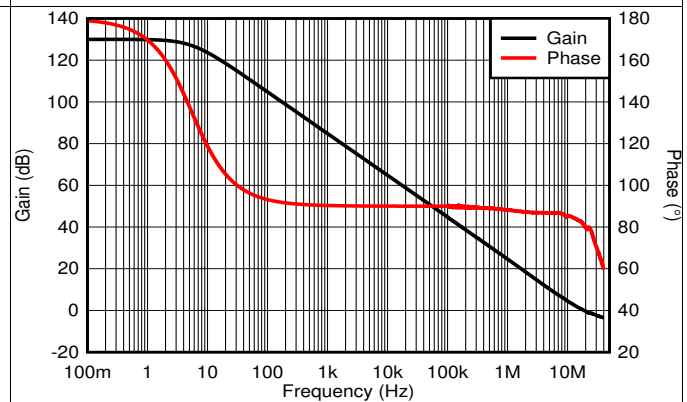


Figure 16. Open-Loop Gain and Phase vs Frequency

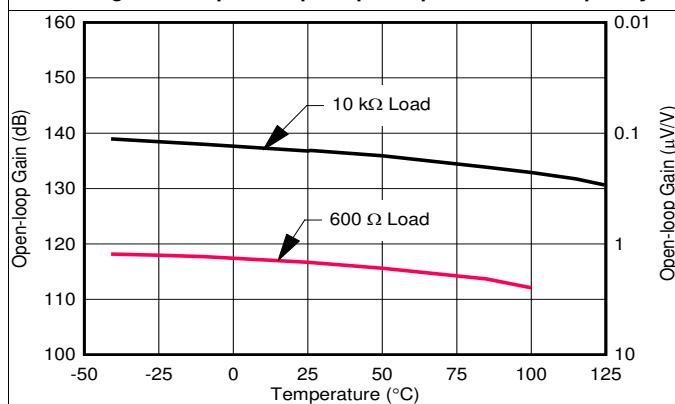


Figure 17. Open-Loop Gain vs Temperature

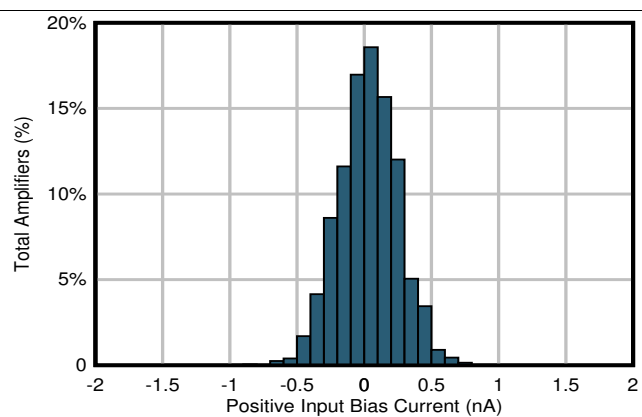


Figure 18. Positive Input Bias Current Production Distribution

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)

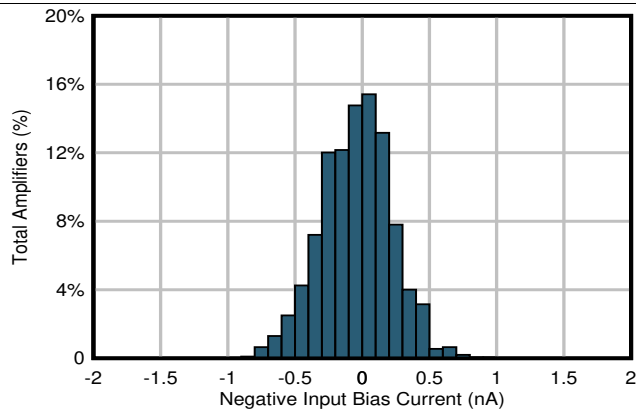


Figure 19. Negative Input Bias Current Production Distribution

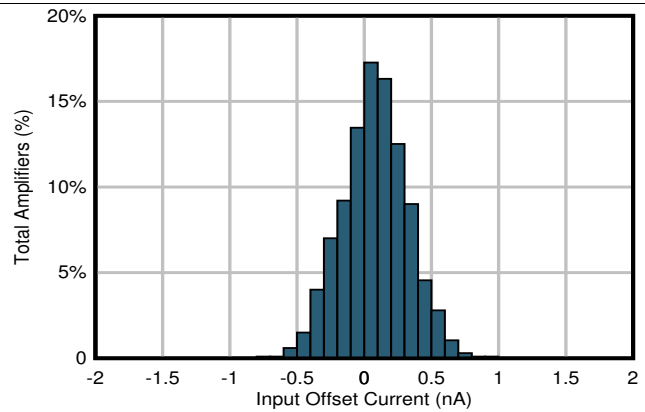


Figure 20. Input Offset Current Production Distribution

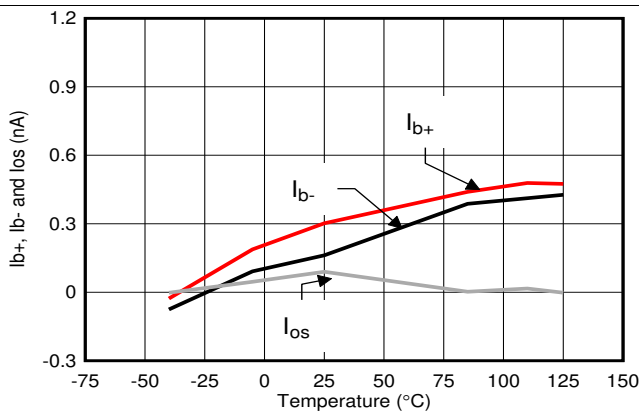


Figure 21. Input Bias and Input Offset Currents vs Temperature

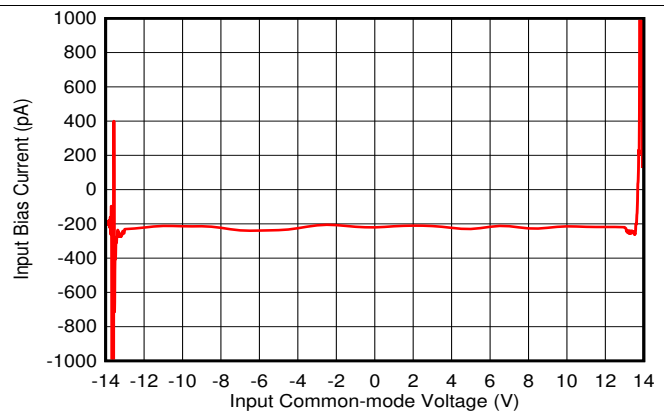


Figure 22. Positive Input Bias Current vs Common-Mode Voltage

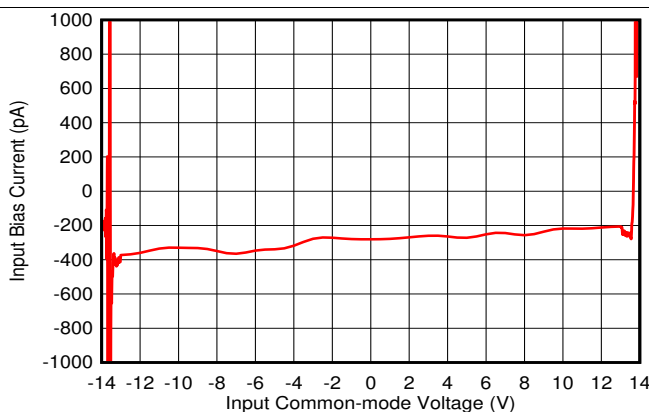


Figure 23. Negative Input Bias Current vs Common-Mode Voltage

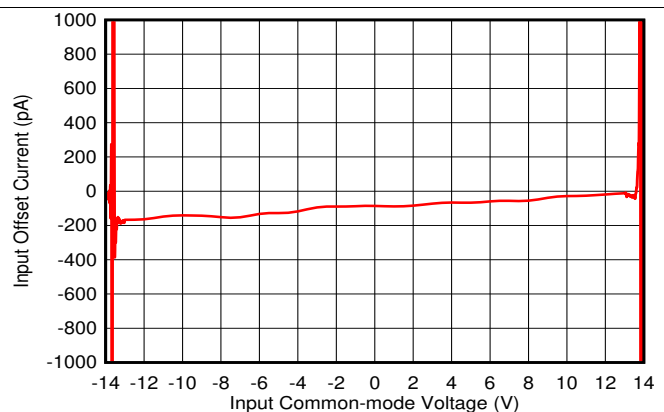


Figure 24. Input Offset Current vs Common-Mode Voltage

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)

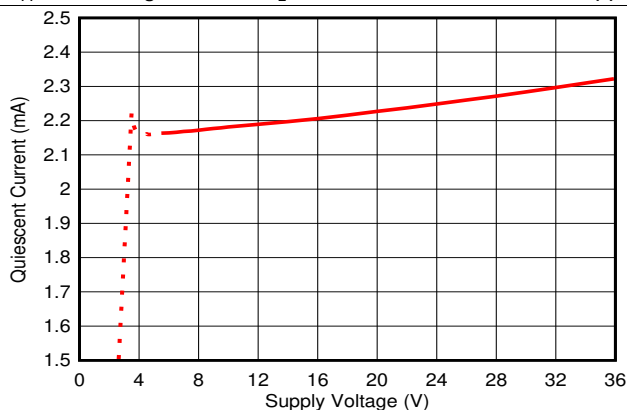


Figure 25. Quiescent Current vs Supply Voltage

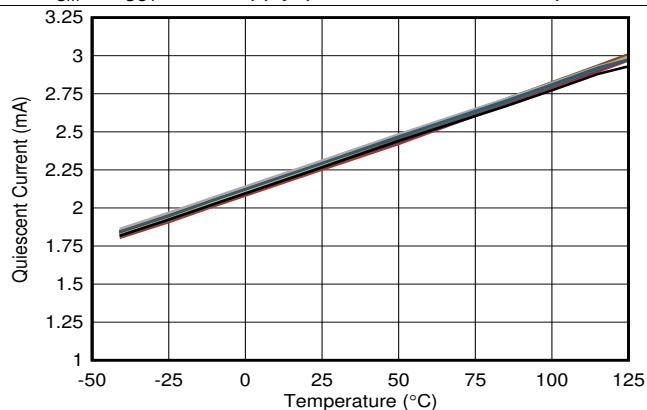


Figure 26. Quiescent Current vs Temperature

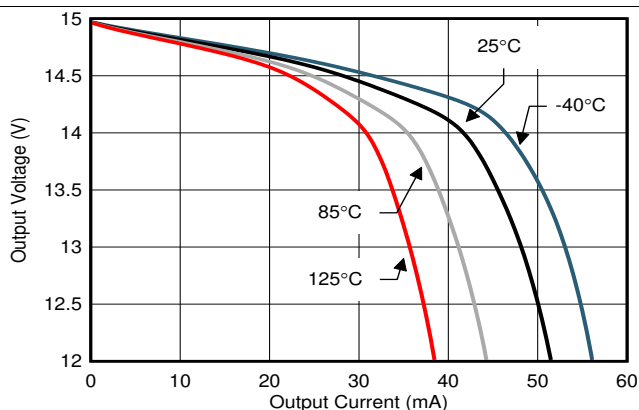


Figure 27. Output Voltage vs Output Current (Sourcing)

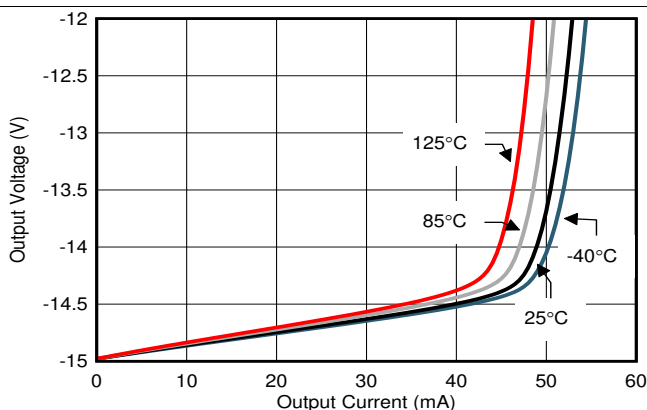


Figure 28. Output Voltage vs Output Current (Sinking)

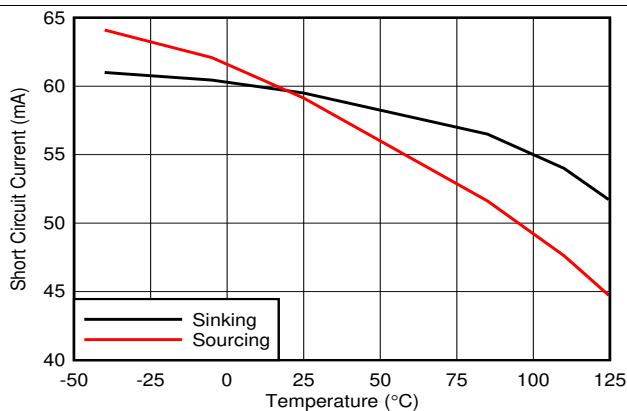


Figure 29. Short-Circuit Current vs Temperature

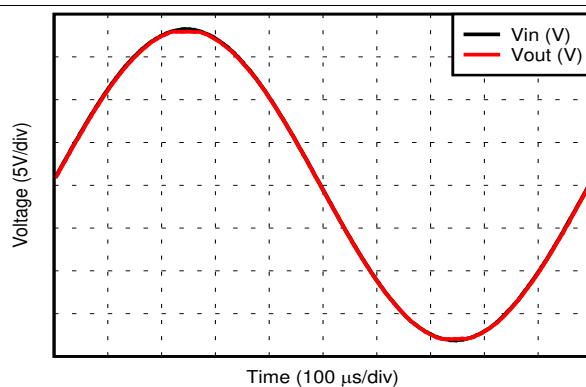
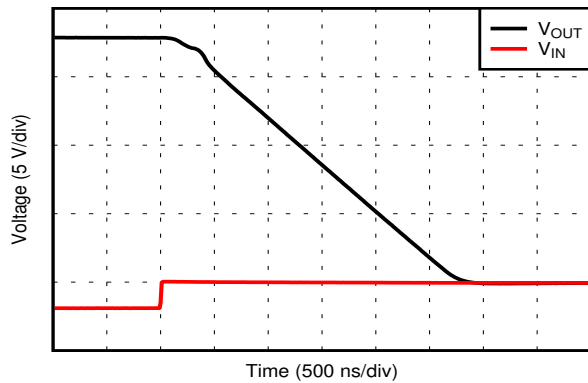


Figure 30. No Phase Reversal

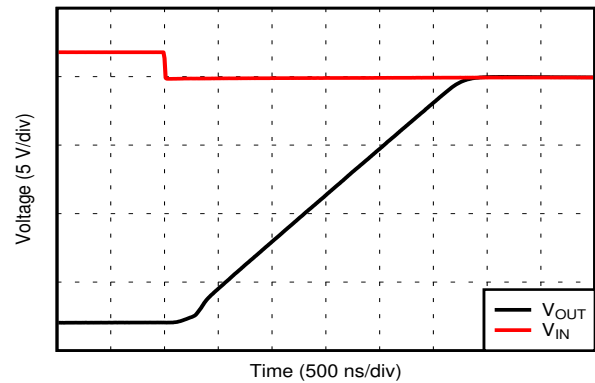
Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)



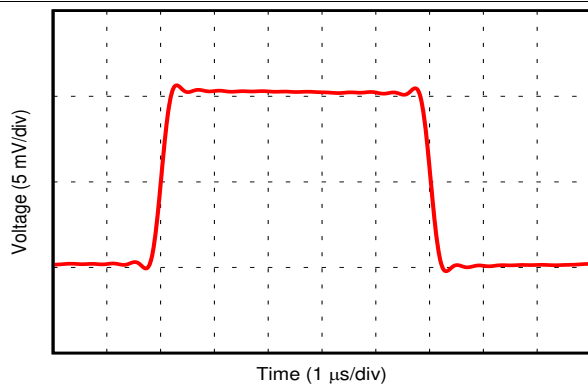
$G = -10$

Figure 31. Positive Overload Recovery



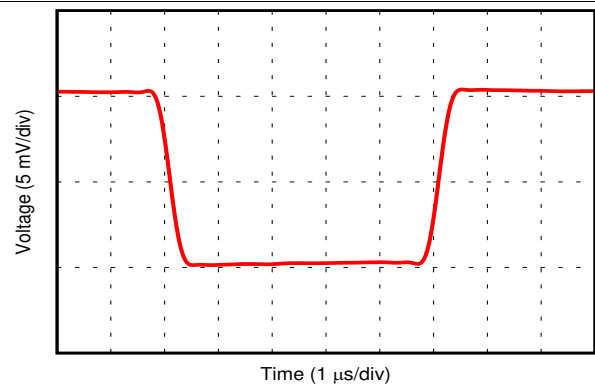
$G = -10$

Figure 32. Negative Overload Recovery



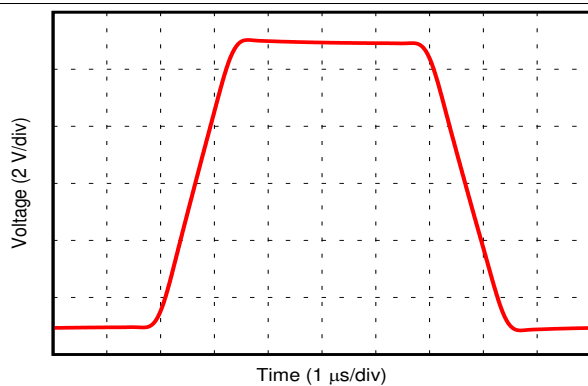
$G = +1$ 10-mV step, $C_L = 100\text{ pF}$, $R_L = 600\text{ }\Omega$

Figure 33. Small-Signal Step Response



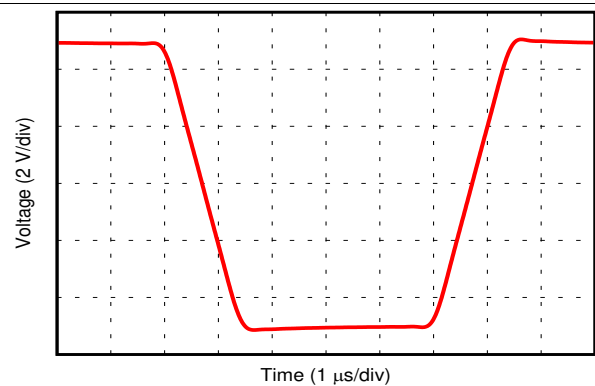
$G = -1$ 10-mV step, $C_L = 100\text{ pF}$, $R_L = 600\text{ }\Omega$

Figure 34. Small-Signal Step Response



$G = +1$ 10-V step, $C_L = 100\text{ pF}$, $R_L = 600\text{ }\Omega$

Figure 35. Large-Signal Step Response

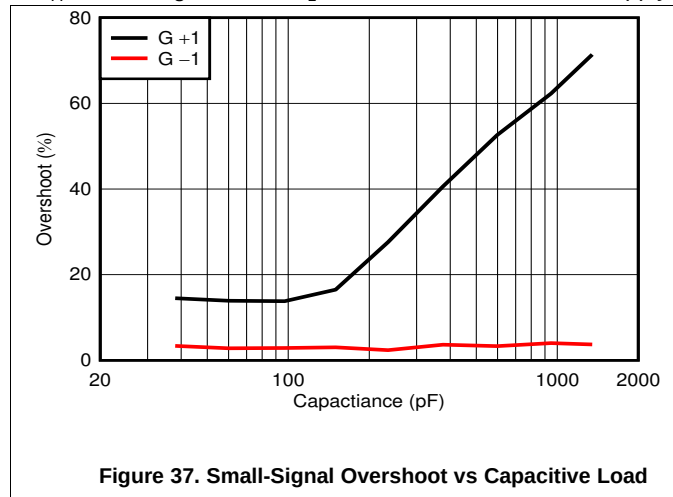
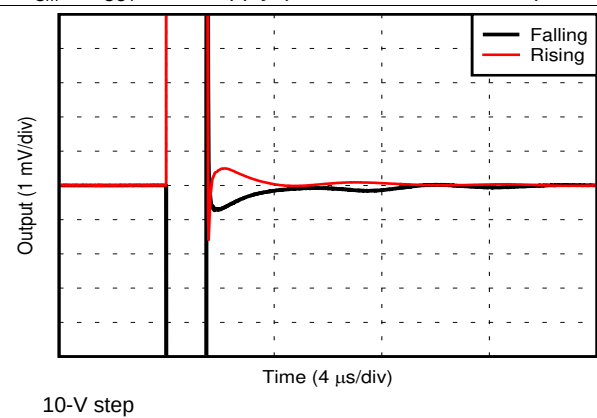
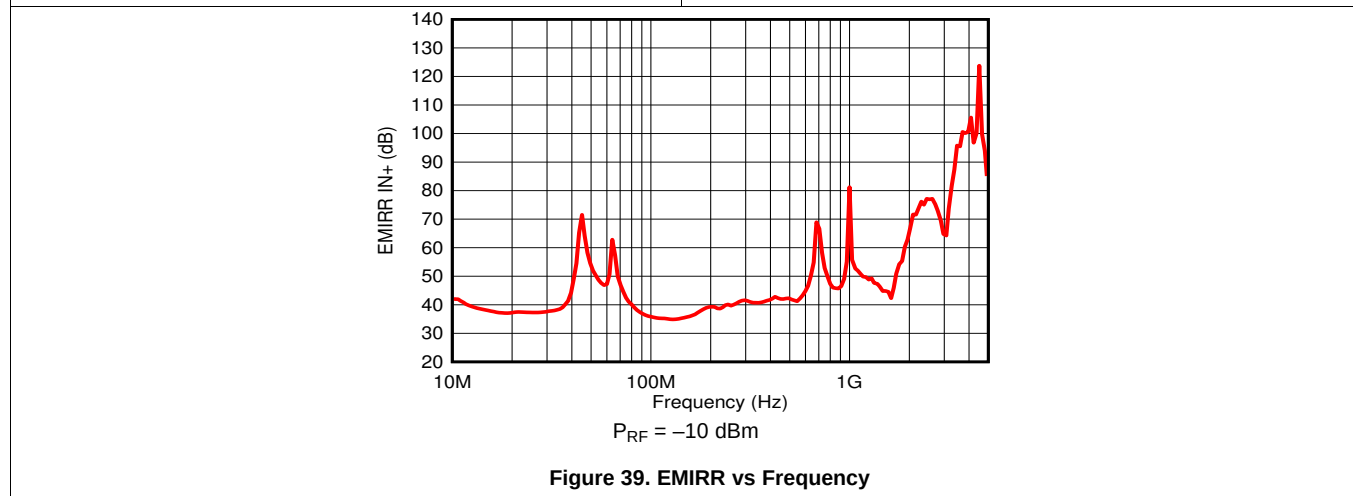


$G = -1$ 10-V step, $C_L = 100\text{ pF}$, $R_L = 600\text{ }\Omega$

Figure 36. Large-Signal Step Response

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)

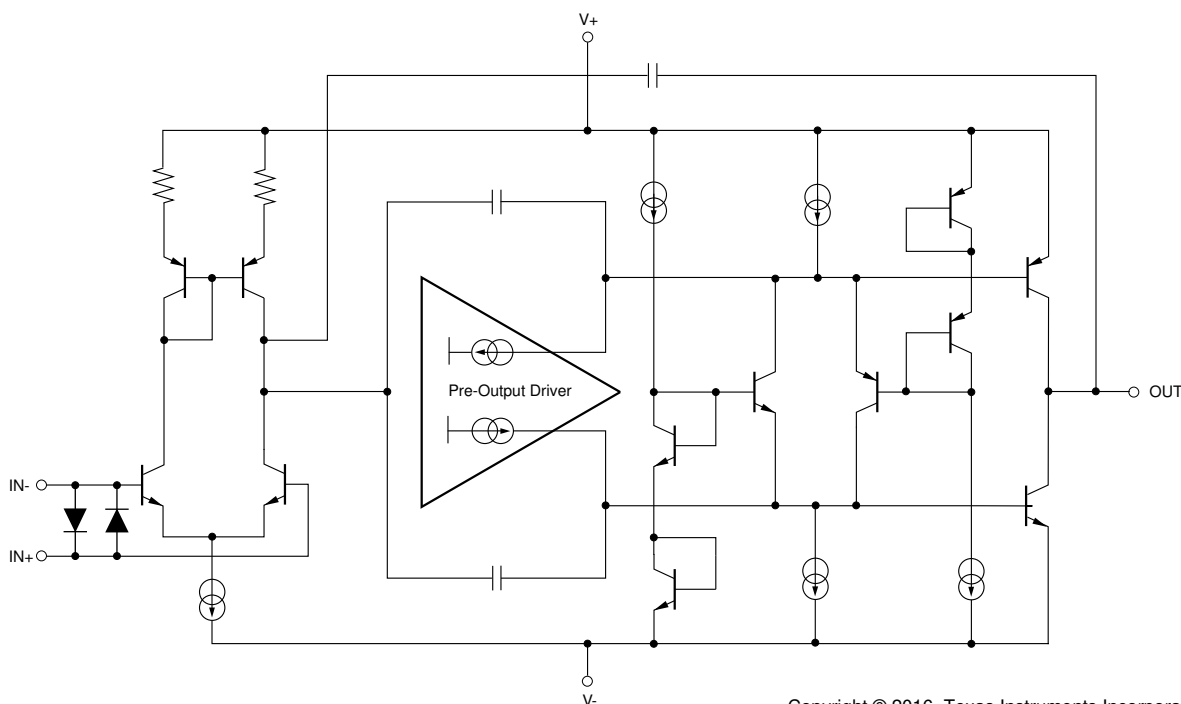


7 Detailed Description

7.1 Overview

The OPA2210 is the next generation of OPA2209 operational amplifier. The OPA2210 offers improved input offset voltage, offset voltage temperature drift, input bias current and lower 1/f noise corner frequency. In addition, this device offers excellent overall performance with high CMRR, PSRR, and A_{OL} . The OPA2210 precision operational amplifier is unity-gain stable and free from unexpected output and phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1- μ F capacitors are adequate. The [Functional Block Diagram](#) shows a simplified schematic of the OPA2210. This die uses a SiGe bipolar process and contains 180 transistors.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Operating Voltage

The OPA2210 op amp can be used with single or dual supplies within an operating range of $V_S = 4.5\text{ V} (\pm 2.25\text{ V})$ up to 36 V ($\pm 18\text{ V}$). Supply voltages higher than 40 V total can permanently damage the device.

In addition, key parameters are assured over the specified temperature range, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$. Parameters that vary significantly with operating voltage or temperature are shown in the [Typical Characteristics](#).

7.3.2 Input Protection

The input terminals of the OPA2210 are protected from excessive differential voltage with back-to-back diodes, as shown in [Figure 40](#). In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or $G = 1$ circuits, fast ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in [Figure 35](#) and [Figure 36](#) in the [Typical Characteristics](#) section. If the input signal is fast enough to create this forward-bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA2210. See [Noise Performance](#) for further information on noise performance.

Feature Description (continued)

Figure 40 shows an example configuration that implements a current-limiting feedback resistor.

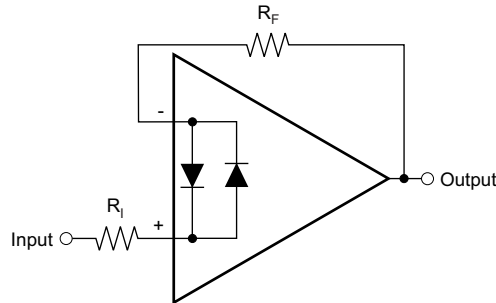


Figure 40. Pulsed Operation

7.3.3 Noise Performance

Figure 41 shows the total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). Two different op amps are shown with the total circuit noise calculated. The OPA2210 has very low voltage noise, making this device a great choice for low source impedances (less than 2 kΩ). As a comparable precision FET-input op amp (very low current noise), the OPA827 has somewhat higher voltage noise, but lower current noise. It provides excellent noise performance at moderate to high source impedance (10 kΩ and up). For source impedance lower than 300 Ω, the OPA211 may provide lower noise.

The equation in Figure 41 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise,
- i_n = current noise,
- R_S = source impedance,
- k = Boltzmann's constant = 1.38×10^{-23} J/K, and
- T = temperature in Kelvins

For more details on calculating noise, see [Basic Noise Calculations](#).

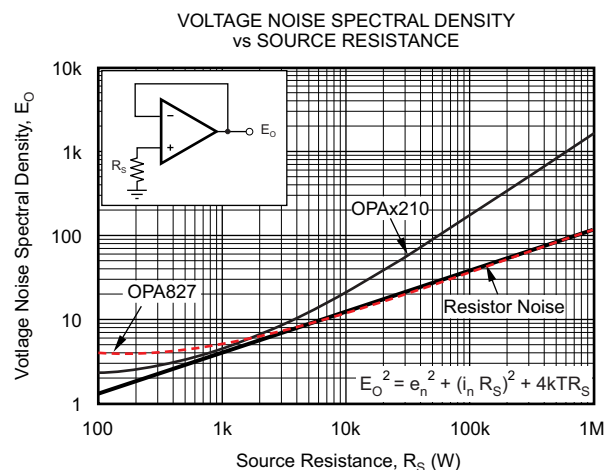


Figure 41. Noise Performance of the OPA2210 and OPA827 in Unity-Gain Buffer Configuration

Feature Description (continued)

7.3.4 Phase-Reversal Protection

The OPA2210 device has internal phase-reversal protection. Many FET- and bipolar-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input circuitry of the OPA2210 device prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail (see [Figure 30](#)).

7.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. See [Figure 42](#) for an illustration of the ESD circuits contained in the OPA2210 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA2210 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as the one [Figure 42](#) shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

[Figure 42](#) depicts a specific example where the input voltage, V_{IN} , exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN} . As a result, the datasheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

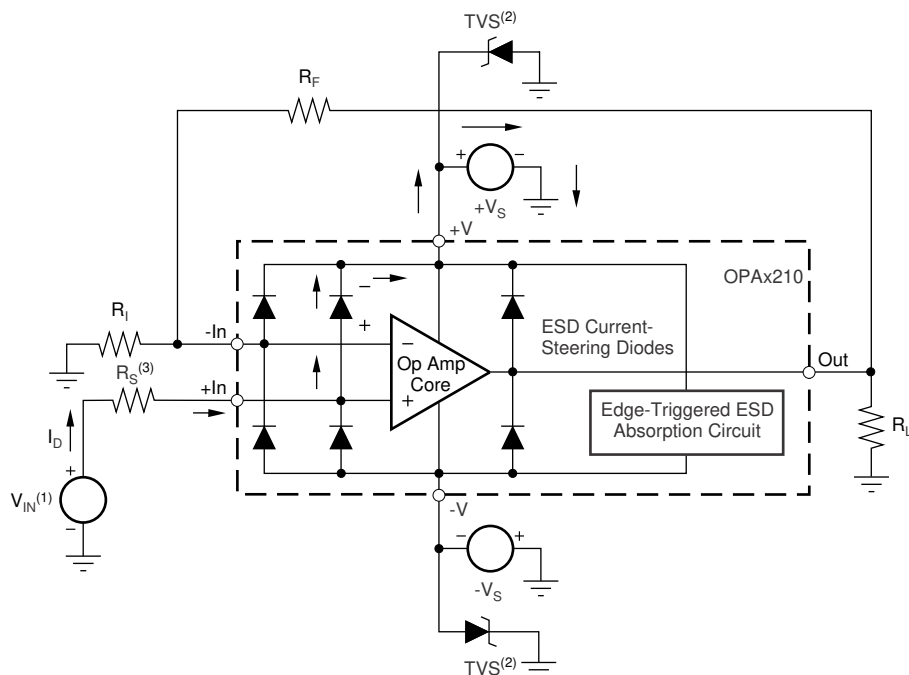
Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $-V_S$ are at 0 V.

Again, it depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

Feature Description (continued)

If there is an uncertainty about the ability of the supply to absorb this current, external Transient Voltage Suppressor (TVS) diodes may be added to the supply pins as shown in Figure 42. The breakdown voltage must be selected such that the diode does not turn on during normal operation.

However, its breakdown voltage must be low enough so that the TVS diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



- (1) $V_{IN} = +V_S + 500 \text{ mV}$
- (2) TVS: $+V_{S(max)} > V_{TVSBR}(\text{Min}) > +V_S$
- (3) Suggested value approximately $1 \text{ k}\Omega$

Figure 42. Equivalent Internal ESD Circuitry and Relation to a Typical Circuit Application

7.4 Device Functional Modes

The OPA2210 is operational when the power-supply voltage is greater than 4.5 V ($\pm 2.25 \text{ V}$). The maximum power-supply voltage for the OPA2210 is 36 V ($\pm 18 \text{ V}$).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA2210 is a unity-gain stable, precision operational amplifier with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1- μ F capacitors are adequate.

8.1.1 Basic Noise Calculations

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

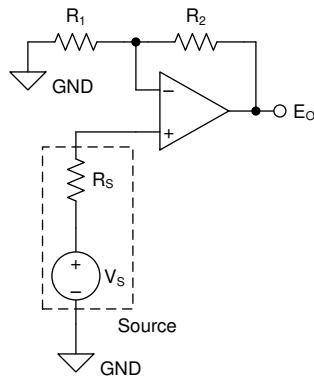
The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in [Figure 41](#). The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

[Figure 43](#) illustrates both noninverting **(A)** and inverting **(B)** op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPA2210 means that its current noise contribution can be neglected.

The feedback resistor values can generally be chosen to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

Application Information (continued)

(A) Noise in Noninverting Gain Configuration



Noise at the output is given as E_O , where

$$(1) \quad E_O = \left(1 + \frac{R_2}{R_1}\right) \cdot \sqrt{(e_S)^2 + (e_N)^2 + (e_{R_1 \parallel R_2})^2 + (i_N \cdot R_S)^2 + \left(i_N \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]\right)^2} \quad [V_{RMS}]$$

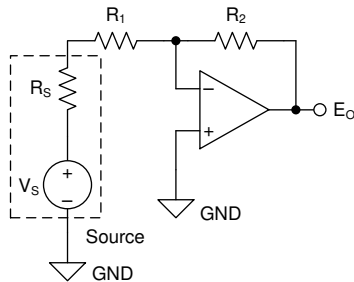
$$(2) \quad e_S = \sqrt{4 \cdot k_B \cdot T(K) \cdot R_S} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } R_S$$

$$(3) \quad e_{R_1 \parallel R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } R_1 \parallel R_2$$

$$(4) \quad k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \quad \text{Boltzmann Constant}$$

$$(5) \quad T(K) = 237.15 + T(^{\circ}C) \quad [K] \quad \text{Temperature in kelvins}$$

(B) Noise in Inverting Gain Configuration



Noise at the output is given as E_O , where

$$(6) \quad E_O = \left(1 + \frac{R_2}{R_S + R_1}\right) \cdot \sqrt{(e_N)^2 + (e_{R_1 + R_S \parallel R_2})^2 + \left(i_N \cdot \left[\frac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]\right)^2} \quad [V_{RMS}]$$

$$(7) \quad e_{R_1 + R_S \parallel R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } (R_1 + R_S) \parallel R_2$$

$$(8) \quad k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \quad \text{Boltzmann Constant}$$

$$(9) \quad T(K) = 237.15 + T(^{\circ}C) \quad [K] \quad \text{Temperature in kelvins}$$

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- (1) e_N is the voltage noise of the amplifier. For the OPA2210 operational amplifier, $e_N = 2.2 \text{ nV}/\sqrt{\text{Hz}}$ at 1 kHz.
- (2) i_N is the current noise of the amplifier. For the OPA2210 operational amplifier, $i_N = 400 \text{ fA}/\sqrt{\text{Hz}}$ at 1 kHz.
- (3) For additional resources on noise calculations visit [TI's Precision Labs Series](#).

Figure 43. Noise Calculation in Gain Configurations

8.2 Typical Application

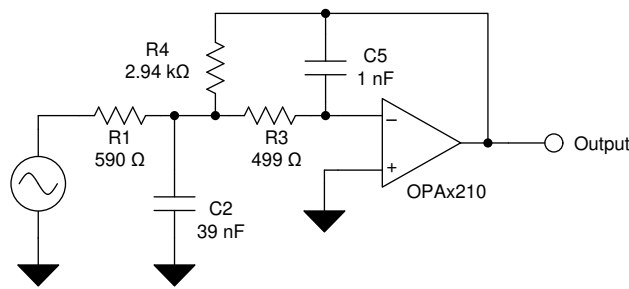


Figure 44. Low-Pass Filter

8.2.1 Design Requirements

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA2210 is designed to construct high-speed, high-precision active filters. [Figure 44](#) shows a second-order, low-pass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in [Figure 44](#). Use [Equation 1](#) to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1 R_3 C_2 C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3 R_4 C_2 C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the low-pass cutoff frequency are calculated by [Equation 2](#):

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_c = \frac{1}{2\pi} \sqrt{(1/R_3 R_4 C_2 C_5)} \quad (2)$$

8.2.3 Application Curve

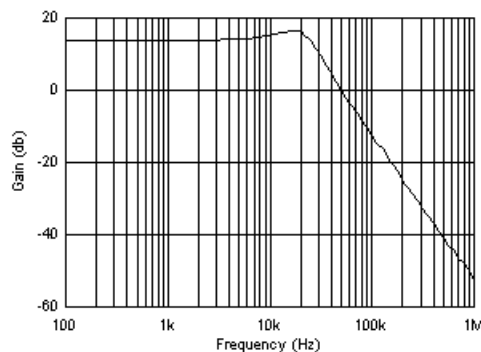


Figure 45. OPA2210 Second-Order, 25-kHz, Chebyshev, Low-Pass Filter

8.3 System Example

8.3.1 Time Gain Control System for Ultrasound Applications

During an ultrasound send-receive cycle, the magnitude of reflected signal depends on the depth of penetration. The ultrasound signal incident on the receiver decreases in amplitude as a function of the time elapsed since transmission, and the TGC helps achieve the best possible signal-to-noise ratio (SNR), even with the decreasing signal amplitude. When the image is displayed, similar material must have similar brightness, regardless of depth; this is achieved by *Linear-in-dB* gain, which means the decibel gain is a linear function of the control voltage (V_{CNTL}).

There are multiple approaches for a TGC control circuit that are based on the type of DAC. [Figure 46](#) shows a high level block diagram for the topology using a current-output multiplying DAC (MDAC) to generate the drive for V_{CNTL} . The op amp used for current-to-voltage (I-to-V) conversion must have low-voltage noise as well as low-current noise density. The current density helps in reducing the overall noise performance because of the DAC output configuration. Because the DAC output can go up to ± 10 V, the op amp must have bipolar operation. The OPA2210 is employed here due to its low voltage-noise density of $2.2 \text{ nV}/\sqrt{\text{Hz}}$, low current-noise density of $500 \text{ fA}/\sqrt{\text{Hz}}$, rail-to-rail output and its ability to accept a wide supply range of ± 2.25 to ± 18 V and provide rail-to-rail output. The low offset voltage and offset drift of the OPA2210 facilitate excellent dc accuracy for the circuit.

The OPA2210 is used to filter and buffer the 10-V reference voltage generated by the REF5010. This serves as the reference voltage for the DAC8802, which generates a current output on I_{OUT} corresponding to the digital input code. The I_{OUT} pin of the DAC8802 is connected to the virtual ground (negative terminal) of the OPA2210; the feedback resistor (R_{FB} is internal to the DAC8802) is connected to the output of the OPA2210, resulting in a current-to-voltage conversion. The output of the OPA2210 has a range of -10 V to 0 V, and it is input to the THS4130, which is configured as a Sallen-Key filter. Finally, the 10-V range is attenuated down to a 1.5-V range, with common mode of 0.75 V using a resistive attenuator. See [2.3-nV/ \$\sqrt{\text{Hz}}\$, Differential, Time Gain Control DAC Reference Design for Ultrasound](#) for an in-depth analysis of [Figure 46](#).

System Example (continued)

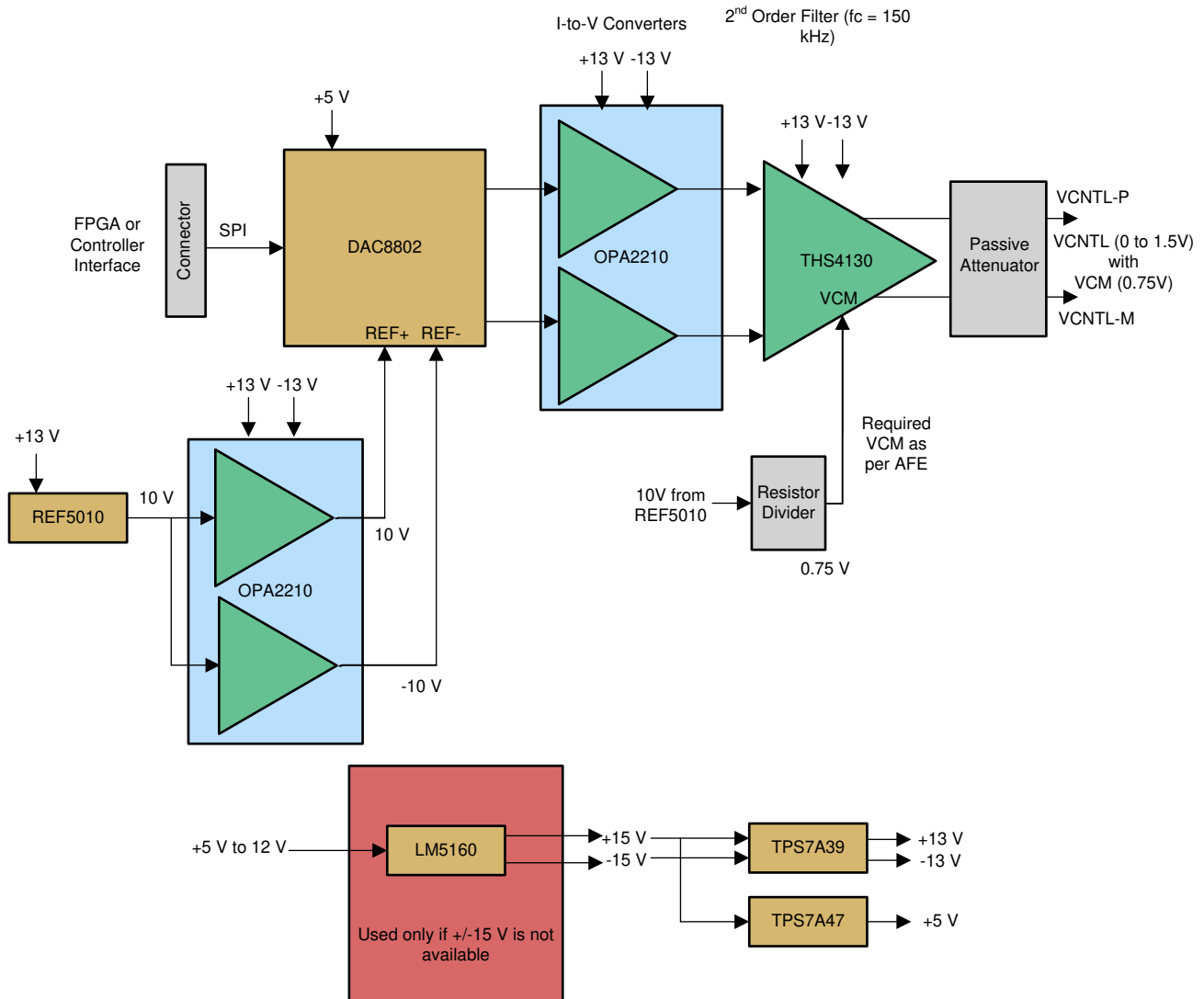


Figure 46. Block Diagram for Time Gain Control System for Ultrasound

9 Power Supply Recommendations

The OPA2210 is specified for operation from 4.5 V to 36 V (± 2.25 V to ± 18 V); many specifications apply from -40°C to 125°C . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including the following guidelines:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1- μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from $V+$ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

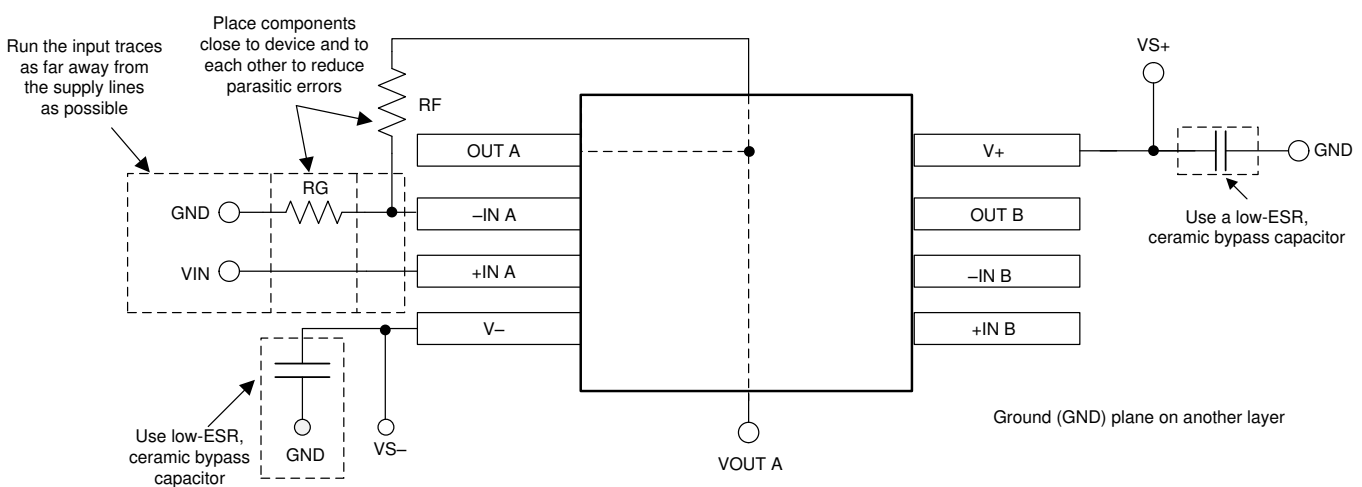


Figure 47. OPA2210 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

11.1.1.2 DIP Adapter EVM

The [DIP Adapter EVM](#) tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT23-6, SOT23-5 and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

11.1.1.3 Universal Operational Amplifier EVM

The [Universal Op Amp EVM](#) is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, VSSOP, TSSOP, and SOT-23 packages are all supported.

NOTE

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

11.1.1.4 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at <http://www.ti.com/www/en/analog/precision-designs/>.

11.1.1.5 WEBENCH® Filter Designer

[WEBENCH® Filter Designer](#) is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, [WEBENCH® Filter Designer](#) allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

11.2 Documentation Support

11.2.1 Related Documentation

The following documents are relevant to using the OPA2210 and recommended for reference. All are available for download at www.ti.com (unless otherwise noted):

- Texas Instruments, [OPA827 Low-Noise, High-Precision, JFET-Input Operational Amplifier data sheet](#)
- Texas Instruments, [OPA2x11 1.1-nV/√Hz Noise, Low Power, Precision Operational Amplifier data sheet](#)
- Texas Instruments, [OPA210, OPA2210, OPA4210 EMI Immunity Performance technical brief](#)
- Texas Instruments, [OPAx209 2.2-nV/√Hz, Low-Power, 36-V Operational Amplifier data sheet](#)
- Texas Instruments, [Microcontroller PWM to 12-bit Analog Out design guide](#)
- Texas Instruments, [Capacitive Load Drive Solution Using an Isolation Resistor design guide](#)
- Texas Instruments, [Noise Measurement Post Amp design guide](#)
- Texas Instruments, [Diagnostic Patient Monitoring and Therapy Application guide](#)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 Trademarks

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WEBENCH is a registered trademark of Texas Instruments.

TINA, DesignSoft are trademarks of DesignSoft, Inc.

All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2210ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2210	Samples
OPA2210IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1OHQ	Samples
OPA2210IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1OHQ	Samples
OPA2210IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2210	Samples
OPA2210IDRGR	PREVIEW	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2210	
OPA2210IDRGT	PREVIEW	SON	DRG	8	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2210	
POPA2210IDRGT	ACTIVE	SON	DRG	8	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

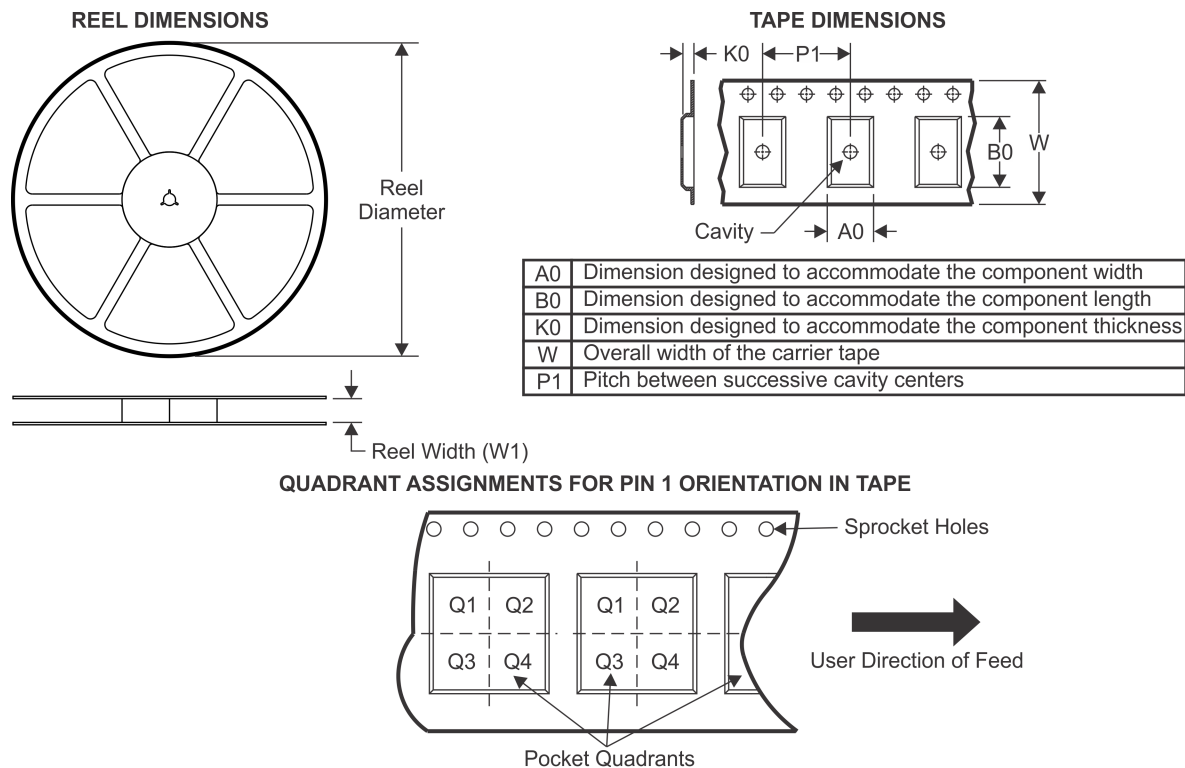
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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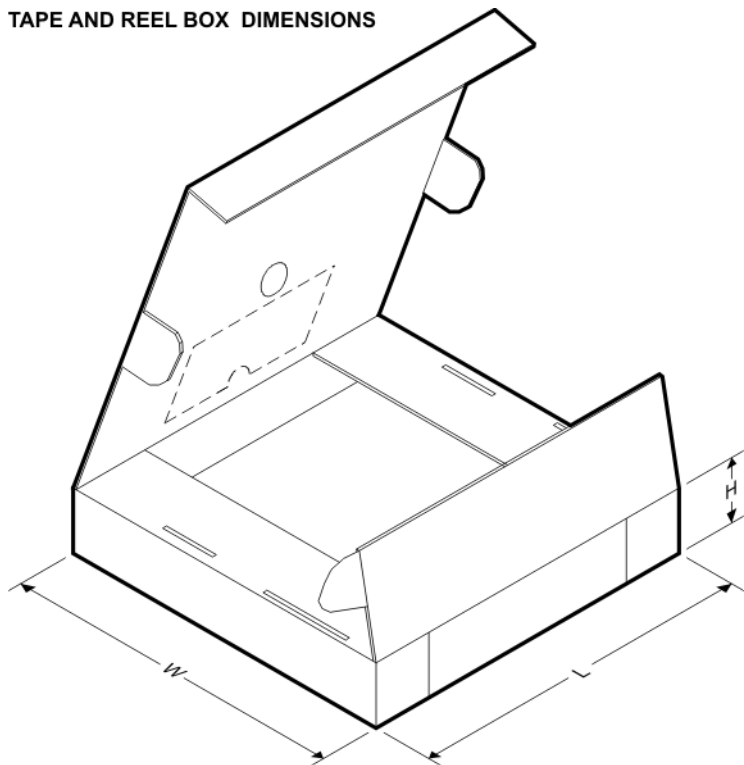
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2210IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2210IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2210IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2210IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2210IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2210IDR	SOIC	D	8	2500	367.0	367.0	35.0



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

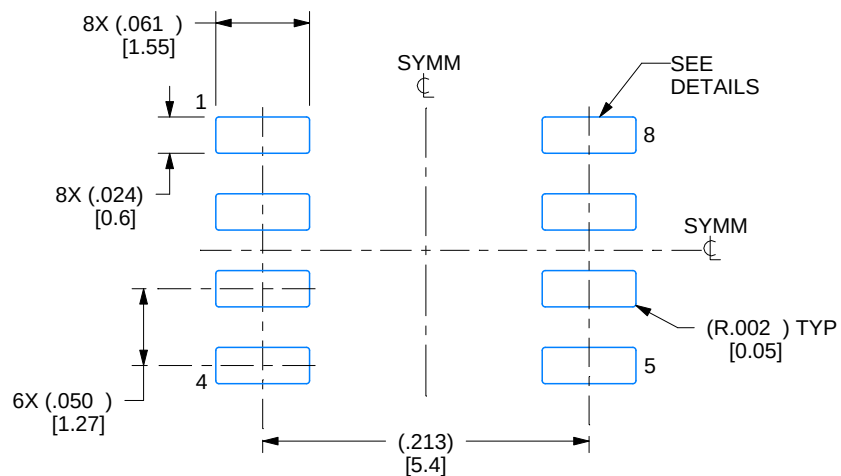


1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

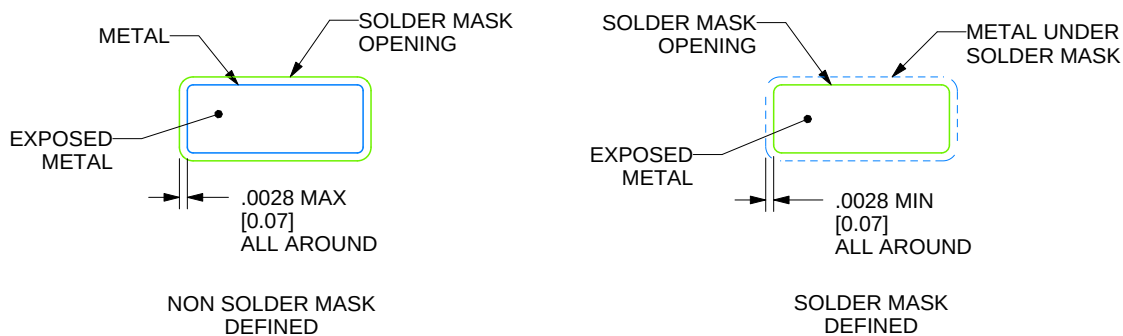
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

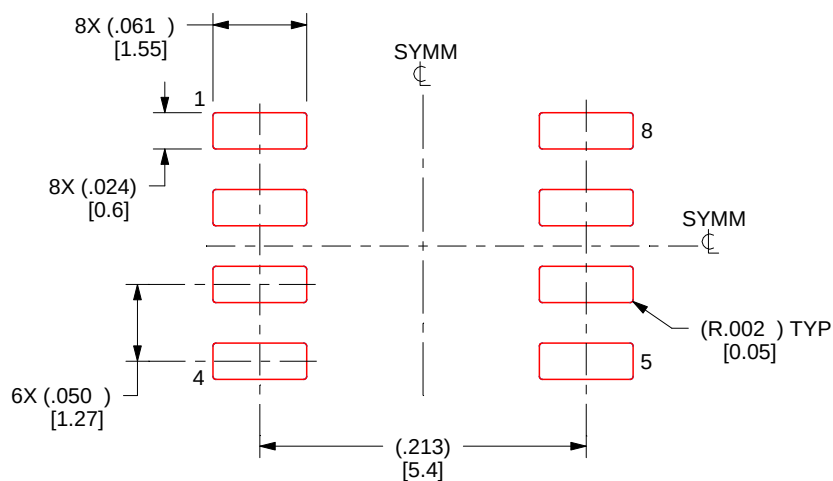
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

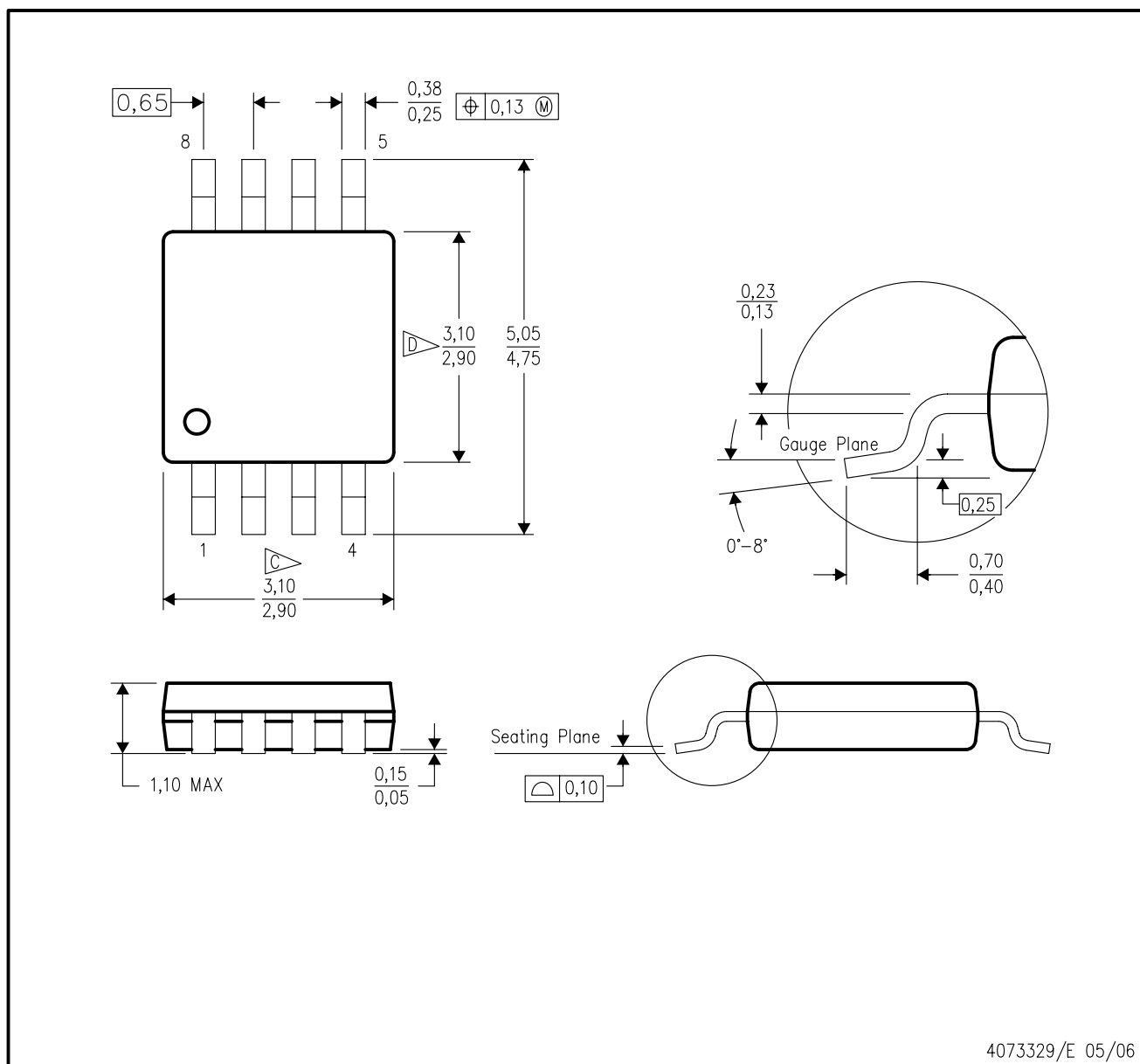
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

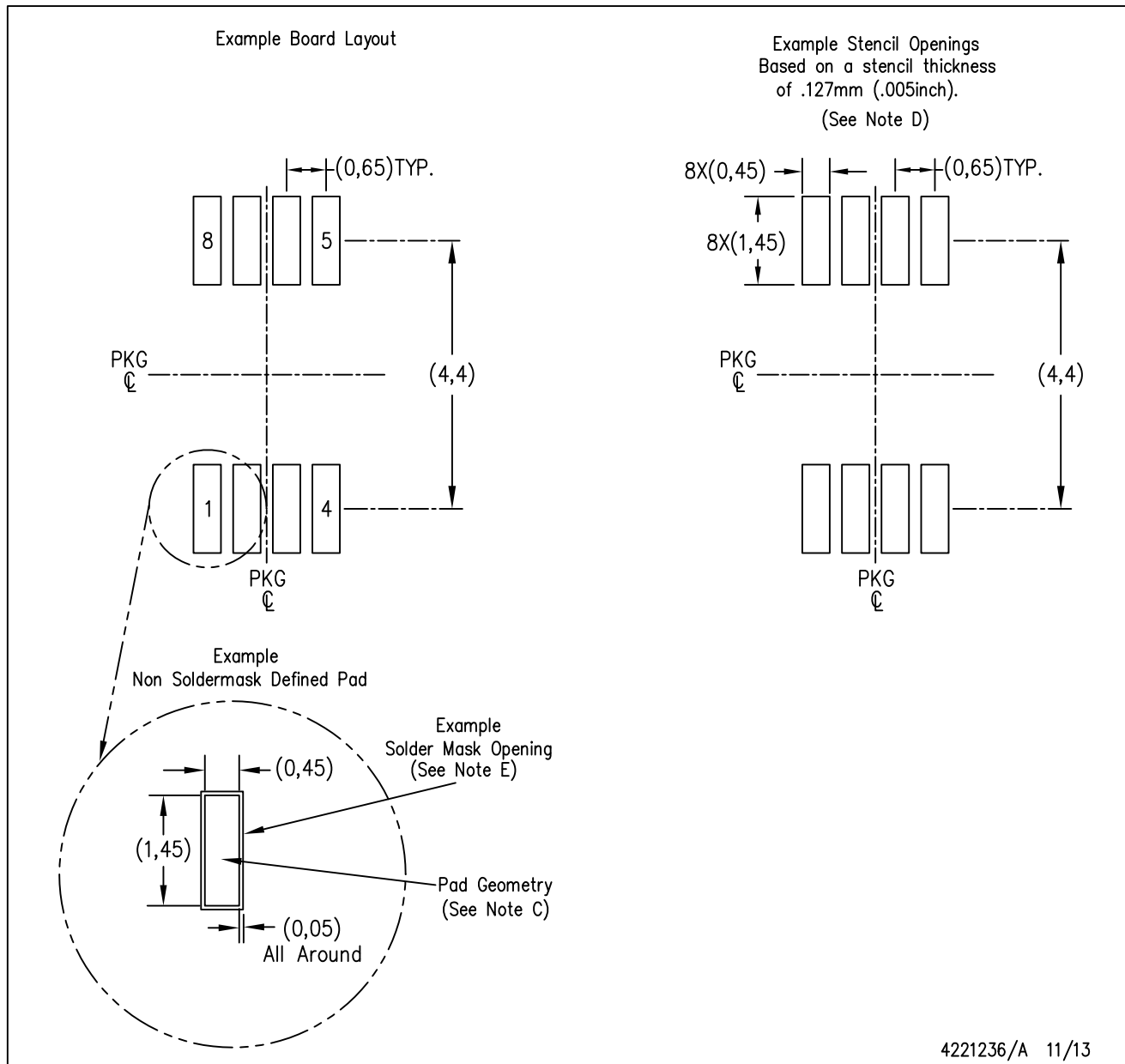
PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

DGK (S-PDSO-G8)

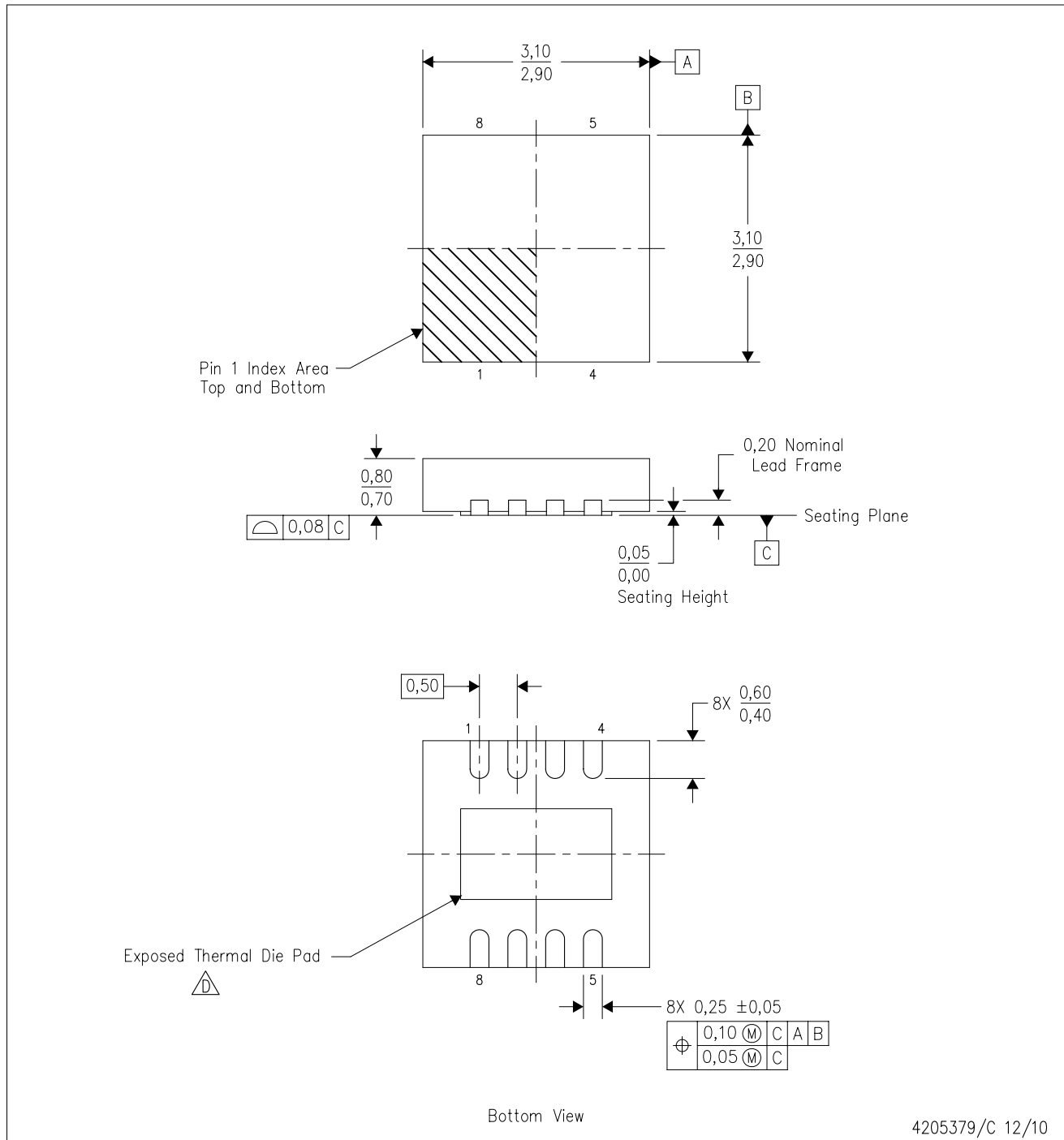
PLASTIC SMALL OUTLINE PACKAGE



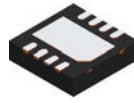
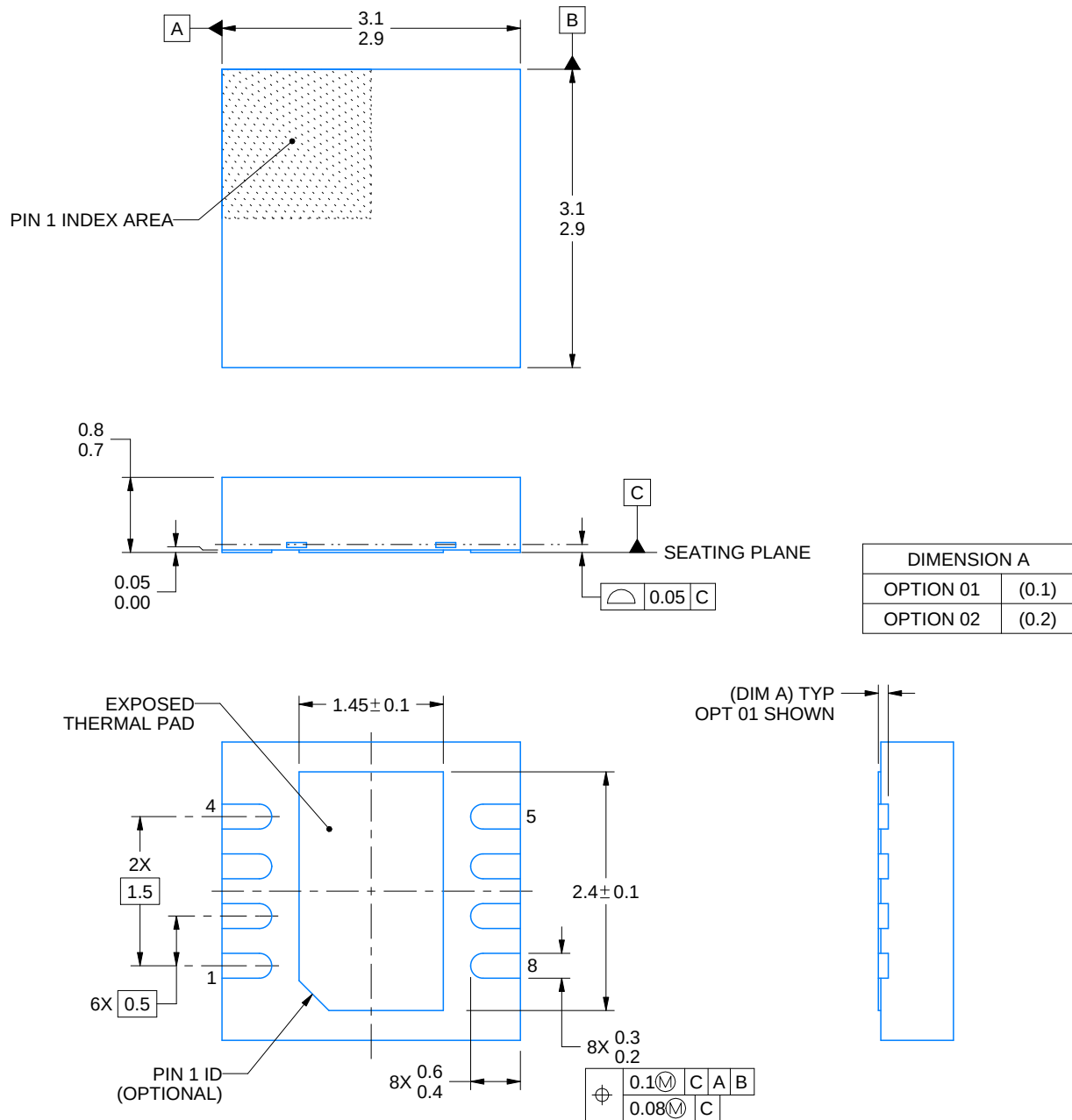
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. JEDEC MO-229 package registration pending.



4218886/A 01/2020

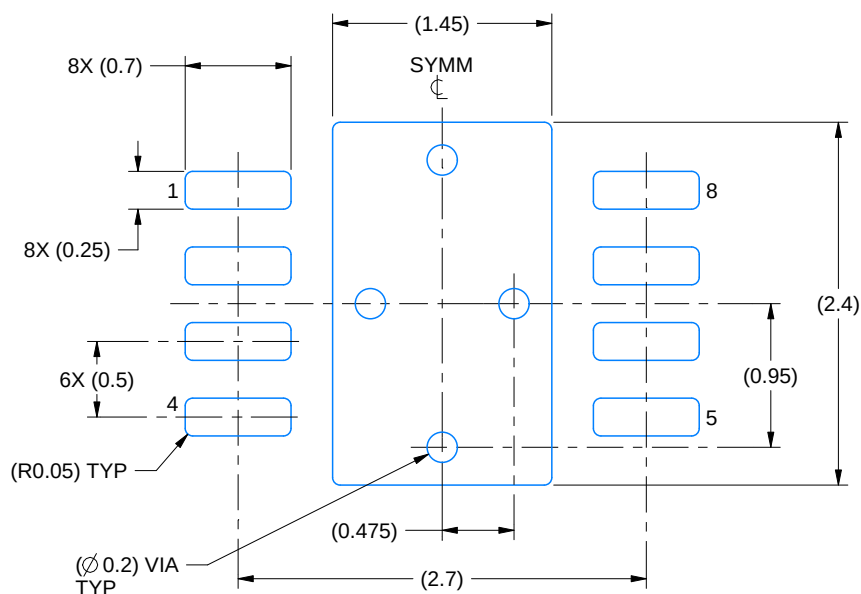
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

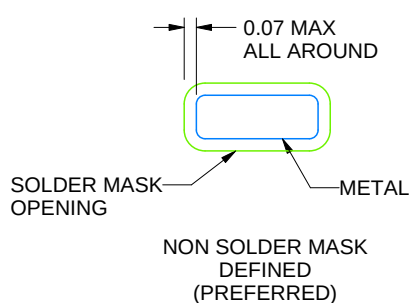
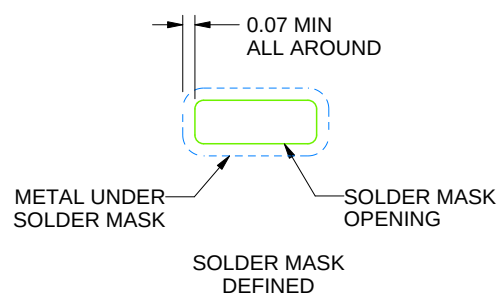
DRG0008B

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218886/A 01/2020

NOTES: (continued)

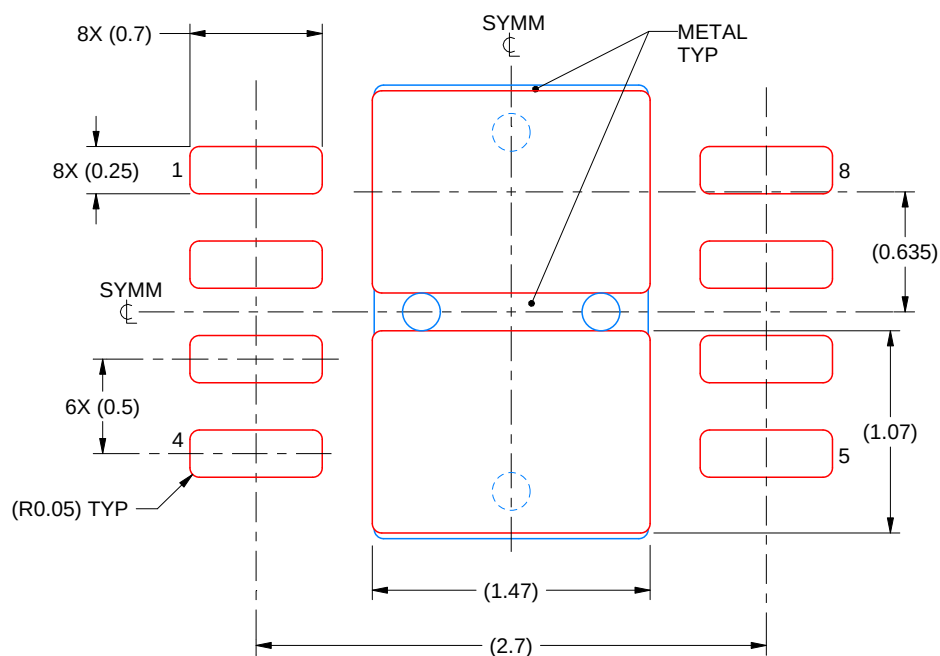
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRG0008B

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218886/A 01/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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