

TS12A12511 5-Ω Single-Channel SPDT Analog Switch With Negative Signaling Capability

1 Features

- $\pm 2.7\text{-V}$ to $\pm 6\text{-V}$ Dual Supply
- 2.7-V to 12-V Single Supply
- $5\text{-}\Omega$ (Typical) ON-State Resistance
- $1.6\text{-}\Omega$ (Typical) ON-State Resistance Flatness
- 3.3-V , 5-V Compatible Digital Control Inputs
- Rail-to-Rail Analog Signal Handling
- Fast t_{ON} , t_{OFF} Times
- Supports Both Digital and Analog Signal Applications
- Tiny 8-Lead SOT-23, 8-Lead MSOP, and QFN-8 Packages
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested per JESD 22
 - $\pm 2000\text{-V}$ Human Body Model (A114-B, Class II)
 - $\pm 1000\text{-V}$ Charged-Device Model (C101)

2 Applications

- Automatic Test Equipment
- Power Routing
- Communication Systems
- Data Acquisition Systems
- Sample-and-Hold Systems
- Relay Replacement
- Battery-Powered Systems

3 Description

The TS12A12511 is a bidirectional, single-channel, single-pole double-throw (SPDT) analog switch that can pass signals with swings of 0 to 12 V or -6 V to 6 V. This switch conducts equally well in both directions when it is on. The device also offers a low ON-state resistance of $5\text{ }\Omega$ (typical), which is matched to within $1\text{ }\Omega$ between channels. The maximum current consumption is $<1\text{ }\mu\text{A}$ and -3 dB bandwidth is $>93\text{ MHz}$. The TS12A12511 exhibits break-before-make switching action, preventing momentary shorting when switching channels. This device is available packaged in an 8-lead VSSOP, 8-lead SOT-23, and a 8-pin WSON.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS12A12511	SOT (8)	2.90 mm $\times$ 1.63 mm
	VSSOP (8)	3.00 mm $\times$ 3.00 mm
	WSON (8)	4.00 mm $\times$ 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

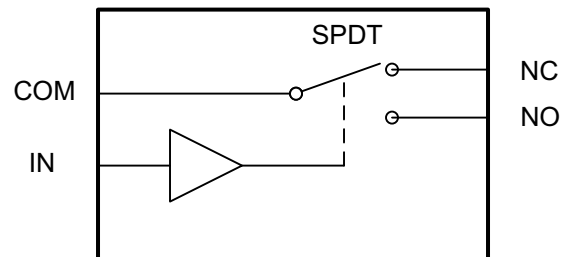


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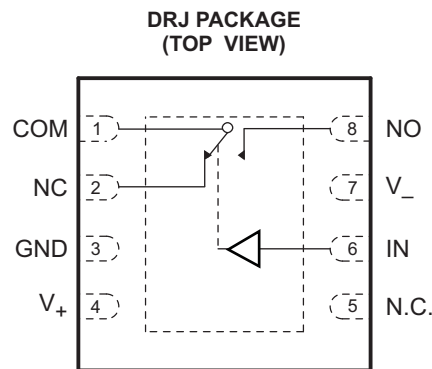
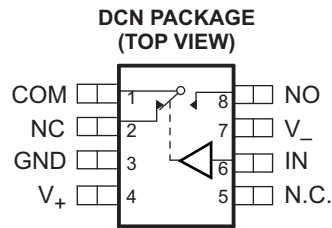
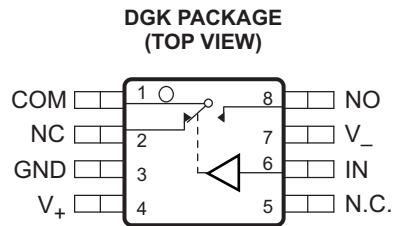
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2015) to Revision D	Page
• Added Junction temperature to the <i>Absolute Maximum Ratings</i> table	4
Changes from Revision B (April 2011) to Revision C	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
Changes from Revision A (May 2010) to Revision B	Page
• Deleted preview status from DGK and DCN packages	3

5 Pin Configuration and Functions



N.C. – Not internally connected

NC – Normally closed

NO – Normally open

The Exposed Thermal Pad must be electrically connected to V₋ or left floating.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COM	1	I/O	Common. Can be an input or output.
GND	3	—	Ground (0 V) reference
IN	6	I	Logic control input
NC	2	I/O	Normally closed. Can be an input or output.
N.C.	5	—	No connect. Not internally connected.
NO	8	I/O	Normally open. Can be an input or output.
V _{CC}	4	I	Most positive power supply
–V _{CC}	7	I	Most negative power supply. This pin is only used in dual-supply applications and should be tied to ground in single-supply applications.

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

T_A = 25°C (unless otherwise noted).

			MIN	MAX	UNIT
V _{CC} to -V _{CC}			0	13	V
V _{CC} to GND			-0.3	13	V
-V _{CC} to GND			-6.5	0.3	V
V _{I/O}	Analog inputs	NC, NO, or COM	-V _{CC} - 0.5	V _{CC} + 0.5	V
I _{IN}	Digital inputs			±30	mA
I _{I/O}	Peak current	NC, NO, or COM		±100	mA
	Continuous current	NC, NO, or COM		±50	mA
T _A	Operating temperature		-40	85	°C
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V _{CC}	0	12	V
-V _{CC}	-6	0	V
V _{I/O}	-V _{CC}	V _{CC}	V
V _{IN}	0	V _{CC}	V

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TS12A12511			UNIT
		DCN	DGK	DRJ	
		8 PINS			
R _{θJA}	Junction-to-ambient thermal resistance	218.4	184.5	47.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	89.9	71.0	48.6	
R _{θJB}	Junction-to-board thermal resistance	144.4	104.5	24.2	
ψ _{JT}	Junction-to-top characterization parameter	7.8	11.3	1.2	
ψ _{JB}	Junction-to-board characterization parameter	141.7	103.3	24.4	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	9.0	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics: ±5-V Dual Supply

 $V_{CC} = 5\text{ V} \pm 10\%$, $-V_{CC} = -5\text{ V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A = 25°C			T _A = –40°C to 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH									
Analog signal range						–V _{CC}	V _{CC}	V	
R _{ON}	ON-state resistance	V _{NC} = –4.5 V to +4.5 V or V _{NO} = –4.5 V to 4.5 V, I _{COM} = –10 mA; see Figure 12	5			5	8	Ω	
ΔR _{ON}	ON-state resistance match between channels	V _{NC} = –4.5 V to +4.5 V or V _{NO} = –4.5 V to +4.5 V, I _{COM} = –10 mA	1			1.2	1.6	Ω	
R _{ON(flat)}	ON-state resistance flatness	V _{NC} = –3.3 V to +3.3 V or V _{NO} = –3.3 V to +3.3 V, I _{COM} = –10 mA	1.6			2.2	2.2	Ω	
LEAKAGE CURRENTS									
I _{NC(OFF)} , I _{NO(OFF)}	OFF leakage current	V _{NC} = –4.5 V to +4.5 V or V _{NO} = –4.5 V to +4.5 V V _{COM} = –4.5 V to +4.5 V; see Figure 13	–1	±0.5	1	–50	50	nA	
I _{NC(ON)} , I _{NO(ON)}	ON leakage current	V _{NC} = –4.5 V to +4.5 V or V _{NO} = –4.5 V to +4.5 V V _{COM} = open; see Figure 14	–1	±0.5	1	–50	50	nA	
DIGITAL INPUTS									
V _{INH}	High-level input voltage					2.4	V _{CC}	V	
V _{INL}	Low-level input voltage					0	0.8	V	
I _{INL} , I _{INH}	Input current	V _{IN} = V _{INL} or V _{INH}	0.005			–1	1	μA	
C _{IN}	Control input capacitance		2.5					pF	
DYNAMIC ⁽¹⁾									
t _{ON}	Turn-ON time	R _L = 300 Ω, C _L = 35 pF, V _{COM} = 3.3 V; see Figure 16	80	95		115		ns	
t _{OFF}	Turn-OFF time	R _L = 300 Ω, C _L = 35 pF, V _{COM} = 3.3 V	41	50		56		ns	
t _{BBM}	Break-before-make time delay	R _L = 300 Ω, C _L = 35 pF, V _{NC} = V _{NO} = 3.3 V; see Figure 17	36			18		ns	
Q _C	Charge injection	V _{NC} = V _{NO} = 0 V, R _{GEN} = 0 Ω, C _L = 1 nF; see Figure 18	26					pC	
O _{ISO}	OFF isolation	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 19	–70					dB	
X _{TALK}	Channel-to-channel crosstalk	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz, see Figure 20	–70					dB	
BW	Bandwidth –3 dB	R _L = 50 Ω, C _L = 5 pF; see Figure 21	93					MHz	
THD	Total harmonic distortion	R _L = 600 Ω, C _L = 15pF, V _{NO} = 1V _{RMS} , f = 20 kHz; see Figure 22	0.004%						
C _{NC(OFF)} , C _{NO(OFF)}	NC, NO OFF capacitance	f = 1 MHz; see Figure 15	14					pF	
C _{COM(ON)} , C _{NC(ON)} , C _{NO(ON)}	COM, NC, NO ON capacitance	f = 1 MHz; see Figure 15	60					pF	
SUPPLY									
I _{CC}	Positive supply current		0.03			1		μA	

(1) Specified by design, not subject to production test.

6.6 Electrical Characteristics: 12-V Single Supply

 $V_{CC} = 12\text{ V} \pm 10\%$, $-V_{CC} = 0\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A = 25°C			T _A = −40°C to 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH									
Analog signal range						0	V _{CC}	V	
R _{on}	ON-state resistance	V _{NC} = 0 V to 10.8 V or V _{NO} = 0 V to 10.8 V, I _{COM} = −10 mA, see Figure 12	5			5	8	Ω	
ΔR _{on}	ON-state resistance match between channels	V _{NC} = 0 V to 10.8 V or V _{NO} = 0 V to 10.8 V, I _{COM} = −10 mA	1.6			2.4	2.6	Ω	
R _{on(flat)}	ON-state resistance flatness	V _{NC} = 3.3 V to 7V or V _{NO} = 3.3 V to 7 V, I _{COM} = −10 mA	1.7			1.8	3.2	Ω	
LEAKAGE CURRENTS									
I _{NC(OFF)} , I _{NO(OFF)}	OFF leakage current	V _{NC} = 0 V to 10.8 V or V _{NO} = 0 V to 10.8 V, V _{COM} = 0 V to 10.8 V; see Figure 13	−10	±0.5	10	−50	50	nA	
I _{NC(ON)} , I _{NO(ON)}	ON leakage current	V _{NC} = 0 V to 10.8V or V _{NO} = 0 V to 10.8 V, V _{COM} = open; see Figure 14	−10	±0.5	10	−50	50	nA	
DIGITAL INPUTS									
V _{INH}	High-level input voltage					5	V _{CC}	V	
V _{INL}	Low-level input voltage					0	0.8	V	
I _{INL} , I _{INH}	Input current	V _{IN} = V _{INL} or V _{INH}	±0.005			−0.1	0.1	μA	
C _{IN}	Digital input capacitance		2.7					pF	
DYNAMIC ⁽¹⁾									
t _{ON}	Turn-ON time	R _L = 300 Ω, C _L = 35 pF, V _{COM} = 3.3 V; see Figure 16	56			85	110	ns	
t _{OFF}	Turn-OFF time	R _L = 300 Ω, C _L = 35 pF, V _{COM} = 3.3 V; see Figure 16	25			30	31	ns	
t _{BBM}	Break-before-make time delay	R _L = 300 Ω, C _L = 35 pF, V _{NC} = V _{NO} = 3.3 V; see Figure 17	30			19		ns	
Q _C	Charge injection	R _{GEN} = V _{NC} = V _{NO} = 0 V, R _{GEN} = 0 Ω, C _L = 1 nF; see Figure 18	491					pC	
O _{ISO}	OFF isolation	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz, see Figure 19	−70					dB	
X _{TALK}	Channel-to-channel crosstalk	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz, see Figure 20	−70					dB	
BW	Bandwidth −3 dB	R _L = 50 Ω, C _L = 5 pF, see Figure 21	122					MHz	
THD	Total harmonic distortion	R _L = 600 Ω, C _L = 15pF, V _{NO} = 1 V _{RMS} , f = 20 kHz; see Figure 22	0.04%						
C _{NC(OFF)} , C _{NO(OFF)}	NC, NO OFF capacitance	f = 1 MHz, see Figure 15	14					pF	
C _{COM(ON)} , C _{NC(ON)} , C _{NO(ON)}	COM, NC, NO ON capacitance	f = 1 MHz, see Figure 15	55					pF	
SUPPLY									
I _{CC}	Positive supply current		0.07			1		μA	

(1) Specified by design, not subject to production test.

6.7 Electrical Characteristics: 5-V Single Supply

 $V_{CC} = 5\text{ V} \pm 10\%$, $-V_{CC} = 0\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A = 25°C			T _A = −40°C to 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH									
Analog signal range						0	V _{CC}	V	
R _{on}	ON-state resistance	V _{NC} = 0 V to 4.5 V or V _{NO} = 0 V to 4.5 V, I _{COM} = −10 mA; see Figure 12	8	10			12.5	Ω	
ΔR _{on}	ON-state resistance match between channels	V _{NC} = 0 V to 4.5 V or V _{NO} = 0 V to 4.5 V, I _{COM} = −10 mA	1	1.1			1.5	Ω	
R _{on(flat)}	ON-state resistance flatness	V _{NC} = 0 V to 4.5 V or V _{NO} = 0 V to 4.5 V, I _{COM} = −10 mA	1.3			1.3	2	Ω	
LEAKAGE CURRENTS									
I _{NC(OFF)} , I _{NO(OFF)}	OFF leakage current	V _{NC} = 0 V to 4.5 V or V _{NO} = 0 V to 4.5 V, V _{COM} = 0 V to 4.5 V; see Figure 13	−1	±0.5	1	−50	50	nA	
I _{NC(ON)} , I _{NO(ON)}	ON leakage current	V _{NC} = 0 V to 4.5V or V _{NO} = 0 V to 4.5 V, V _{COM} = open; see Figure 14	−1	±0.5	1	−50	50	nA	
DIGITAL INPUTS									
V _{INH}	High-level input voltage					2.4	V _{CC}	V	
V _{INL}	Low-level input voltage					0	0.8	V	
I _{INL} , I _{INH}	Input current	V _{IN} = V _{INL} or V _{INH}	0.01			−0.1	0.1	μA	
C _{IN}	Digital input capacitance		2.8			pF			
DYNAMIC ⁽¹⁾									
t _{ON}	Turn-ON time	R _L = 300 Ω, C _L = 35 pF, V _{COM} = 3.3 V; see Figure 16	119	145			178	ns	
t _{OFF}	Turn-OFF time	R _L = 300 Ω, C _L = 35 pF, V _{COM} = 3.3 V; see Figure 16	38	47			95.2	ns	
t _{BBM}	Break-before-make time delay	R _L = 300 Ω, C _L = 35 pF, V _{NC} = V _{NO} = 3.3 V; see Figure 17	79			44		ns	
Q _C	Charge injection	V _{GEN} = V _{NC} = V _{NO} = 0 V, R _{GEN} = 0 Ω, C _L = 1 nF; see Figure 18	65					pC	
O _{ISO}	OFF isolation	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz, see Figure 19	−70					dB	
X _{TALK}	Channel-to-channel crosstalk	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz, see Figure 20	−70					dB	
BW	Bandwidth −3 dB	R _L = 50 Ω, see Figure 21	152					MHz	
THD	Total harmonic distortion	R _L = 600 Ω, C _L = 15 pF, V _{NO} = 1 VRMS, f = 20 kHz; see Figure 22	0.04%						
C _{NC(OFF)} , C _{NO(OFF)}	NC, NO OFF capacitance	f = 1 MHz, see Figure 15	15					pF	
C _{COM(ON)} , C _{NC(ON)} , I _{NO(ON)}	COM, NC, NO ON capacitance	f = 1 MHz, see Figure 15	55					pF	
POWER REQUIREMENTS									
I _{CC}	Positive supply current	V _{IN} = 0 V or V _{CC}	0.02				1	μA	

(1) Specified by design, not subject to production test.

6.8 Typical Characteristics

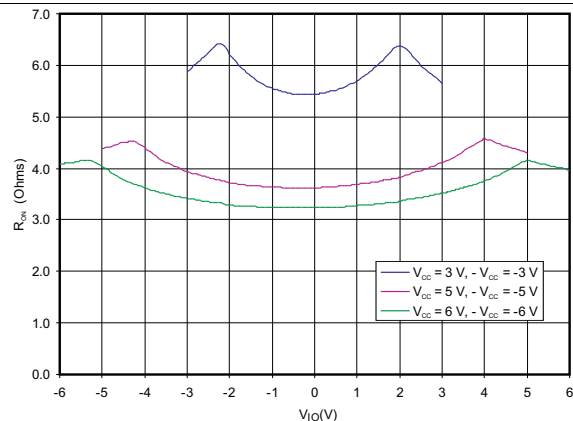


Figure 1. R_{ON} vs V_{IO}

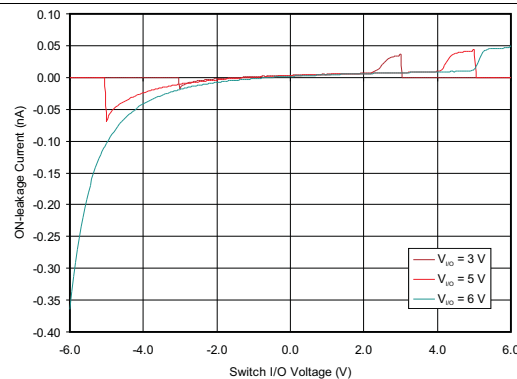


Figure 2. Leakage Current vs I/O voltage (Switch ON)

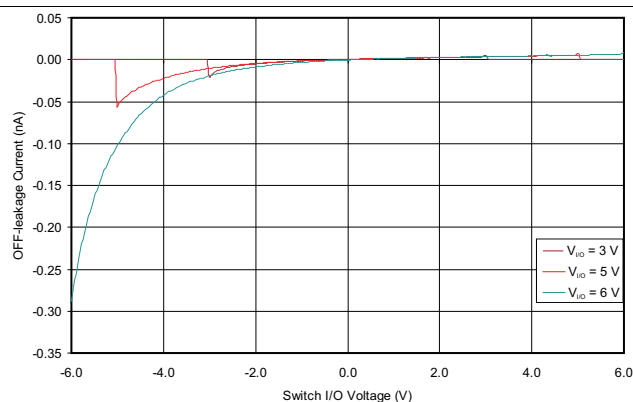


Figure 3. Leakage Current vs I/O Voltage (Switch OFF)

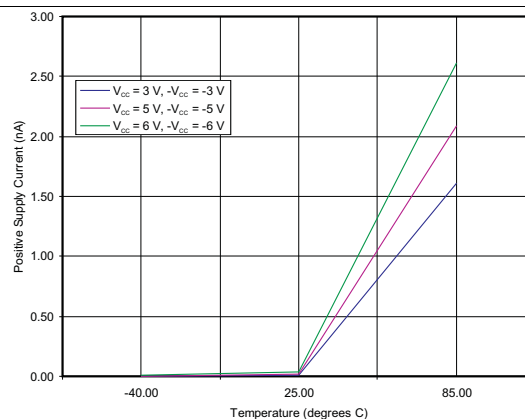


Figure 4. Positive Supply Current vs Temperature

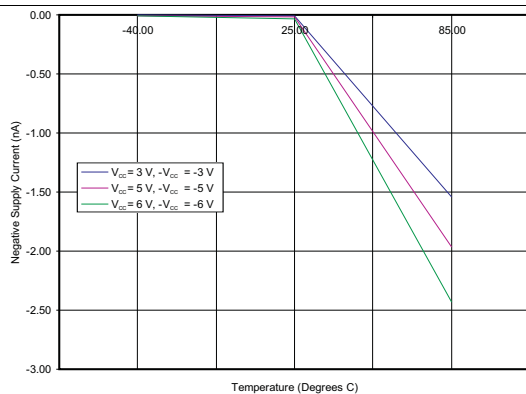


Figure 5. Negative Supply Current vs Temperature

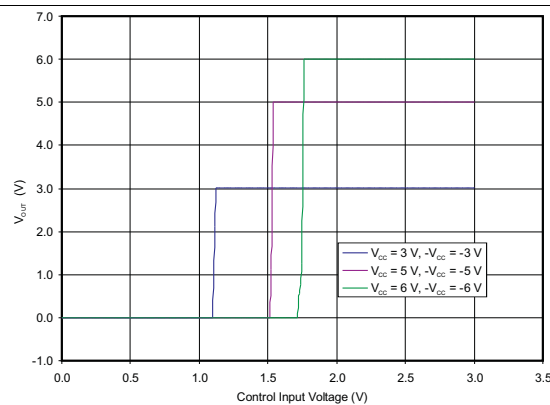


Figure 6. Control Input (IN) Threshold Voltage

Typical Characteristics (continued)

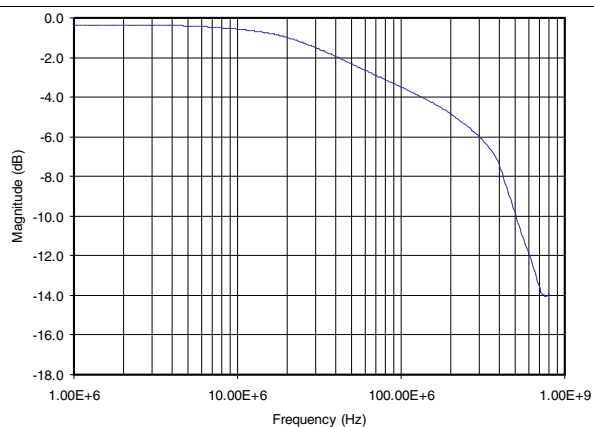


Figure 7. Bandwidth Dual Supply (± 5 V)

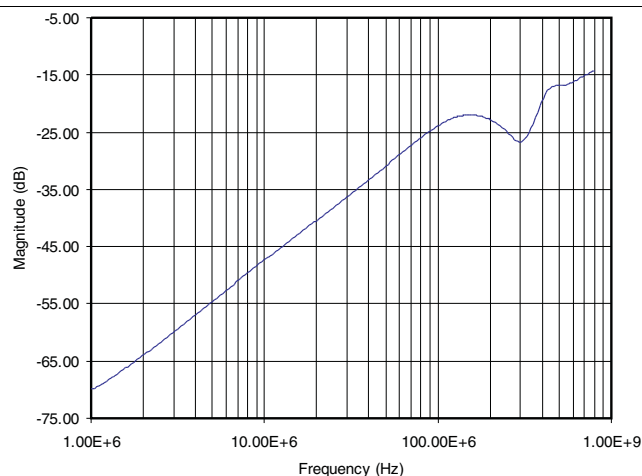


Figure 8. Off Isolation vs Frequency Dual Supply (± 5 V)

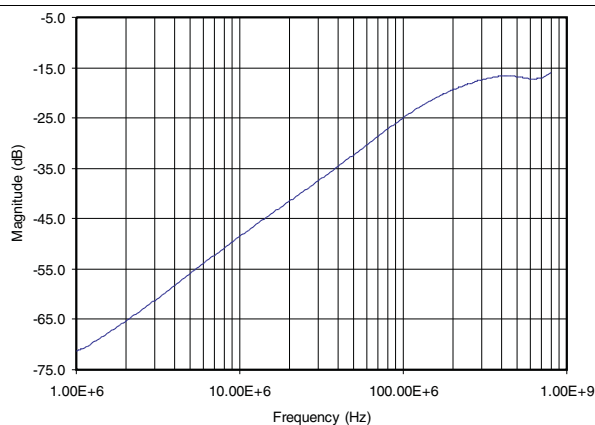


Figure 9. Crosstalk vs Frequency Dual Supply (± 5 V)

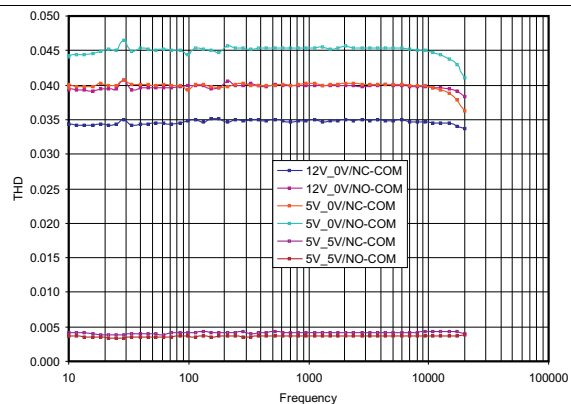


Figure 10. THD+N (%) vs Frequency

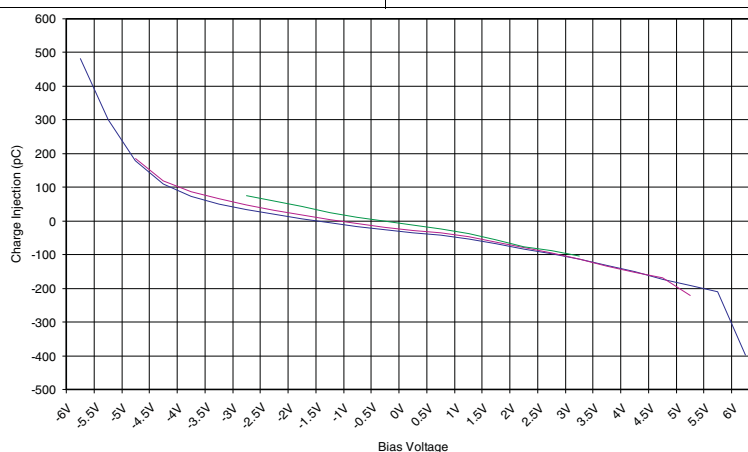


Figure 11. Charge Injection vs Bias Voltage

7 Parameter Measurement Information

7.1 Test Circuits

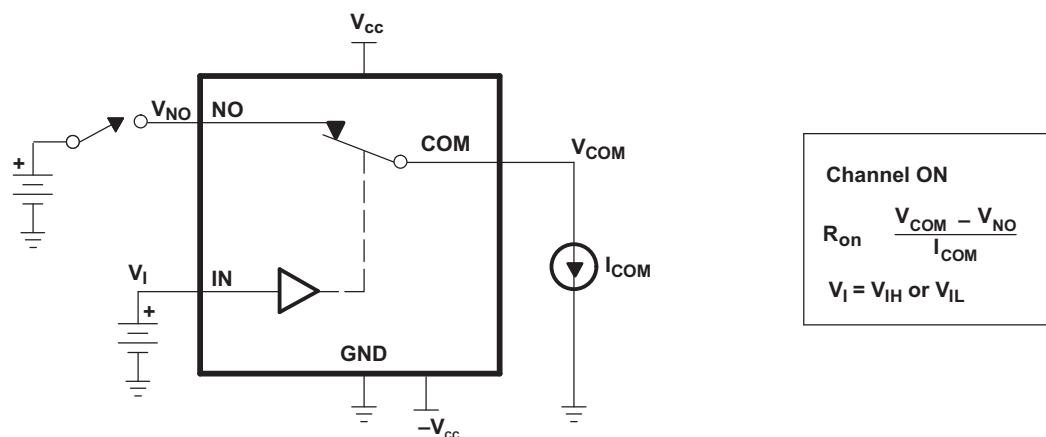


Figure 12. ON-State Resistance

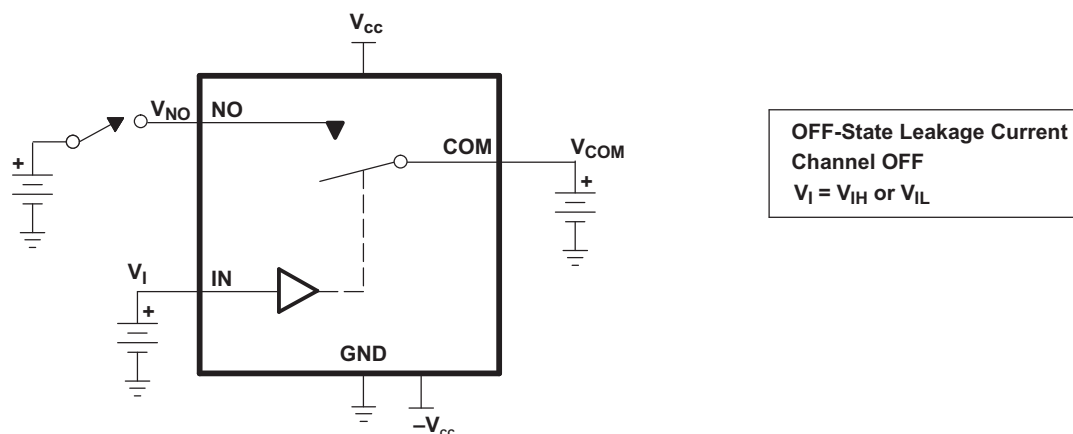


Figure 13. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$)

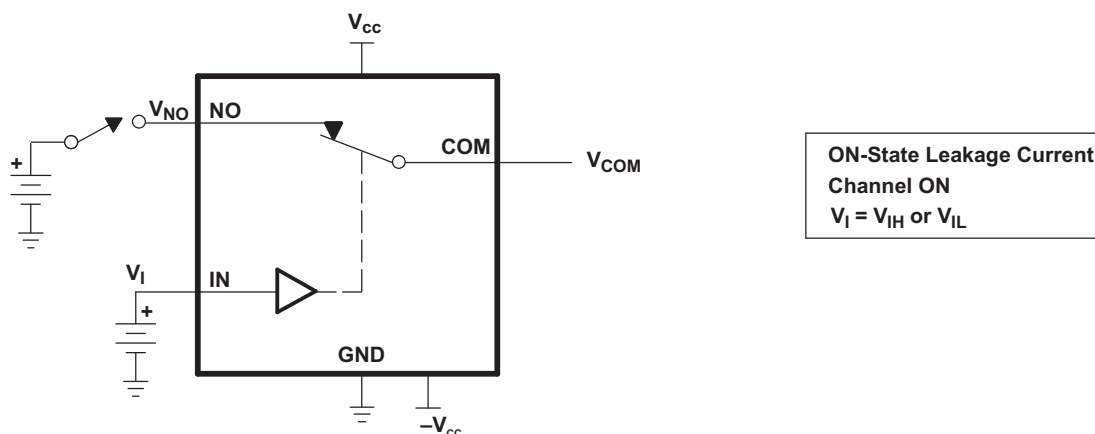


Figure 14. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

Test Circuits (continued)

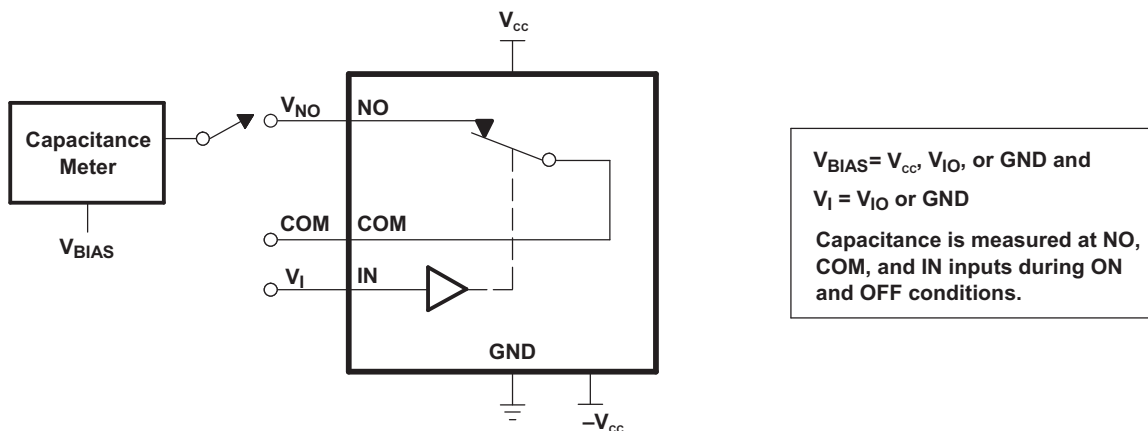
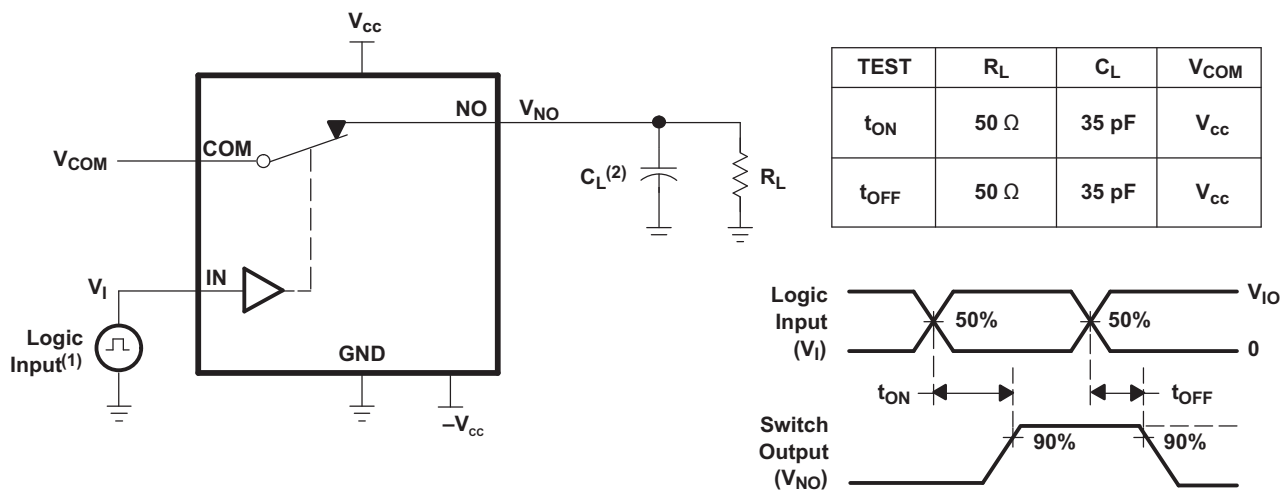


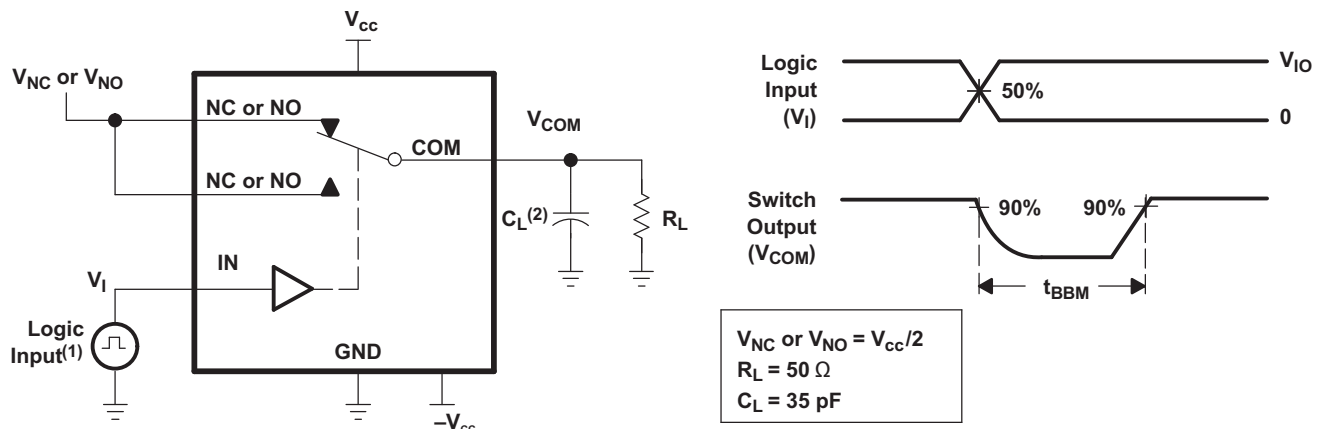
Figure 15. Capacitance ($C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)



(1) All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.

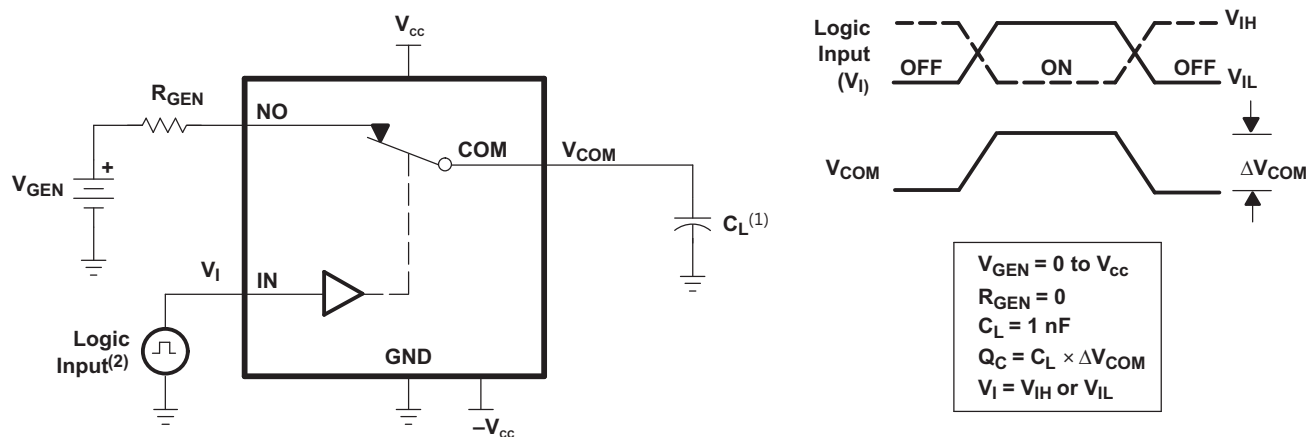
(2) C_L includes probe and jig capacitance.

Figure 16. Turn-ON (t_{ON}) and Turn-OFF Time (t_{OFF})

Test Circuits (continued)


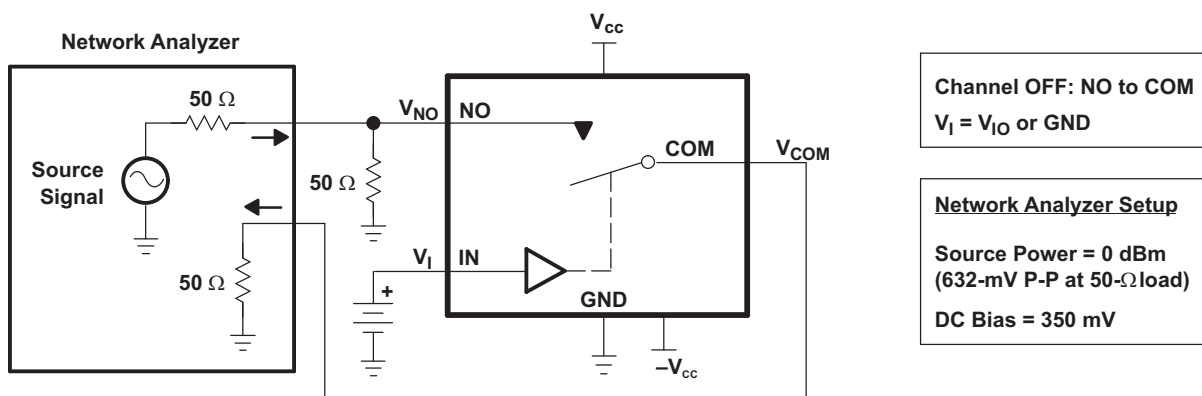
(1) All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.

(2) C_L includes probe and jig capacitance.

Figure 17. Break-Before-Make Time Delay (t_{BBM})


(1) C_L includes probe and jig capacitance.

(2) All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.

Figure 18. Charge Injection (Q_C)

Figure 19. OFF Isolation (O_{ISO})

Test Circuits (continued)

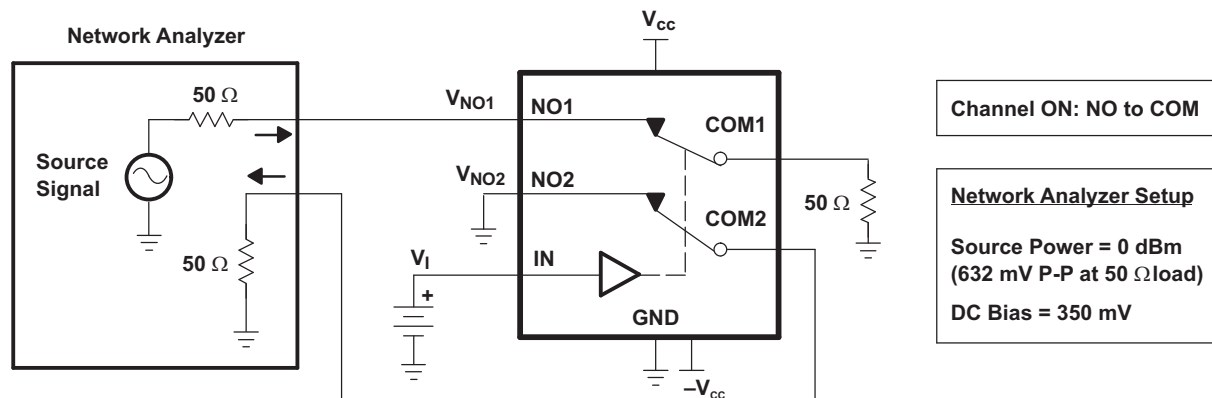


Figure 20. Channel-to-Channel Crosstalk (X_{TALK})

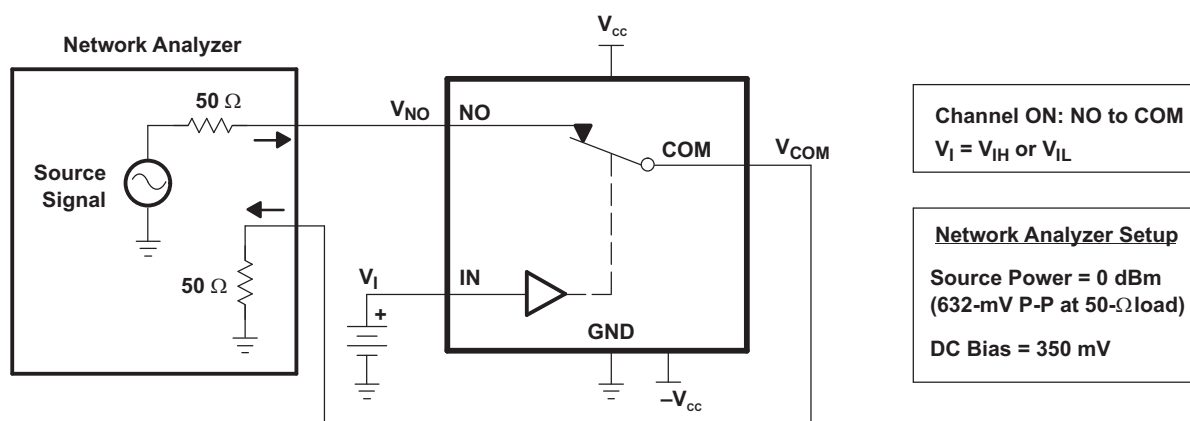
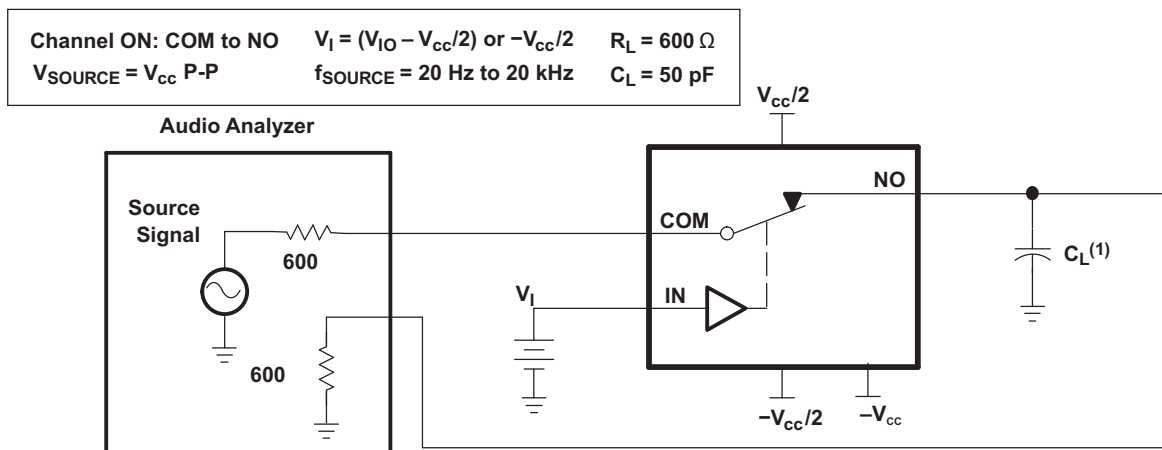


Figure 21. Bandwidth (BW)



(1) C_L includes probe and jig capacitance.

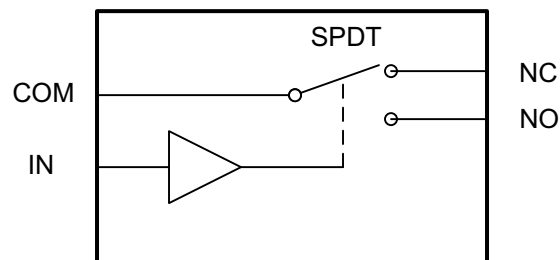
Figure 22. Total Harmonic Distortion

8 Detailed Description

8.1 Overview

The TS12A12511 is a bidirectional, single channel, single-pole double-throw (SPDT) analog switch that can pass signals with swings of 0 to 12 V or –6 V to 6 V. This switch conducts equally well in both directions when it is on. It also offers a low ON-state resistance of 5 Ω (typical), which is matched to within 1 Ω between channels. The max current consumption is < 1 μ A and –3 dB bandwidth is > 93 MHz. The TS12A12511 exhibits break-before-make switching action, preventing momentary shorting when switching channels. This device is available packaged in an 8-lead MSOP, 8-lead SOT-23, and a 8-pin QFN.

8.2 Functional Block Diagram



8.3 Feature Description

The TS12A12511 can pass signals with swings of 0 to 12 V or –6 V to 6. The device is great for applications where the AC signals do not have a common mode voltage since both the positive and negative swing of the signal can be passed through the device with little distortion.

8.4 Device Functional Modes

Table 1. Truth Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	On	Off
H	Off	On

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Analog signals that range over the entire supply voltage (V_{CC} to GND) or (V_{CC} to $-V_{CC}$) can be passed with very little change in ON-state resistance. The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs.

9.2 Typical Application

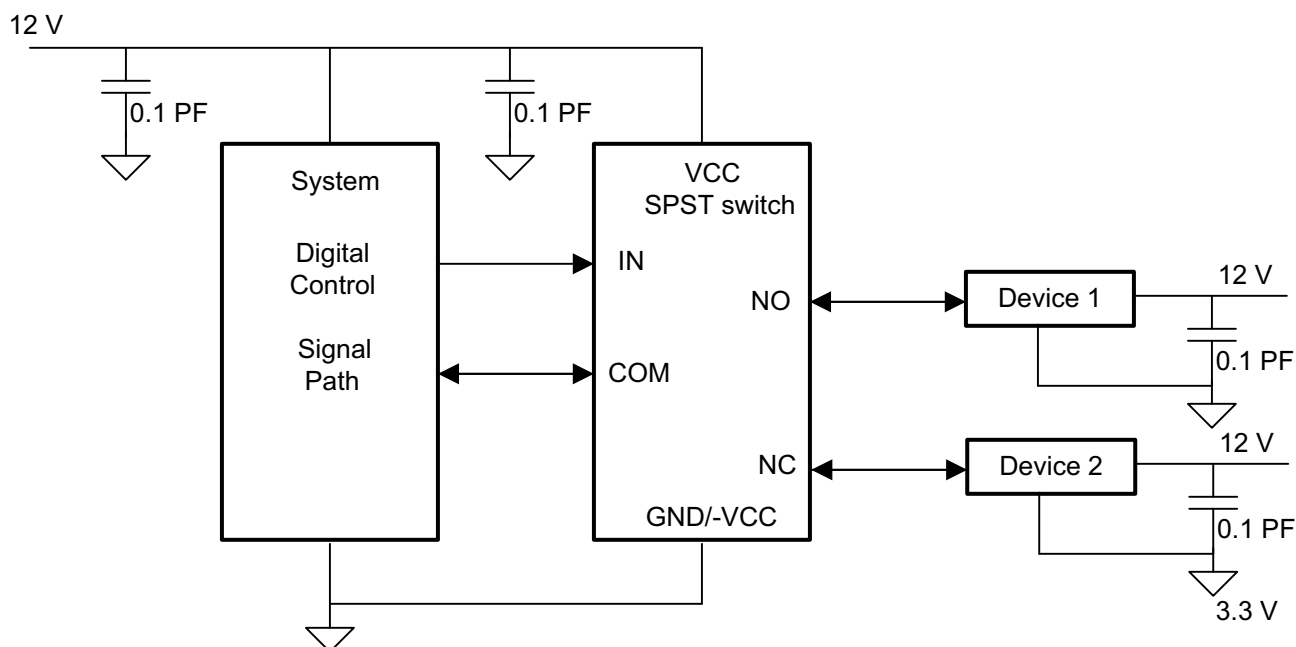


Figure 23. Typical Application Schematic

9.2.1 Design Requirements

Pull the digitally controlled input select pin IN to VCC or GND to avoid unwanted switch states that could result if the logic control pin is left floating.

9.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch since the TS12A12511 input/output signal swing of the device is dependant of the supply voltage V_{CC} and $-V_{CC}$.

Typical Application (continued)

9.2.3 Application Curve

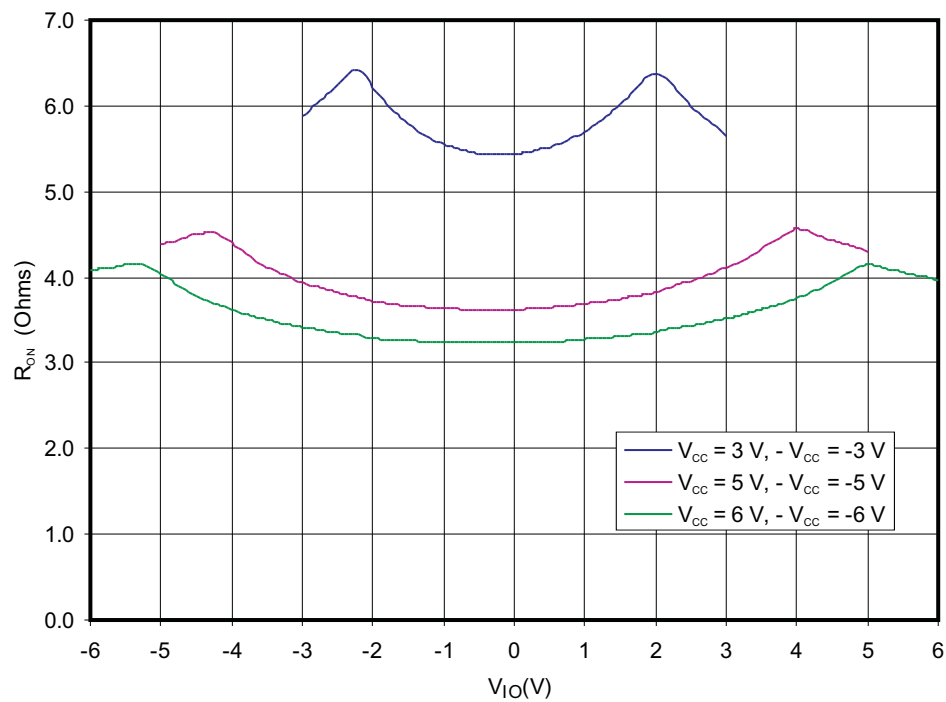


Figure 24. R_{ON} vs V_{IO}

10 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence VCC and -VCC on first, followed by NO, NC, or COM.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components. A 0.1- μ F capacitor, connected from VCC to GND, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

It is recommended to place a bypass capacitor as close to the supply pins, VCC and -VCC, as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum. Minimize trace lengths and vias on the signal paths in order to preserve signal integrity.

11.2 Layout Example

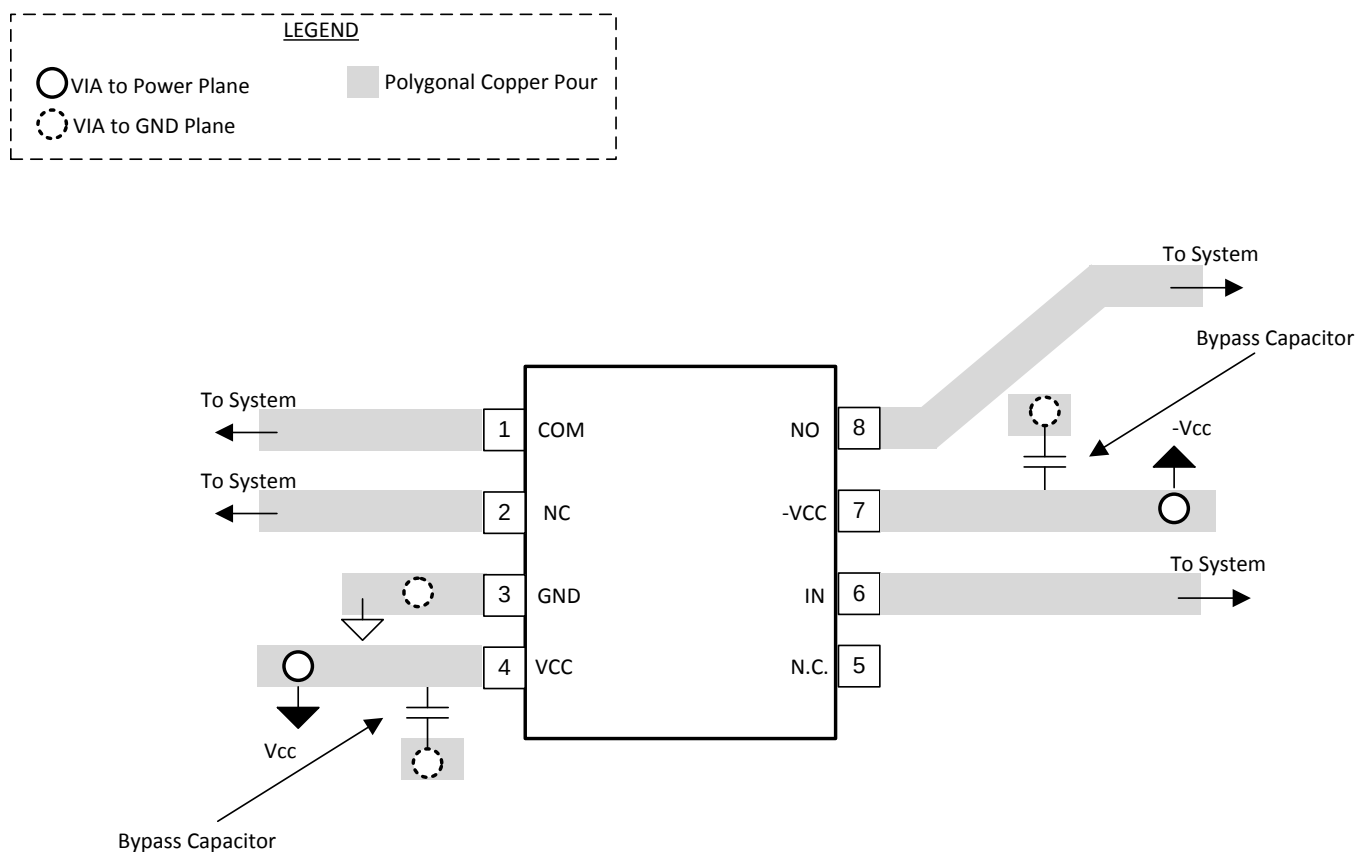


Figure 25. Layout Schematic

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS12A12511DCNR	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFHS HFHA	Samples
TS12A12511DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2US 2UA	Samples
TS12A12511DRJR	ACTIVE	SON	DRJ	8	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVE	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

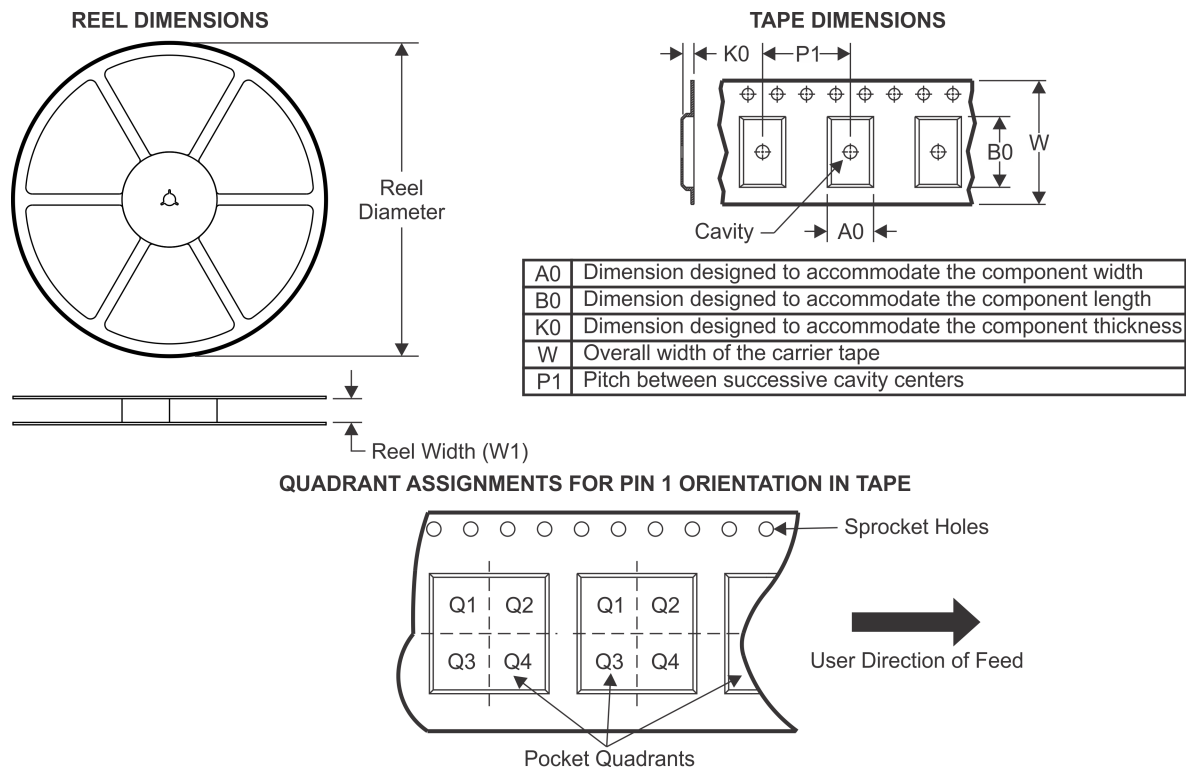


www.ti.com

PACKAGE OPTION ADDENDUM

6-Feb-2020

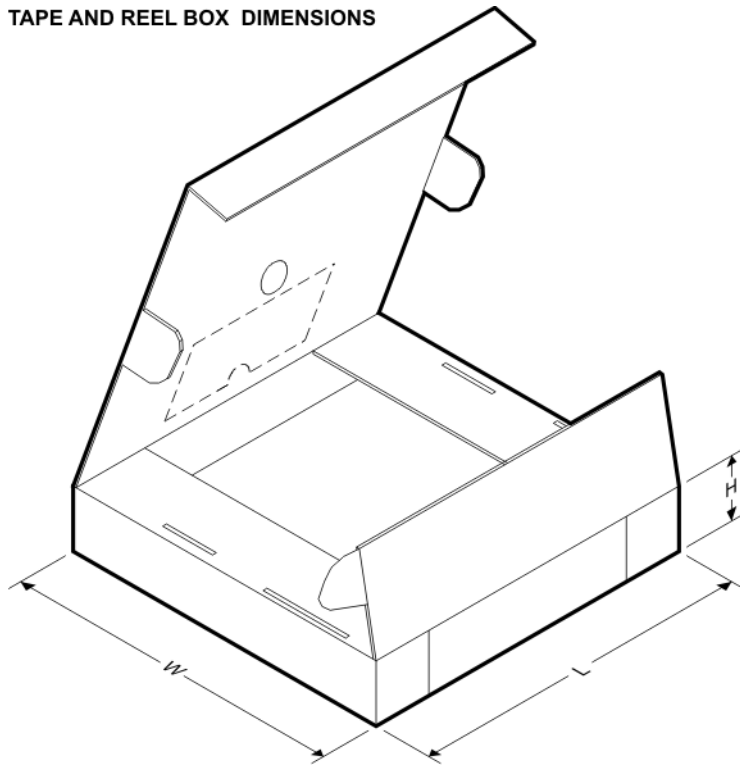
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS12A12511DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS12A12511DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS12A12511DRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

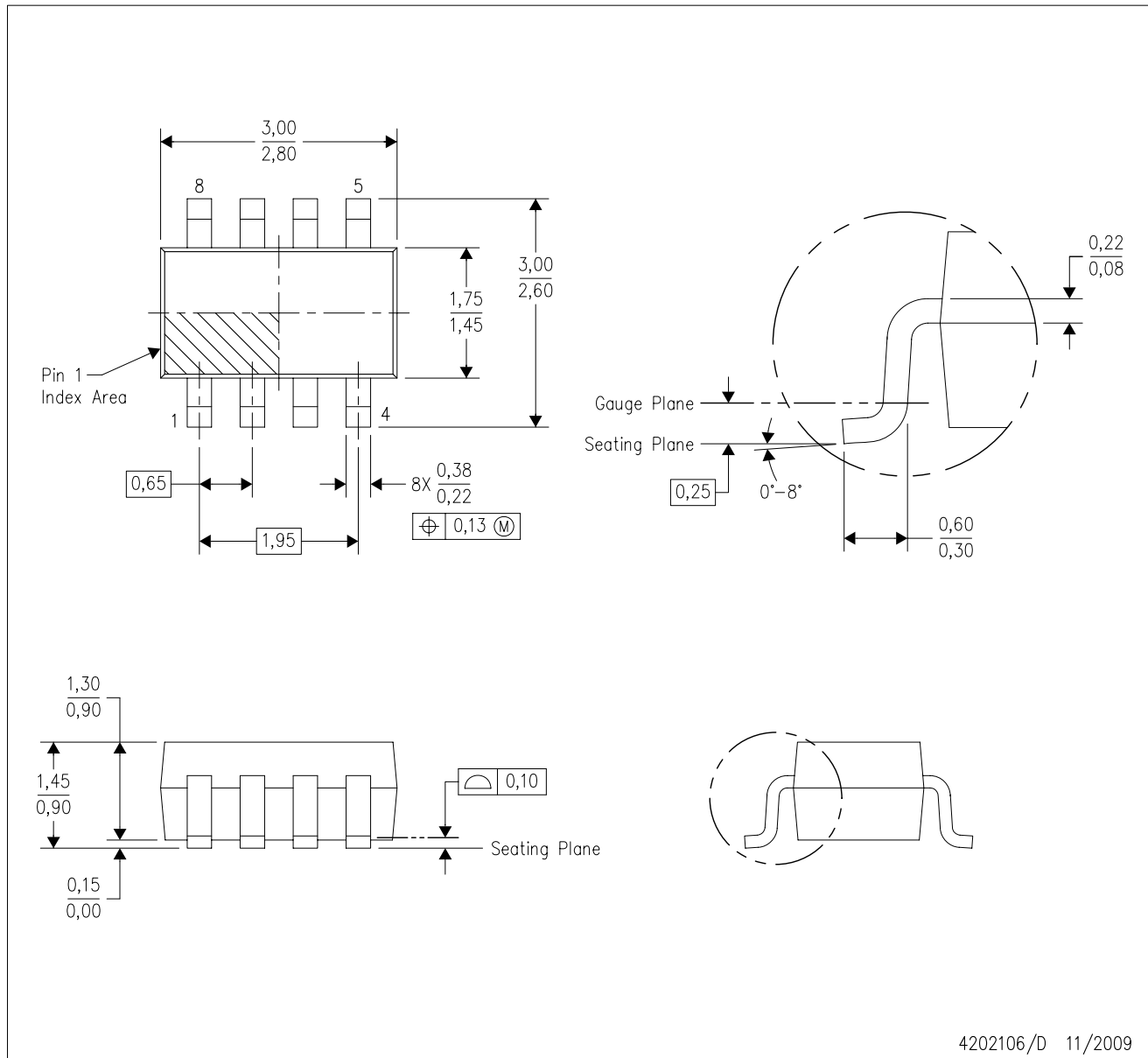


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS12A12511DCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TS12A12511DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TS12A12511DRJR	SON	DRJ	8	1000	210.0	185.0	35.0

DCN (R-PDSO-G8)

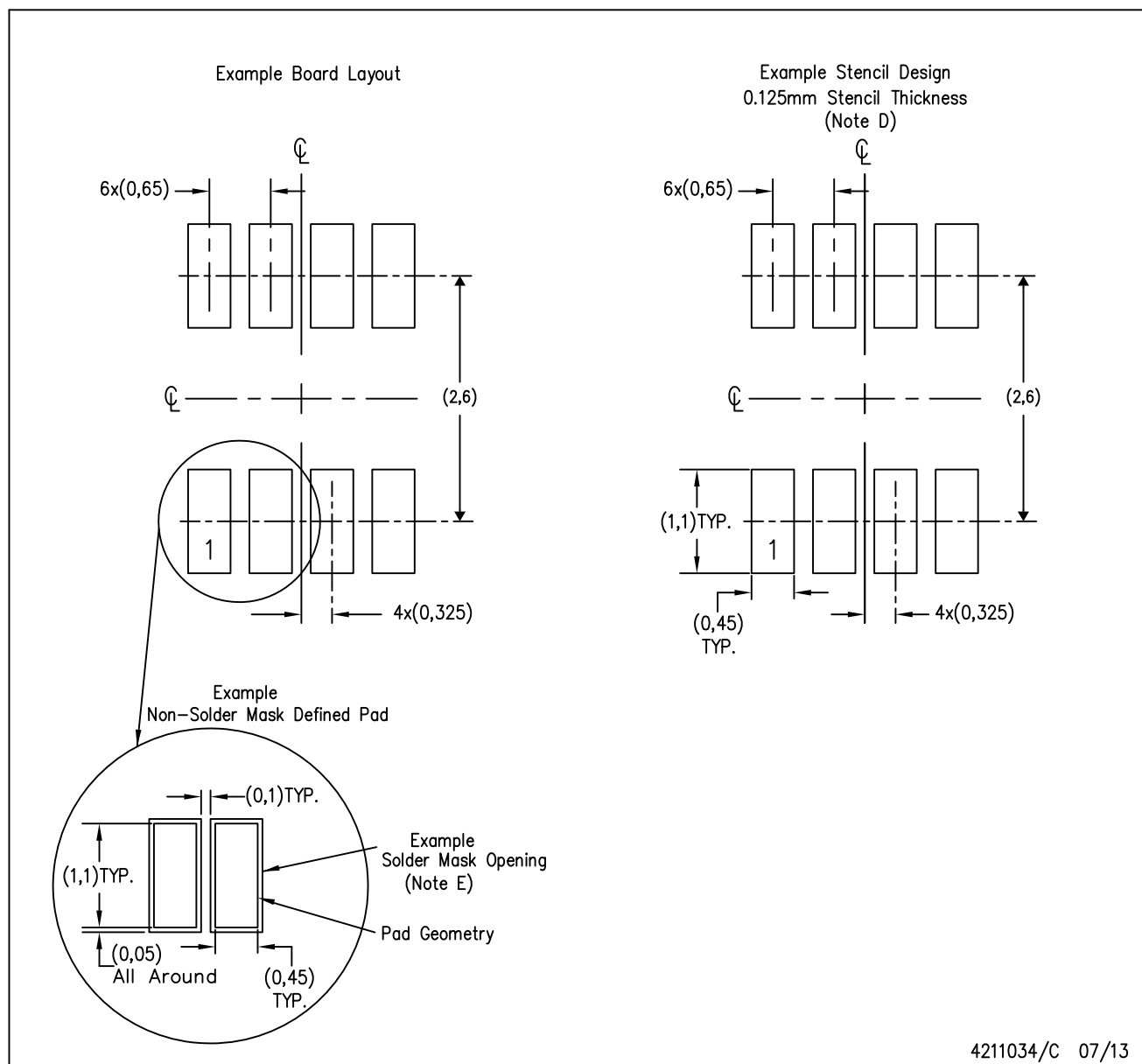
PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
 - D. Package outline inclusive of solder plating.
 - E. A visual index feature must be located within the Pin 1 index area.
 - F. Falls within JEDEC MO-178 Variation BA.
 - G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R-PDSO-G8)

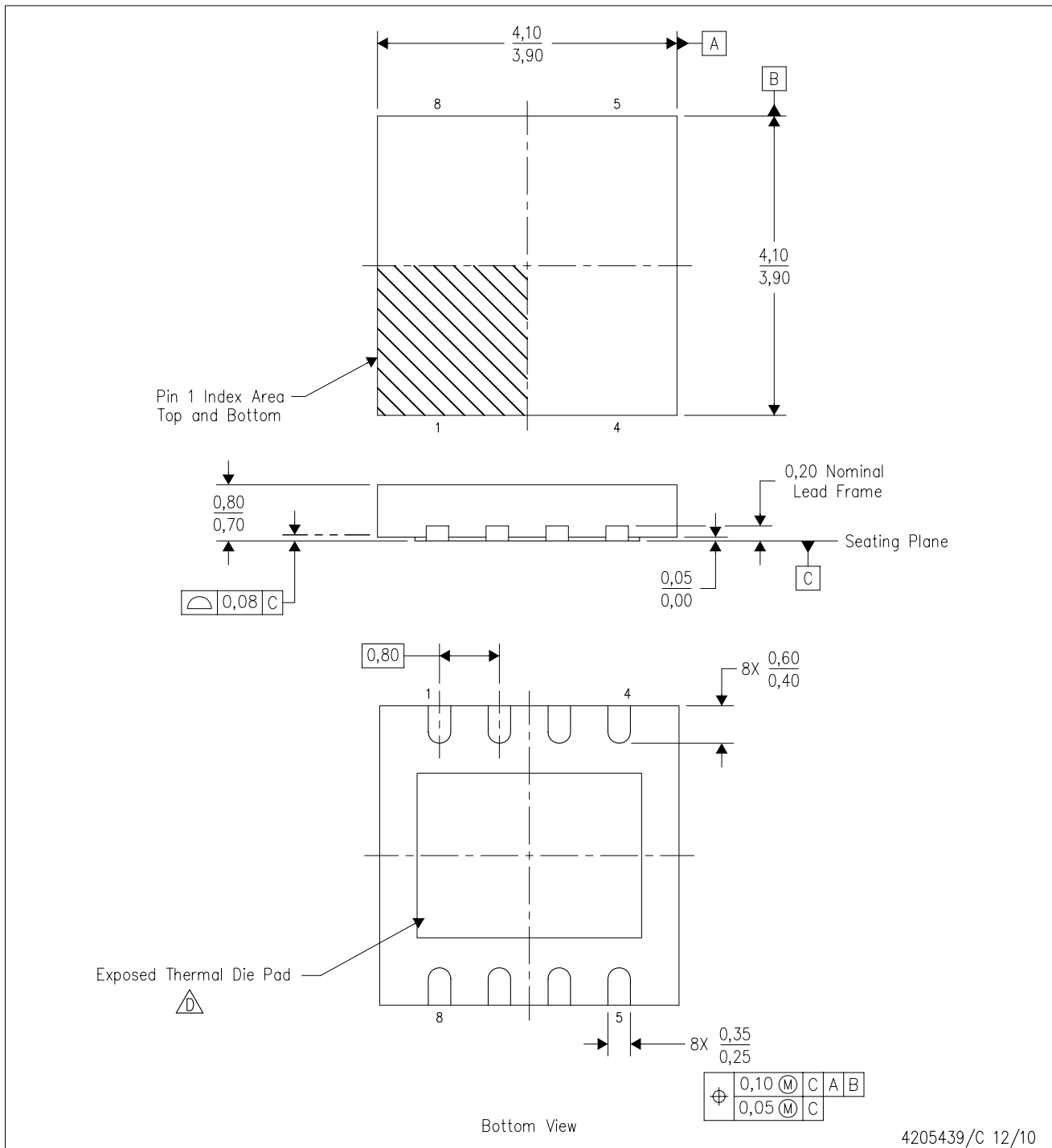
PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRJ (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



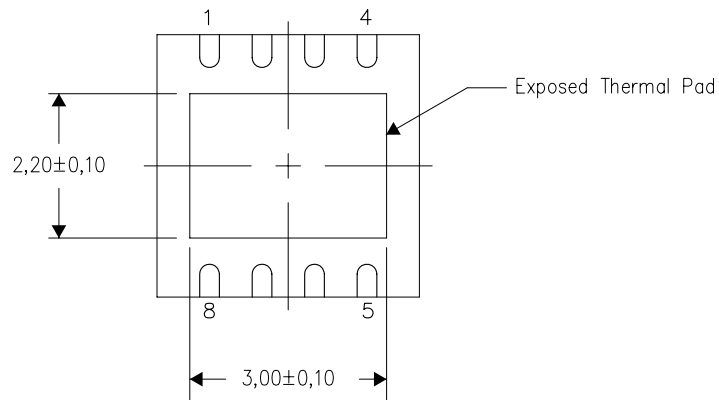
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Package complies to JEDEC MO-229 variation WGGB.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

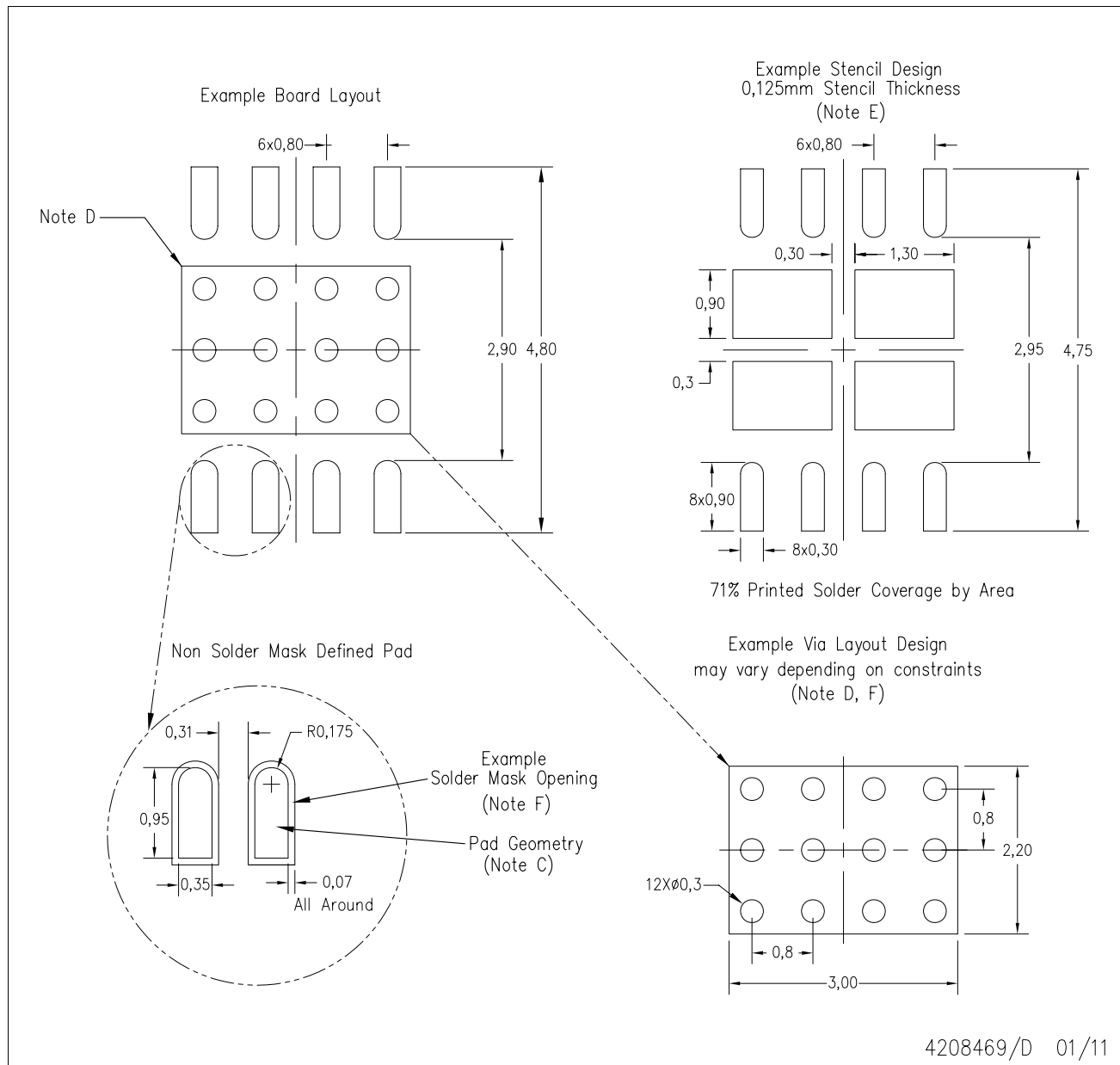
Exposed Thermal Pad Dimensions

4206882/F 01/11

NOTE: All linear dimensions are in millimeters

DRJ (S-PWSON-N8)

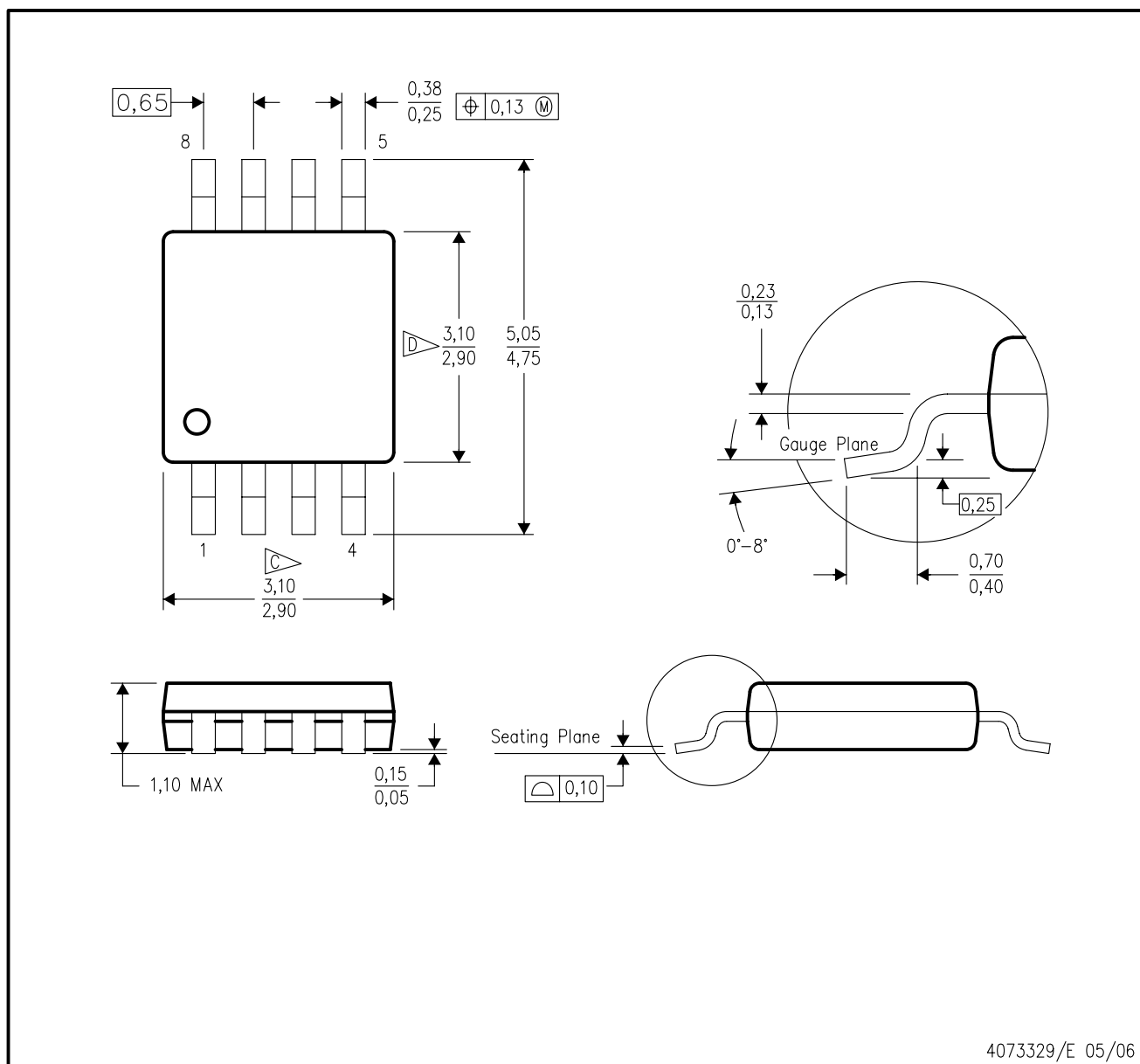
SMALL PACKAGE OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances and vias tenting recommendations for vias placed in the thermal pad.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

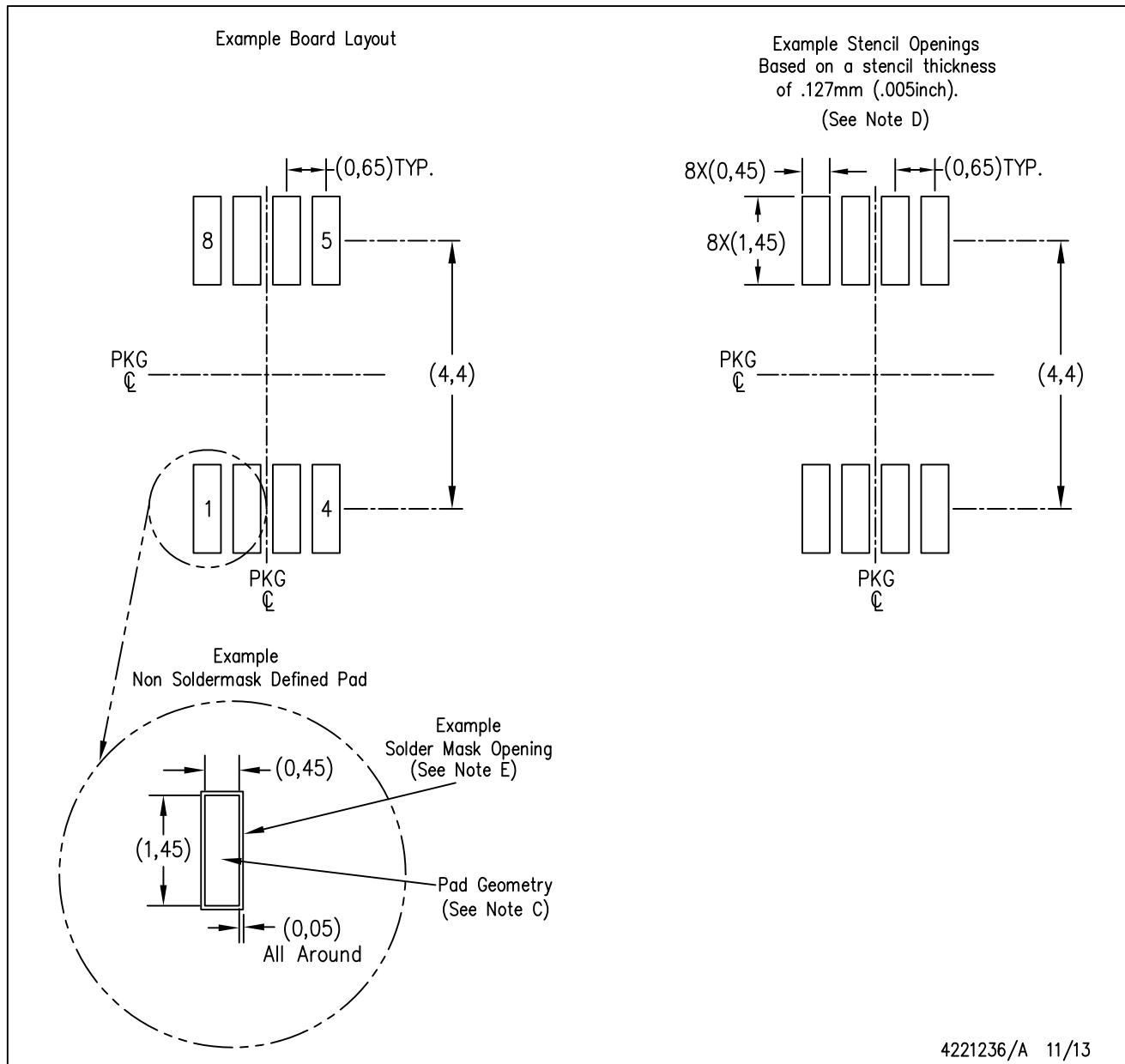


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D GK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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