MP1906

80V, Half-Bridge, Gate Driver

The Future of Analog IC Technology

DESCRIPTION

The MP1906 is a high-performance, 80V, gate driver that can drive two external N-MOSFETs in a half-bridge configuration with a 12V gate supply. It accepts independent gate input signals and provides shoot-through prevention. During under-voltage lockout, the output of the high- and low-side drivers goes low to prevent erratic operation under low supply conditions.

The high-current driving capability and short dead time make it suitable for high-power and high-efficiency power applications, such as telecom DC-DC converters. The compact 8-pin SOIC package minimizes the component count and the board space.

FEATURES

- Drives Two Low-Cost, High-Efficiency N-MOSFETs
- 10V-16V Gate Drive Supply
- 3.3V, 5V Logic Compatibility
- 80ns Propagation Delay
- Less than 90μA Quiescent Current
- Under-Voltage Lockout for Both Channels
- Input-Signal-Overlap Protection
- Internal 150ns Dead Time
- Available in a Compact 8-pin SOIC Package

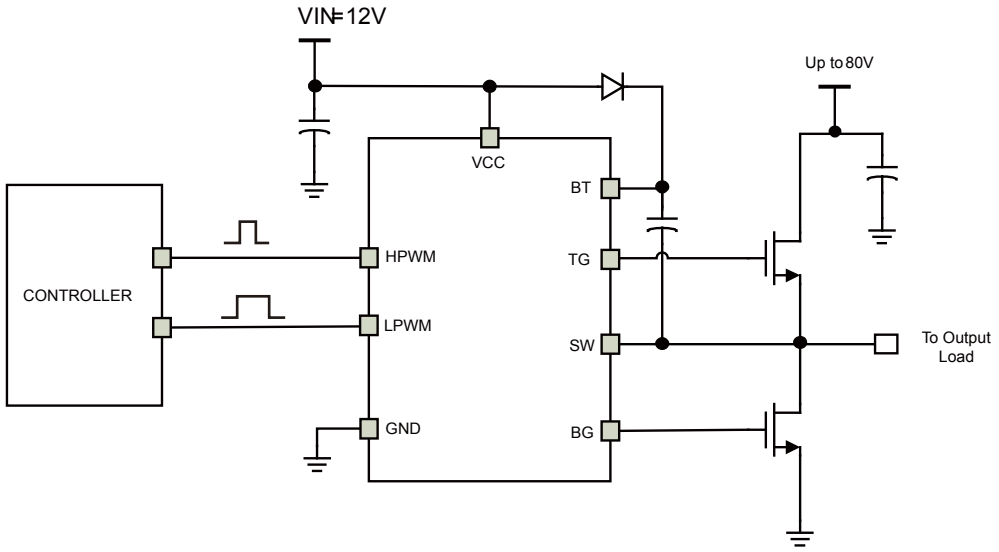
APPLICATIONS

- Motor Drivers
- Half-Bridge Power Supplies
- Avionics DC-DC Converters
- Active-Clamp Forward Converters

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TYPICAL APPLICATION



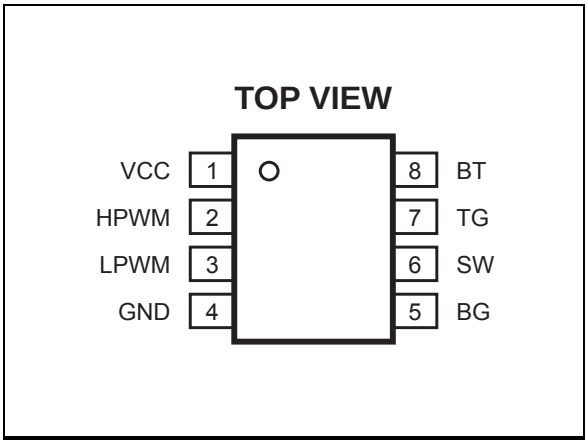
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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP1906DS	SOIC8	MP1906

*For Tape & Reel, add suffix –Z (e.g. MP1906DS–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP1906DS–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage V_{CC} .....-0.3V to +18V
Voltage on SW V_{SW} .....
-0.3V (-5V < 10ns) to +100V
Voltage on BT V_{BT} ..... V_{SW} +18V
Logic Inputs .....
-0.3 to (V_{CC}+6.5V), or 18.5V for V_{CC} ⩾ 12V
Continuous Power Dissipation (T_A = 25°C) (2)
.....1.4W
Junction Temperature ..... -40°C to +150°C
Lead Temperature (Solder 10sec) .....260°C
Storage Temperature ..... -55°C to +150°C

Recommended Operating Conditions (3)

Input Voltage V_{CC} .....10V to 16V
Maximum Voltage on SW V_{SW} 80V
Logic Inputs .....0V to V_{CC}
Voltage slew rate on SW..... < 50V/ns
PWM frequency ..... < 300kHz
Operating Junction Temp. (T_J) . -40°C to 125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC8 ..... 90 ..... 45... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, V_{SW}=0V, no load on TG or BG, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
V_{CC} quiescent current	I_{CCQ}	V_{LPWM}=5V, V_{HPWM}= 0V	70	90	110	μA
V_{CC} operation current	I_{CC}	f=50kHz, $C_{LOAD\ BG}$=1nF		0.9	1.5	mA
Bootstrap quiescent current	I_{BTQ}	V_{LPWM}=5V, V_{HPWM}= 0V		30		μA
Bootstrap operation current	I_{BT}	f=50kHz, $C_{LOAD\ TG}$=1nF		0.7	1	mA
SW BT leakage current	I_{LK}	V_{SW}=V_{BT}=80V		0.1	0.5	μA
Input						
LPWM falling threshold	V_{LPWMF}				0.8	V
LPWM rising threshold	V_{LPWMR}		2.5			V
HPWM falling threshold	V_{HPWMF}				0.8	V
HPWM rising threshold	V_{HPWMR}		2.5			V
Under-Voltage Protection (UVLO)						
V_{CC} rising threshold	V_{CCTHR}		8.2	8.8	9.4	V
V_{CC} threshold hysteresis	V_{CCTHH}			0.7		V
Bootstrap rising threshold	V_{BTTHR}		4.5	5.5	6.5	V
Bootstrap threshold hysteresis	V_{BTTHH}			0.65		V
Gate Driver Output						
Low-side gate pull-up peak current (5)	I_{BGU}	V_{BG}=0V		350		mA
Low-side gate pull-down peak current (5)	I_{BGD}	V_{BG}=12V		1		A
High-side gate pull-up peak current (5)	I_{TGU}	V_{TG}=0V		350		mA
High-side gate pull-down peak current (5)	I_{TGD}	V_{TG}=12V		1		A
Propagation Delays, Dead Times and Output Rising and Falling Times (C_{Load}=1nF cap) (please see timing diagram)						
Turn-on propagation delay (TG)	$\tau_{ON\ TG}$	V_{SW}=0V		80	150	ns
Turn-off propagation delay (TG)	$\tau_{OFF\ TG}$	V_{SW}=0V		80	150	ns
Turn-on rise time (TG)	$\tau_{RISE\ TG}$			50	100	ns
Turn-off fall time (TG)	$\tau_{FALL\ TG}$			30	100	ns
Turn-on propagation delay (BG)	$\tau_{ON\ BG}$			80	150	ns
Turn-off propagation delay (BG)	$\tau_{OFF\ BG}$			80	150	ns
Turn-on rise time (BG)	τ_{RISE_BG}			50	100	ns
Turn-off fall time (BG)	τ_{FALL_BG}			30	100	ns
Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	τ_{DT}			150	250	ns

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ELECTRICAL CHARACTERISTICS(CONTIUUED)

V_{CC} = 12V, V_{SW}=0V, no load on TG or BG, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LPWM source current	I_{LPWM}	I_{LPWM}=5V	-8	-3	-1	μA
HPWM sink current	I_{HPWM}	I_{HPWM}=5V	1	3	8	μA
Floating Gate Driver						
BG-output-low to GND	V_{BGL}	I_{BG}=100mA		0.4	0.7	V
BG-output-high to rail	V_{BGH}	I_{BG}=-100mA, V_{BGH}=V_{CC}-V_{BG}		1.5	1.7	V
TG-output-low to SW	V_{TGL}	I_{TG}=100mA		0.4	0.7	V
TG-output-high to rail	V_{TGH}	I_{TG}=-100mA, V_{TGH}=V_{CC}-V_{TG}		1.5	1.7	V
Switching Specifications						
Minimum input pulse width to change the output(5)	τ_{PWM_min}				50	ns

Notes:

5) Guaranteed by design

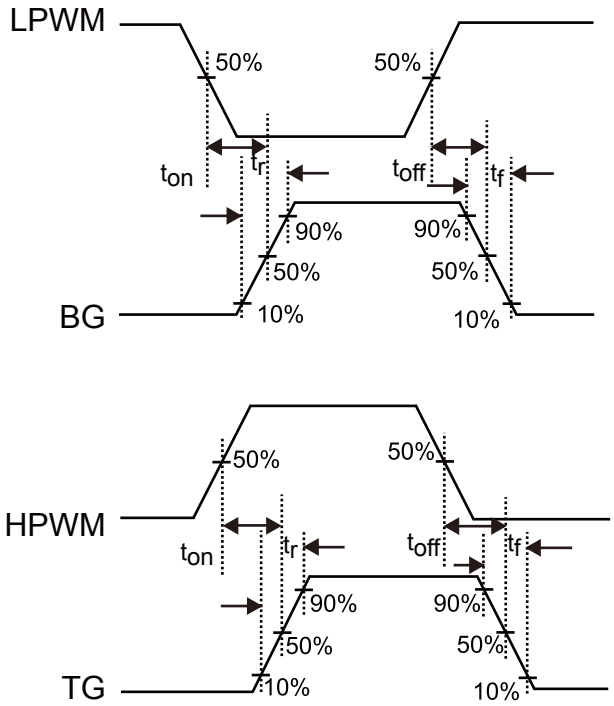


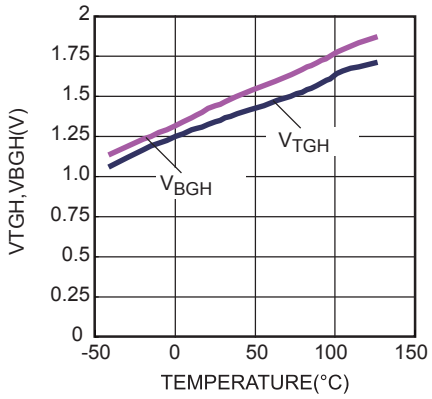
Figure 1: Gate Driver Timing Diagram

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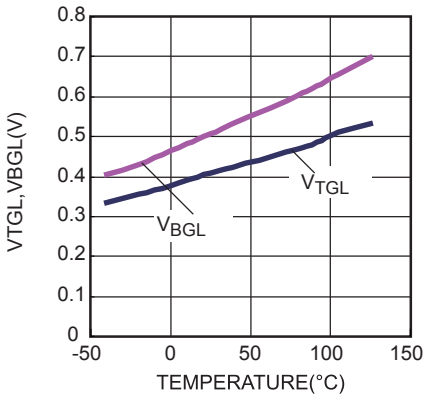
TYPICAL CHARACTERISTICS

V_{DD}=12V, V_{SW}=0V, T_A=+25°C, unless otherwise noted.

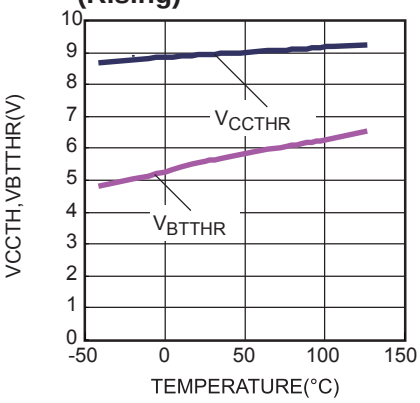
High Level Output Voltage vs. Temperature



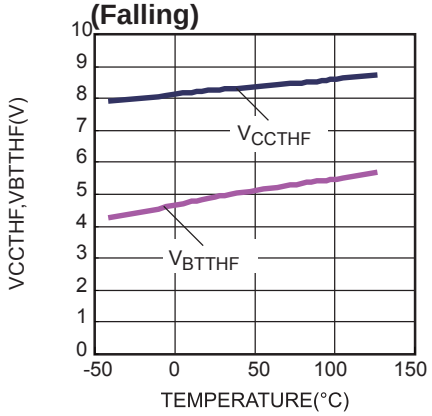
Low Level Output Voltage vs. Temperature



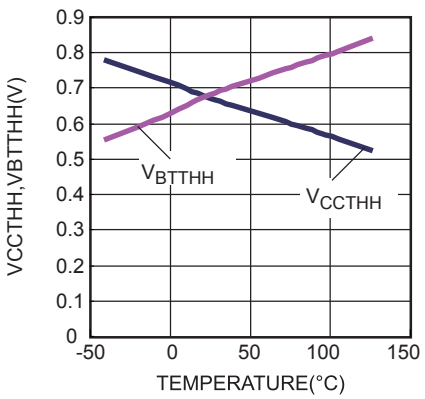
Undervoltage Lockout Threshold vs. Temperature (Rising)



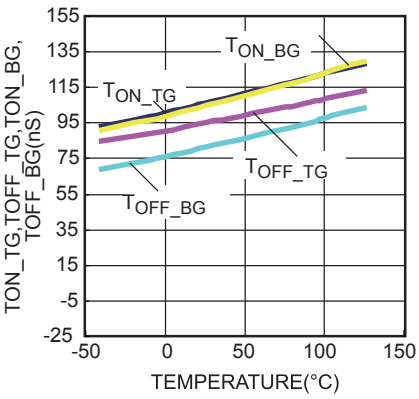
Undervoltage Lockout Threshold vs. Temperature (Falling)



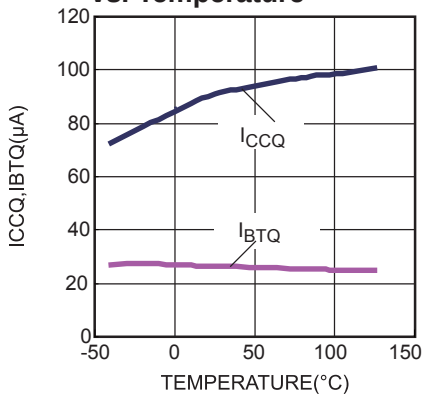
Undervoltage Lockout Hysteresis vs. Temperature



Propagation Delay vs. Temperature



Quiescent Current vs. Temperature

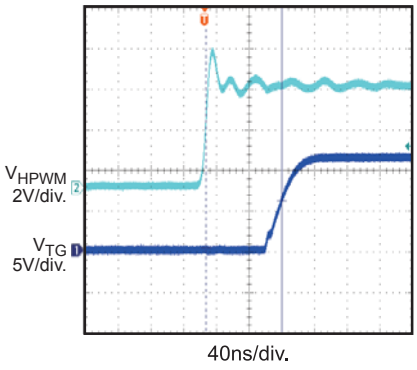


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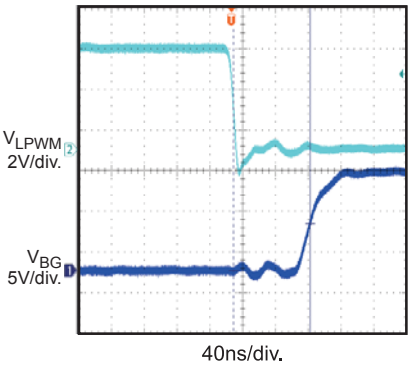
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 12V, V_{SW}=0V, 1nF load on TG and BG, T_A = 25°C, unless otherwise noted.

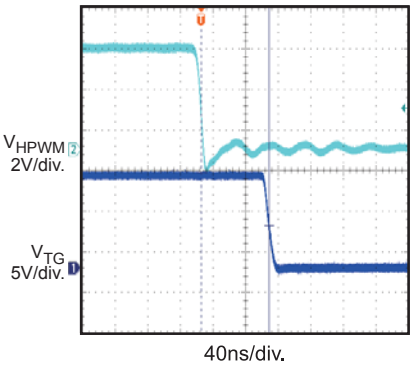
Turn-on Propagation Delay



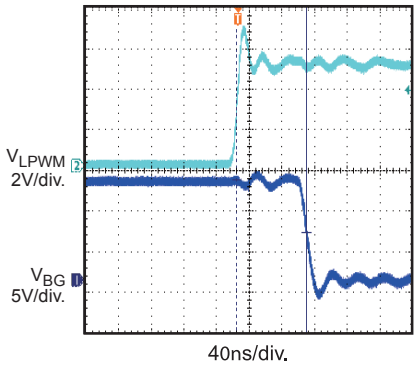
Turn-on Propagation Delay



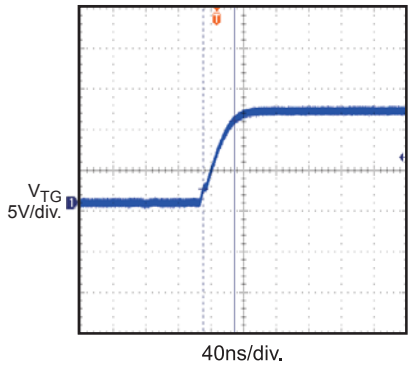
Turn-off Propagation Delay



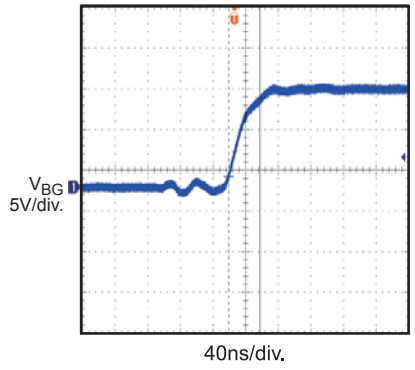
Turn-off Propagation Delay



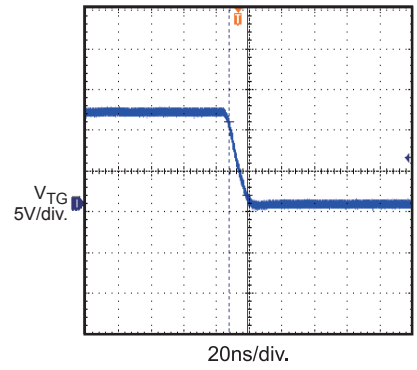
Drive Rise Time(1nF Load)



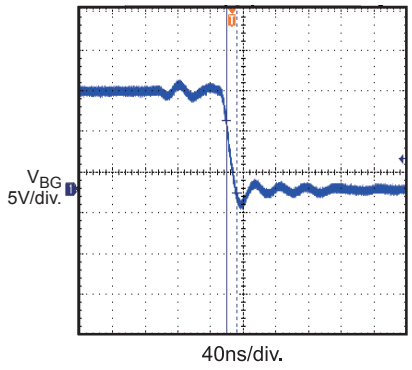
Drive Rise Time(1nF Load)



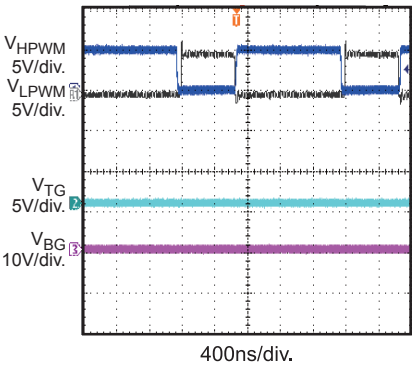
Drive Fall Time(1nF Load)



Drive Fall Time(1nF Load)



Input Signal Overlap Protection



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PIN FUNCTIONS

Pin #	Name	Description
1	VCC	Supply Input. Supplies power to all internal circuitry. Requires a decoupling capacitor to ground placed close to this pin to ensure a stable and clean supply.
2	HPWM	Logic input for high-side gate driver output.
3	LPWM	Logic input for low-side gate driver output. Active low.
4	GND	Ground.
5	BG	Gate Driver Output for low-side MOSFET.
6	SW	Source Return for high-side MOSFET.
7	TG	Gate Driver Output for high-side MOSFET.
8	BT	Bootstrap. Internal power supply pin for high-side floating driver. Add a 1μF ceramic bootstrap capacitor from BT to SW pin.

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FUNCTIONAL BLOCK DIAGRAM

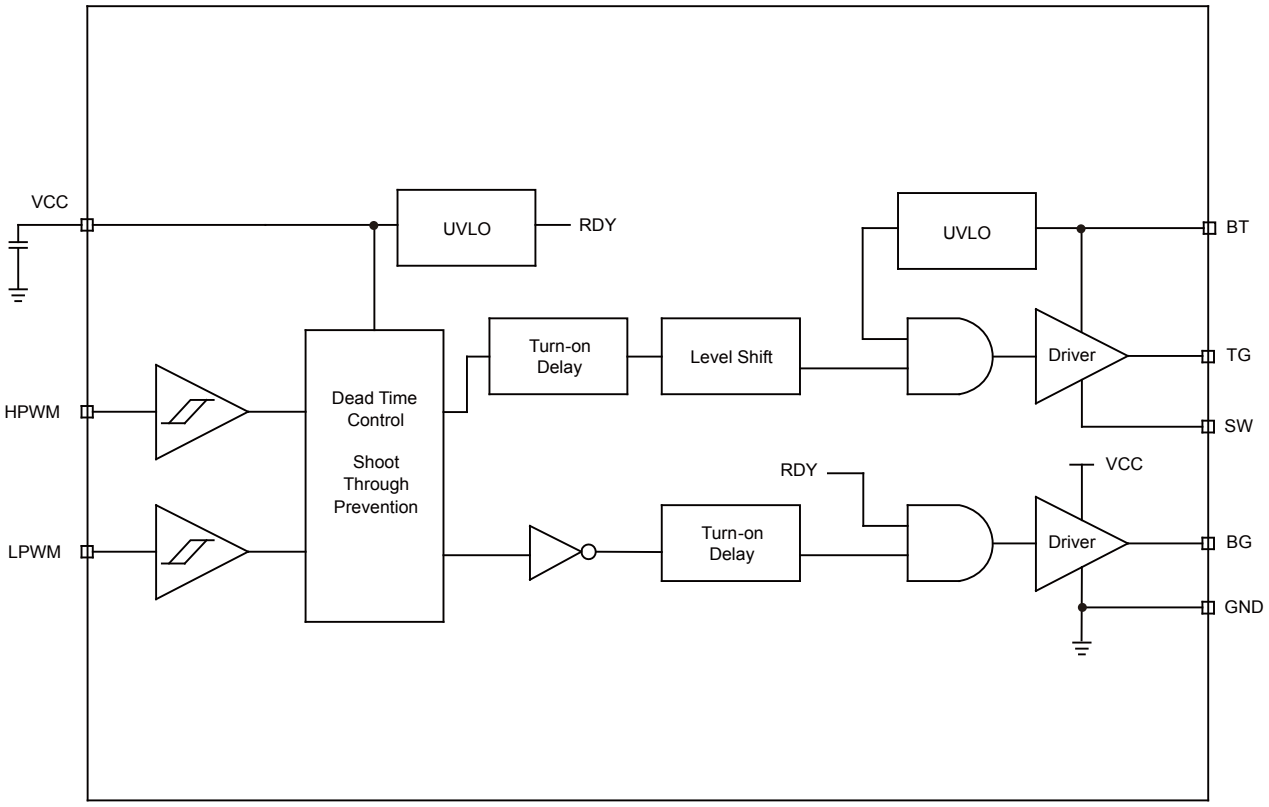


Figure 2: Functional Block Diagram

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OPERATION

Switch Shoot-through Protection

The input signals of HPWM and LPWM are independently controlled. Input shoot-through protection circuitry prevents shoot-through between the TG and BG outputs. Only one of the FET drivers can be on at one time. If HPWM is high and LPWM is low, both TG and BG are OFF.

Under Voltage Lockout

When V_{CC} or V_{BT} goes below their respective UVLO threshold, both BG and TG outputs will go low to both FETS. Once V_{CC} and V_{BT} rises above the UVLO threshold, both TG and BG will stay low until there is a rising edge on either HPWM or LPWM.

Figure 3 shows the operation of the TG and BG under different HPWM and LPWM and UVLO conditions.

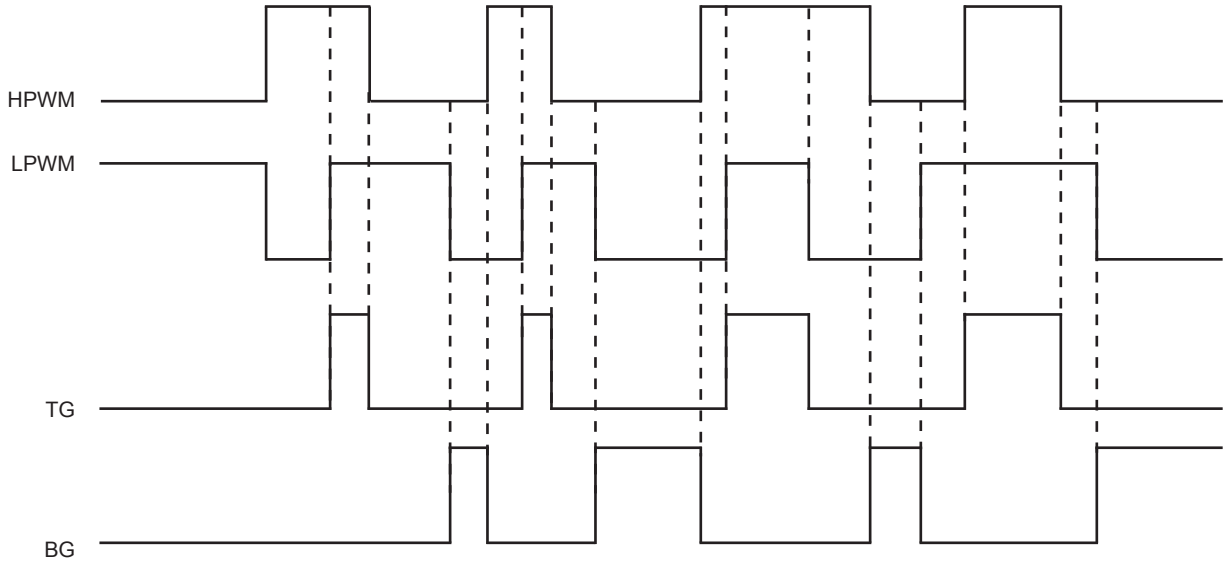


Figure 3: Input/Output Timing Diagram

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APPLICATION INFORMATION

Reference Design Circuits

Half Bridge Motor Driver

In a half-bridge converter topology, the MOSFET-driving signals have a dead time: HPWM and LPWM driven with alternating signals from the PWM controller. The input voltage can be up to 80V in this application.

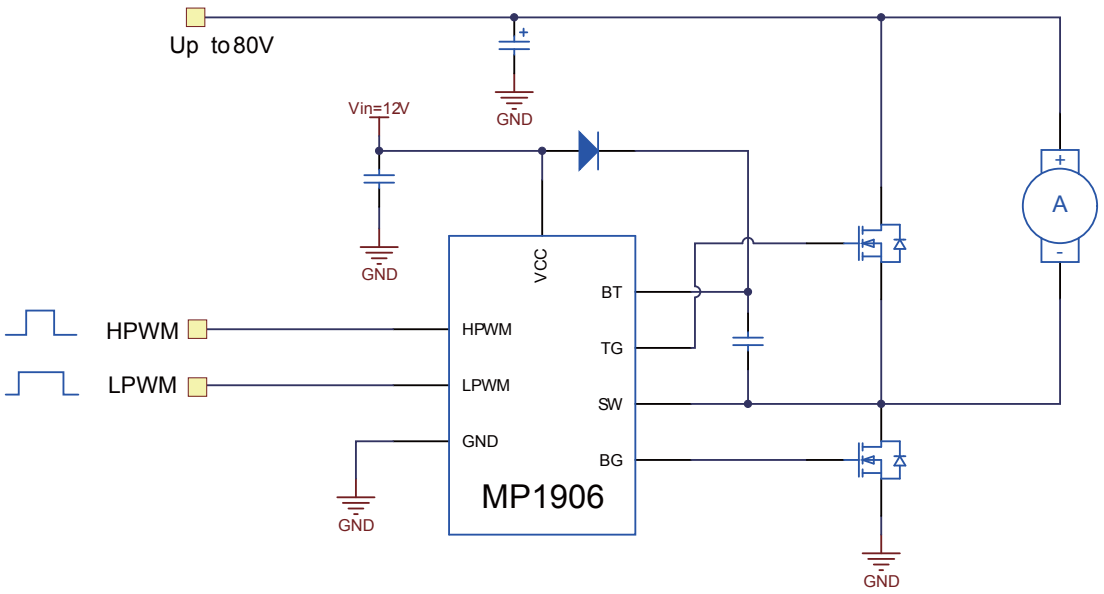


Figure 4: Half-Bridge Motor Driver

Active-Clamp-Forward Converter

An active-clamp-forward-converter topology alternately drives the MOSFETs. The high-side MOSFET and the capacitor, C_{RESET}, reset the power transformer in a lossless manner. This topology runs well at duty cycles exceeding 50%. However, the input voltage may not run at 80V.

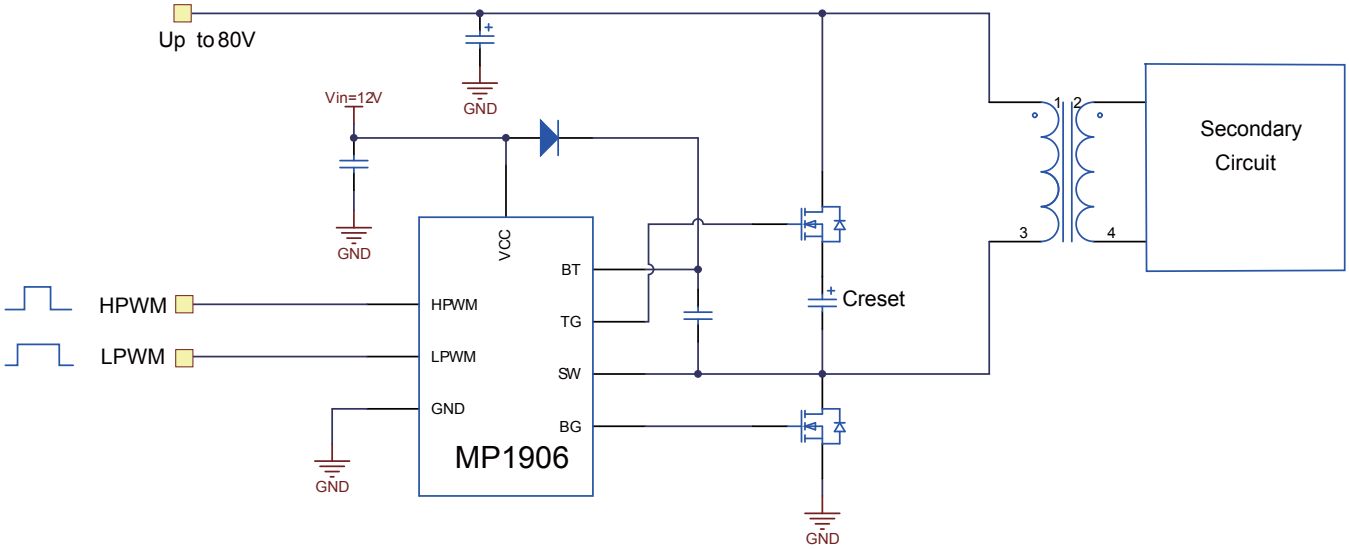
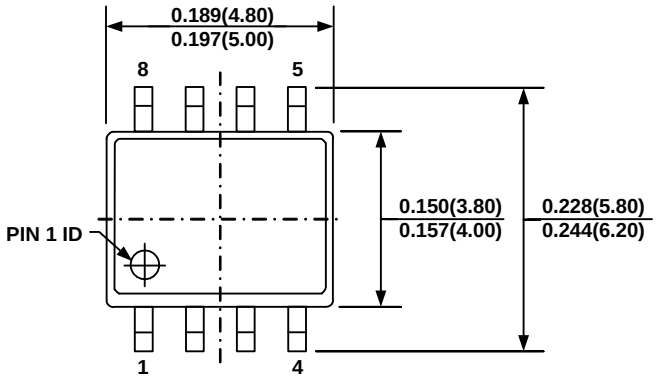


Figure 5: Active-Clamp Forward Converter

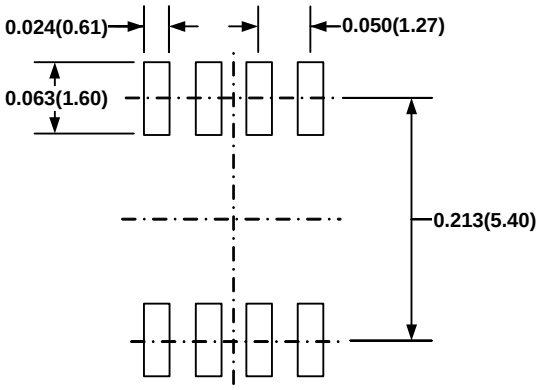
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PACKAGE INFORMATION

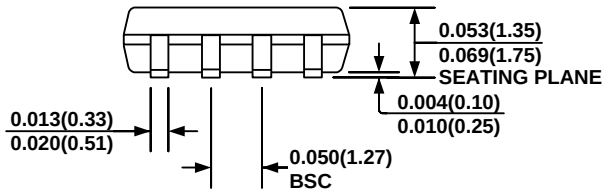
SOIC8



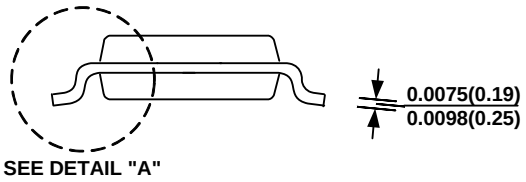
TOP VIEW



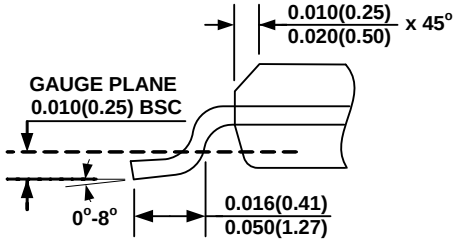
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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