SYNCHRONOUS BUCK CONTROLLER WITH HIGH-CURRENT GATE DRIVER

Check for Samples :TPS51113 TPS51163

FEATURES

- **Flexible Power Rails: 5 V to 12 V**
- **Reference: 800 mV ± 0.8%**
- **Voltage Mode Control**
- **Support Pre-biased Startup**
- **Programmable Overcurrent Protection with Low-Side $R_{DS(on)}$ Current Sensing**
- **Fixed 300-kHz (TPS51113) and 600-kHz (TPS51163) Switching Frequency**
- **UV/OV Protections and Power Good Indicator**
- **Internal Soft-start**
- **Integrated High-Current Drivers Powered by VDD**
- **10-Pin 3 × 3 SON Package**

APPLICATIONS

- **Server and Desktop Computer Subsystem Power Supplies (MCH, IOCH, PCI, Termination)**
- **Distributed Power Supplies**
- **General DC-DC Converters**

DESCRIPTION

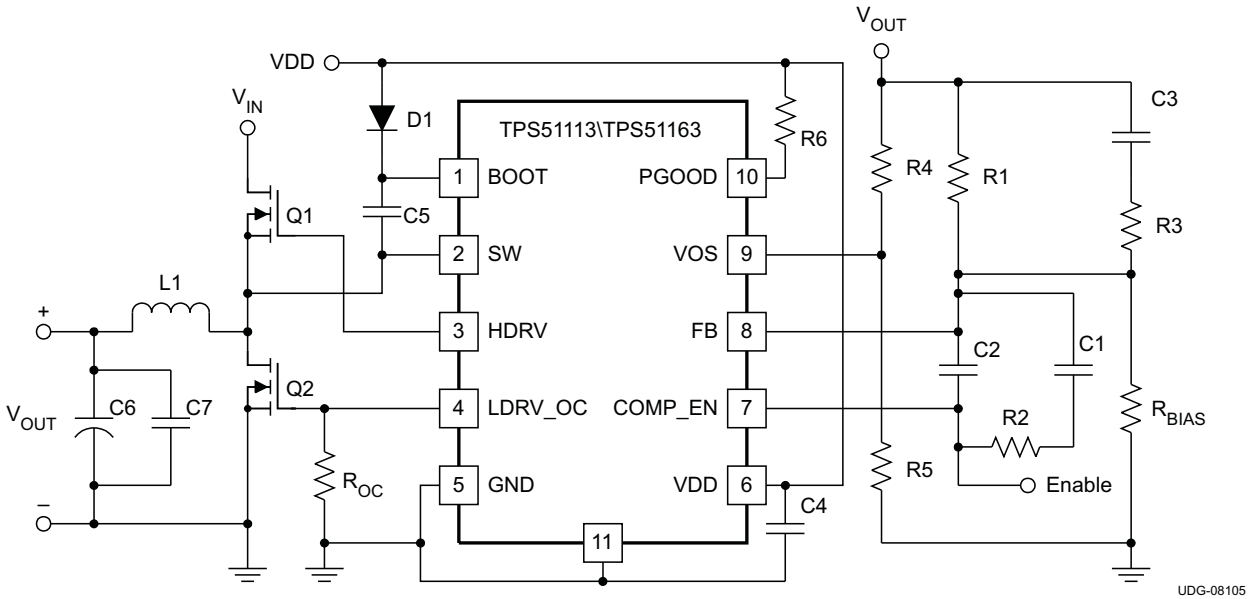
The TPS51113 and TPS51163 are cost-optimized, feature rich, single-channel synchronous-buck controllers that operates from a single 4.5-V to 13.2-V supply and can convert an input voltage as low as 1.5 V.

The controller implements voltage mode control with a fixed 300-kHz (TPS51113) and 600-kHz (TPS51163) switching frequency. The overcurrent (OC) protection employs the low-side $R_{DS(on)}$ current sensing and has user-programmable threshold. The OC threshold is set by the resistor from LDRV_OC pin to GND. The resistor value is read when the over-current programming circuit applies 10 µA of current to the LDRV_OC pin during the calibration phase of the start-up sequence.

The TPS51113/TPS51163 also supports output pre-biased startup.

The integrated gate driver is directly powered by VDD. VDD can be connected to V_{IN} in some applications. The strong gate drivers with low deadtime allow for the utilization of larger MOSFETs to achieve higher efficiency. An adaptive anti-cross conduction scheme is used to prevent shoot-through between the power FETs.

TYPICAL APPLICATION CIRCUIT



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Table 1. ORDERING INFORMATION(1)

ORDERABLE DEVICE	TYPE	DRAWING	PINS	QTY	ECO PLAN	LEAD/BALL FINISH	MSL PEAK TEMPERATURE
TPS51113DRCR	SON	DRC	10	3000	Green (RoHS and no Sb/Br)	CU NiPDAU	Level-2-260C-1Year
TPS51163DRCR							
TPS51113DRCT	SON	DRC	10	250	Green (RoHS and no Sb/Br)	CU NiPDAU	Level-2-260C-1Year
TPS51163DRCT							

(1) For the most current package and ordering information see the *Package Option Addendum* at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1) (2)

Over operating free-air temperature range (unless otherwise noted, all voltages are with respect to GND.)

PARAMETER		VALUE	UNIT
Input voltage range	VDD	–0.3 to 15	V
	BOOT	–0.3 to 30	
	BOOT, to SW (negative overshoot –5 V for t < 25 ns, 125 V × ns/t for 25 ns < t< 100 ns)	–5.0 to 15	
	BOOT, (negative overshoot –5 V for t < 25ns, 125 V × ns/t for 25 ns < t < 100 ns)	–5.0 to 37	
	All other pins	–0.3 to 3.6	
Output voltage range	SW	–0.3 to 22	V
	SW, (negative overshoot –5 V for t < 25ns, 125 V × ns/t for 25 ns < t < 100 ns)	–5.0 to 30	
	HDRV	–0.3 to 30	
	HDRV to SW (negative overshoot –5 V for t < 25 ns, 125 V × ns/t for 25 ns < t< 100 ns)	–5.0 to 15	
	HDRV (negative overshoot –5 V for t < 25ns, 125 V × ns/t for 25 ns < t < 100 ns)	–5.0 to 37	
	LDRV_OC	–0.3 to 15	
	LDRV_OC (negative overshoot –5 V for t < 25ns, 125 V × ns/t for 25 ns < t < 100 ns)	–5.0 to 15	
	PGOOD	–0.3 to 15	
	All other pins	–0.3 to 3.6	
T_J Operating junction temperature		–40 to 125	°C
T_{stg} Storage junction temperature		–55 to 150	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	TYP	MAX	UNIT
Human Body Model (HBM)			2500	V
Charged Device Model (CDM)			1500	

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PACKAGE DISSIPATION RATINGS

PACKAGE	AIRFLOW (LFM)	$R_{\theta JA}$ HIGH-K BOARD (1) (°C/W)	POWER RATING (W) T_A = 25°C	POWER RATING (W) T_A = 85°C
DRC	0 (natural convection)	47.9	2.08	0.835
	200	40.5	2.46	0.987
	400	38.2	2.61	1.04

(1) Ratings based on JEDEC High Thermal Conductivity (High K) Board. For more information on the test method, see TI Technical Brief (SZZA017).

RECOMMENDED OPERATING CONDITIONS

(unless otherwise noted, all voltages are with respect to GND)

		MIN	TYP	MAX	UNIT
Supply voltages	VDD	–0.1		13.2	V
	BOOT	–0.1		28.0	
	BOOT, to SW (negative overshoot –5 V for t < 25 ns, 125 V × ns/t for 25 ns < t< 100 ns)	–3.0		13.2	
	BOOT, (negative overshoot –5 V for t < 25 ns, 125 V × ns/t for 25 ns < t < 100 ns)	–3.0		35.0	
	All other pins	–0.1		3.0	
Output voltages	SW	–0.1		20.0	V
	SW, (negative overshoot –5 V for t < 25 ns, 125 V × ns/t for 25 ns < t < 100 ns)	–3.0		28.0	
	HDRV	–0.1		28.0	
	HDRV to SW (negative overshoot –5 V for t < 25 ns, 125 V × ns/t for 25 ns < t< 100 ns)	–3.0		13.2	
	HDRV (negative overshoot –5 V for t < 25 ns, 125 V × ns/t for 25 ns < t < 100 ns)	–3.0		35.0	
	LDRV_OC	–0.1		13.2	
	LDRV_OC (negative overshoot –5 V for t < 25 ns, 125 V × ns/t for 25 ns < t < 100 ns)	–3.0		13.2	
	PGOOD	–0.1		13.2	
	All other pins	–0.1		3.0	
T_A Operating ambient temperature		–40		85	°C

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ELECTRICAL CHARACTERISTICS

These specifications apply for -40°C ≤ T_A ≤ to 85°C, V_{VDD} = 12 Vdc. (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY							
V_{VDD}				4.5		13.2	V
I_{VDD}	Supply current		Switching enabled(1)			30	mA
	Shutdown current		Switching inhibited			6	mA
VDD UVLO							
UVLO	VDD UVLO		VDD raising	4.0	4.3	4.6	V
$UVLO_{HYS}$	UVLO threshold hysteresis				250		mV
REFERENCE							
V_{REF}	Reference voltage		0°C ≤ T_A ≤ 85°C	794	800	806	mV
	Reference voltage		–40°C ≤ T_A ≤ 85°C	792	800	808	mV
OSCILLATOR							
f_{SW}	Switching frequency	TPS51113	Measured on the SW pin, T_A = 25°C	270	300	330	kHz
		TPS51163		540	600	660	
V_{RAMP}	PWM ramp amplitude(1)				1.5		V
PWM							
D_{MAX}	Maximum duty cycle	TPS51113		72%			
		TPS51163		69%			
TON_{MIN}	Minimum controlled pulse(1)					100	ns
T_{NO}	Output driver dead time				30		ns
SOFT START							
T_{SSD}	Soft-start delay time			4.0	5.5	7.0	ms
T_{SS}	Soft-start time			2.0	3.5	5.0	ms
ERROR AMPLIFIER							
GBWP	Gain bandwidth product(1)		C_{COMP} < 20 pF		16		MHz
AoI	DC gain(1)			89			dB
I_{IB}	Input bias current			–100			nA
EA_{SR}	Error amplifier output slew rate(1)		C_{COMP} < 20 pF	6			V/µs
$V_{COMPDIS}$	COMP_EN pin disabling voltage				0.8		V
SHORT CIRCUIT PROTECTION							
I_{ILIM}	Overcurrent threshold set current			9.3	10.0	10.7	µA
GATE DRIVERS							
I_{HDHI}	High-side driver pull-up current(1)		BOOT to HDRV voltage is 5 V		1.5		A
R_{HDLO}	High-side driver pull-down resistance		V_{VDD} = 12 V; I_{DRV} = –100 mA		1.4		Ω
I_{LDHI}	Low-side driver pull-up current(1)		VDD to LDRV voltage is 5 V		1.5		A
R_{LDLO}	Low-side driver pull-down resistance		V_{VDD} = 12 V		0.8		Ω

(1) Ensured by design. Not production tested.

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ELECTRICAL CHARACTERISTICS (continued)

These specifications apply for -40°C ≤ T_A ≤ to 85°C, V_{VDD} = 12 Vdc. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD						
V_{PGLR}	Lower powergood threshold	VOS voltage rising	0.728	0.752	0.776	V
V_{PGLF}	Lower powergood threshold	VOS voltage falling	0.696	0.720	0.744	V
V_{PGUR}	Upper powergood threshold	VOS voltage rising	0.856	0.880	0.904	V
V_{PGUF}	Upper powergood threshold	VOS voltage falling	0.824	0.848	0.872	V
V_{PG}	PGOOD pin voltage	I_{PDG} = 4 mA			0.4	V
I_{PGDLK}	Leakage current	V_{PGOOD} = 5 V			20	µA
UV/OV PROTECTION						
V_{UVP}	UVP threshold	VOS voltage falling	0.576	0.600	0.624	V
V_{OVP}	OVP threshold	VOS voltage rising	0.96	1.00	1.04	V
V_{OVPL}	OVP latch threshold	VOS voltage falling	0.376	0.400	0.424	V
I_{OS}	VOS input bias current		–100		100	nA

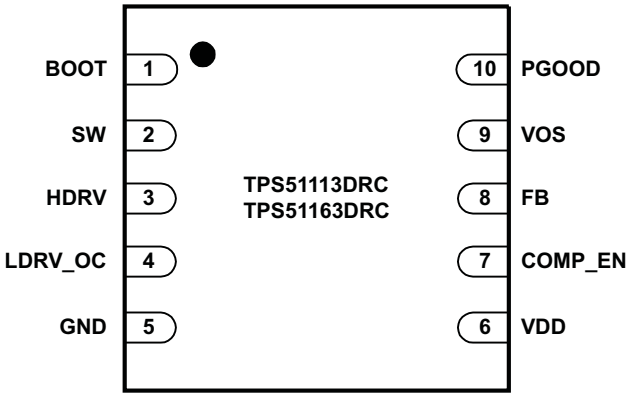
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TERMINAL INFORMATION

TERMINAL FUNCTIONS

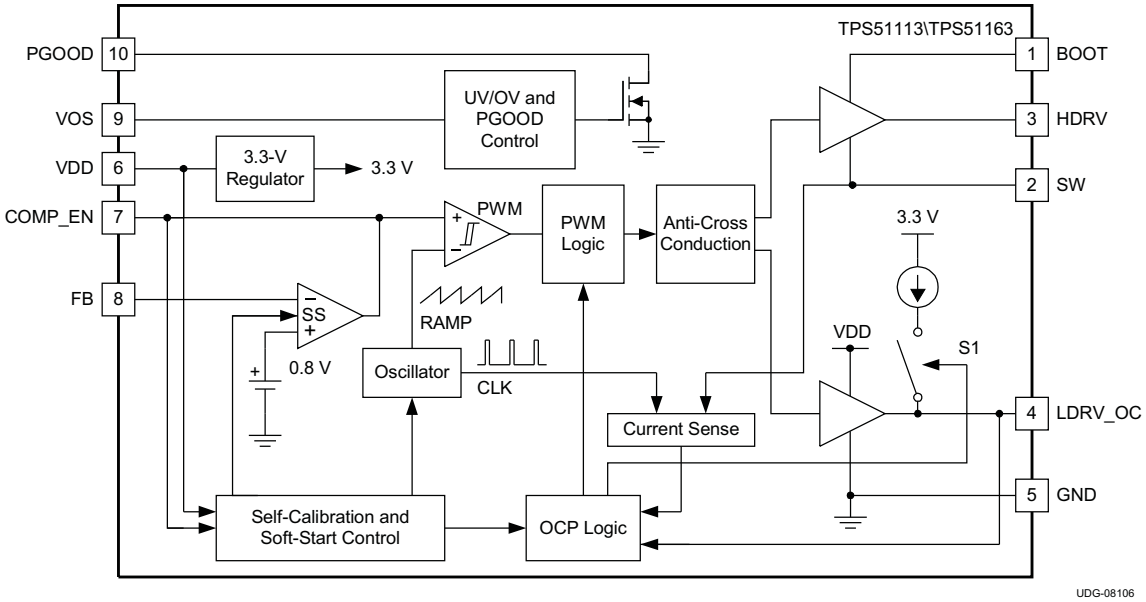
TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
BOOT	1	I	Gate drive voltage for the high-side N-channel MOSFET. Typically, a 100 nF capacitor must be connected between this pin and SW. Also, a diode from VDD to BOOT should be externally provided.
COMP_EN	7	I/O	Output of the error amplifier and the shutdown pin. Pulling the voltage on this pin lower than 800 mV shuts the controller down.
FB	8	I	Inverting input to the error amplifier. In normal operation, the voltage on this pin is equal to the internal reference voltage of 800 mV.
GND	5	–	Common reference for the device.
HDRV	3	O	Gate drive output for the high-side N-channel MOSFET.
LDRV_OC	4	O	Gate drive output for the low-side or rectifier MOSFET. The set point is read during start up calibration with the 10 µA current source present.
PGOOD	10	O	Open drain power good output. An external pull-up resistor is required.
SW	2	O	Sense line for the adaptive anti-cross conduction circuitry. Serves as common connection for the flying high-side FET driver.
VDD	6	I	Power input to the controller, 4.5 V to 13.2 V.
VOS	9	I	Input to set undervoltage and overvoltage protections. Undervoltage protection occurs when VOS voltage is lower than 600 mV. The controller shuts down with both MOSFETs latched off. Overvoltage protection occurs when VOS voltage is higher than 1V, the upper MOSFET is turned off and the lower MOSFET is forced on until VOS voltage reaches 400 mV. Then the lower MOSFET is also turned off. After the undervoltage or overvoltage events, normal operation can be restored only by cycling the VDD voltage.

SON PACKAGE
(TOP VIEW)



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FUNCTIONAL BLOCK DIAGRAM



PERFORMANCE DATA

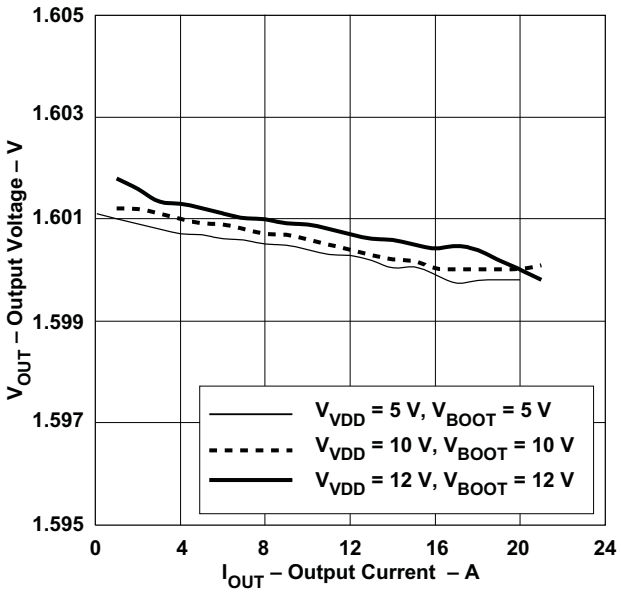


Figure 1. Load Regulation

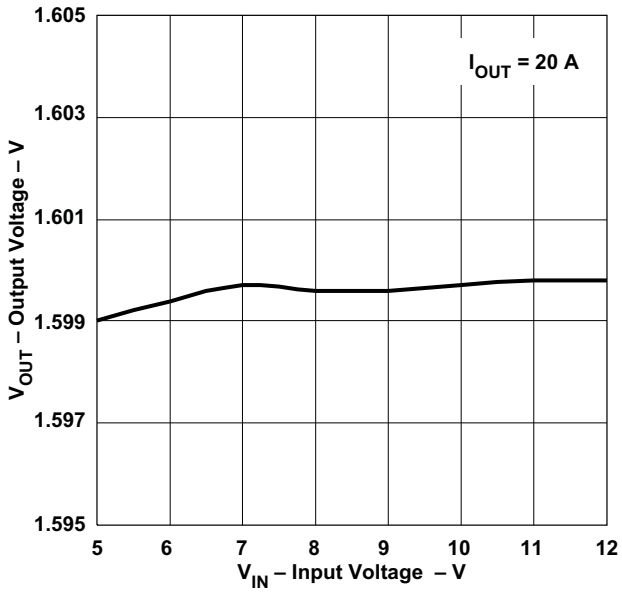


Figure 2. Line Regulation

PERFORMANCE DATA (continued)

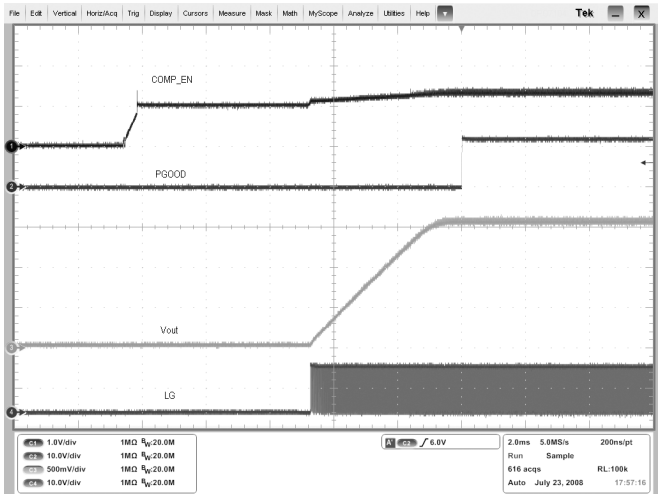


Figure 3. Startup Waveform at V_{IN} = 5 V, V_{OUT} = 1.6 V, I_{OUT} = 0 A

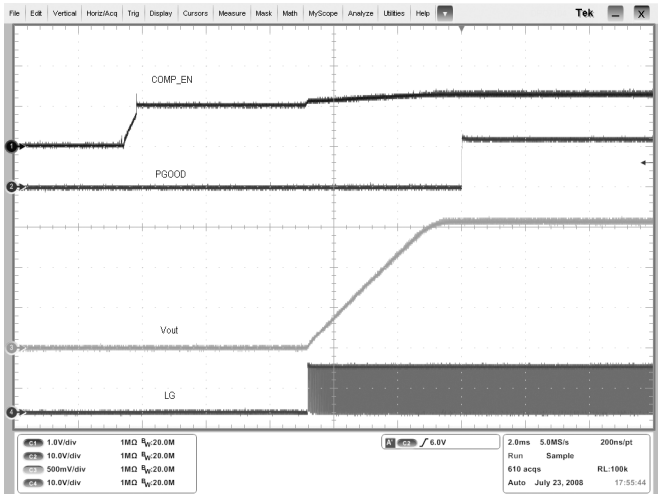


Figure 4. Startup Waveform at V_{IN}= 12 V, V_{OUT}= 1.6 V, I_{OUT}=0 A

CH1: COMP_EN
CH2: PGOOD
CH3: VOUT
CH4: LDRV

CH1: COMP_EN
CH2: PGOOD
CH3: VOUT
CH4: LDRV

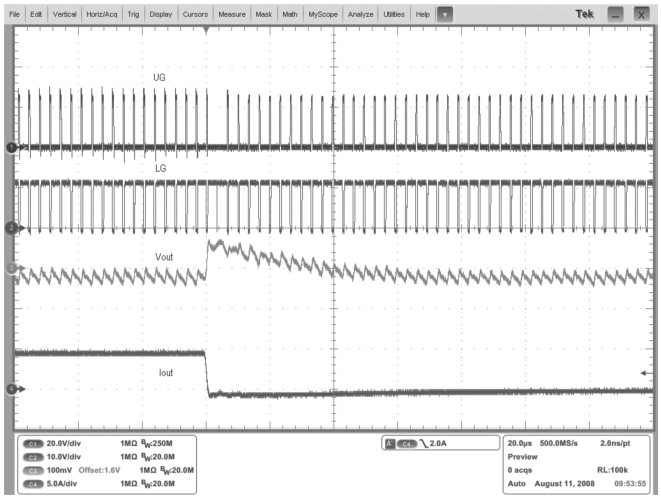


Figure 5. Load Step 0 A to 5 A

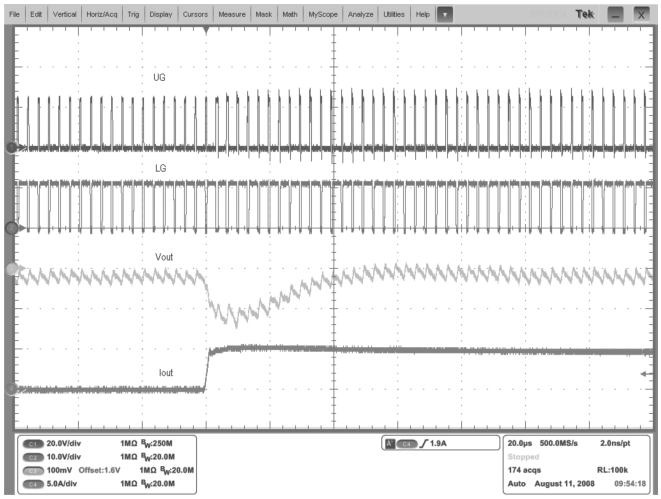


Figure 6. Load Step 5 A to 0 A

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DETAILED DESCRIPTION

TPS51113 and TPS51163 are cost-optimized, single channel synchronous buck controllers that operate at a 300-kHz (TPS51113) and 600-kHz (TPS51163) fixed switching frequency, from a single 4.5-V to 13.2-V supply, and supports output pre-biased startup. The overcurrent protection uses the low-side $R_{DS(on)}$ current sensing for a low-cost, loss-less solution. Other features include input undervoltage lockout (UVLO), programmable overcurrent threshold, soft-start, output oververvoltage/undervoltage (OV/UV) protection. The integrated gate driver is powered directly by VDD. This makes the gate drive voltage more flexible.

SOFT START AND SELF-CALIBRATION

When VDD is above 4.3 V and the COMP_EN pin is released from being pulled low with open-drain system logic, the controller enters the start-up sequence. There is a two stage start-up sequence for the COMP_EN voltage. In the first phase of start-up (t_{SS_delay}), the controller completes self-calibration and inhibits FET switching, leaving both the upper and lower MOSFETs in the off state. In the second phase of start-up (t_{SS}), soft-start begins and switching is enabled. The internal reference gradually rises to 800 mV, and the output voltage gets within its regulation point. The soft-start time (t_{SS}) is internally programmed at 3.5 ms, and t_{SS_Delay} is programmed at 5.5 ms. On average, it takes approximately 9 ms for the output voltage to come into regulation after the COMP_EN pin is released.

Figure 7 shows the typical startup and shutdown sequence. The overcurrent protection is enabled when the soft-start begins and the soft-start voltage exceeds the pre-biased VOS voltage. The output overvoltage protection is enabled approximately 64 clock cycles after the COMP pin voltage rises above 0.8 V (thereby enabling the device). When the soft-start ends, the output undervoltage protection is enabled, and PGOOD signal also goes high at the same time.

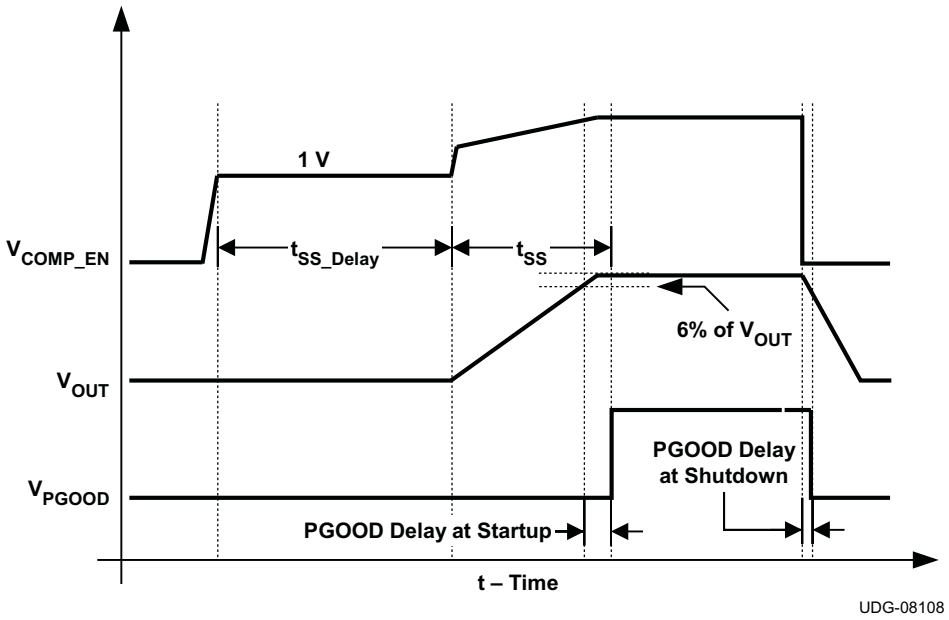


Figure 7. Typical Startup and Shutdown Sequence

OVERCURRENT PROTECTION

Overcurrent detection is done by comparing a user programmable threshold with the voltage drop across the low-side FET at the end of the switching period (The low-side FET is on). The OC threshold is set with a single external resistor connected from the LDRV_OC pin to GND.

The overcurrent programming circuit applies 10-µA of current to the LDRV_OC pin during the calibration phase of the start-up sequence. Voltage drop on the LDRV_OC pin is measured and digitized, and the related code is stored in the internal latch. This code determines a reference level for the overcurrent comparator. The value of the OC set resistor R_{OCSET} can be determined in Equation 1.

$$R_{OCSET} = \frac{R_{LDS(on)} \times \left(I_{OC} - \frac{I_{RIPPLE}}{2} \right)}{10\,\mu A} \quad (1)$$

where

- $R_{LDS(on)}$ is the drain-to-source resistance of the lower MOSFET in the ON state
- I_{OC} is the desired value of the overcurrent protection threshold for load current
- I_{RIPPLE} is the peak-to-peak amplitude of the inductor ripple current
- the valley of the inductor current is compared with the overcurrent threshold for protection

When the controller senses the overcurrent condition for more than two clock cycles, both the upper and the lower MOSFETs are latched off. To restart the controller, the VDD input should be cycled.

If the overcurrent set resistor value is higher than 50 kΩ, for example, the voltage drop on the LDRV_OC pin exceeds 0.5 V, the controller stays in the calibration state without entering soft-start. This prevents the controller from being activated if the overcurrent set resistor is missing.

OVERVOLTAGE (OV) AND UNDERVOLTAGE (UV) PROTECTION

The controller employs the dedicated VOS input to set output undervoltage and overvoltage protections. A resistor divider with the same ratio as on the FB input is recommended for the VOS input. The overvoltage and undervoltage thresholds for VOS are set to ± 25% of the internal reference, which is 800 mV.

When the voltage on VOS is lower than 600 mV, the undervoltage protection is triggered. The controller is latched off with both the upper and lower MOSFETs turned off.

When the voltage on VOS is higher than 1 V, the overvoltage protection is activated. In the event of overvoltage, the upper MOSFET is turned off and the lower MOSFET is forced on until VOS voltage reaches 400 mV. Then the lower MOSFET is also turned off, and the controller is latched off.

After both the undervoltage and overvoltage events, normal operation can only be restored by cycling the VDD voltage.

PGOOD

The TPS51113 and TPS51163 have a power good output that indicates HIGH when the output voltage is within the target range. The PGOOD function is activated as soon as the soft-start ends. When the output voltage goes ± 10% outside of the target value, PGOOD goes low. When the output voltage returns to be within ± 6% of the target value, PGOOD signal goes HIGH again. The PGOOD output is an open drain and needs external pull up resistor.

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APPLICATION INFORMATION

EXTERNAL PARTS SELECTION

CHOOSING THE INDUCTOR

The value of the output filtering inductor determines the magnitude of the current ripple, which also affects the output voltage ripple for a certain output capacitance value. Increasing the inductance value reduces the ripple current, and thus, results in reduced conduction loss and output ripple voltage. On the other hand, low inductance value is needed due to the demand of low profile and fast transient response. Therefore, it is important to obtain a compromise between the low ripple current and low inductance value.

In practical application, to ensure high power conversion efficiency at light load condition, the peak-to-peak current ripple is usually designed to be between 1/4 to 1/2 of the rated load current. Since the magnitude of the current ripple is determined by inductance value, switching frequency, input voltage and output voltage, the required inductance value for a certain required ripple ΔI is shown in Equation 2,

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times I_{RIPPLE} \times f_{SW}} \quad (2)$$

where

- V_{IN} is the input voltage
- V_{OUT} is the output voltage
- I_{RIPPLE} is the required current ripple
- f_{SW} is the switching frequency

CALCULATING OUTPUT CAPACITANCE

When the inductance value is determined, the output capacitance value can also be derived according to the output ripple voltage and output load transient response requirement. The output ripple voltage is a function of both the output capacitance and capacitor ESR. Considering the worst case and assume the capacitance value is C_{OUT}, the peak-to-peak ripple voltage can be derived in Equation 3.

$$\Delta V = I_{RIPPLE} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right) \quad (3)$$

Thus, output capacitors with suitable ESR and capacitance value should be chosen to meet the ripple voltage (ΔV) requirement.

Minimum capacitance value is also calculated according to the demand of the load transient response. When the load current changes, the energy that the inductor needs to release or absorb is derived in Equation 4.

$$E_L = \frac{1}{2} \times L \times \left((I_{OH})^2 - (I_{OL})^2 \right) \quad (4)$$

At the same time, the energy that is delivered to or provided by the output capacitor can also be derived as shown in Equation 5.

$$E_C = \frac{1}{2} \times C_{OUT} \times \left((Vf)^2 - (Vi)^2 \right) \quad (5)$$

As a result, to meet the load transient response demand, the minimum output capacitance should be

$$C_{OUT} = \frac{L \times \left((I_{OH})^2 - (I_{OL})^2 \right)}{\left| (V_f)^2 - (V_i)^2 \right|} \quad (6)$$

where

- I_{OH} is the output current under heavy load conditions
- I_{OL} is the output current under light load conditions
- V_f is the final peak capacitor voltage
- V_i is the initial capacitor voltage

By considering the demand of both output ripple voltage and load transient response, the minimum output capacitance can be determined.

INPUT CAPACITOR SELECTION

For a certain rated load current, input and output voltage, the input ripple voltage caused by the input capacitance value and ESR are shown in Equation 7 and Equation 8, respectively.

$$V_{RIPPLE}(C_{IN}) = \frac{I_{OUT} \times V_{OUT}}{C_{IN(min)} \times V_{IN} \times f_{SW}} \quad (7)$$

$$V_{RIPPLE}(ESR_C_{IN}) = ESR_{C_{IN}} \times \left(I_{OUT} + \frac{1}{2} \times I_{RIPPLE} \right) \quad (8)$$

Based on the required input voltage ripple, suitable capacitors can be chosen by using the above equations.

CHOOSING MOSFETS

Choosing suitable MOSFETs is extremely important to achieve high power conversion efficiency for the converter. For a buck converter, suitable MOSFETs should not only meet the requirement of voltage and current rating, but also ensure low power loss. VDD can be connected to the 5-V rail when Ciclon FETs are used. But when less expensive FETs are used, direct gate drive facilitates the use of a higher drive voltage (such as V_{IN}) to boost the efficiency.

High-Side MOSFET

Power loss of the high-side MOSFETs primarily consists of the conduction loss (P_{COND1}) and the switching loss (P_{SW1}).

The conduction loss of the high-side MOSFET is the I^2R loss in the MOSFET's on-resistance, $R_{DS(on)1}$. The RMS value of the current passing through the top MOSFET depends on the average load current, ripple current and duty cycle the converter is operating.

$$I_{RMS1} = \sqrt{D \times \left((I_{OUT})^2 + \frac{(I_{RIPPLE})^2}{12} \right)} \quad (9)$$

The conduction loss can, thus, be calculated as follows.

$$P_{COND1} = (I_{RMS1})^2 \times R_{DS(ON)1} \quad (10)$$

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Also, the switching loss can be approximately described as

$$P_{SW1} = V_{IN} \times \left(\left(\frac{I_{D1} \times t_{S1}}{6} \right) + \left(\frac{I_{D2} \times t_{S2}}{2} \right) \right) \times f_{SW} \quad (11)$$

where

- I_{D1} and I_{D2} are the current magnitudes at the time instance when the MOSFETs switch

$$I_{D1} = I_{OUT} - \frac{1}{2} \times I_{RIPPLE} \quad \text{and} \quad I_{D2} = I_{OUT} + \frac{1}{2} \times I_{RIPPLE} \quad (12)$$

where

- t_{s1} is the MOSFET switching-on time
- t_{s2} is the MOSFET switching-off time

Therefore, the total power loss of the high-side MOSFET is estimated by the sum of the above power losses,

$$P_{HFET_Loss} = P_{COND1} + P_{SW1} \quad (13)$$

Synchronous Rectifier MOSFET Power Loss

Power loss associated with the synchronous rectifier (SR) MOSFET mainly consists of $R_{DS(on)}$ conduction loss, body diode conduction loss and reverse recovery loss.

Similarly to the high-side MOSFET, the conduction loss of the SR MOSFET is also the I^2R loss of the MOSFET's on-resistance, $R_{DS(on)2}$. Since the switching on-time of the SR MOSFET is (1-D)×T , where T is the duration of one switching cycle, the RMS current of the SR MOSFET can be calculated as follows.

$$I_{RMS2} = \sqrt{(1-D) \times \left((I_{OUT})^2 + \frac{(I_{RIPPLE})^2}{12} \right)} \quad (14)$$

The symchronous rectifier (SR) MOSFET conduction loss is

$$P_{COND2} = (I_{RMS2})^2 \times R_{DS(ON)2} \quad (15)$$

The body diode conduction loss is

$$P_{COND3} = I_{OUT} \times V_F \times t_D \times f_{SW} \quad (16)$$

where

- V_F is the forward voltage of the MOSFET body diode
- t_D is the total conduction time of the body diode in one switching cycle

The body diode recovery time – the time it takes for the body diode to restore its blocking capability from forward conduction state, determines the reverse recovery losses.

$$P_{RR} = \frac{1}{2} \times Q_{RR} \times V_{IN} \times f_{SW} \quad (17)$$

where

- Q_{RR} is the reverse recovery charge of the body diode

Therefore, the total power loss of the SR MOSFET is estimated by the sum of the above power losses.

$$P_{SR_Loss} = P_{COND2} + P_{COND3} + P_{RR} \quad (18)$$

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Feedback Loop Compensation

Since TPS51113/TPS51163 utilizes voltage-mode control for buck converters, Type III network is recommended for loop compensation. Suitable poles and zeros can be set by choosing proper parameters for the loop compensation network.

To calculate loop compensation parameters, the poles and zeros for the buck converter should be obtained. The double pole, determined by the L, and C_{OUT} of the buck converter, is located at the frequency as shown in the following equation.

$$f_0 = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}} \tag{19}$$

Also, the ESR zero of the buck converter can be achieved.

$$f_Z = \frac{1}{2\pi \times ESR \times C_{OUT}} \tag{20}$$

Figure 8 shows the configuration of Type III compensation. The transfer function of the compensator is described in Equation 21. Also, poles and zeros for the Type III network are shown in Equation 22 through Equation 26.

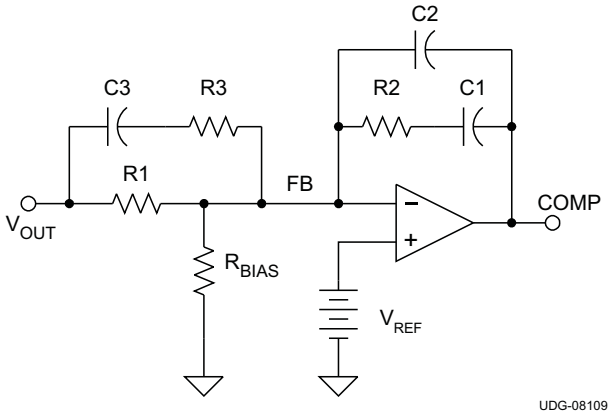


Figure 8. Type III Compensation Network

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$$G(s) = \frac{(sR_2C_1 + 1) \times (s(R_1 + R_3)C_3 + 1)}{sR_1(C_1 + C_2) \times \left(s\left(\frac{R_2C_1C_2}{C_1 + C_2}\right) + 1\right) \times (sR_3C_3 + 1)} \quad (21)$$

$$f_{Z1} = \frac{1}{2\pi \times R_2 \times C_1} \quad (22)$$

$$f_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{(C_1 \times C_2)}{(C_1 + C_2)}\right)} \quad (23)$$

$$f_{P2} = \frac{1}{2\pi \times R_3 \times C_3} \quad (24)$$

$$f_{Z2} = \frac{1}{2\pi \times (R_1 + R_3) \times C_3} \quad (25)$$

$$f_C = \frac{1}{2\pi \times R_1 \times (C_1 + C_2)} \quad (26)$$

f_{P1} is usually used to cancel the ESR zero in Equation 20. f_{P2} can be placed at higher frequency in order to attenuate the high frequency noise and the switching ripple. f_{Z1} and f_{Z2} are chosen to be lower than the switching frequency, and f_{Z1} is lower than resonant frequency f_0. Suitable values can be selected to achieve the compromise between high phase margin and fast response. A phase margin of over 60° is usually recommended. Then, the compensator gain is chosen to achieve the desired bandwidth.

The value of R_{BIAS} is calculated to set the output voltage V_{OUT}.

$$R_{BIAS} = \frac{0.8 \times R_1}{V_{OUT} - 0.8} \quad (27)$$

Layout Considerations

For the grounding and circuit layout, certain points need to be considered.

- It is important that the signal ground and power ground properly use separate copper planes to prevent the noise of power ground from influencing the signal ground. The impedance of each ground is minimized by using its copper plane. Sensitive nodes, such as the FB resistor divider and VOS resistor divider, should be connected to the signal ground plane, which is also connected with the GND pin of the device. The high power noisy circuits, such as synchronous rectifier, MOSFET driver decoupling capacitors, the input capacitors and the output capacitors should be connected to the power ground plane. Finally, the two separate ground planes should be strongly connected together near the device by using a single path/trace.
- A minimum of 0.1-µF ceramic capacitor must be placed as close to VDD pin and GND pin as possible with a trace at least 20 mils wide, from the bypass capacitor to the GND. Usually a capacitance value of 1 µF is recommended for the bypass capacitor.
- The PowerPAD should be electrically connected to GND.
- A parallel pair of trace (with at least 15 mils wide) connects the regulated voltage back to the chip. The trace should be away from the switching components. The bias resistor of the resistor divider should be connected to the FB pin and GND pin as close as possible.
- The component placement of the power stage should ensure minimized loop areas to suppress the radiated emissions. The input current loop is consisted of the input capacitors, the main switching MOSFET, the inductor, the output capacitors and the ground path back to the input capacitors. The SR MOSFET, the inductor, the output capacitors and the ground path back to the source of the SR MOSFET consists of the output current loop. The connection/trace should be as short as possible to reduce the parasitic inductance.
- Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. A trace of 25 mils or wider is recommended.
- Connect the overcurrent setting resistor from LDRV_OC to GND close to the device.

TPS51113 Design Example

The following example illustrates the design process and component selection for a single output synchronous buck converter using the TPS51113. The schematic of a design example is shown in Figure 9. The specification of the converter is listed in Table 2.

Table 2. Specification of the Single Output Synchronous Buck Converter

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		10.8	12	13.2	V
V_{OUT}	Output voltage			1.6		V
V_{RIPPLE}	Output ripple	I_{OUT} = 10 A		2% of V_{OUT}		V
I_{OUT}	Output current			10		V
f_{SW}	Switching frequency			300		kHz

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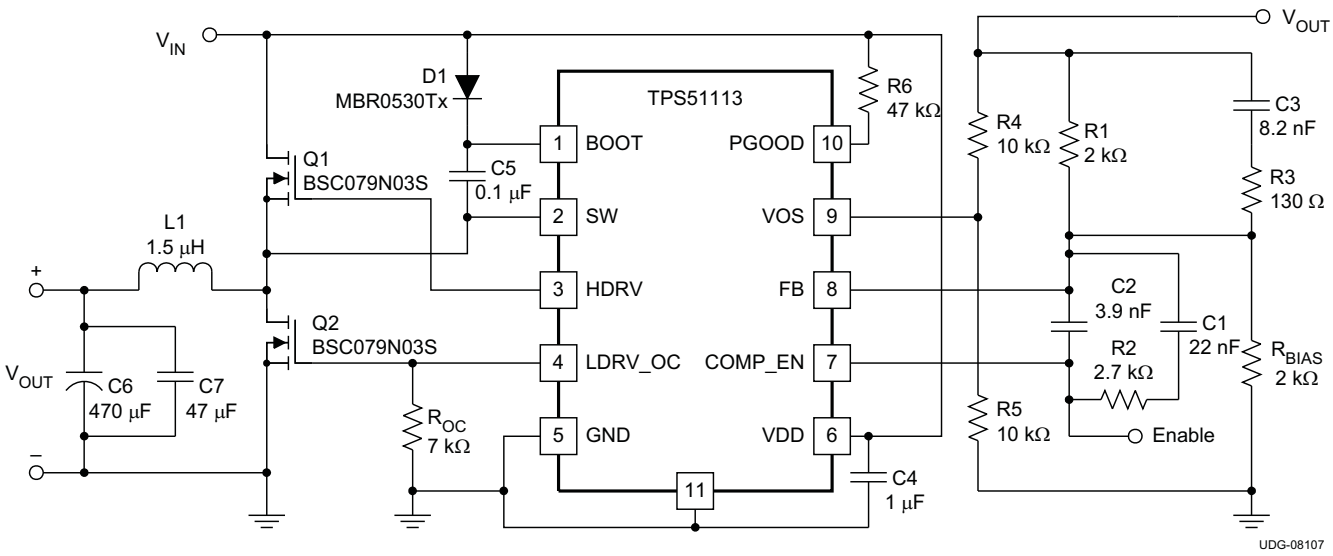


Figure 9. Design Example, 12 V to 1.6 V/10 A DC-DC Converter

Choosing the Inductor

Typically the peak-to-peak inductor current ΔI is selected to be approximately between 20% and 40% of the rated output current. In this design, I_{RIPPLE} is targeted at around 30% of the load current. Using Equation 2.

$$L = \frac{(V_{IN} - V_O) \times V_O}{V_{IN} \times I_{RIPPLE} \times f_{SW}} = 1.534\,\mu H \tag{29}$$

Therefore, an inductor value of 1.5 µH is selected in practical, and the inductor ripple current is 3.08 A.

Calculating Output Capacitance

Minimum capacitance value can be calculated according to the demand of the load transient response. Considering 0-A to 10-A step load and 10% overshoot and undershoot, the output capacitance value can be estimated by using Equation 6,

$$C_{OUT} = \frac{L \times \left((I_{OH})^2 - (I_{OL})^2 \right)}{\left| (V_f)^2 - (V_i)^2 \right|} = 279\,\mu F \tag{30}$$

A 470-µF POS-CAP with 18-mΩ ESR and a 47-µF ceramic capacitor are paralleled for the output capacitor.

Input Capacitor Selection

Considering 100 mV $V_{RIPPLE(Cin)}$ and 50 mV $V_{RIPPLE(ESR_Cin)}$, the input capacitance value and ESR value can be calculated according to Equation 7 and Equation 8, respectively.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{RIPPLE(C_{IN})} \times V_{IN} \times f_{SW}} = 44\,\mu F \tag{31}$$

$$ESR_{C_{IN}} = \frac{V_{RIPPLE(ESR_C_{IN})}}{\left(\frac{(I_{OUT} + I_{RIPPLE})}{2}\right)} = 4.3\,m\Omega \tag{32}$$

Therefore, two 22-µF ceramic capacitors with 2-mΩ ESR can meet this requirement.

Choosing MOSFETS

High-Side MOSFET Power Loss

BSC079N03S is used for the high-side MOSFET. The on-resistance, $R_{DS(on)1}$ is 7.9 mΩ. MOSFET switching-on time (t_{s1}) and switching-off time (t_{s2}) are approximately 9 ns and 24 ns, respectively. By using Equation 9 through Equation 13, the total power loss of the high-side MOSFET is estimated.

$$P_{HFET_Loss} = P_{COND1} + P_{SW1} = (I_{RMS1})^2 \times R_{DS(on)1} + V_{IN} \times \left(\frac{I_{D1} \times t_{S1}}{6} + \frac{I_{D2} \times t_{S2}}{2}\right) \times f_{SW} = 649\,mW \tag{33}$$

Synchronous Rectifier MOSFET Power Loss

BSC032N03S is used for the synchronous rectifier MOSFET. The on-resistance, $R_{DS(on)1}$ is 3.2 mΩ. The body diode has a 0.84-V diode forward voltage and 15-nC reverse recovery charge. The output driver deadtime is 30 ns. By using Equation 14 through Equation 18, the total power loss of the synchronous MOSFET is estimated,

$$P_{SR_Loss} = P_{COND2} + P_{COND3} + P_{RR} = \left[I_{RMS2}\right]^2 \times R_{DS(on)2} + I_O \times V_F \times t_D \times f_{SW} + \frac{1}{2} \times Q_{RR} \times V_{IN} \times f_{SW} = 382\,mW \tag{34}$$

Feedback Loop Compensation

Since TPS51113 and TPS51163 utilize voltage-mode control for buck converters, Type III network is recommended for loop compensation. The converter utilizes a 1.5-µH inductor and 470-µF capacitor with 18-mΩ ESR. The double pole, determined by the L, and C_{OUT} of the buck converter, is derived by Equation 19

$$f_0 = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}} = 6.0\,kHz \tag{35}$$

Also, the ESR zero of the buck converter can be achieved by using Equation 20.

$$f_Z = \frac{1}{2\pi \times ESR \times C_{OUT}} = 18.8\,kHz \tag{36}$$

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Figure 10 shows the detailed parameters used for the Type III compensation. Also, poles and zeros for the Type III network are derived based on Equation 22 through Equation 26.

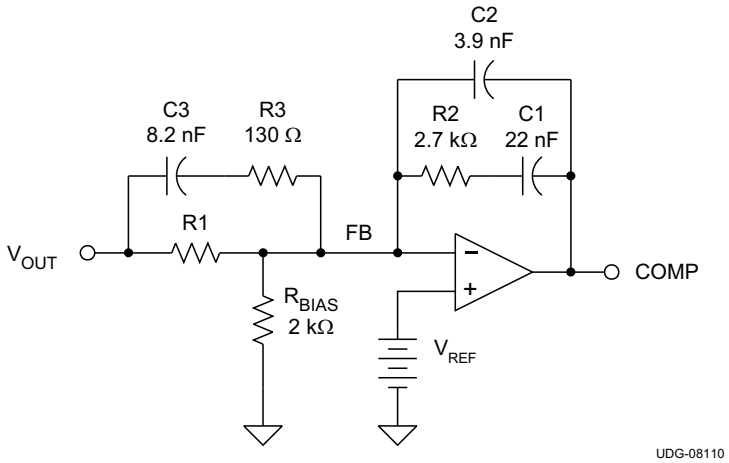


Figure 10. Parameters for Type III Compensation Network

$$G(s) = \frac{(sR_2C_1 + 1) \times (s(R_1 + R_3)C_3 + 1)}{sR_1(C_1 + C_2) \times \left(s\left(\frac{R_2C_1C_2}{C_1 + C_2}\right) + 1\right) \times (sR_3C_3 + 1)} \quad (37)$$

$$f_{Z1} = \frac{1}{2\pi \times R_2 \times C_1} = 2.7\,kHz \quad (38)$$

$$f_{Z2} = \frac{1}{2\pi \times (R_1 + R_3) \times C_3} = 9.2\,kHz \quad (39)$$

$$f_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{(C_1 \times C_2)}{(C_1 + C_2)}\right)} = 17.8\,kHz \quad (40)$$

$$f_{P2} = \frac{1}{2\pi \times R_3 \times C_3} = 149.4\,kHz \quad (41)$$

$$f_C = \frac{1}{2\pi \times R_1 \times (C_1 + C_2)} = 3.1kHz \quad (42)$$

f_{P1} is used to cancel the ESR zero. f_{P2} is placed at higher frequency to attenuate the high-frequency noise and the switching ripple. f_{Z1} is lower than resonant frequency f_0.

The value of R_{BIAS} is calculated to set the output voltage V_{OUT} by using Equation 27.

$$R_{BIAS} = \frac{0.8 \times R_1}{V_O - 0.8} = 2k\Omega \quad (43)$$

Based on Equation 43 and the power stage parameters, the bode-plot by simulation is shown in Figure 10 (V_{IN}=12 V and I_{OUT}=0 A). The achieved cross-over frequency is approximately 35.7 kHz, and the phase margin is approximately 60°.

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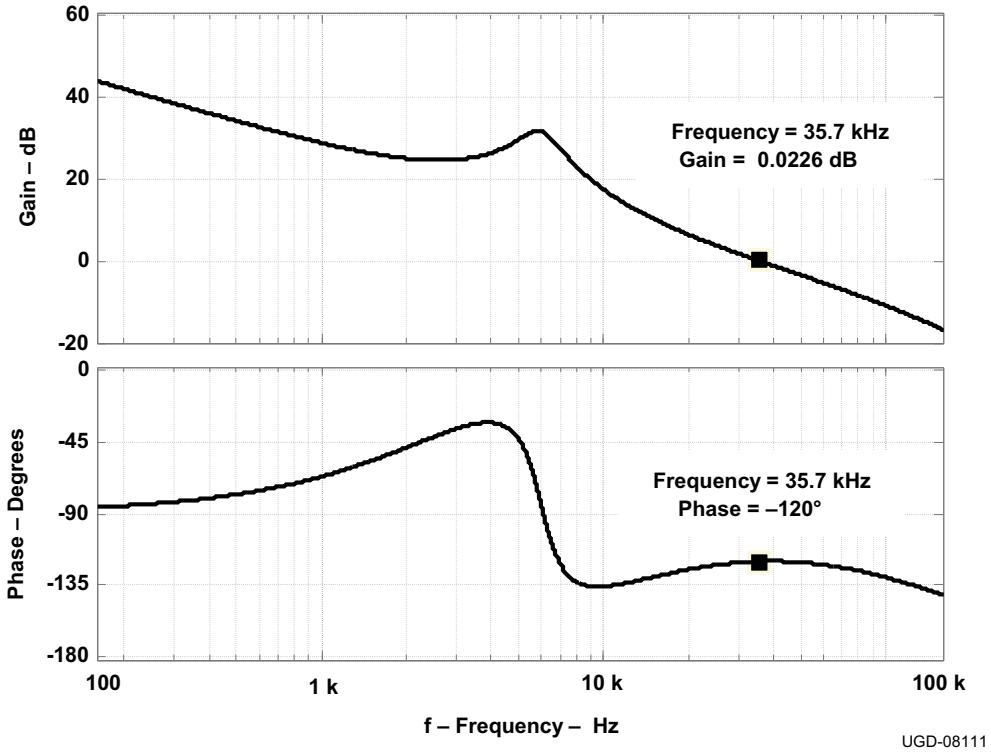
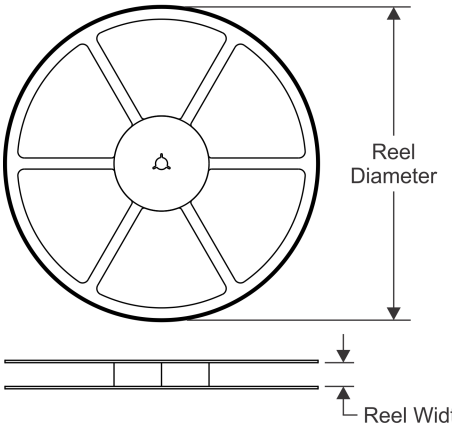


Figure 11. Bode Plot of the Design Example Circuit by Simulation (V_{IN}=12 V and I_{OUT}=0 A)

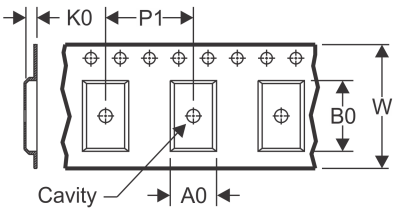
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

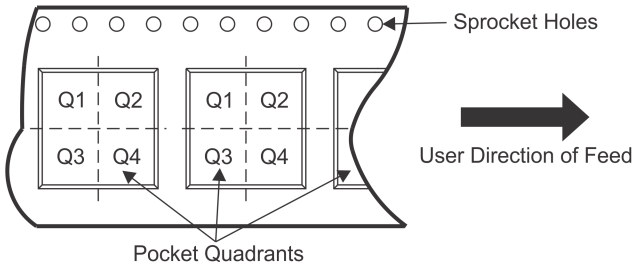


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

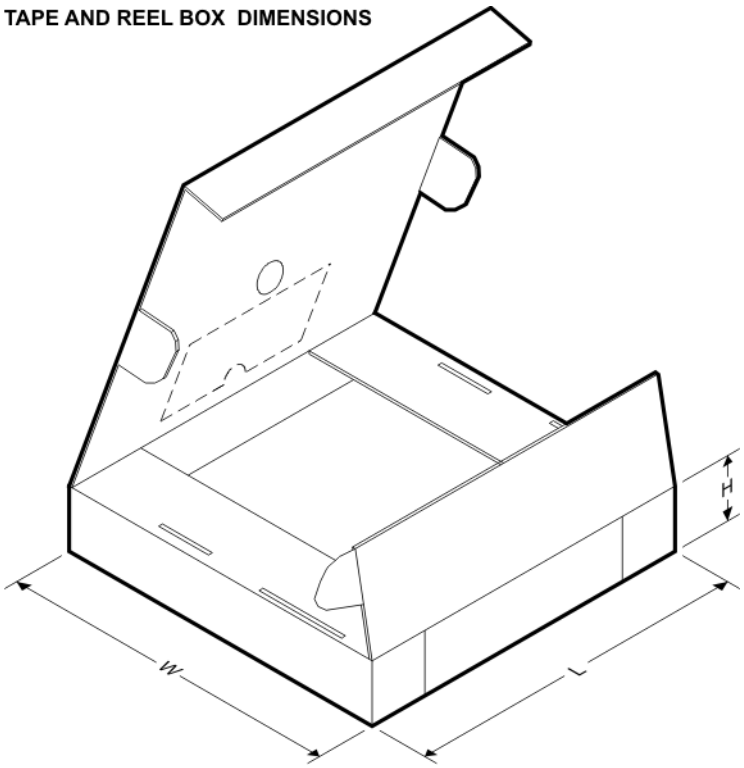
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51113DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51113DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51163DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51163DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



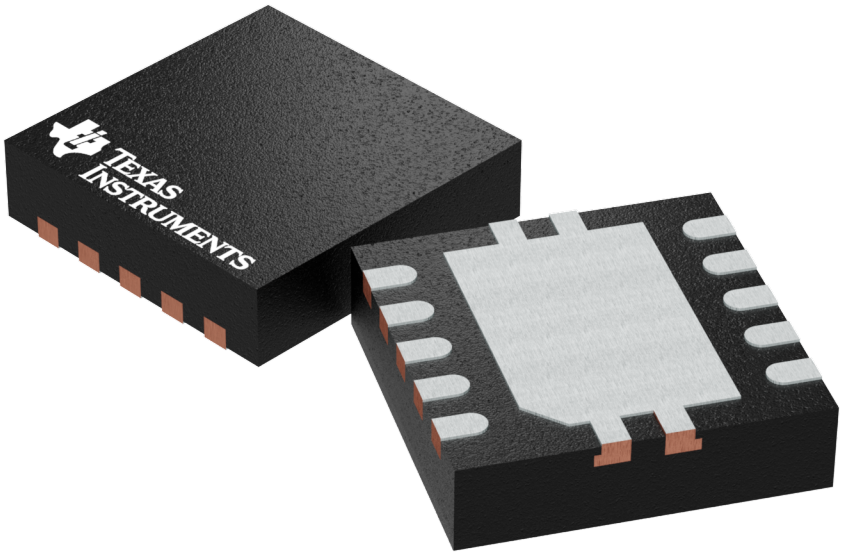
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51113DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS51113DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS51163DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS51163DRCT	VSON	DRC	10	250	210.0	185.0	35.0

DRC 10

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



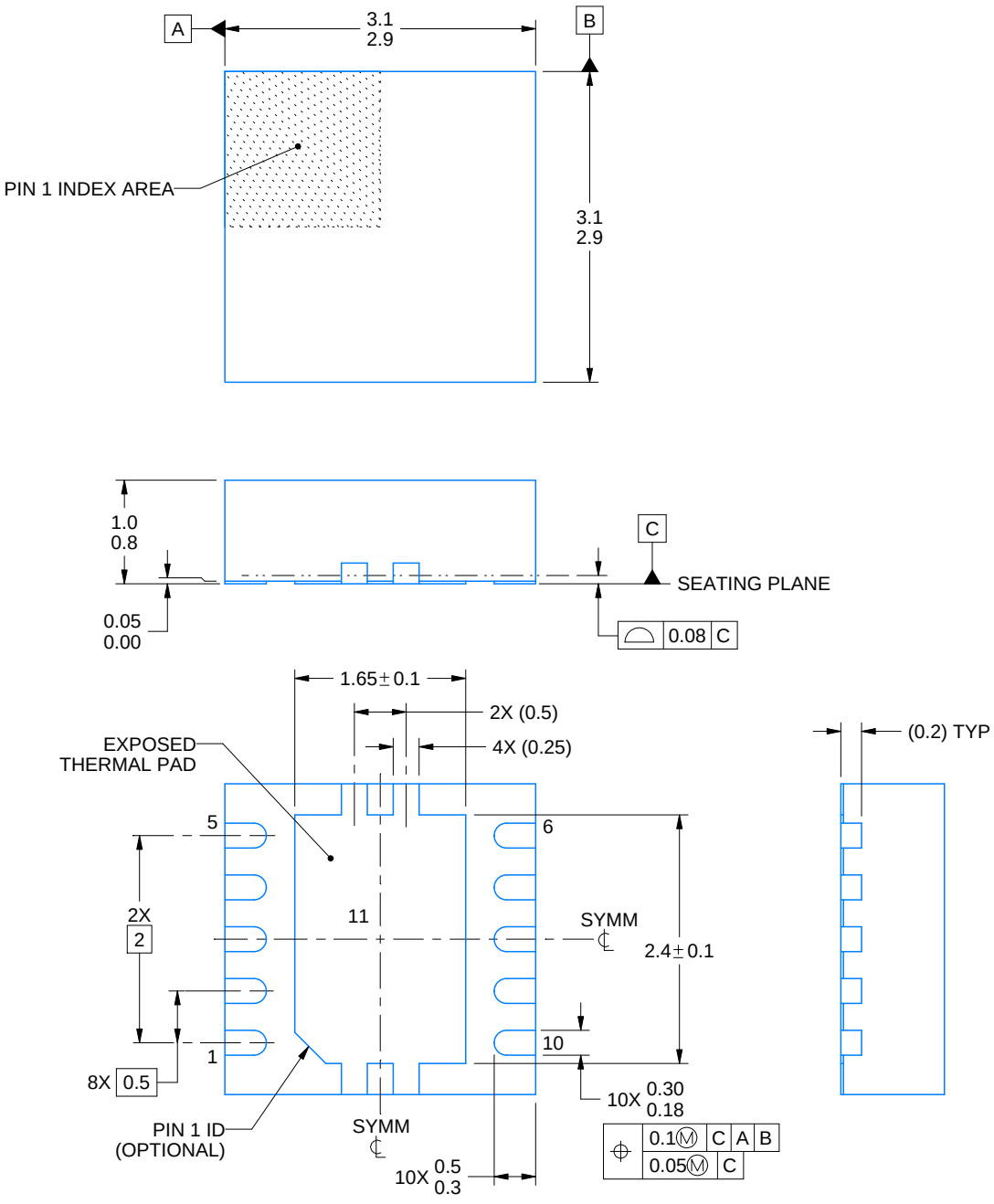
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRC0010J

PACKAGE OUTLINE

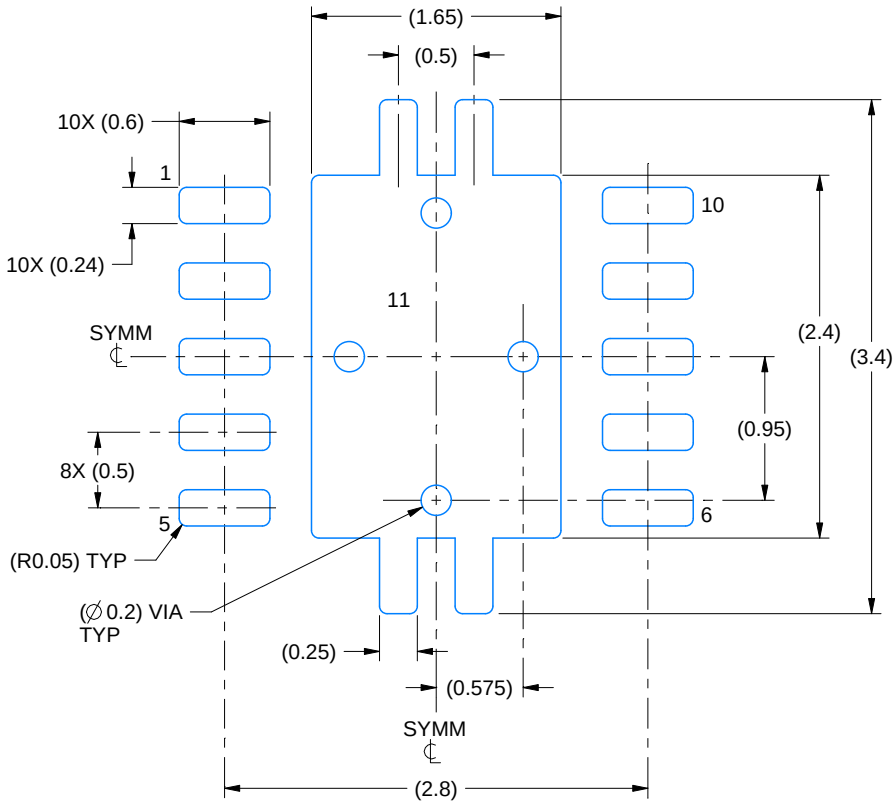
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

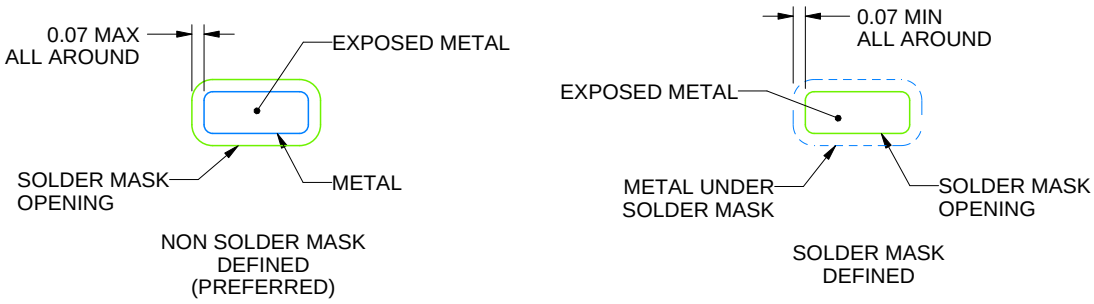


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

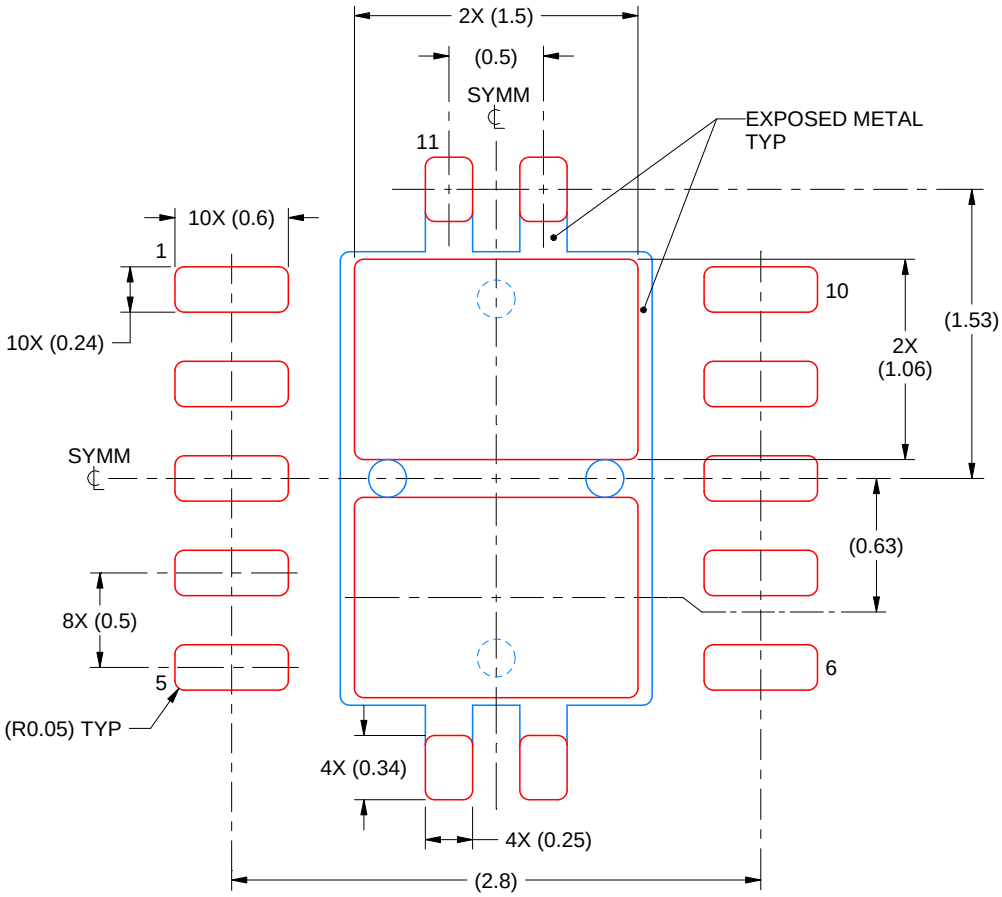
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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