

# SN54F27, SN74F27 TRIPLE 3-INPUT POSITIVE-NOR GATES

SDFS042A – MARCH 1987 – REVISED OCTOBER 1993

- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

## description

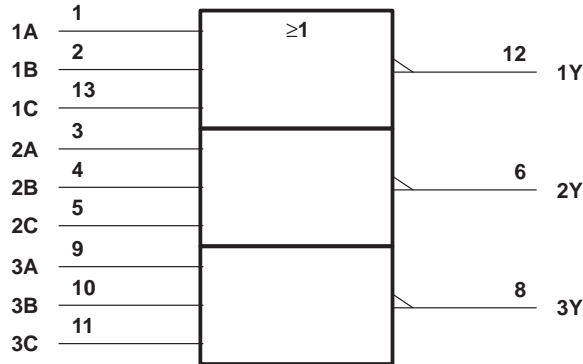
These devices contain three independent 3-input NOR gates. They perform the Boolean functions  $Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$  or  $Y = A + B + C$  in positive logic.

The SN54F27 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74F27 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE  
(each gate)

| INPUTS |   |   | OUTPUT |
|--------|---|---|--------|
| A      | B | C | Y      |
| H      | X | X | L      |
| X      | H | X | L      |
| X      | X | H | L      |
| L      | L | L | H      |

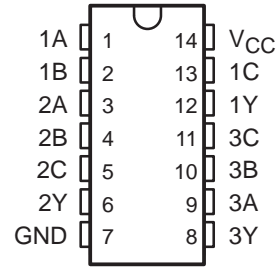
## logic symbol†



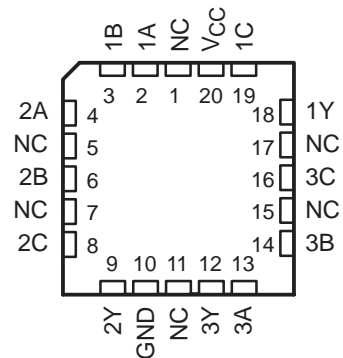
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

SN54F27 ... J PACKAGE  
SN74F27 ... D OR N PACKAGE  
(TOP VIEW)



SN54F27 ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## logic diagram, each gate (positive logic)



# SN54F27, SN74F27 TRIPLE 3-INPUT POSITIVE-NOR GATES

SDFS042A – MARCH 1987 – REVISED OCTOBER 1993

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|   |                    |
|---|--------------------|
| Supply voltage range, $V_{CC}$                        | –0.5 V to 7 V      |
| Input voltage range, $V_I$ (see Note 1)               | –1.2 V to 7 V      |
| Input current range                                   | –30 mA to 5 mA     |
| Voltage range applied to any output in the high state | –0.5 V to $V_{CC}$ |
| Current into any output in the low state              | 40 mA              |
| Operating free-air temperature range: SN54F27         | –55°C to 125°C     |
| SN74F27   | 0°C to 70°C        |
| Storage temperature range                             | –65°C to 150°C     |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

|          |                                | SN54F27 |     |     | SN74F27 |     |     | UNIT |
|----------|--------------------------------|---------|-----|-----|---------|-----|-----|------|
|          |                                | MIN     | NOM | MAX | MIN     | NOM | MAX |      |
| $V_{CC}$ | Supply voltage                 | 4.5     | 5   | 5.5 | 4.5     | 5   | 5.5 | V    |
| $V_{IH}$ | High-level input voltage       | 2       |     |     | 2       |     |     | V    |
| $V_{IL}$ | Low-level input voltage        |         |     | 0.8 |         |     | 0.8 | V    |
| $I_{IK}$ | Input clamp current            |         |     | –18 |         |     | –18 | mA   |
| $I_{OH}$ | High-level output current      |         |     | –1  |         |     | –1  | mA   |
| $I_{OL}$ | Low-level output current       |         |     | 20  |         |     | 20  | mA   |
| $T_A$    | Operating free-air temperature | –55     |     | 125 | 0       |     | 70  | °C   |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER     | TEST CONDITIONS                     | SN54F27 |      |      | SN74F27 |      |      | UNIT |
|---------------|-------------------------------------|---------|------|------|---------|------|------|------|
|               |                                     | MIN     | TYP‡ | MAX  | MIN     | TYP‡ | MAX  |      |
| $V_{IK}$      | $V_{CC} = 4.5$ V, $I_I = -18$ mA    |         |      | –1.2 |         |      | –1.2 | V    |
| $V_{OH}$      | $V_{CC} = 4.5$ V, $I_{OH} = -1$ mA  | 2.5     | 3.4  |      | 2.5     | 3.4  |      | V    |
|               | $V_{CC} = 4.75$ V, $I_{OH} = -1$ mA |         |      |      | 2.7     |      |      |      |
| $V_{OL}$      | $V_{CC} = 4.5$ V, $I_{OL} = 20$ mA  |         | 0.3  | 0.5  |         | 0.3  | 0.5  | V    |
| $I_I$         | $V_{CC} = 5.5$ V, $V_I = 7$ V       |         |      | 0.1  |         |      | 0.1  | mA   |
| $I_{IH}$      | $V_{CC} = 5.5$ V, $V_I = 2.7$ V     |         |      | 20   |         |      | 20   | μA   |
| $I_{IL}$      | $V_{CC} = 5.5$ V, $V_I = 0.5$ V     |         |      | –0.6 |         |      | –0.6 | mA   |
| $I_{OS}^{\S}$ | $V_{CC} = 5.5$ V, $V_O = 0$         | –60     |      | –150 | –60     |      | –150 | mA   |
| $I_{CCH}$     | $V_{CC} = 5.5$ V, $V_I = 0$         |         | 3.8  | 5.5  |         | 3.8  | 5.5  | mA   |
| $I_{CCL}$     | $V_{CC} = 5.5$ V, See Note 2        |         | 8.4  | 12   |         | 8.4  | 12   | mA   |

‡ All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2:  $I_{CCL}$  is measured with one input at 4.5 V and all others grounded.



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SDFS042A – MARCH 1987 – REVISED OCTOBER 1993

## switching characteristics (see Note 3)

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | V <sub>CC</sub> = 5 V,<br>C <sub>L</sub> = 50 pF,<br>R <sub>L</sub> = 500 Ω,<br>T <sub>A</sub> = 25°C |     |     | V <sub>CC</sub> = 4.5 V to 5.5 V,<br>C <sub>L</sub> = 50 pF,<br>R <sub>L</sub> = 500 Ω,<br>T <sub>A</sub> = MIN to MAX† |     |         |     | UNIT |
|------------------|-----------------|----------------|---|-----|-----|---|-----|---------|-----|------|
|                  |                 |                | 'F27  |     |     | SN54F27   |     | SN74F27 |     |      |
|                  |                 |                | MIN   | TYP | MAX | MIN   | MAX | MIN     | MAX |      |
| t <sub>PLH</sub> | A, B, or C      | Y              | 1.2   | 3.1 | 5   | 1   | 6   | 1       | 5.5 | ns   |
| t <sub>PHL</sub> |                 |                | 1   | 2.1 | 4.5 | 1   | 5.5 | 1       | 4.5 |      |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.



**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)          | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|----------------------------------|-------------------------|
| 5962-89510012A   | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-<br>89510012A<br>SNJ54F27FK | <a href="#">Samples</a> |
| 5962-8951001CA   | ACTIVE        | CDIP         | J                  | 14   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 5962-8951001CA<br>SNJ54F27J      | <a href="#">Samples</a> |
| SN74F27D         | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | F27                              | <a href="#">Samples</a> |
| SN74F27DR        | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | F27                              | <a href="#">Samples</a> |
| SN74F27DRE4      | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | F27                              | <a href="#">Samples</a> |
| SN74F27N         | ACTIVE        | PDIP         | N                  | 14   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | N / A for Pkg Type   | 0 to 70      | SN74F27N                         | <a href="#">Samples</a> |
| SN74F27NE4       | ACTIVE        | PDIP         | N                  | 14   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | N / A for Pkg Type   | 0 to 70      | SN74F27N                         | <a href="#">Samples</a> |
| SN74F27NSR       | ACTIVE        | SO           | NS                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | 74F27                            | <a href="#">Samples</a> |
| SNJ54F27FK       | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-<br>89510012A<br>SNJ54F27FK | <a href="#">Samples</a> |
| SNJ54F27J        | ACTIVE        | CDIP         | J                  | 14   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 5962-8951001CA<br>SNJ54F27J      | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54F27, SN74F27 :**

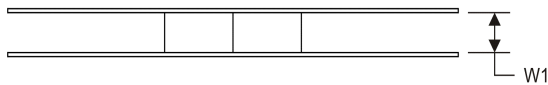
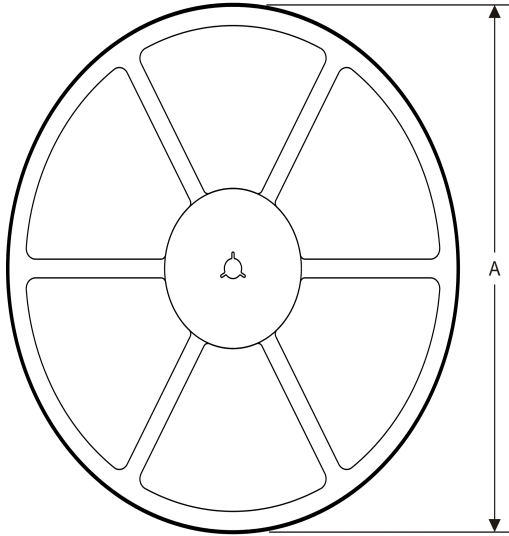
- Catalog: [SN74F27](#)
- Military: [SN54F27](#)

NOTE: Qualified Version Definitions:

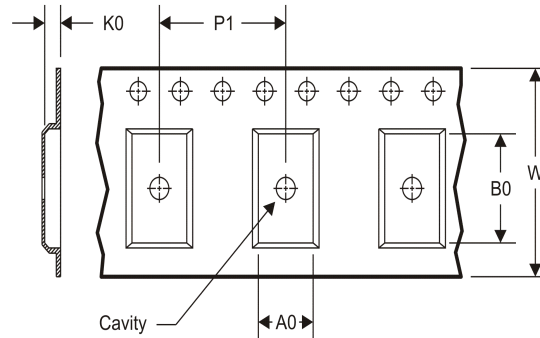
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

TAPE AND REEL INFORMATION

\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74F27DR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74F27NSR | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74F27DR  | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| SN74F27NSR | SO           | NS              | 14   | 2000 | 367.0       | 367.0      | 38.0        |

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A                |                  | B                |                  |
|---------------------|------------------|------------------|------------------|------------------|
|                     | MIN              | MAX              | MIN              | MAX              |
| 20                  | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                  | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                  | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                  | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                  | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                  | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



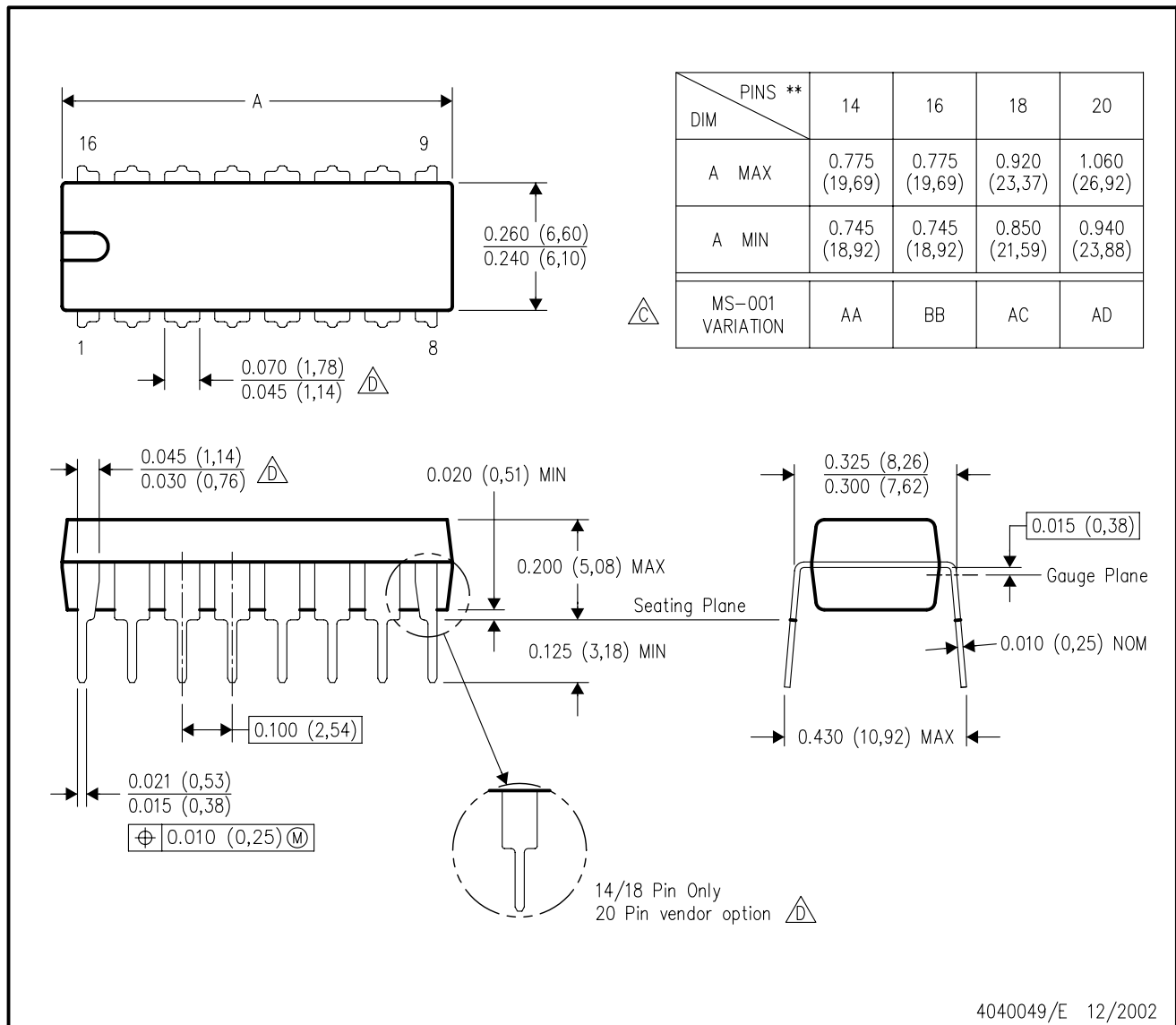
4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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