DIGITAL AUDIO PROCESSOR WITH ANALOG INTERFACE

Check for Samples: TAS3308

FEATURES

- **Digital Audio Processor**
  - **Fully Programmable With the Graphical, Drag-and-Drop PurePath Studio™ Software Development Environment**
  - **135-MHz Operation 48-Bit Data Path With 76-Bit Accumulator**
  - **Hardware Single-Cycle Multiplier (28 × 48)**
  - **Five Simultaneous Operations Per Clock Cycle**
  - **Usable 1k Data RAM Words (48 Bit), Usable 1k Coefficient RAM (28 Bit)**
  - **Usable 2.8k Program RAM**
  - **360 ms at 48 kHz, 17k Words 24-Bit Delay Memory**
  - **Slave Mode F_s is 32.44.1 and 48 kHz With Auto Sample Rate Detection**
  - **Master Mode F_s is 48 kHz**
- **Analog Audio Input/Output**
  - **10:1 Stereo Analog Input MUX**
  - **Stereo Analog Pass-Through Channel**
  - **Stereo, Single-Ended ADC (100 dB DNR Typical)**
  - **Six Differential PWM Outputs (105 dB DNR Typical)**
  - **PurePath™ Digital Technology Minimizes Pop/Click**
  - **Fourth Order Chaotic Noise Shaper With Non-Linear Correction**
- **Digital Audio Input/Output**
  - **Three Synchronous Serial Audio Inputs (Six Channels)**
  - **Two Synchronous Serial Audio Outputs (Four Channels)**
  - **Input and Output Data Formats: 16-, 20-, or 24-Bit Data Left, Right, and I^2S**
  - **S/PDIF Transmitter**
- **System Control Processor**
  - **Embedded 8051 WARP Microprocessor**
  - **Programmable Using Standard 8051 C Compilers**
  - **Four Programmable GPIO pins**
- **General Features**
  - **Two I^2C Ports for Slave or Master Download**
  - **Single 3.3-V Power Supply**
  - **Integrated Regulators**

APPLICATIONS

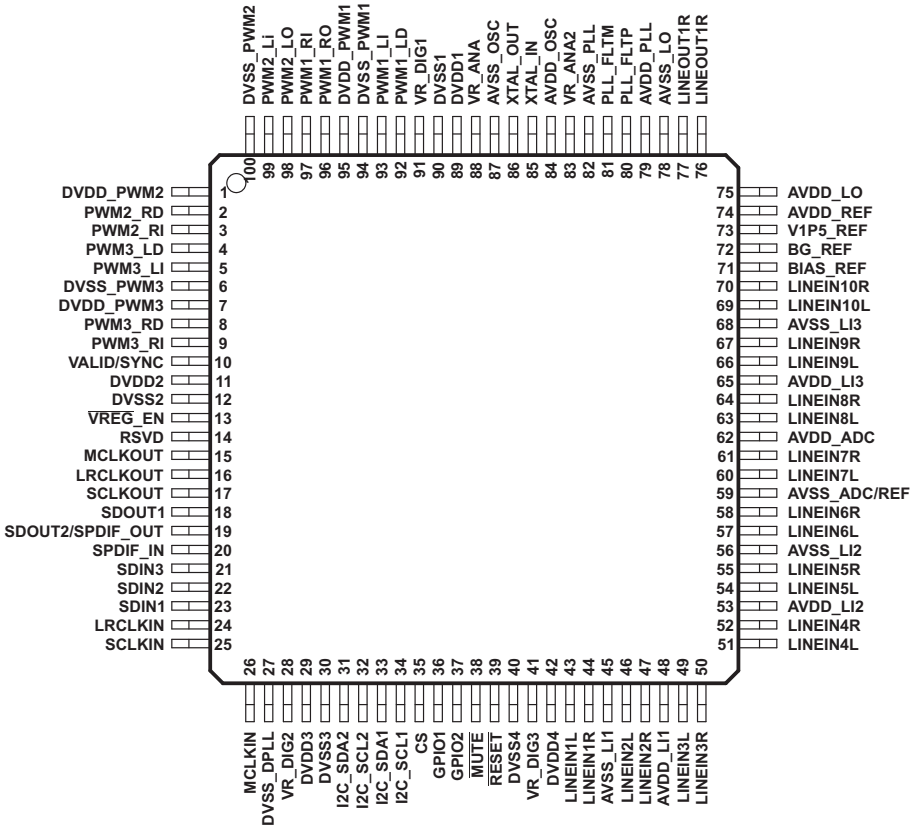
- **Flat-Screen Televisions**
- **MP3 Player/Music Phone Docks**
- **Speaker Bars**
- **Mini/Micro-Component Systems**
- **Automotive Head Units**
- **Musical Instruments**

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PZT PACKAGE
(TOP VIEW)



DESCRIPTION

The TAS3308 is a highly-integrated audio system-on-chip (SOC) consisting of a fully-programmable 48-bit digital audio processor, 10:1 stereo analog input MUX, stereo ADC, six PWM output channels, and other analog functionality. The TAS3308 is programmable with the graphical PurePath Studio™ and suite of DSP code development software. PurePath Studio™ is a highly intuitive, drag-and-drop development environment that minimizes software development effort while allowing the end user to utilize the power and flexibility of the TAS3308's digital audio processing core.

TAS3308 processing capability includes speaker equalization and cross over, volume/bass/treble control, signal mixing/MUXing/splitting, delay compensation, dynamic range compression, and many other basic audio functions. Audio functions such as matrix decoding, stereo widening, surround sound virtualization and psychoacoustic bass boost are also available with either third-party or TI royalty-free algorithms.

The TAS3308 contains a custom-designed, fully-programmable 135-MHz, 48-bit digital audio processor. A 76-bit accumulator ensures that the high precision necessary for quality digital audio is maintained during arithmetic operations.

A stereo 100-dB DNR ADC and six 105-dB DNR PWM output channels ensure that high quality audio is maintained through the whole signal chain. The PWM outputs utilize TI's PurePath Digital PWM technology and seamlessly interface with TI's extensive line of PWM input class D audio amplifiers.

Ordering Information

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	TQFP – PZT	Tray	TAS3308PZT	TAS3308PZT
		Tape and reel	TAS3308PZTR	

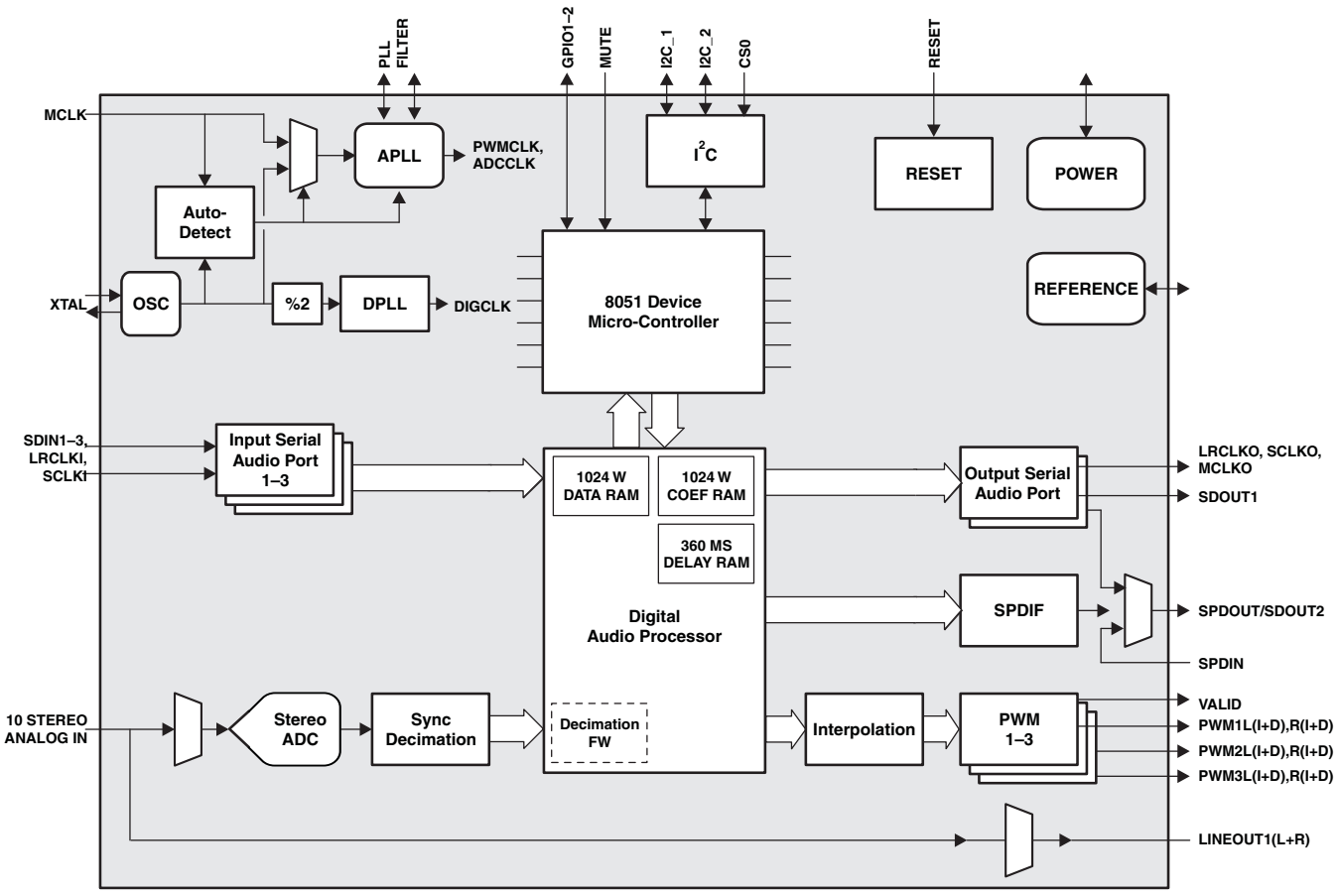
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

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The TAS3308 comprises nine functional blocks:

- Analog input/MUX/stereo ADC
- Three stereo PWM output for speaker/headphone/stereo
- Line driver outputs
- Clock, digital PLL, analog PLL, serial data interface, and auto-detect system
- Serial control interface/device control
- Audio DSP – digital audio processing
- 8051 device controller
- Power supply
- Internal references

Block Diagram



APPLICATION INFORMATION

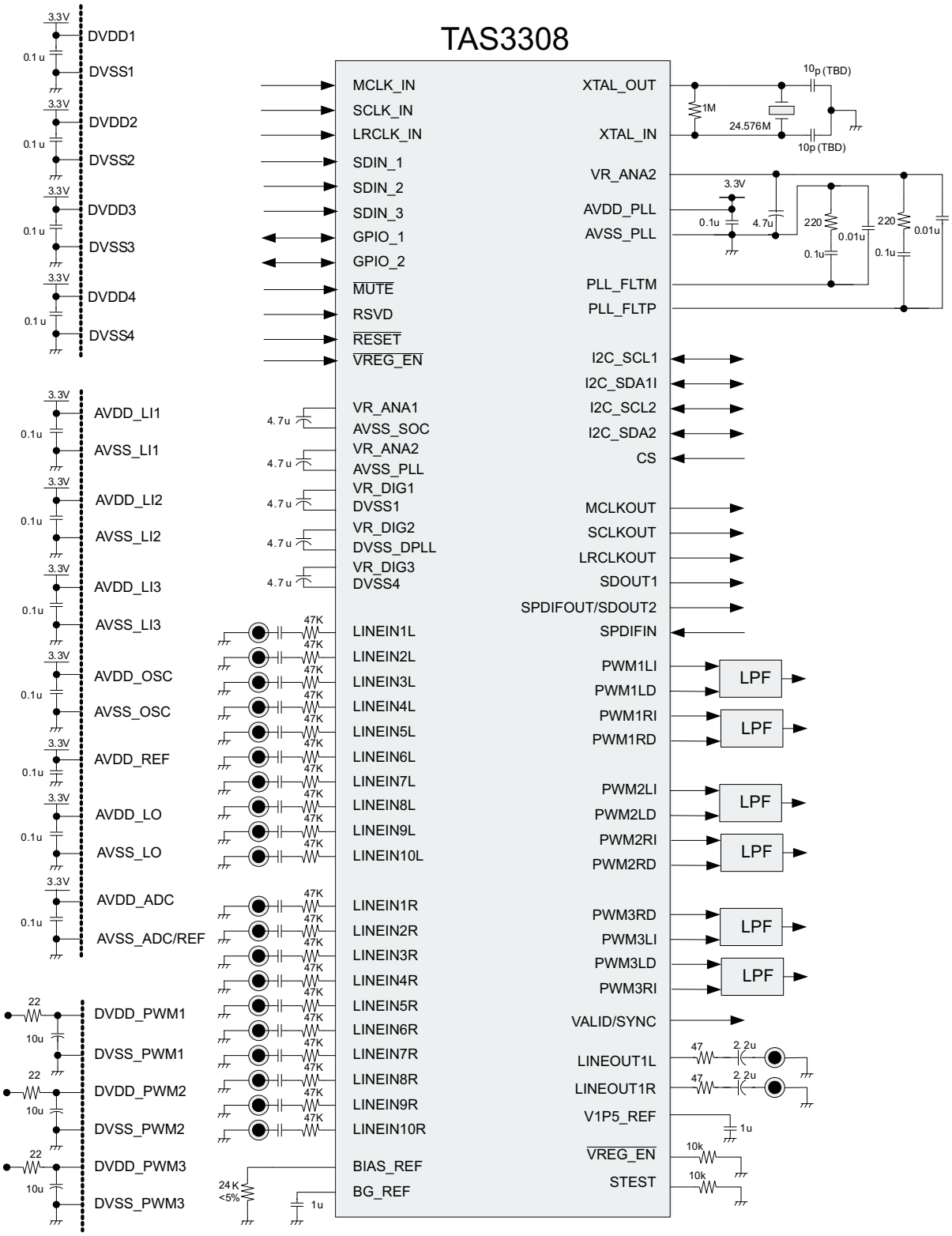


Figure 1. Peripheral Connections

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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
DVDD	Supply voltage range		–0.5	3.8	V
AVDD			–0.5	3.8	
DVDD_PWM			–0.5	3.8	
V_I	Input voltage range	3.3 V TTL	–0.5	VDDS + 0.5	V
		3.3 V LVCMOS	–0.5	VDDS + 0.5	
		3.3 V analog	–0.5	AVDDS + 0.5	
		1.8 V LVCMOS	–0.5	AVDD(2) + 0.5	
V_O	Output voltage range	3.3 V TTL	–0.5	VDDS + 0.5	V
		3.3 V LVCMOS	–0.5	VDDS + 0.5	
		3.3 V analog	–0.5	AVDDS + 0.5	
		1.8 V LVCMOS	–0.5	DVDD(3) + 0.5	
			–0.5	AVDD(4) + 0.5	
I_{IK}	Input clamp current	V_I < 0 or V_I > DVDD		±20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > DVDD		±20	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operation conditions* is not implied. Exposure to absolute-maximum conditions for extended periods may affect device reliability.
(2) AVDD is an internal 1.8-V supply derived from a regulator in the TAS3308 chip. Pin XTAL_IN is the only TAS3308 input that is referenced to this 1.8-V logic supply. The absolute maximum rating listed is for reference; only a crystal should be connected to XTAL_IN.
(3) DVDD is an internal 1.8-V supply derived from regulators in the TAS3308 chip. DVDD is routed to DVDD_BYPASS_CAP to provide access to external filter capacitors, but should not be used to source power to external devices.
(4) Pin XTAL_OUT is the only TAS3308 output that is derived from the internal 1.8-V logic supply AVDD. The absolute maximum rating listed is for reference; only a crystal should be connected to XTAL_OUT. AVDD is also routed to AVDD_BYPASS_CAP to provide access to external filter capacitors, but should not be used to source power to external devices.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MEASUREMENTS	MIN	NOM	MAX	UNIT
DVDD	Digital supply voltage		3	3.3	3.6	V
AVDD	Analog supply voltage	3.3 V analog	3	3.3	3.6	V
DVDD_PWM	PWM supply voltage	3.3 V PWM	3	3.3	3.6	V
V_{IH}	High-level input voltage	3.3 V TTL	2			V
		3.3 V LVCMOS (I^2C)	0.7 × V_{DDS}			
		1.8 V LVCMOS (XTAL_IN)	1.26			
V_{IL}	Low-level input voltage	3.3 V TTL			0.8	V
		3.3 V LVCMOS (I^2C)	0		0.3 × V_{DDS}	
		1.8 V LVCMOS (XTAL_IN)			0.54	
T_A	Operating ambient air temperature	Specifying parametrics	0	25	70	°C
		Specifying functions	–20	25	70	
T_J	Junction temperature		0		96	°C

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ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MEASUREMENT	TEST CONDITIONS	MIN	MAX	UNITS
V_{OH}	High-level output voltage	3.3 V TTL	I_{OH} = –4 mA	2.4		V
		3.3 V LVCMOS (I^2C)	I_{OH} = –0.10 mA	V_{DDS} – 0.2		
		1.8 V LVCMOS (XTAL_OUT)	I_{OH} = –0.6 mA	1.197		
V_{OL}	Low-level output voltage	3.3 V TTL	I_{OL} = 4 mA		0.5	V
		3.3 V LVCMOS (I^2C)	I_{OL} = 0.10 mA		0.2	
		1.8 V LVCMOS (XTAL_OUT)	I_{OL} = 1.8 mA		0.585	
I_{OZ}	High-impedance output current	3.3 V TTL			±20	µA
		3.3 V LVCMOS (I^2C)	Driver only, driver disable		±20	
I_{IL} (1)	Low-level input current	3.3 V TTL	$V_I = V_{IL}$		±1	µA
		3.3 V LVCMOS (I^2C)	$V_I = V_{IL}$, Receiver only		±1	
		1.8 V LVCMOS (XTAL_IN)	$V_I = V_{IL}$		±1	
I_{IH} (2)	High-level input current	1.8 V LVCMOS (XTAL_IN)	$V_I = V_{IH}$		±1	µA
		3.3 V LVCMOS (I^2C)	$V_I = V_{IH}$, Receiver only		±1	
		3.3 V TTL	$V_I = V_{IH}$		±1	
I_{DVDD}	Digital supply current		DSP clock = 135 MHz LRCLKIN/LRCLKOUT = 48 KHz, XTALI = 24.576 MHz		160	mA
I_{AVDD}	Analog supply current		DSP clock = 135 MHz LRCLKIN/LRCLKOUT = 48 KHz, XTALI = 24.576 MHz		40	mA
I_{DVDD}	Digital supply current		$\overline{RESET}$ = LOW		100	mA
I_{AVDD}	Analog supply current		$\overline{RESET}$ = LOW		10	mA

(1) Value given is for those input pins that connect to an internal pullup resistor as well as an input buffer. For inputs that have a pulldown resistor or no resistor, I_{IL} is ±1 µA.

(2) Value given is for those input pins that connect to an internal pulldown resistor as well as an input buffer. For inputs that have a pullup resistor or no resistor, I_{IH} is ±1 µA.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS3308PZT	ACTIVE	TQFP	PZT	100	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS3308PZT	Samples
TAS3308PZTR	ACTIVE	TQFP	PZT	100	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS3308PZT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

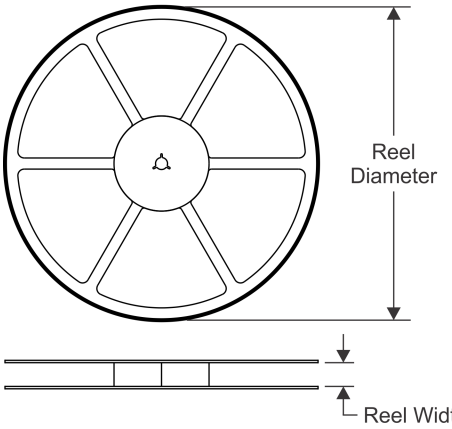
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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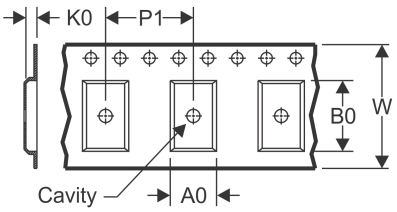
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

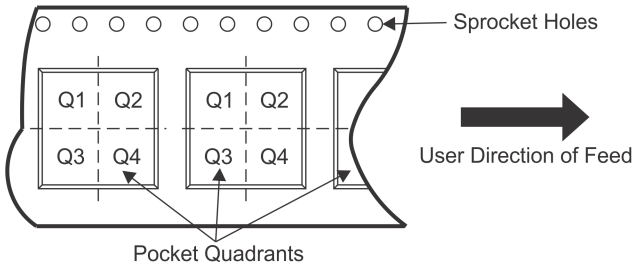


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

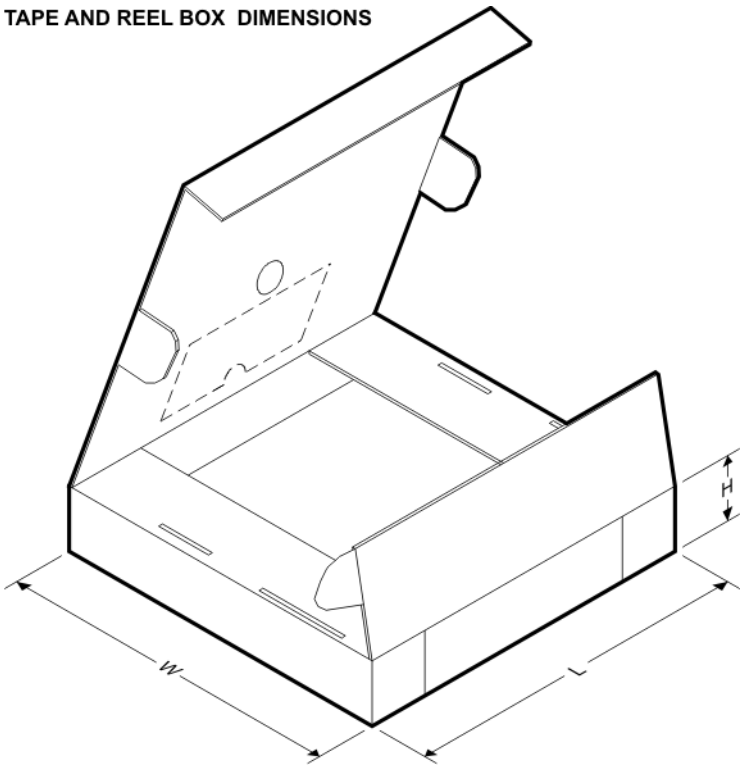
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS3308PZTR	TQFP	PZT	100	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

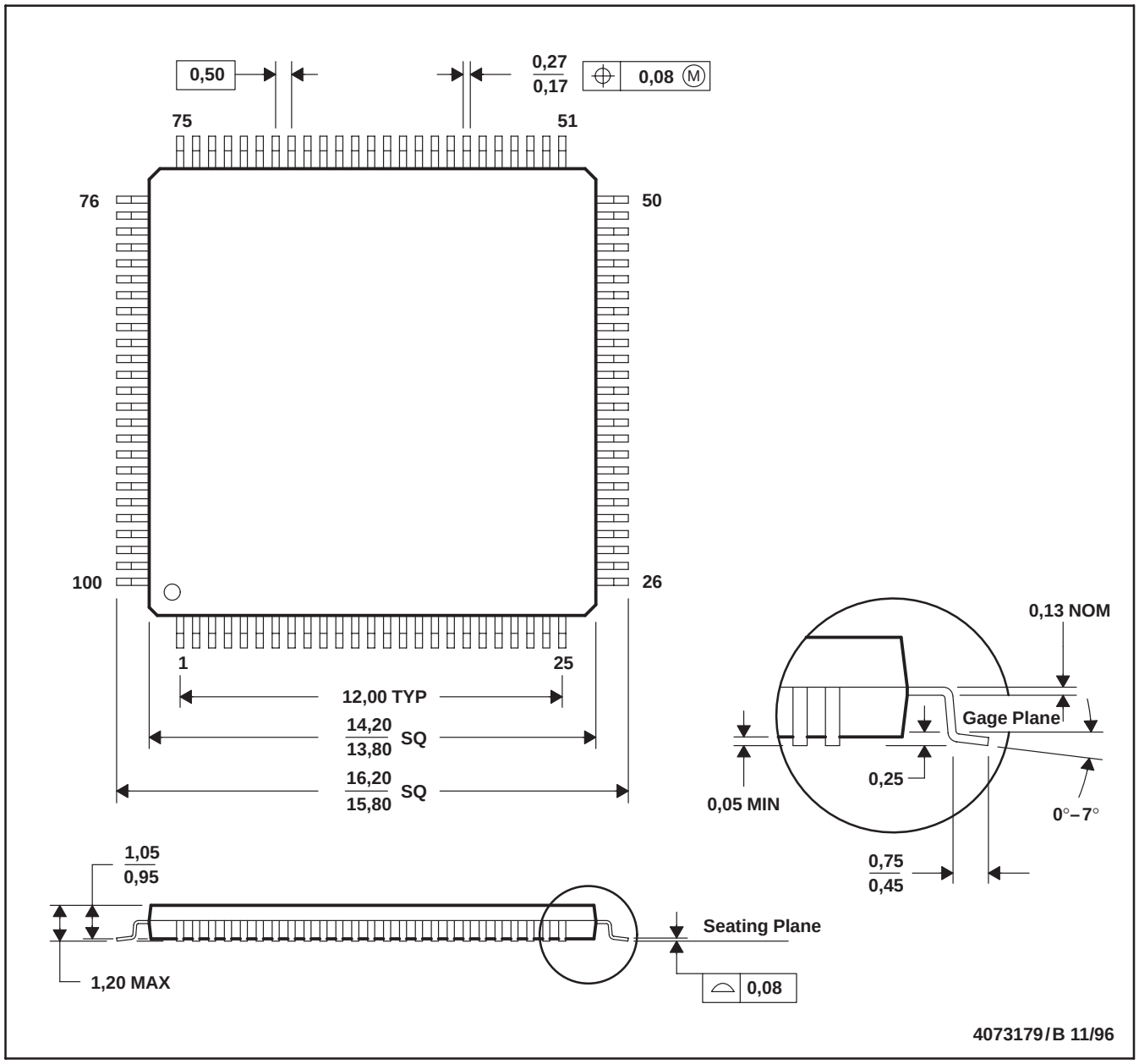


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS3308PZTR	TQFP	PZT	100	1000	350.0	350.0	43.0

MTQF012B – OCTOBER 1994 – REVISED DECEMBER 1996

PZT (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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