TPS7A3401EVM-042 Evaluation Module

This user's guide describes operational use of the TPS7A3401EVM-042 evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS7A3401, negative voltage, low dropout linear regulator (LDO). Included in this user's guide are setup instructions, a schematic diagram, layout and thermal guidelines, and bill of materials.

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1 Introduction

The Texas Instruments TPS7A3401EVM-042 evaluation module helps design engineers to evaluate the operation and performance of the TPS7A3401 negative voltage linear regulator for use in their own circuit application. This particular EVM configuration contains a single linear regulator with internal thermal and current-limit shutdowns, and enable (disable) circuitry in a 3-mm x 5-mm, MSOP-8, thermally enhanced PowerPAD™ package. The regulator, including external components, is capable of delivering up to –200 mA to the load, depending on the input-output power dissipation, at an operating input voltage down to –20 V. The EVM output voltage is adjustable by an external resistor divider from –1.2 V to –17 V. The resistor divider is preset to provide VOUT approximately equal to –15 V.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS7A3401EVM.

2.1 Input/Output Connectors and Jumper Descriptions

JP1 – EN	Output enable. To enable the output, connect a jumper to short ON (pin 1) to EN (center pin 2). To disable the output, connect a jumper to short EN (pin 2) to OFF (pin 3).
J1 – VIN	Negative input power supply voltage connector. Twist the negative lead and positive return lead from the input power supply and keep them as short as possible to minimize lead inductance and EMI transmission. If the supply leads are greater than 6 inches, add additional bulk capacitance between J2 and J4. For example, an additional 47-µF leaded electrolytic capacitor connected from J1 to ground can improve the transient response of the TPS7A3401 while eliminating unwanted ringing on the input due to long wire connections.
J2 – GND	Ground-return connector for the input power supply (positive side connection).
J3 – GND	Output ground-return connector.
J4 – VOUT	Regulated output voltage connector.

2.2 Soldering Guidelines

Any solder re-work to modify the EVM for the purpose of repair or other application reasons must be performed using a hot-air system to avoid damaging the integrated circuit (IC) especially.

2.3 Equipment Interconnect

- Turn off the input power supply after verifying that its output voltage is set to approximately –18 V (–20 V maximum negative) and the current limit is set to approximately 600 mA. Connect the negative voltage lead from input power supply to VIN, at the J1 connector of the EVM. Connect the positive-side return lead from the input power supply to GND at the J2 connector of the EVM.
- Connect a 0-mA to 200-mA load (I_{Load}) between VOUT at the J4 connector and the GND at the J3 connector.
- Disable the output by connecting a jumper at J1 to short the EN (pin 2) to the OFF (pin 3).

3 Operation

- Turn on the input power supply. Verify that the output voltage is near 0 V.
- Enable the output by reconnecting the jumper on J1 to short the EN (pin 2) to the ON (pin 1).
- Vary the load current and VIN voltage as necessary for test purposes

Note that the power dissipation (P_{disp}) across the TPS7A3401 is calculated to be P_{disp} = (VIN – VOUT) × I_{Load}). Be aware that for some applications where the VIN to VOUT difference is large, the maximum junction temperature for the part may be exceeded and that thermal shutdown cycling may occur.

4 Test Results

See the Typical Characteristics section of the TPS7A3401 data sheet (SBVS163) to find characteristic performance.

5 Thermal Guidelines and Layout Recommendations

Thermal management is a key component of design of any power converter and is especially important when the power dissipation in the LDO is high. Use the following formula to approximate the maximum power dissipation for the particular ambient temperature:

$$T_J = T_A + P_d \times \theta_{JA}$$

Where:

T_J is the junction temperature.
T_A is the ambient temperature.
P_d is the power dissipation in the device (watts).
θ_{JA} is the thermal resistance from junction to ambient.

All temperatures are in degrees Celsius. The maximum, continuous, operating junction temperature, T_J, must not be allowed to exceed 125°C. The layout design must use copper trace and plane areas effectively, as thermal sinks, in order not to allow T_J to exceed the maximum rating under all temperature and voltage conditions for a given application.

The layout must consider carefully the thermal design of the printed-circuit board (PCB) for optimal performance over temperature. The MSOP-8 (DGN) package employs a metal PowerPAD™ IC to be soldered to the PCB in order for the PCB to act as a sink to dissipate heat from the LDO. This thermal sink connection, under the LDO, is typically connected to the top layer ground copper, as illustrated in the Figure 2 layer routing for the EVM. It is also a good practice to use plated vias placed in the PowerPAD™ footprint of the PCB to further sink heat to the bottom side copper ground plane. Figure 4 shows that this EVM has nine, 10-mil vias to serve this purpose. The PCB for this TPS7A3401EVM-042 EVM is a two-layer board with 2-oz. copper on top and bottom layers. The DGN package drawing can be found at the Texas Instruments Web site in the product folder for the TPS7A3401 LDO.

Table 1 repeats information from the Dissipation Ratings Table of the TPS7A3401 data sheet (SBVS163) for comparison with the thermal resistance, θ_{JA}, calculated for this EVM layout to show the variation in thermal resistances for given copper areas. The High-K value is determined using a standard JEDEC high-k (2s2p) board having dimensions of 3-inch x 3-inch with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

Table 1. Thermal Resistance, θ_{JA}, and Maximum Power Dissipation

Board	Package	θ_{JA}	Maximum Dissipation Without Derating (T_A = 25°C)	Maximum Dissipation Without Derating (T_A = 70°C)
High-K	DGN	55.1°C/W	1.83 W	1.08 W
TPS7A3401EVM-042	DGN	49.0°C/W	2.04 W	1.12 W

The thermal resistance for the TPS7A3401EVM-042, θ_{JA}, is the measured value for this particular layout scheme. The maximum power dissipation is proportional to the copper volume connected to the package.

6 Board Layout

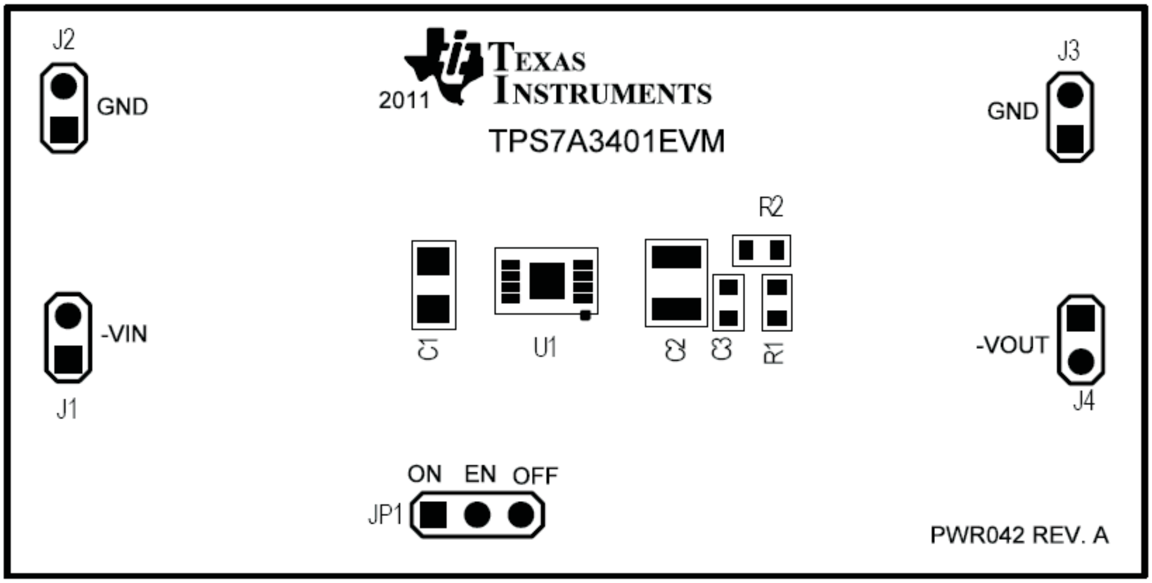

Figure 1. Top Assembly Layer

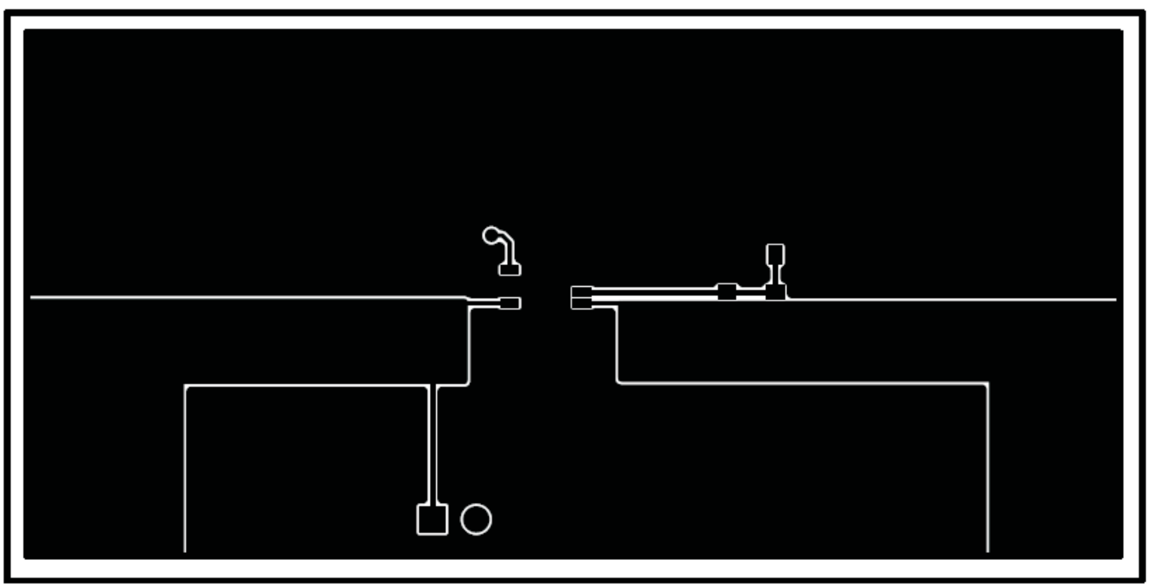

Figure 2. Top Layer Routing

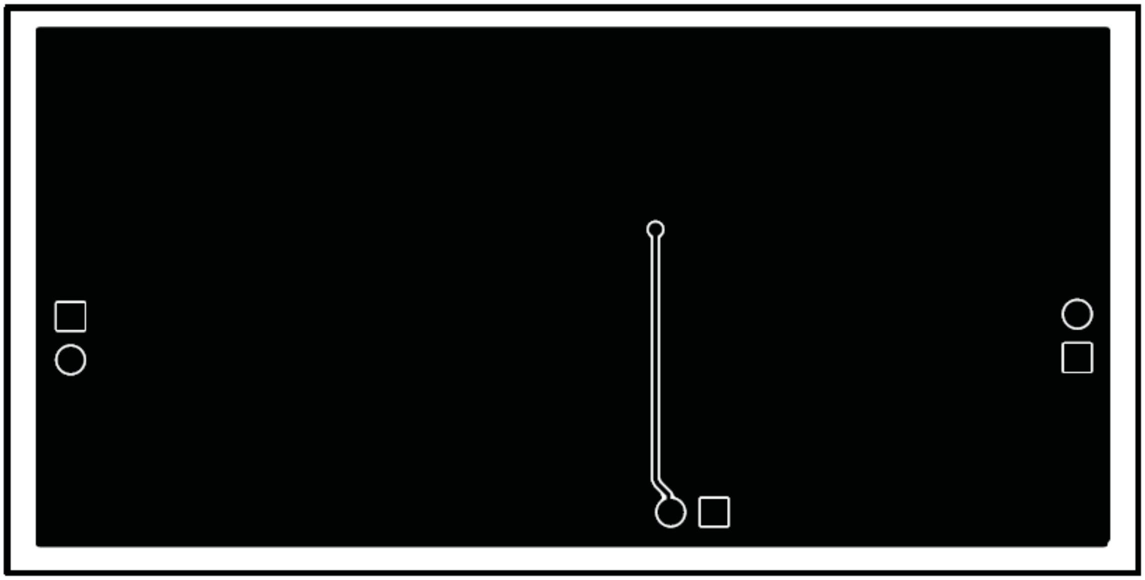

Figure 3. Bottom Layer Routing

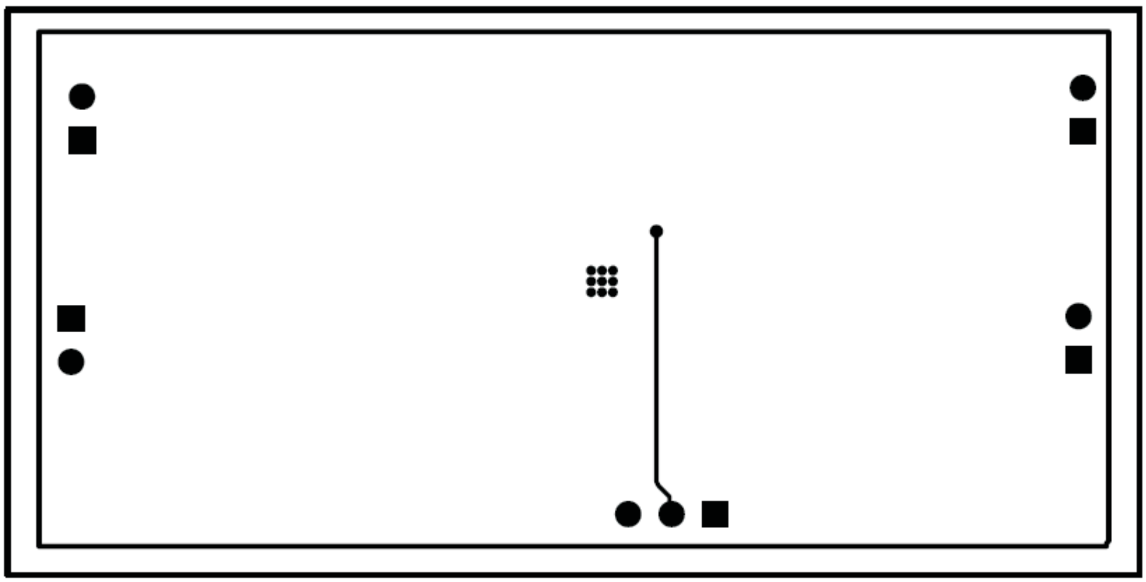

Figure 4. Bottom Assembly Layer

7 Schematic and Bill of Materials

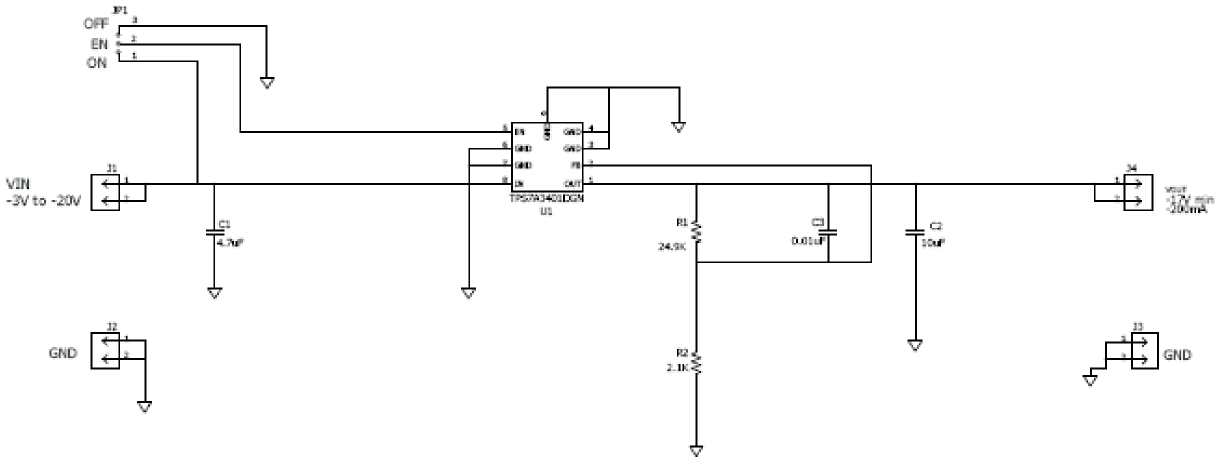

Figure 5. TPS7A3401EVM-042 Schematic

Table 2. TPS7A4001EVM-709 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	4.7 µF	Capacitor, Ceramic, 25V, X7R, 20%	1206	STD	STD
1	C3	0.01 µF	Capacitor, Ceramic, 25V, X5R, 20%	0603	STD	STD
1	C4	10 µF	Capacitor, Ceramic, 25V, X5R, 20%	1210	STD	STD
4	J1-2, J4-5	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	JP1	PEC03SAAN	Header, Male 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
1	R1	24.9 K	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R2	2.1 K	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	U1	TPS7A3401DGN	IC, –20V, –200mA, Low-Noise Voltage Regulator	HTSSOP	TPS7A3401DGN	TI
1			Shunt, Black	100-mil	929950-00	3M
1	–	PWR042	1.3 x 2.8 inch 2 layer, PCB		PWR042	Any

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of -22 V to 0.3 V and the output voltage range of -20 V to -3 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125° C. The EVM is designed to operate properly with certain components above 125° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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