CSD13383F4 12 V N-Channel FemtoFET™ MOSFET

1 Features

- Low On-Resistance
- Ultra Low Q_g and Q_{gd}
- Ultra-Small Footprint (0402 Case Size)
  - 1.0 mm × 0.6 mm
- Low Profile
  - 0.35 mm Height
- Integrated ESD Protection Diode
  - Rated >2 kV HBM
  - Rated >2 kV CDM
- Lead and Halogen Free
- RoHS Compliant

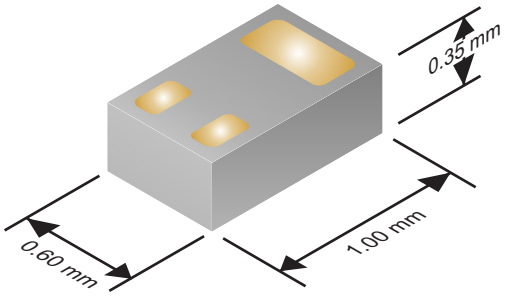
2 Applications

- Optimized for Load Switch Applications
- Optimized for General Purpose Switching Applications
- Single-Cell Battery Applications
- Handheld and Mobile Applications

3 Description

This 37 mΩ, 12 V N-channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.

Typical Part Dimensions



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	12		V
Q_g	Gate Charge Total (4.5 V)	2.0		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.6		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 2.5 V	53	mΩ
		V_{GS} = 4.5 V	37	
$V_{GS(th)}$	Threshold Voltage	1.0		V

Ordering Information[1]

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD13383F4	3000	7-Inch Reel	Femto (0402) 1.0 mm × 0.6 mm SMD Lead Less	Tape and Reel
CSD13383F4T	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

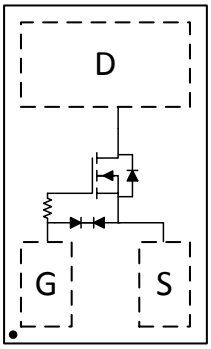
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	±10	V
I_D	Continuous Drain Current[1]	2.9	A
I_{DM}	Pulsed Drain Current[1][2]	18.5	A
I_G	Continuous Gate Clamp Current	25	mA
	Pulsed Gate Clamp Current[1][2]	250	
P_D	Power Dissipation	500	mW
ESD Rating	Human Body Model (HBM)	2	kV
	Charged Device Model (CDM)	2	kV
T_J, T_{stg}	Operating Junction Temperature Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 6.7, L = 0.1 mH, R_G = 25 Ω	2.2	mJ

(1) Typical $R_{\theta JA}$ = 250°C/W.

(2) Pulse duration ≤100 μs, duty cycle ≤1%.

Top View



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2016) to Revision B **Page**

- Changed I_{DM} value From: 27 A To: 18.5 A in the *Absolute Maximum Ratings* table. ... 1
- Updated Figure 1. ... 4
- Updated Figure 10 using Typ $R_{\theta JA}$ = 250°C/W. ... 5
- Updated all mechanical drawings, increased the size of the pads in the *Recommended Stencil Pattern* section. ... 8

Changes from Original (December 2014) to Revision A **Page**

- Changed the $t_{d(on)}$ value From: 39 ns To: 46 ns in the *Electrical Characteristics* table. ... 3
- Changed the t_r value From: 123 ns To: 122 ns in the *Electrical Characteristics* table. ... 3
- Changed the $t_{d(off)}$ value From: 96 ns To: 250 ns in the *Electrical Characteristics* table. ... 3
- Changed the t_f value From: 315 ns To: 290 ns in the *Electrical Characteristics* table. ... 3
- Added *Community Resources* section. ... 7

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5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 µA	12			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 9.6 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 10 V			10	µA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	0.70	1.00	1.25	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 2.5 V, I_{DS} = 0.5 A		53	65	mΩ
		V_{GS} = 4.5 V, I_{DS} = 0.5 A		37	44	mΩ
g_{fs}	Transconductance	V_{DS} = 6 V, I_{DS} = 0.5 A		5.4		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 6 V, f = 1 MHz		224	291	pF
C_{oss}	Output capacitance			68	88	pF
C_{rss}	Reverse transfer capacitance			47	61	pF
R_G	Series gate resistance			240		Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 6 V, I_{DS} = 0.5 A		2.0	2.6	nC
Q_{gd}	Gate charge gate-to-drain			0.6		nC
Q_{gs}	Gate charge gate-to-source			0.4		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.1		nC
Q_{oss}	Output charge	V_{DS} = 6 V, V_{GS} = 0 V		0.9		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 6 V, V_{GS} = 4.5 V, I_{DS} = 0.5 A, R_G = 2 Ω		46		ns
t_r	Rise time			122		ns
$t_{d(off)}$	Turn off delay time			250		ns
t_f	Fall time			290		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 0.5 A, V_{GS} = 0 V		0.7	1.0	V

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)		90		°C/W
	Junction-to-ambient thermal resistance(2)		250		

(1) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

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5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

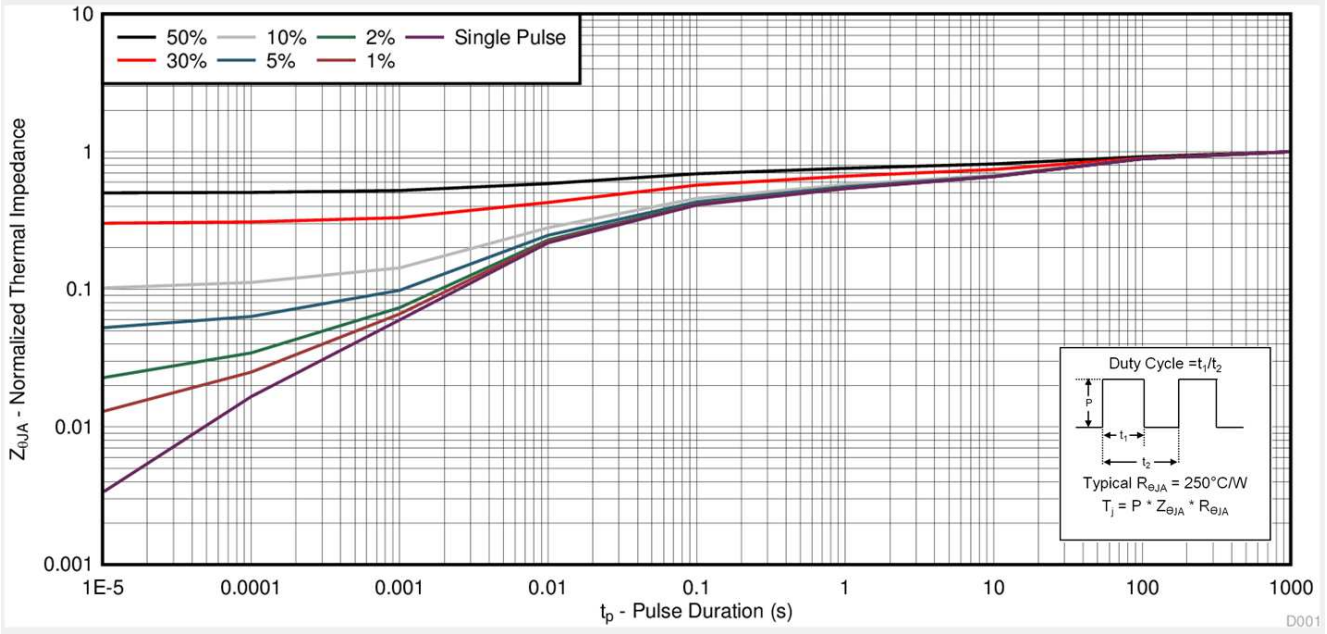


Figure 1. Transient Thermal Impedance

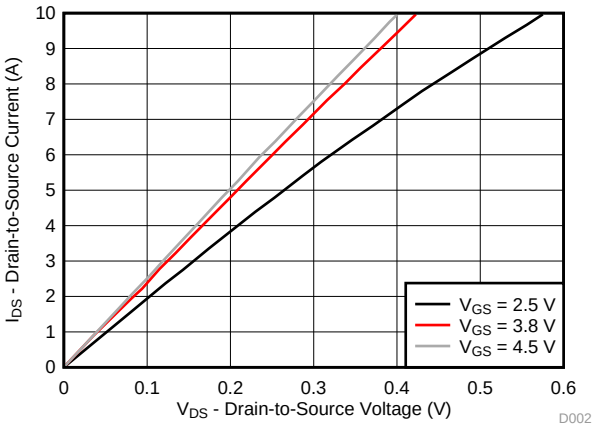


Figure 2. Saturation Characteristics

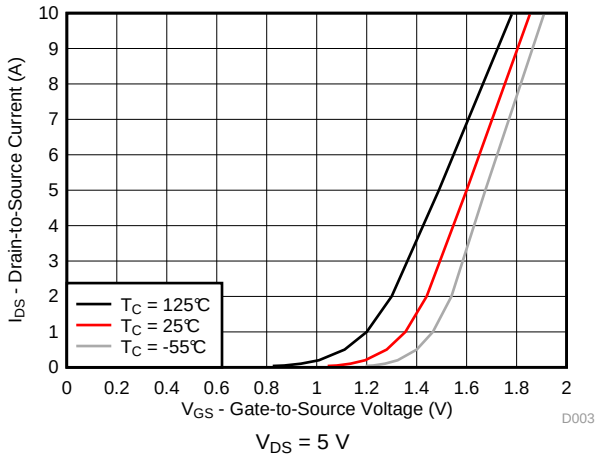


Figure 3. Transfer Characteristics

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

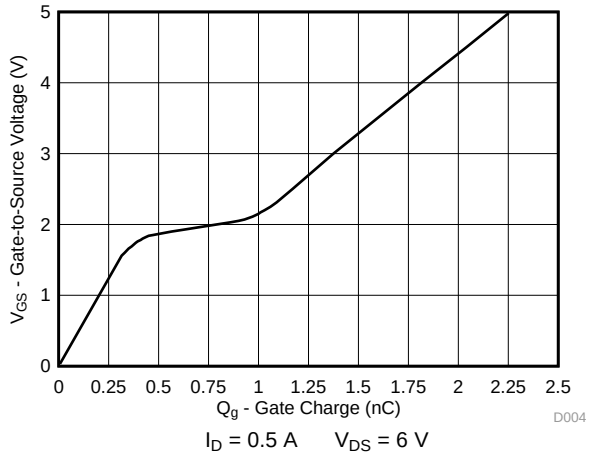


Figure 4. Gate Charge

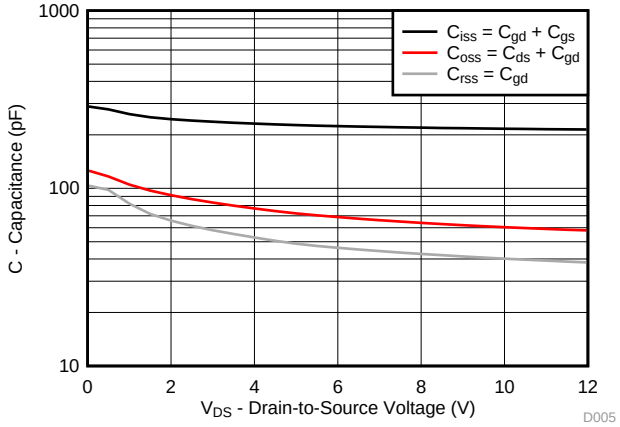


Figure 5. Capacitance

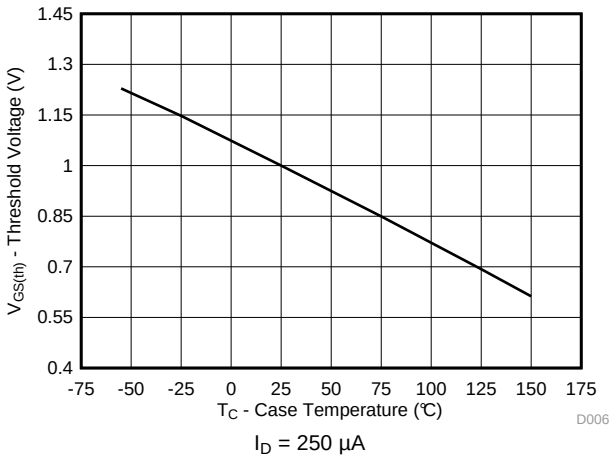


Figure 6. Threshold Voltage vs Temperature

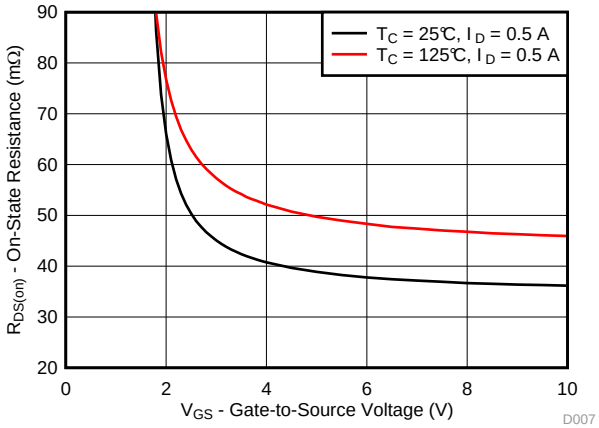


Figure 7. On-State Resistance vs Gate-to-Source Voltage

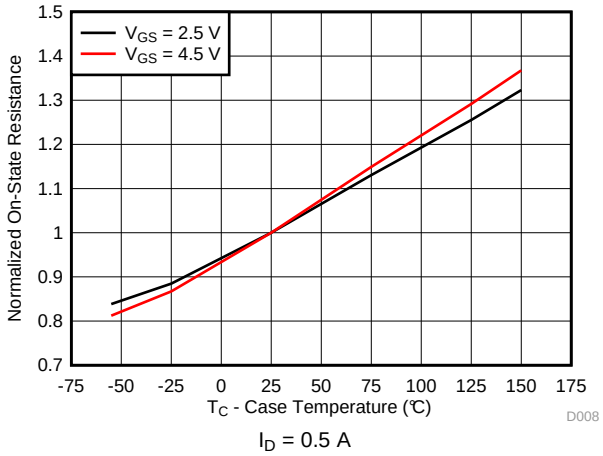


Figure 8. Normalized On-State Resistance vs Temperature

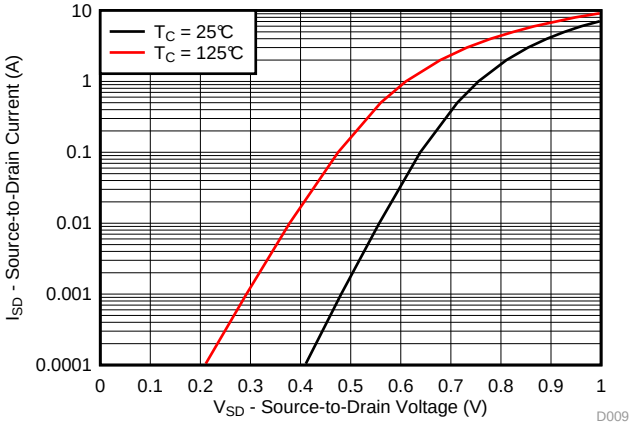


Figure 9. Typical Diode Forward Voltage

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

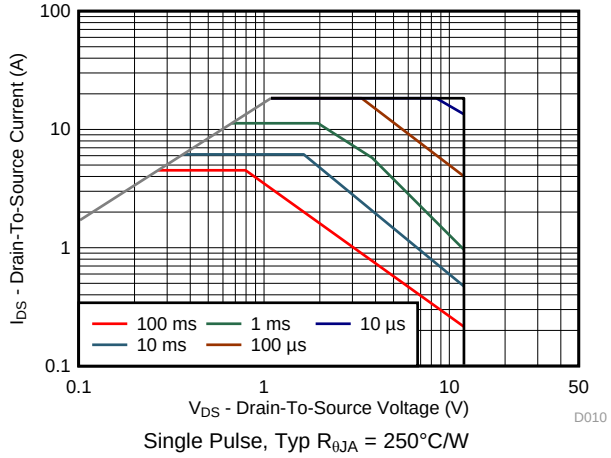


Figure 10. Maximum Safe Operating Area (SOA)

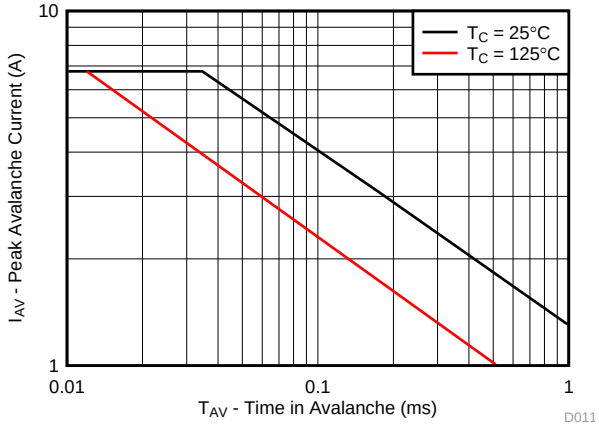


Figure 11. Single Pulse Unclamped Inductive Switching

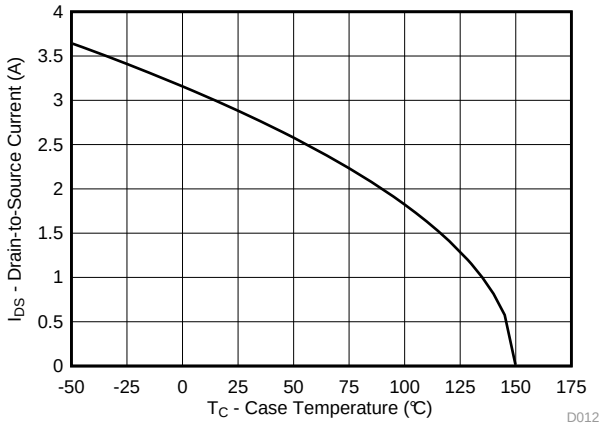


Figure 12. Maximum Drain Current vs Temperature

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6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

FemtoFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

SLYZ022 — *TI Glossary*.

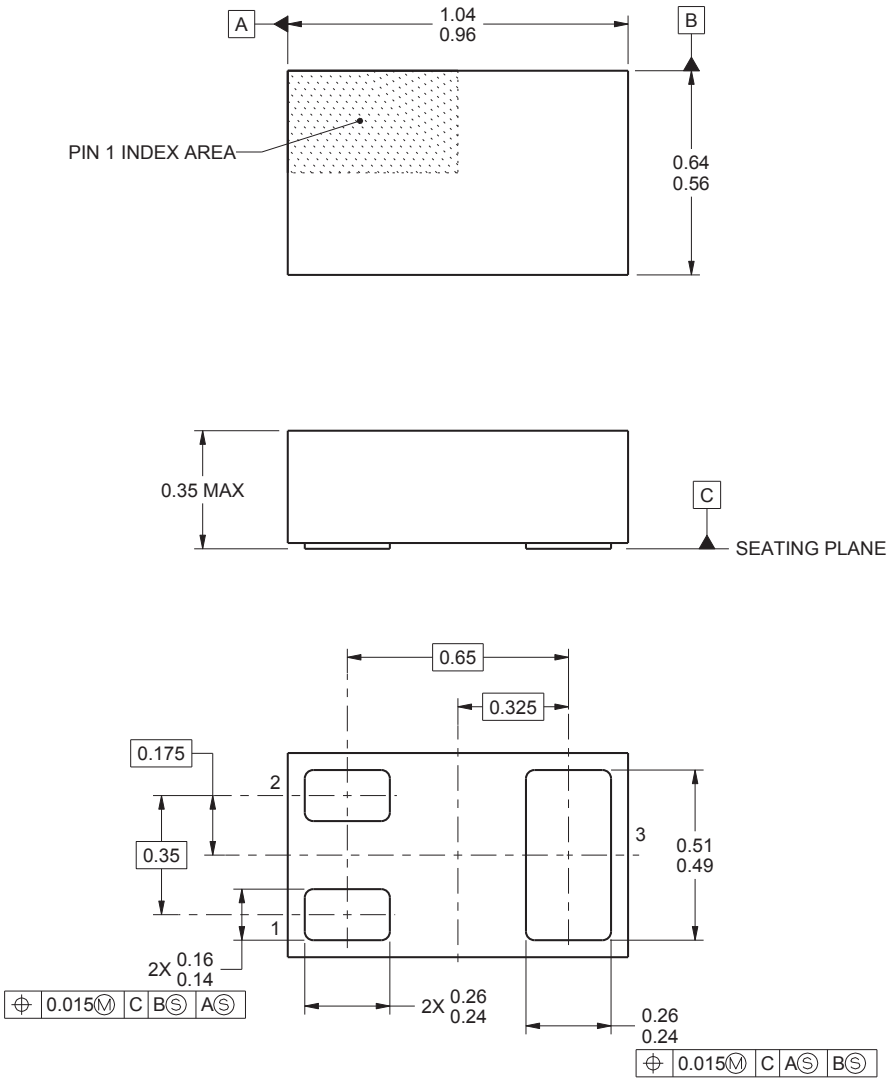
This glossary lists and explains terms, acronyms, and definitions.

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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



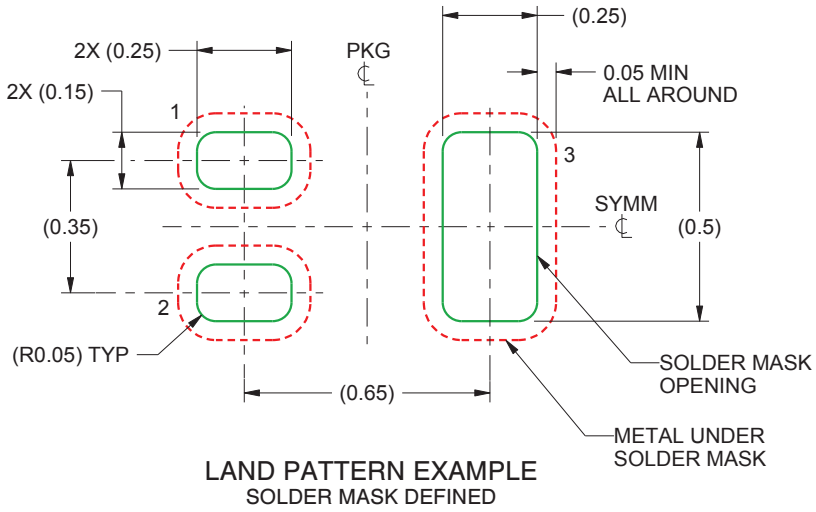
(1) All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

(2) This drawing is subject to change without notice.

(3) This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device data sheet or contact a local TI representative.

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7.2 Recommended Minimum PCB Layout

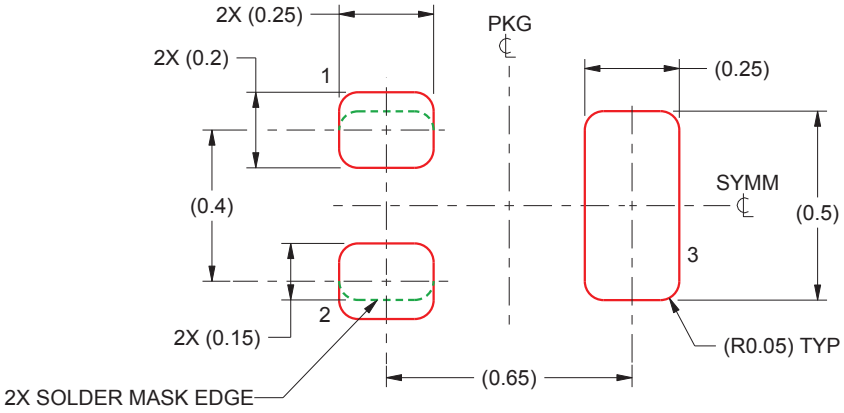


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED

(1) All dimensions are in millimeters.

(2) For more information, see *QFN/SON PCB Attachment* (SLUA271).

7.3 Recommended Stencil Pattern



SOLDER PASTE EXAMPLE

(1) All dimensions are in millimeters.

(2) Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13383F4	ACTIVE	PICOSTAR	YJC	3	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM		GC	Samples
CSD13383F4T	ACTIVE	PICOSTAR	YJC	3	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	GC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

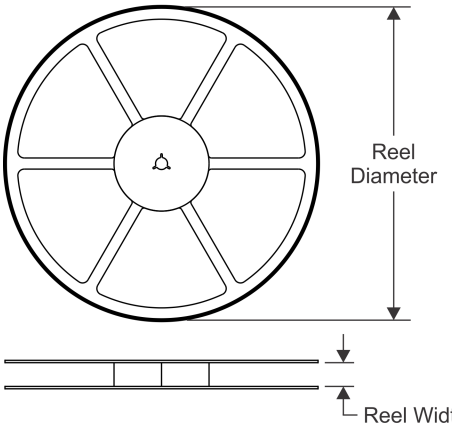
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

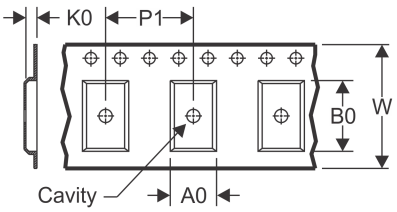
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

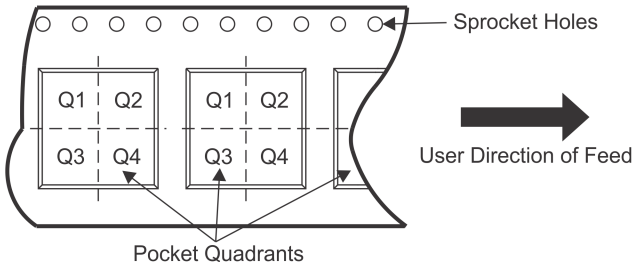


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

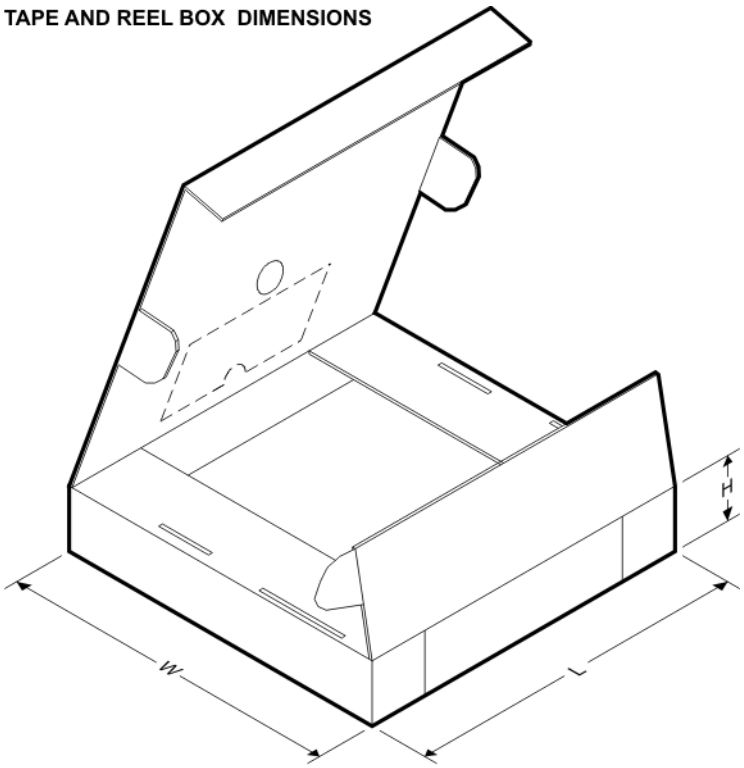
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD13383F4	PICOSTAR	YJC	3	3000	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD13383F4	PICOSTAR	YJC	3	3000	178.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD13383F4T	PICOSTAR	YJC	3	250	178.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD13383F4T	PICOSTAR	YJC	3	250	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD13383F4	PICOSTAR	YJC	3	3000	182.0	182.0	20.0
CSD13383F4	PICOSTAR	YJC	3	3000	220.0	220.0	35.0
CSD13383F4T	PICOSTAR	YJC	3	250	220.0	220.0	35.0
CSD13383F4T	PICOSTAR	YJC	3	250	182.0	182.0	20.0

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