USB Charging Port Controller and Power Switch with Load Detection

1 Features

- Qualified for Automotive Application
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C5
- D+/D– CDP/DCP Modes per USB Battery Charging Specification 1.2
- D+/D– Shorted Mode per Chinese Telecommunication Industry Standard YD/T 1591-2009
- Supports non-BC1.2 Charging Modes by Automatic Selection
  - D+/D– Divider Modes 2V/2.7V and 2.7/2V
- Supports Sleep-Mode Charging and Low Speed Mouse/Keyboard Wake Up
- Load Detection for Power Supply Control in S4/S5 Charging and Port Power Management in all Charge Modes
- Compatible with USB 2.0 and 3.0 Power Switch requirements
- Integrated 73-mΩ (typ) High-Side MOSFET
- Adjustable Current-Limit up to 3 A (Typical)
- Operating Range: 4.5 V to 5.5 V
- Max Device Current
  - 2 µA When Device Disabled
  - 260 µA When Device Enabled
- Drop-In and BOM Compatible with TPS2543
- Available in 16-Pin QFN (3x3) Package

2 Applications

- USB Ports (Host and Hubs)
- Notebook and Desktop PCs
- Automotive Infotainment System

3 Description

The TPS2543-Q1 is a USB charging port controller and power switch with an integrated USB 2.0 high-speed data line (D+/D–) switch. TPS2543-Q1 provides the electrical signatures on D+/D– lines to support charging schemes listed under device feature section. TI tests charging of popular mobile phones, tablets and media devices with the TPS2543-Q1 to ensure compatibility with both BC1.2 compliant and non-BC1.2 compliant devices.

In addition to charging popular devices, the TPS2543-Q1 also supports two distinct power management features, namely, power wake and port power management (PPM) via the $\overline{\text{STATUS}}$ pin. Power wake allows for power supply control in S4/S5 charging and PPM the ability to manage port power in a multi-port applications. Additionally, system wake up (from S3) with a mouse/keyboard (low speed only) is also supported in the TPS2543-Q1.

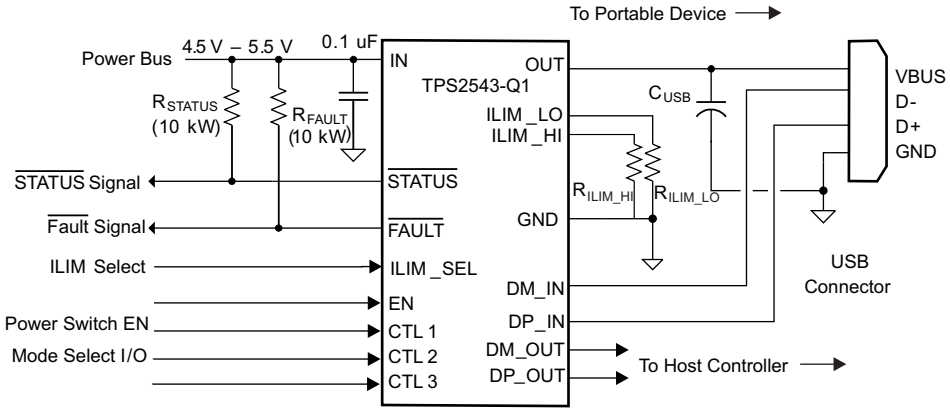
The TPS2543-Q1 73-mΩ power-distribution switch is intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. Two programmable current thresholds provide flexibility for setting current limits and load detect thresholds.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2543-Q1	WQFN (16)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



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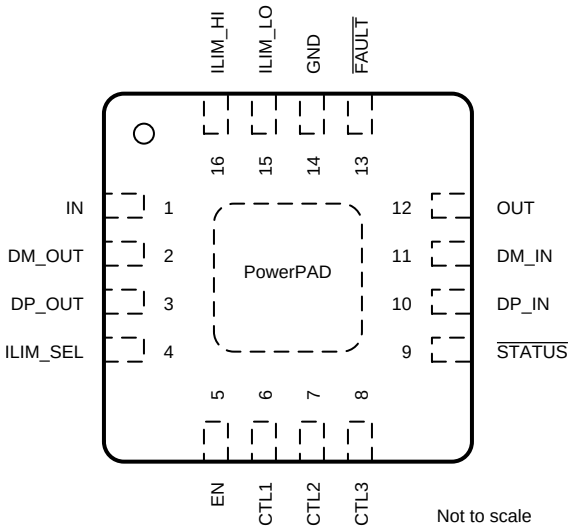
4 Revision History

Changes from Original (March 2013) to Revision A **Page**

- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Feature* : "UL Listed and CB File No. E169910" ... 1
- Changed ILIM_LO+60mA for 200 ms To: ILIM_LO + 75 mA for 200 ms and ILIM_LO+10mA for 3s To: ILIM_LO + 25 mA for 3s in section *PPM Details* ... 24
- Changed text From: "it switches to Divider2 scheme" To: "it discharges and then switches to Divider2 scheme." in section *DCP Auto Mode* ... 26
- Changed text From: "it will revert to Divider1 scheme" To: "it performs OUT discharge and will revert to Divider1 scheme" in section *DCP Auto Mode* ... 26
- Changed the description of S0 and S3 From: ILIM_LO + 60 mA thresholds To: ILIM_LO + 75 mA thresholds in *Table 2* 27

5 Pin Configuration and Functions

RTE Package
16 Pin (WQFN)
Top View



Pin Functions

NO.	NAME	TYPE(1)	DESCRIPTION
1	IN	P	Input voltage and supply voltage; connect 0.1 μF or greater ceramic capacitor from IN to GND as close to the device as possible
2	DM_OUT	I/O	D– data line to USB host controller
3	DP_OUT	I/O	D+ data line to USB host controller
4	ILIM_SEL	I	Logic-level input signal used to control the charging mode, current limit threshold, and load detection; see the control truth table. Can be tied directly to IN or GND without pull-up or pull-down resistor.
5	EN	I	Logic-level input for turning the power switch and the signal switches on/off; logic low turns off the signal and power switches and holds OUT in discharge. Can be tied directly to IN or GND without pull-up or pull-down resistor.
6	CTL1	I	Logic-level inputs used to control the charging mode and the signal switches; see the control truth table. Can be tied directly to IN or GND without pull-up or pull-down resistor.
7	CTL2	I	
8	CTL3	I	
9	$\overline{\text{STATUS}}$	O	Active-low open-drain output, asserted in load detection conditions
10	DP_IN	I/O	D+ data line to downstream connector
11	DM_IN	I/O	D– data line to downstream connector
12	OUT	P	Power-switch output
13	$\overline{\text{FAULT}}$	O	Active-low open-drain output, asserted during over-temperature or current limit conditions
14	GND	P	Ground connection
15	ILIM_LO	I	External resistor connection used to set the low current-limit threshold and the load detection current threshold. A resistor to ILIM_LO is optional; see the *Current-Limit Settings* section.
16	ILIM_HI	I	External resistor connection used to set the high current-limit threshold
NA	PowerPAD™		Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect to GND plane.

(1) G = Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range	IN, EN, ILIM_LO, ILIM_HI, $\overline{\text{FAULT}}$, $\overline{\text{STATUS}}$, ILIM_SEL, CTL1, CTL2, CTL3, OUT	–0.3	7	V
	IN to OUT	–7	7	
	DP_IN, DM_IN, DP_OUT, DM_OUT	–0.3 to (IN + 0.3)	5.7	
Input clamp current	DP_IN, DM_IN, DP_OUT, DM_OUT	–20	20	mA
Continuous current in SDP or CDP mode	DP_IN to DP_OUT or DM_IN to DM_OUT	–100	100	mA
Continuous current in BC1.2 DCP mode	DP_IN to DM_IN	–50	50	mA
Continuous output current	OUT	Internally limited		
Continuous output sink current	$\overline{\text{FAULT}}$, $\overline{\text{STATUS}}$		25	mA
Continuous output source current	ILIM_LO, ILIM_HI	Internally limited		mA
Operating junction temperature, T_J		–40	Internally limited	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000(2)	V
		Charged-device model (CDM), per AEC Q100-011	±500(3)	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) The passing level per AEC-Q100 Classification H2.
(3) The passing level per AEC-Q100 Classification C5.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage, IN	4.5		5.5	V
	Input voltage, logic-level inputs, EN, CTL1, CTL2, CTL3, ILIM_SEL	0		5.5	V
	Input voltage, data line inputs, DP_IN, DM_IN, DP_OUT, DM_OUT	0		V_{IN}	V
V_{IH}	High-level input voltage, EN, CTL1, CTL2, CTL3, ILIM_SEL	1.8			V
V_{IL}	Low-level input voltage, EN, CTL1, CTL2, CTL3, ILIM_SEL			0.8	V
	Continuous current, data line inputs, SDP or CDP mode, DP_IN to DP_OUT, DM_IN to DM_OUT			±30	mA
	Continuous current, data line inputs, BC1.2 DCP mode, DP_IN to DM_IN			±15	mA
I_{OUT}	Continuous output current, OUT	0		2.5	A
	Continuous output sink current, $\overline{\text{FAULT}}$, $\overline{\text{STATUS}}$	0		10	mA
R_{ILIM_XX}	Current-limit set resistors	16.9		750	kΩ
T_J	Operating virtual junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS2543-Q1 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise noted: $-40 \le T_J \le 125°C$, $4.5V \le V_{IN} \le 5.5$ V, $V_{EN} = V_{IN}$, $V_{ILIM\_SEL} = V_{IN}$, $V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN}$. $R_{\overline{FAULT}} = R_{\overline{STATUS}} = 10$ kΩ, $R_{ILIM\_HI} = 20$ kΩ, $R_{ILIM\_LO} = 80.6$ kΩ. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH						
$R_{DS(on)}$	On resistance[1]	$T_J = 25°C$, $I_{OUT} = 2$ A		73	84	mΩ
		$-40°C \le T_J \le 85°C$, $I_{OUT} = 2$ A		73	105	
		$-40°C \le T_J \le 125°C$, $I_{OUT} = 2$ A		73	120	
t_r	OUT voltage rise time	$V_{IN} = 5$ V, $C_L = 1$ µF, $R_L = 100$ Ω (see Figure 23 and Figure 24)	0.7	1.0	1.60	ms
t_f	OUT voltage fall time		0.2	0.35	0.5	
t_{on}	OUT voltage turn-on time	$V_{IN} = 5$V, $C_L = 1$ µF, $R_L = 100$ Ω (see Figure 23 and Figure 25)		2.7	4	ms
t_{off}	OUT voltage turn-off time			1.7	3	
I_{REV}	Reverse leakage current	$V_{OUT} = 5.5$ V, $V_{IN} = V_{EN} = 0$ V, $-40 \le T_J \le 85°C$, Measure I_{OUT}			2	µA
DISCHARGE						
R_{DCHG}	OUT discharge resistance	$V_{OUT} = 4$ V, $V_{EN} = 0$ V	400	500	630	Ω
t_{DCHG}	OUT discharge hold time	Time $V_{OUT} < 0.7$ V (see Figure 26)	205	310	450	ms
EN, ILIMSEL, CTL1, CTL2, CTL3 INPUTS						
	Input pin rising logic threshold voltage		1	1.35	1.70	V
	Input pin falling logic threshold voltage		0.85	1.15	1.45	
	Hysteresis[2]			200		mV
	Input current	Pin voltage = 0 V or 5.5 V	–0.5		0.5	µA
ILIMSEL CURRENT LIMIT						
I_{OS}	OUT short circuit current limit[1]	$V_{ILIM\_SEL} = 0$ V, $R_{ILIM\_LO} = 210$ kΩ	205	240	275	mA
		$V_{ILIM\_SEL} = 0$ V, $R_{ILIM\_LO} = 80.6$ kΩ	575	625	680	
		$V_{ILIM\_SEL} = 0$ V, $R_{ILIM\_LO} = 22.1$ kΩ	2120	2275	2430	
		$V_{ILIM\_SEL} = V_{IN}$, $R_{ILIM\_HI} = 20$ kΩ	2340	2510	2685	
		$V_{ILIM\_SEL} = V_{IN}$, $R_{ILIM\_HI} = 16.9$ kΩ	2770	2970	3170	
t_{IOS}	Response time to OUT short-circuit[2]	$V_{IN} = 5.0$ V, $R = 0.1$Ω, lead length = 2 inches (see Figure 27)		1.5		µs

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; Thermal effects must be taken into account separately.
(2) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

Electrical Characteristics (continued)

Unless otherwise noted: –40 ≤ T_J ≤ 125°C, 4.5V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN}, V_{ILIM_SEL} = V_{IN}, V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN}. R $\overline{FAULT}$ = R $\overline{STATUS}$ = 10 kΩ, R_{ILIM_HI} = 20 kΩ, R_{ILIM_LO} = 80.6 kΩ. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN_OFF}	Disabled IN supply current	V_{EN} = 0 V, V_{OUT} = 0 V, –40 ≤ T_J ≤ 85°C		0.1	2	µA
I_{IN_ON}	Enabled IN supply current	V_{CTL1} = V_{CTL2} = V_{IN}, V_{CTL3} = 0 V or V_{IN}, V_{ILIM_SEL} = 0 V		155	210	µA
		V_{CTL1} = V_{CTL2} = V_{IN}, V_{CTL3} = 0V, V_{ILIM_SEL} = V_{IN}		175	230	
		V_{CTL1} = V_{CTL2} = V_{IN}, V_{CTL3} = VIN, V_{ILIM_SEL} = V_{IN}		185	240	
		V_{CTL1} = 0V, V_{CTL2} = V_{CTL3} = V_{IN}		205	260	
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	IN rising UVLO threshold voltage		3.9	4.1	4.3	V
	Hysteresis (2)			100		mV
$\overline{FAULT}$						
	Output low voltage	I $\overline{FAULT}$ = 1 mA			100	mV
	Off-state leakage	V $\overline{FAULT}$ = 5.5 V			1	µA
	Over current $\overline{FAULT}$ rising and falling deglitch		5	8.2	12	ms
$\overline{STATUS}$						
	Output low voltage	I $\overline{STATUS}$ = 1 mA			100	mV
	Off-state leakage	V $\overline{STATUS}$ = 5.5 V			1	µA
THERMAL SHUTDOWN						
	Thermal shutdown threshold		155			°C
	Thermal shutdown threshold in current-limit		135			
	Hysteresis (2)			20		

6.6 Electrical Characteristics, High-Bandwidth Switch

Unless otherwise noted: –40 ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN}, V_{ILIM_SEL} = V_{IN}, V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN}. R $\overline{FAULT}$ = R $\overline{STATUS}$ = 10 kΩ, R_{ILIM_HI} = 20 kΩ, R_{ILIM_LO} = 80.6 kΩ, Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-BANDWIDTH ANALOG SWITCH						
	DP/DM switch on resistance	V_{DP/DM_OUT} = 0 V, I_{DP/DM_IN} = 30 mA		2	4	Ω
		V_{DP/DM_OUT} = 2.4 V, I_{DP/DM_IN} = –15 mA		3	6	
	Switch resistance mismatch between DP / DM channels	V_{DP/DM_OUT} = 0 V, I_{DP/DM_IN} = 30 mA		0.05	0.15	Ω
		V_{DP/DM_OUT} = 2.4 V, I_{DP/DM_IN} = –15 mA		0.05	0.15	
	DP/DM switch off-state capacitance(1), (2)	V_{EN} = 0 V, V_{DP/DM_IN} = 0.3 V, V_{ac} = 0.6 V_{pk-pk}, f = 1 MHz		3		pF
	DP/DM switch on-state capacitance(3), (2)	V_{DP/DM_IN} = 0.3 V, V_{ac} = 0.6 V_{pk-pk}, f = 1 MHz		5.4		pF
O_{IRR}	Off-state isolation(2)	V_{EN} = 0 V, f = 250 MHz		33		dB
X_{TALK}	On-state cross channel isolation(2)	f = 250 MHz		52		dB
	Off state leakage current	V_{EN} = 0 V, V_{DP/DM_IN} = 3.6 V, V_{DP/DM_OUT} = 0 V, measure I_{DP/DM_OUT}		0.1	1.5	µA
BW	Bandwidth (–3dB)(2)	R_L = 50 Ω		2.6		GHz
t_{pd}	Propagation delay(2)			0.25		ns
t_{SK}	Skew between opposite transitions of the same port (t_{PHL} – t_{PLH})(2)			0.1		ns

(1) The resistance in series with the parasitic capacitance to GND is typically 250 Ω.
(2) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.
(3) The resistance in series with the parasitic capacitance to GND is typically 150 Ω

6.7 Electrical Characteristics, Charging Controller

Unless otherwise noted: –40 ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN}, V_{ILIM_SEL} = V_{IN}, V_{CTL1} = 0 V, V_{CTL2} = V_{CTL3} = V_{IN}. R $\overline{FAULT}$ = R $\overline{STATUS}$ = 10 kΩ, R_{ILIM_HI} = 20 kΩ, R_{ILIM_LO} = 80.6 kΩ, Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SHORTED MODE (BC1.2 DCP)		**VCTL1 = VIN, VCTL2 = VCTL3 = 0V**				
	DP_IN / DM_IN shorting resistance			125	200	Ω
DIVIDER1 MODE						
	DP_IN Divider1 output voltage		1.9	2.0	2.1	V
	DM_IN Divider1 output voltage		2.57	2.7	2.84	V
	DP_IN output impedance		8	10.5	12.5	kΩ
	DM_IN output impedance		8	10.5	12.5	kΩ
DIVIDER2 MODE		**IOUT = 1A**				
	DP_IN Divider2 output voltage		2.57	2.7	2.84	V
	DM_IN Divider2 output voltage		1.9	2.0	2.1	V
	DP_IN output impedance		8	10.5	12.5	kΩ
	DM_IN output impedance		8	10.5	12.5	kΩ
CHARGING DOWNSTREAM PORT		**VCTL1 = VCTL2 = VCTL3 = VIN**				
V_{DM_SRC}	DM_IN CDP output voltage	V_{DP_IN} = 0.6 V, –250 µA < I_{DM_IN} < 0 µA	0.5	0.6	0.7	V
V_{DAT_REF}	DP_IN rising lower window threshold for V_{DM_SRC} activation		0.25		0.4	V
	Hysteresis(1)			50		mV
V_{LGC_SRC}	DP_IN rising upper window threshold for V_{DM_SRC} de-activation		0.8		1	V
	hysteresis(1)			100		mV
I_{DP_SINK}	DP_IN sink current	V_{DP_IN} = 0.6 V	40	70	100	µA
LOAD DETECT – NON POWER WAKE		**VCTL1 = VCTL2 = VCTL3 = VIN**				
I_{LD}	IOUT rising load detect current threshold		635	700	765	mA
	hysteresis(1)			50		mA
t_{LD_SET}	Load detect set time		140	200	275	ms
	Load detect reset time		1.9	3	4.2	s
LOAD DETECT – POWER WAKE		**VCTL1 = VCTL2 = 0V, VCTL3 = VIN**				
I_{OS_PW}	Power wake short circuit current limit		32	55	78	mA
	I_{OUT} falling power wake reset current detection threshold		23	45	67	mA
	Reset current hysteresis(1)			5		mA
	Power wake reset time		10.7	15	20.6	s

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

6.8 Typical Characteristics

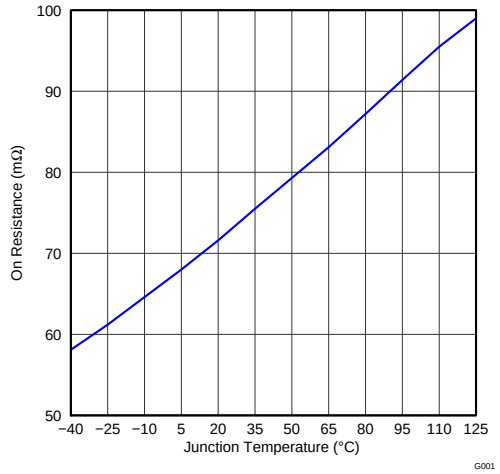


Figure 1. Power Switch On Resistance vs Temperature

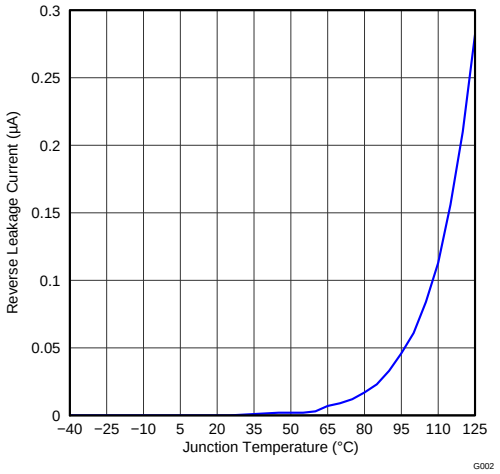


Figure 2. Reverse Leakage Current vs Temperature

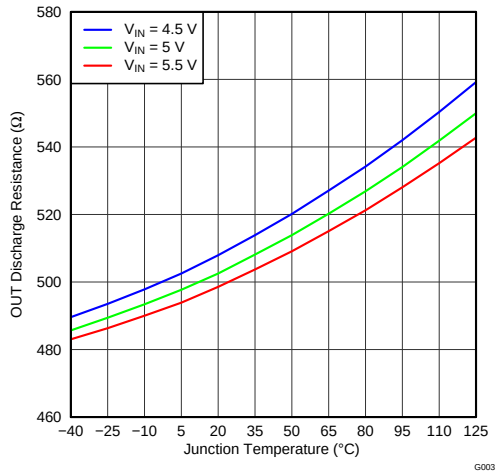


Figure 3. Out Discharge Resistance vs Temperature

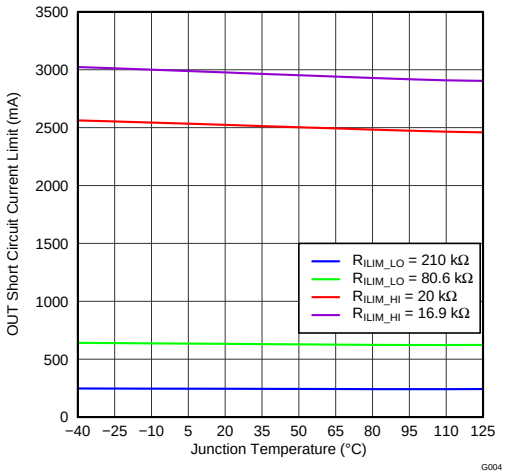


Figure 4. Out Short Circuit Current Limit vs Temperature

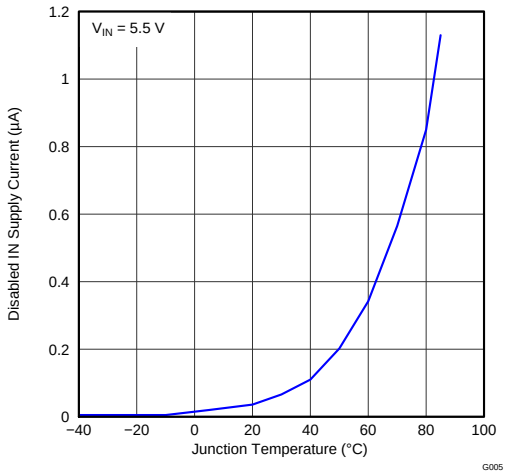


Figure 5. Disabled In Supply Current vs Temperature

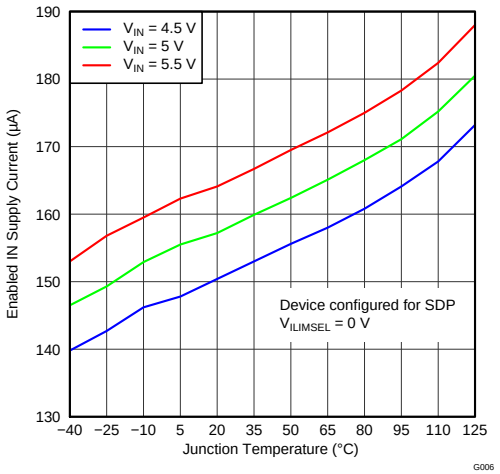


Figure 6. Enabled In Supply Current - SDP vs Temperature

Typical Characteristics (continued)

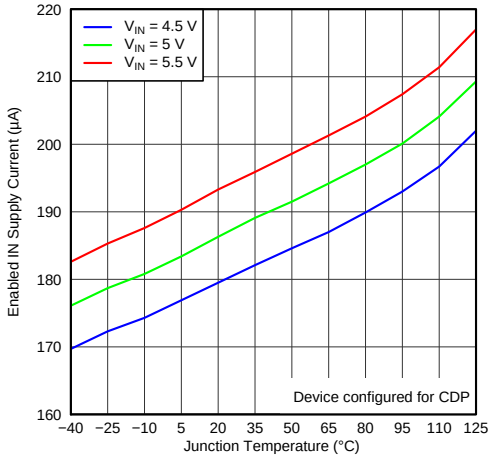


Figure 7. Enabled In Supply Current - CDP vs Temperature

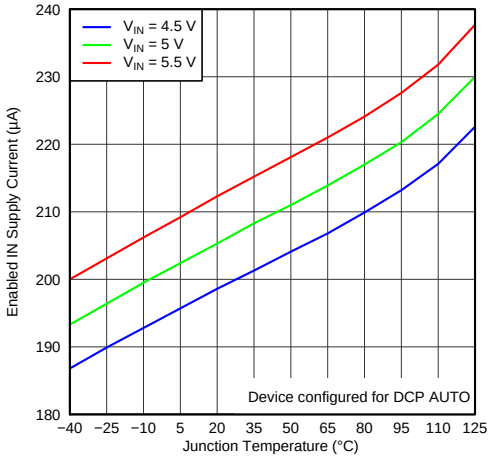


Figure 8. Enabled In Supply Current - DCP Auto vs Temperature

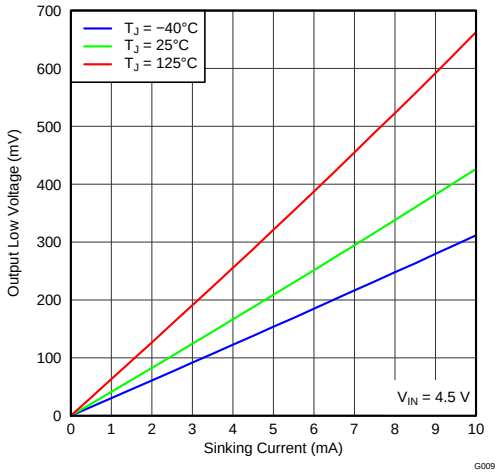


Figure 9. $\overline{\text{STATUS}}$ and $\overline{\text{FAULT}}$ Output Low Voltage vs Sinking Current

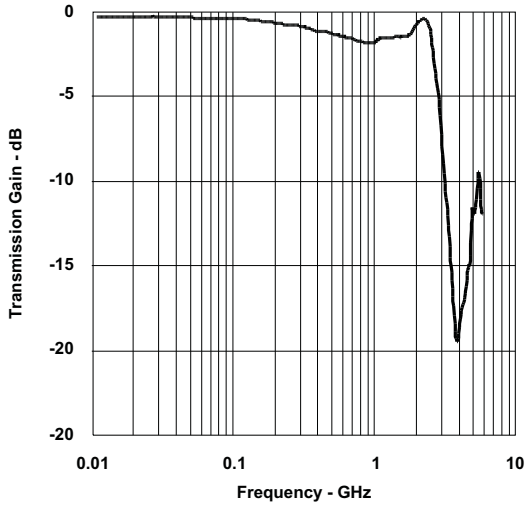


Figure 10. Data Transmission Characteristics vs Frequency

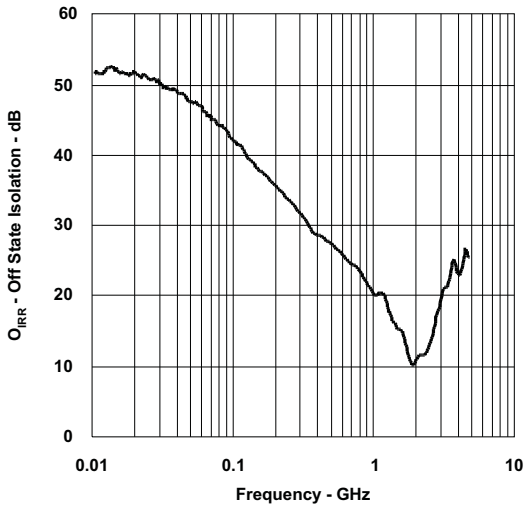


Figure 11. Off State Data Switch Isolation vs Frequency

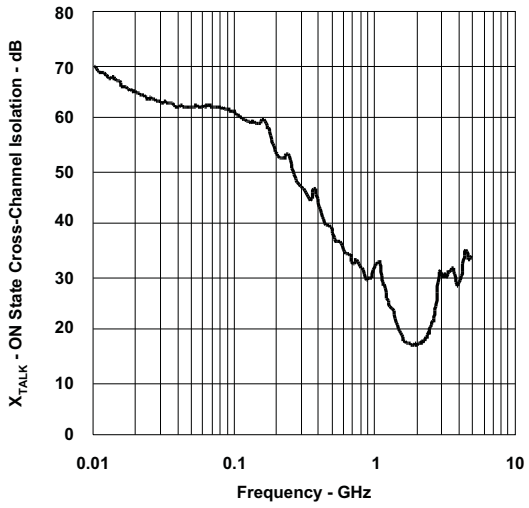


Figure 12. On State Cross-Channel Isolation vs Frequency

Typical Characteristics (continued)

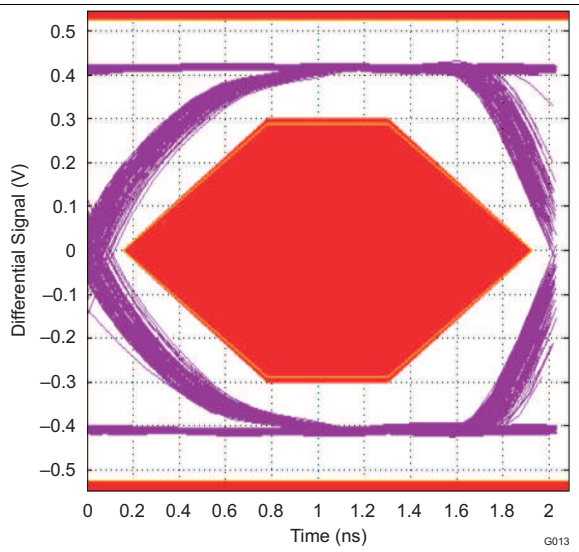


Figure 13. Eye Diagram Using USB Compliance Test Pattern (with no switch)

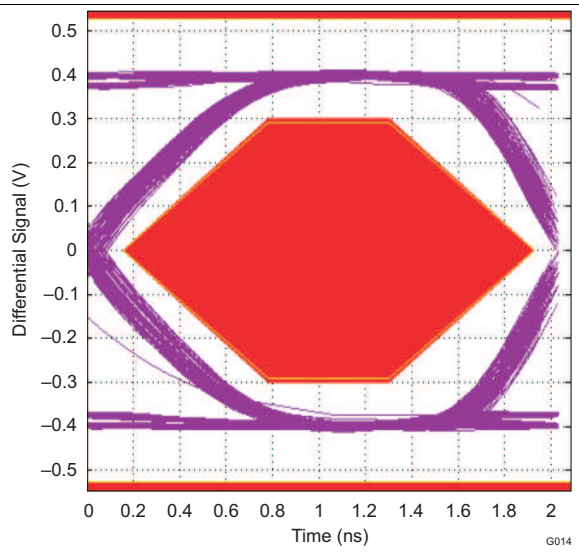


Figure 14. Eye Diagram Using USB Compliance Test Pattern (with data switch)

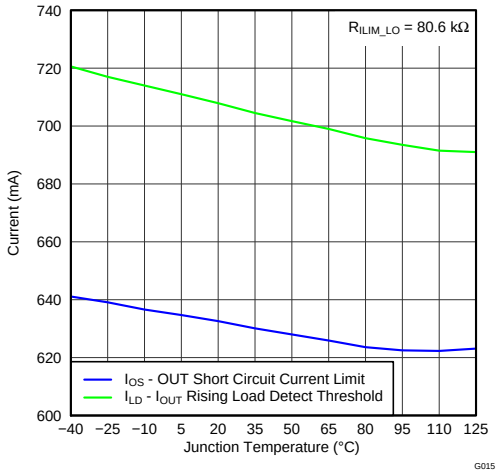


Figure 15. I_{OUT} Rising Load Detect Threshold and Out Short Circuit Current Limit vs Temperature

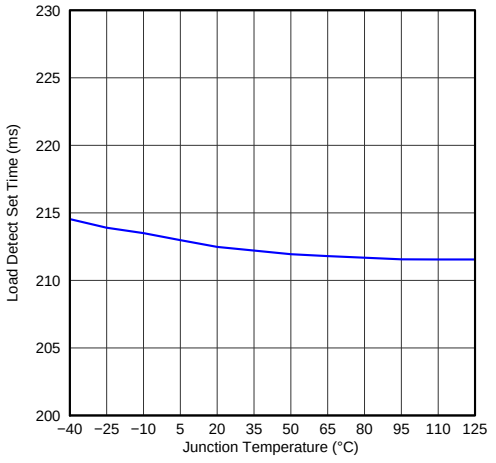


Figure 16. Load Detect Set Time vs Temperature

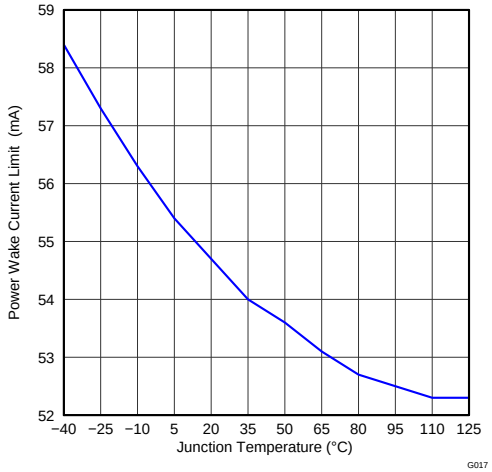


Figure 17. Power Wake Current Limit vs Temperature

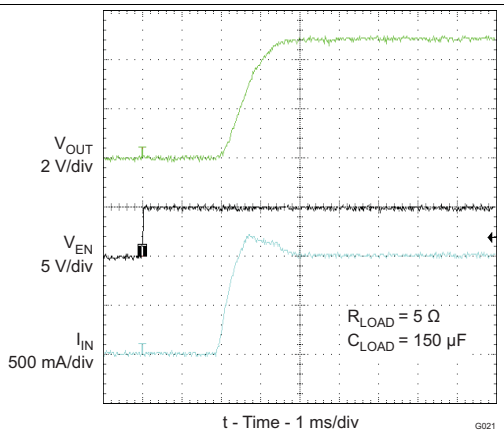


Figure 18. Turn-On Response

Typical Characteristics (continued)

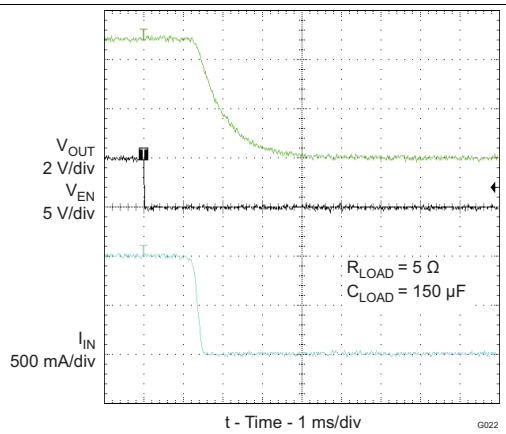


Figure 19. Turn-Off Response

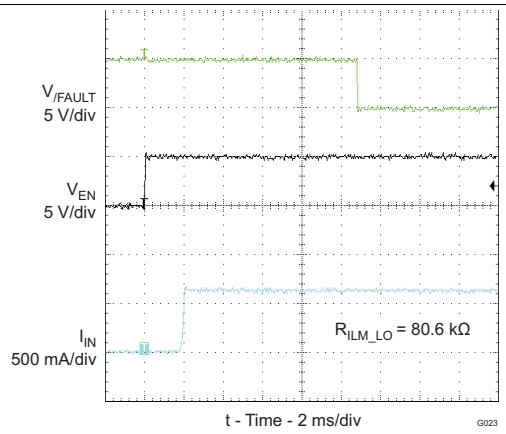


Figure 20. Device Enabled Into Short Circuit

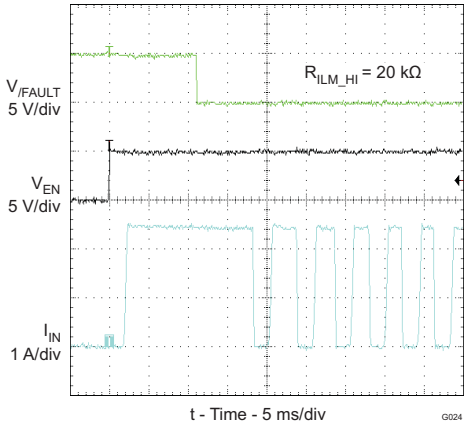


Figure 21. Device Enabled Into Short Circuit - Thermal Cycling

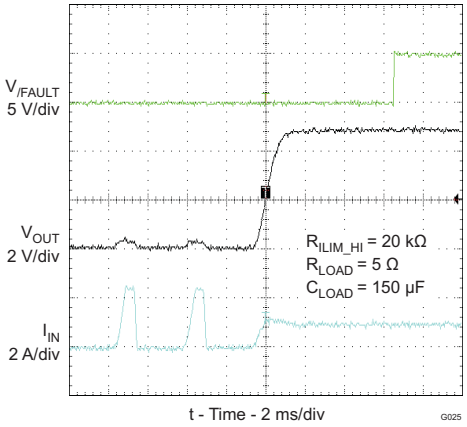


Figure 22. Short Circuit to Full Load Recovery

7 Parameter Measurement Information

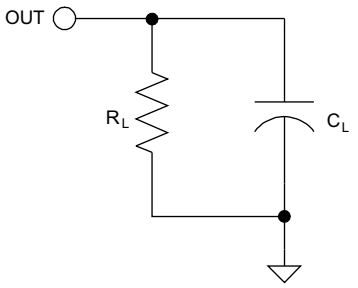


Figure 23. OUT Rise/Fall Test Load

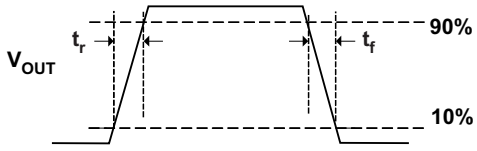


Figure 24. Power-On and Off Timing

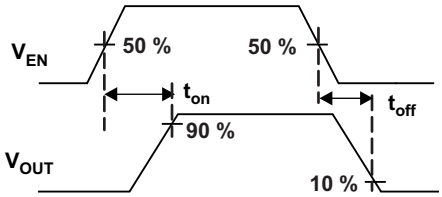


Figure 25. Enable Timing, Active High Enable

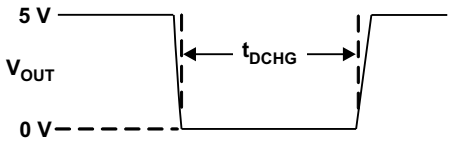


Figure 26. OUT Discharge During Mode Change

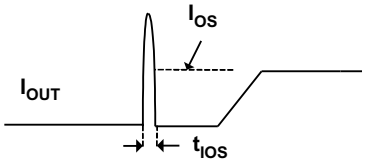


Figure 27. Output Short Circuit Parameters

8 Detailed Description

8.1 Overview

The following overview references various industry standards. It is always recommended to consult the most up-to-date standard to ensure the most recent and accurate information. Rechargeable portable equipment requires an external power source to charge its batteries. USB ports are a convenient location for charging because of an available 5-V power source. Universally accepted standards are required to make sure host and client-side devices operate together in a system to ensure power management requirements are met. Traditionally, host ports following the USB 2.0 specification must provide at least 500 mA to downstream client-side devices. Because multiple USB devices can be attached to a single USB port through a bus-powered hub, it is the responsibility of the client-side device to negotiate its power allotment from the host to ensure the total current draw does not exceed 500 mA. In general, each USB device is granted 100 mA and may request more current in 100 mA unit steps up to 500 mA. The host may grant or deny based on the available current. A USB 3.0 host port not only provides higher data rate than USB 2.0 port but also raises the unit load from 100 mA to 150 mA. It is also required to provide a minimum current of 900 mA to downstream client-side devices.

Additionally, the success of USB has made the mini-USB connector a popular choice for wall adapter cables. This allows a portable device to charge from both a wall adapter and USB port with only one connector. As USB charging has gained popularity, the 500 mA minimum defined by USB 2.0 or 900 mA for USB 3.0 has become insufficient for many handset and personal media players which need a higher charging rate. Wall adapters can provide much more current than 500 mA/900 mA. Several new standards have been introduced defining protocol handshaking methods that allow host and client devices to acknowledge and draw additional current beyond the 500 mA/900 mA minimum defined by USB 2.0/3.0 while still using a single micro-USB input connector.

The TPS2543-Q1 supports three of the most common USB charging schemes found in popular hand-held media and cellular devices:

- USB Battery Charging Specification BC1.2
- Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider Mode

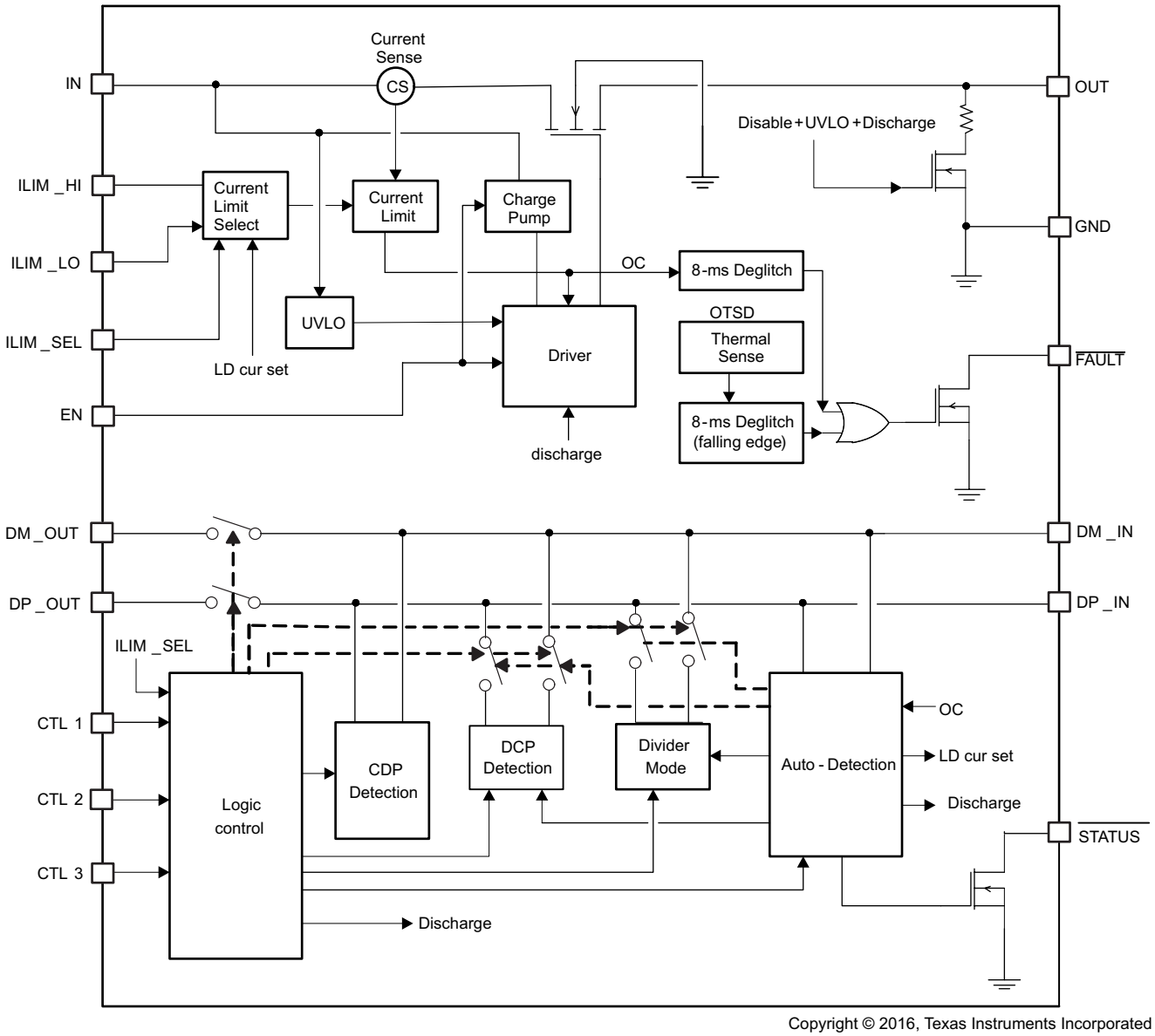
YD/T 1591-2009 is a subset of BC1.2 spec. supported by vast majority of devices that implement USB changing. Divider charging scheme is supported in devices from specific yet popular device maker.

BC1.2 lists three different port types as listed below.

- Standard Downstream Port (SDP)
- Charging Downstream Port (CDP)
- Dedicated Charging Port (DCP)

BC1.2 defines a charging port as a downstream facing USB port that provides power for charging portable equipment, under this definition CDP and DCP are defined as charging ports

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Standard Downstream Port (SDP) USB 2.0/USB 3.0

An SDP is a traditional USB port that follows USB 2.0/3.0 protocol and supplies a minimum of 500mA/900mA per port. USB 2.0/3.0 communications is supported, and the host controller must be active to allow charging. TPS2543-Q1 supports SDP mode in system power state S0 when system is completely powered ON and fully operational. For more details on control pin (CTL1-CTL3) settings to program this state please refer to device truth table.

Feature Description (continued)

8.3.2 Charging Downstream Port (CDP)

A CDP is a USB port that follows USB BC1.2 and supplies a minimum of 1.5 A per port. It provides power and meets USB 2.0 requirements for device enumeration. USB 2.0 communications is supported, and the host controller must be active to allow charging. What separates a CDP from an SDP is the host-charge handshaking logic that identifies this port as a CDP. A CDP is identifiable by a compliant BC1.2 client device and allows for additional current draw by the client device.

The CDP hand-shaking process is done in two steps. During step one the portable equipment outputs a nominal 0.6 V output on its D+ line and reads the voltage input on its D- line. The portable device concludes it is connected to an SDP if the voltage is less than the nominal data detect voltage of 0.3 V. The portable device concludes that it is connected to a Charging Port if the D- voltage is greater than the nominal data detect voltage of 0.3V and optionally less than 0.8 V.

The second step is necessary for portable equipment to determine if it is connected to CDP or DCP. The portable device outputs a nominal 0.6 V output on its D- line and reads the voltage input on its D+ line. The portable device concludes it is connected to a CDP if the data line being read remains less than the nominal data detect voltage of 0.3V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data detect voltage of 0.3 V.

TPS2543-Q1 supports CDP mode in system power state S0 when system is completely powered ON and fully operational. For more details on control pin (CTL1-CTL3) settings to program this state please refer to device truth table.

8.3.3 Dedicated Charging Port (DCP)

A DCP only provides power but does not support data connection to an upstream port. As shown in following sections, a DCP is identified by the electrical characteristics of its data lines. The TPS2543-Q1 emulates DCP in two charging states, namely DCP Forced and DCP Auto as shown in Figure 28. In DCP Forced state the device will support one of the two DCP charging schemes, namely Divider1 or Shorted. In the DCP Auto state, the device charge detection state machine is activated to selectively implement charging schemes involved with the Shorted, Divider1 and Divider2 modes. Shorted DCP mode complies with BC1.2 and Chinese Telecommunications Industry Standard YD/T 1591-2009, while the Divider mode is employed to charge devices that do not comply with BC1.2 DCP standard.

8.3.3.1 DCP BC1.2 and YD/T 1591-2009

Both standards define that the D+ and D- data lines should be shorted together with a maximum series impedance of 200 Ω. This is shown in Figure 28.

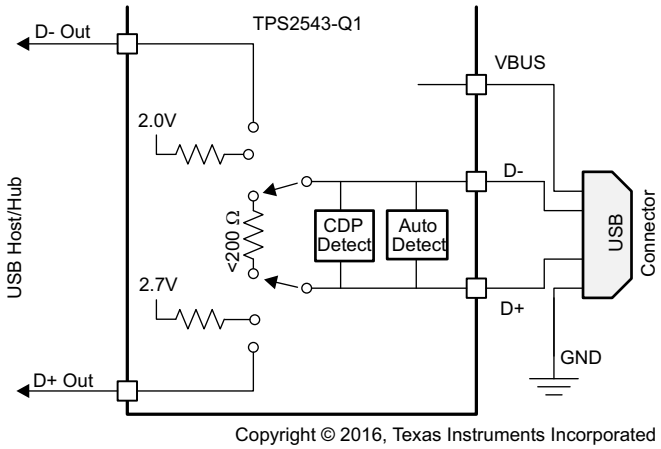


Figure 28. DCP Supporting BC1.2/YD/T 1591-2009

Feature Description (continued)

8.3.3.2 DCP Divider Charging Scheme

There are two Divider charging scheme supported by the device, Divider1 and Divider2 as shown in Figure 29 and Figure 30. In Divider1 charging scheme the device applies 2.0V and 2.7V to D+ and D- data line respectively. This is reversed in Divider2 mode.

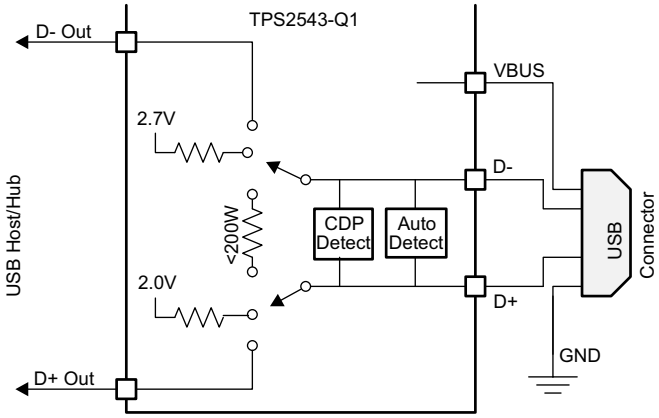


Figure 29. DCP Divider1 Charging Scheme

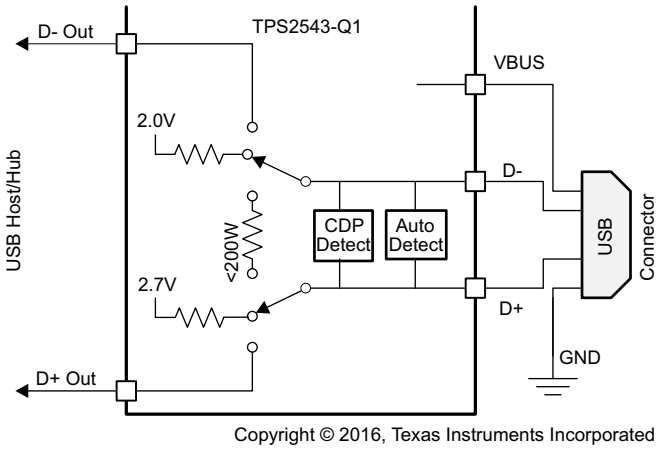


Figure 30. Divider2 Charging Scheme

Feature Description (continued)

8.3.4 Wake on USB Feature (Mouse/Keyboard Wake Feature)

8.3.4.1 USB 2.0 Background Information

The TPS2543-Q1 data lines interface with USB 2.0 devices. USB 2.0 defines three types of devices according to data rate. These devices and their characteristics relevant to TPS2543-Q1 Wake on USB operation are shown below

Low-speed USB devices

- 1.5 Mb/s
- Wired mice and keyboards are examples
- No devices that need battery charging
- All signaling performed at 2.0V and 0.8V hi/lo logic levels
- D- high to signal connect and when placed into suspend
- D- high when not transmitting data packets

Full-speed USB devices

- 12 Mb/s
- Wireless mice and keyboards are examples
- Legacy phones and music players are examples
- Some legacy devices that need battery charging
- All signaling performed at 2.0V and 0.8V hi/lo logic levels
- D+ high to signal connect and when placed into suspend
- D+ high when not transmitting data packets

High-speed USB devices

- 480 Mb/s
- Tablets, phones and music players are examples
- Many devices that need battery charging
- Connect and suspend signaling performed at 2.0V and 0.8V hi/lo logic levels
- Data packet signaling performed a logic levels below 0.8V
- D+ high to signal connect and when placed into suspend (same as a full-speed device)
- D+ and D- low when not transmitting data packets

8.3.4.2 Wake On USB

Wake on USB is the ability of a wake configured USB device to wake a computer system from its S3 sleep state back to its S0 working state. Wake on USB requires the data lines to be connected to the system USB host before the system is placed into its S3 sleep state and remain continuously connected until they are used to wake the system.

The TPS2543-Q1 supports low speed HID (human interface device like mouse/key board) wake function only. There are two scenarios (as listed below) under which wake on HID are supported by the TPS2543-Q1. The specific CTL pin changes that the TPS2543-Q1 will override are shown below. The information is presented as CTL1, CTL2, CTL3. The ILIM_SEL pin plays no role

1. 111 (CDP/SDP2) to 011 (DCP-Auto)
2. 010 (SDP1) to 011 (DCP-Auto)

NOTE

The 110 (SDP1) to 011 (DCP-Auto) transition is not supported. This is done for practical reasons, because the transition involves changes to two CTL pins. Depending on which CTL pin changes first, the device sees either a temporary 111 or 010 command. The 010 command is safe but the 111 command causes an OUT discharge as the TPS2546-Q1 instead proceeds to the 111 state.

Feature Description (continued)

8.3.4.3 USB Slow-Speed Device Recognition and Operation

TPS2543-Q1 is capable of detecting LS device attachment when TPS2543-Q1 is in SDP or CDP mode. Per USB spec when no device is attached, the D+ and D- lines are near ground level. When a low speed compliant device is attached to the TPS2543-Q1 charging port, D- line will be pulled high in its idle state (mouse/keyboard not activated). However when a FS device is attached the opposite is true in its idle state, i.e. D+ is pulled high and D- remains at ground level.

When a low speed compliant device is attached to the TPS2543-Q1, charging port D- line will be pulled high in its idle state (mouse/keyboard not activated). TPS2543-Q1 will monitor D- data line continuously. Since TPS2543-Q1 does not monitor D+ line it cannot detect the attachment of a FS device. When TPS2543-Q1 is in CDP/SDP mode and system is commanded to go to sleep state, the device CTL setting is also changed. Assuming it is changed to DCP/Auto, 011, having previously detected a low speed HID attachment the device will simply ignore the command to go to DCP/Auto mode and stay in CDP/SDP state to support wake on mouse function. When the USB low speed HID is activated (clicked) while system is in S3 (sleep) mode the high speed switch within the TPS2543-Q1 allows the transfer of signal from the LS HID device to the USB host. The USB host subsequently wakes the system and changes CTL setting of the TPS2543-Q1 back to CDP/SDP state. Activating (clicking) the low speed device makes the D- data line go back low momentarily, this triggers an internal timer within the TPS2543-Q1 to count down. If after ~64ms the CTL lines are still set at 011 (DCP/Auto) the device will immediately switch to DCP/Auto mode and disconnect the mouse from the host. To prevent this, the CTL setting must be made in less then 64 ms after HID device activation otherwise mouse/KB function will be lost.

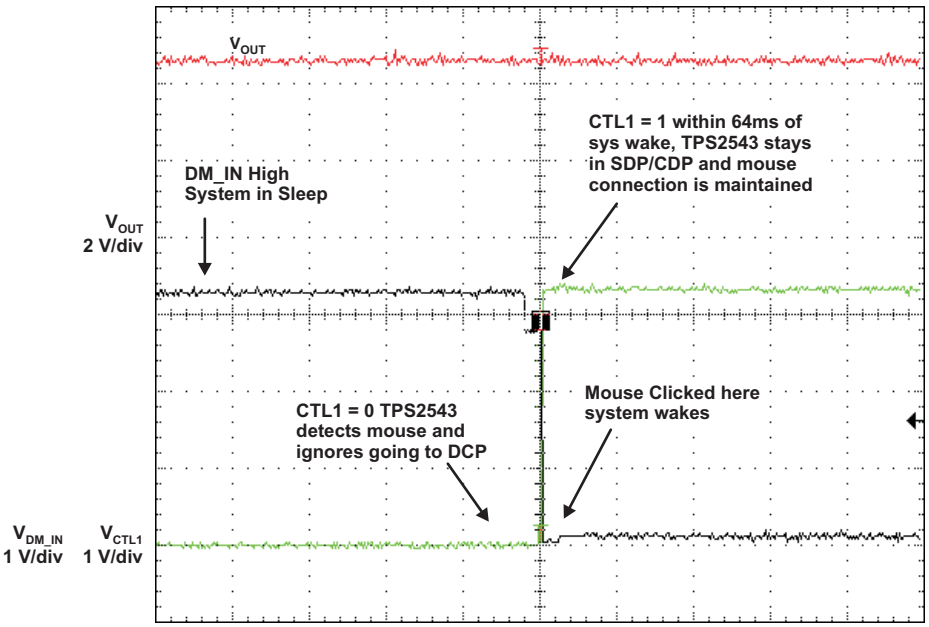


Figure 31. Mouse Wake from Sleep Scope Plot

Feature Description (continued)

8.3.5 Load Detect

TPS2543-Q1 offers system designers unique power management strategy not available in the industry from similar devices. There are two power management schemes supported by the TPS2543-Q1 via the STATUS pin, they are:

1. Power Wake (PW)
2. Port Power Management (PPM)

Either feature may be implemented in a system depending on power savings goals for the system. In general Power Wake feature is used mainly in mobile systems like a notebook where it is imperative to save battery power when system is in deep sleep (S4/S5) state. On the other hand Port Power Management feature would be implemented where multiple charging ports are supported in the same system and system power rating is not capable of supporting high current charging on multiple ports *simultaneously*.

8.3.6 Power Wake

Goal of power wake feature is to save system power when system is in S4/S5 state. In S4/S5 state system is in deep sleep and typically running of the battery; so every “mW” in system power savings will translate to extending battery life. In this state the TPS2543-Q1 will monitor charging current at the OUT pin and provide a mechanism via the STATUS pin to switch out the high power DC-DC controller and switch in a low power LDO when charging current requirement is <45mA (typ). This would be the case when no peripheral device is connected at the charging port or if a device has attained its full battery charge and draws <45mA.. Power wake flow chart and description is shown in Figure 32.

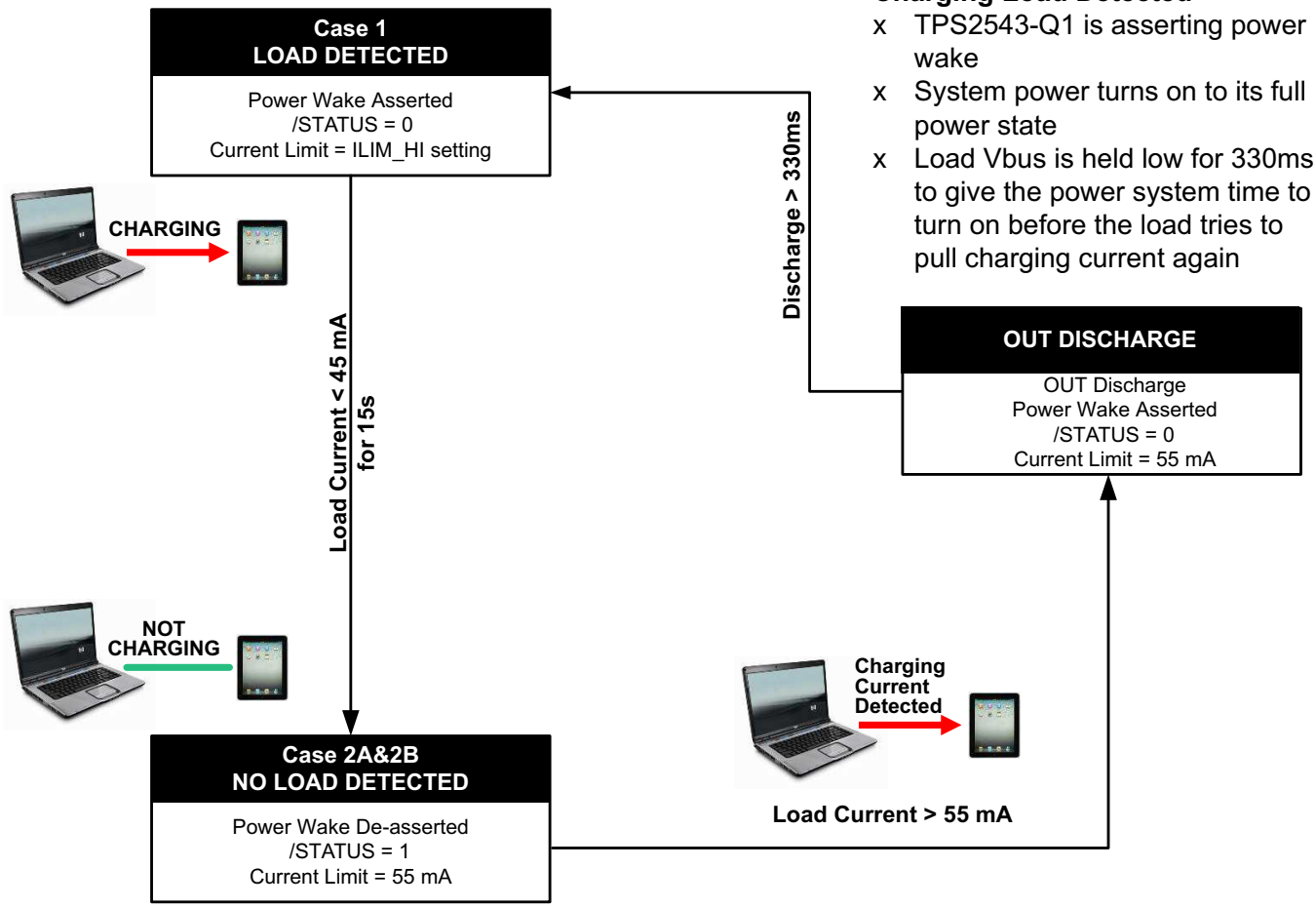
Feature Description (continued)

Load being Charged

- TPS2543-Q1 is asserting power wake
- System power is at its full capability
- Load can charge at high current
- TPS2543-Q1 monitors port to detect when charging load is done charging or removed

Charging Load Detected

- TPS2543-Q1 is asserting power wake
- System power turns on to its full power state
- Load Vbus is held low for 330ms to give the power system time to turn on before the load tries to pull charging current again



Charging Load Not Detected.

- TPS2543-Q1 is not asserting power wake. System power is in a low power state to save energy.
- TPS2543-Q1 monitors port to detect when charging load is attached and tries to charge

Figure 32. Power Wake Flow Chart

Feature Description (continued)

8.3.6.1 Implementing Power Wake in Notebook System

An implementation of power wake in notebook platforms with the TPS2543-Q1 is shown in Figure 33 to Figure 35. Power wake function is used to select between a high power DC-DC converter and low power LDO (100mA) based on charging requirements. System power saving is achieved when under no charging conditions (the connected device is fully charged or no device is connected) the DC-DC converter is turned-off (to save power since it is less efficient in low power operating region) and the low power LDO supplies standby power to the charging port.

Power wake is activated in S4/S5 mode (0011 setting, see device truth table), TPS2543-Q1 is charging connected device as shown in Figure 33, $\overline{\text{STATUS}}$ is pulled LO (Case 1) which switches-out the LDO and switches-in the DC-DC converter to handle high current charging.

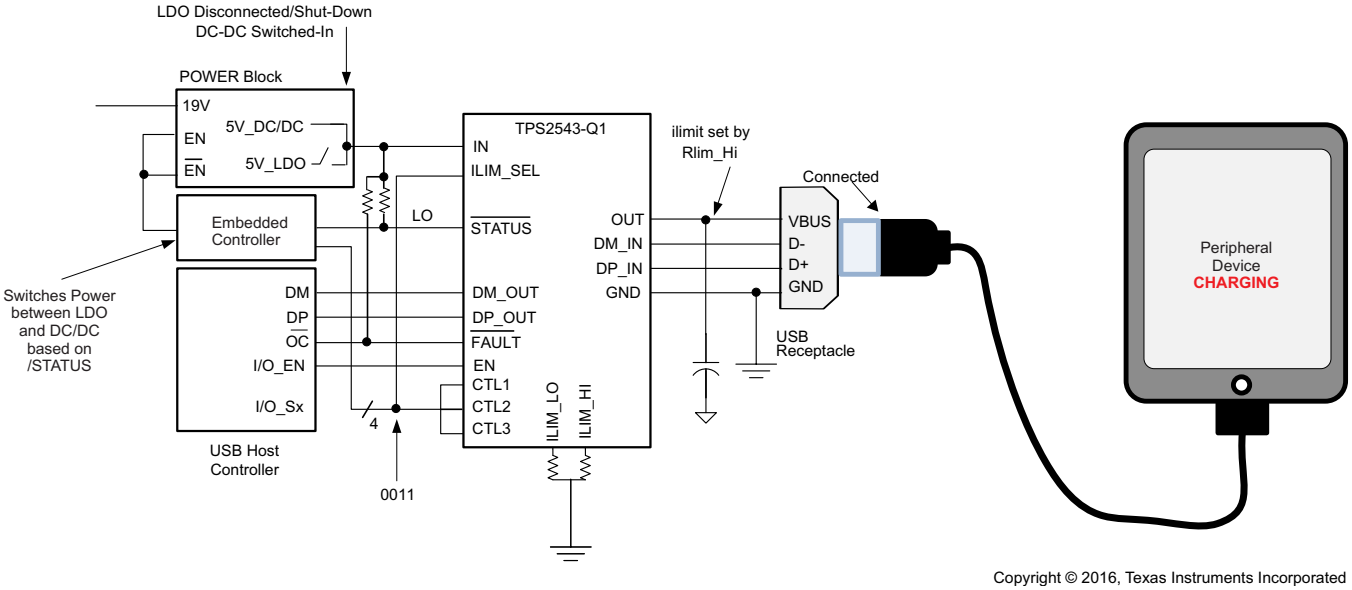


Figure 33. Case 1: System in S4/S5, Device Charging

As shown in Case 2A and Case 2B, when connected device is fully charged or gets disconnected from the charging port, the charging current will fall. If charging current falls to <45mA and stays below this threshold for over 15s, TPS2543-Q1 automatically sets a 55 mA internal current limit and $\overline{\text{STATUS}}$ is de-asserted (pulled HI). As shown in Case 2A and Case 2B. This results in DC-DC converter turning off and the LDO turning on. Current limit of 55 mA is set to prevent the low power LDO output voltage from collapsing in case there is a spike in current draw due to device attachment or other activity such as display panel LED turning ON in connected device.

Following Power Wake flow chart (Figure 32) when a device is attached and draws >55 mA of charging current the TPS2543-Q1 will hit its internal current limit. This will trigger the device to assert $\overline{\text{STATUS}}$ (LO) and turn on the DC-DC converter and turn off the LDO. TPS2543-Q1 will discharge OUT for >330 ms (typ) to allow the main power supply to turn on. After the discharge the device will turn back on with current limit set by ILIM_HI (Case 1)

Feature Description (continued)

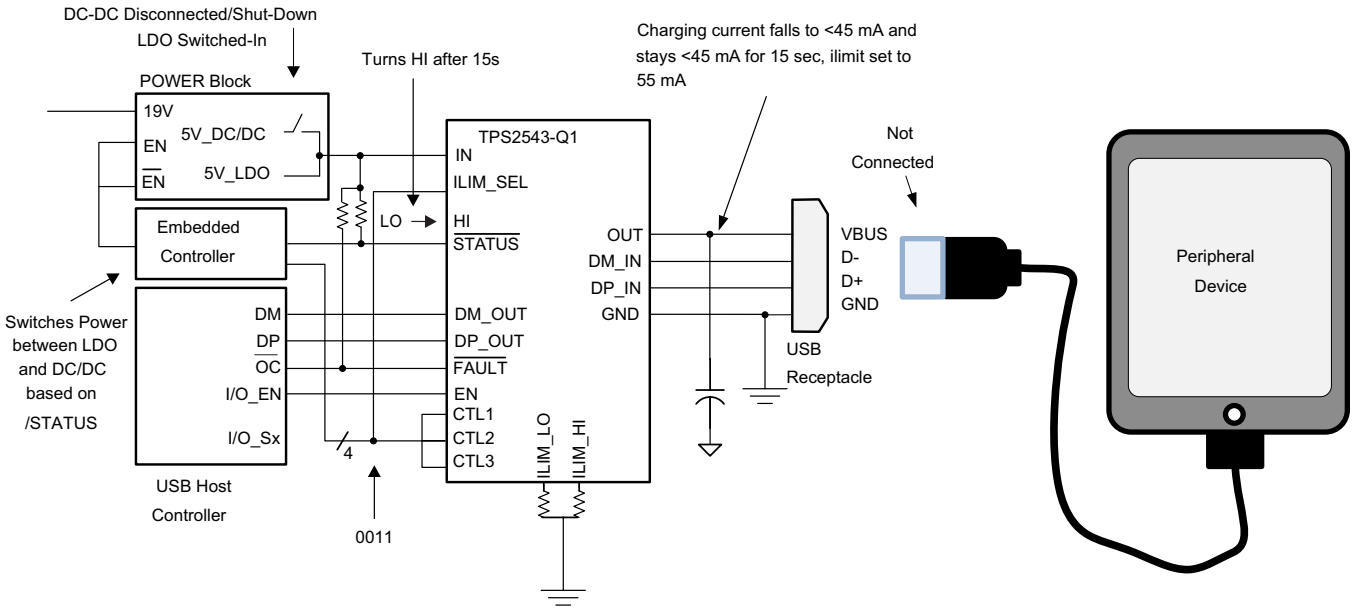


Figure 34. Case 2A: System in S4/S5, No Device Attached

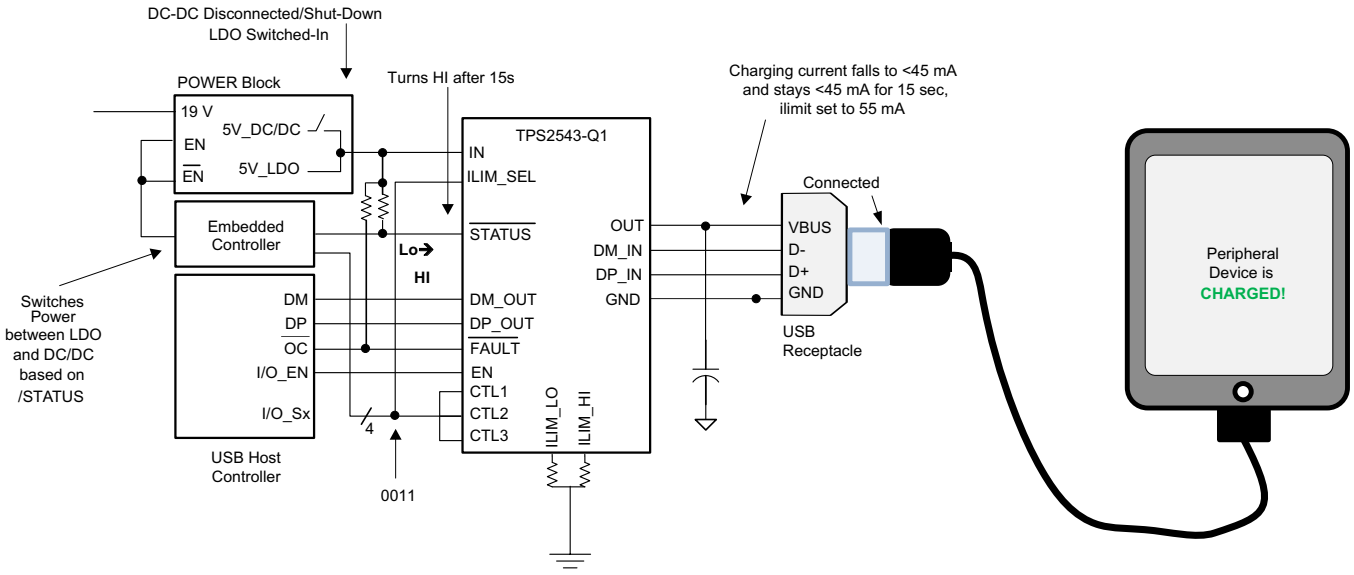


Figure 35. Case 2B: System in S4/S5, Attached Device Fully Charged

Feature Description (continued)

8.3.7 Port Power Management (PPM)

PPM is the intelligent and dynamic allocation of power. It is for systems that have multiple charging ports but cannot power them all simultaneously. Goal of this feature are:

1. Enhances user experience since user does not have to search for charging port
2. Power supply only has to be designed for a reasonable charging load

Initially all ports are allowed to broadcast high current charging, charging current limit is based on ILIM_HI resistor setting. System monitors STATUS to see when high current loads are present. Once allowed number of ports assert STATUS, remaining ports are toggled to a non-charging port. Non-charging ports are SDP ports with current limit based on ILIM_LO. TPS2543-Q1 allows for a system to toggle between charging and non-charging ports either with an OUT discharge or without an OUT discharge.

8.3.7.1 Benefits of PPM

- Delivers better user experience
- Prevents overloading of system power supply
- Allows for dynamic power limits based on system state
- Allows every port to potentially be a high power charging port
- Allows for smaller power supply capacity since the loading is controlled

8.3.7.2 PPM Details

All ports are allowed to broadcast high current charging – CDP or DCP. Current limit is based on ILIM_HI and system monitors STATUS pin to see when high current loads are present. Once allowed number of ports assert STATUS, remaining ports are toggled to a SDP non-charging port. SDP current limit is based on ILIM_LO setting. SDP ports are automatically toggled back to CDP or DCP mode when a charging port de-asserts STATUS.

Based on CTL settings there is a provision for a port to toggle between charging and non-charging ports either with a Vbus discharge or without a Vbus discharge. For example when a port is in SDP2 mode (1110) and its ILIM_SEL pin is toggled to 1 due to another port releasing its high current requirements. The SDP2 port will automatically revert to CDP mode (1111) without a discharge event. This is desirable if this port was connected to a media device where it was syncing data from the SDP2 port; a discharge event would mess-up the syncing activity on the port and cause user confusion.

STATUS trip point is based on the programmable ILIM_LO current limit set point This does not mean STATUS is a current limit – the port itself is using the ILIM_HI current limit. Since ILIM_LO defines the current limit for a SDP port, it works well to use the ILIM_LO value to define a high current load. STATUS asserts in CDP and DCP_Auto when load current is above ILIM_LO + 75 mA for 200 ms. STATUS also asserts in CDP when an attached device does a BC1.2 primary detection. STATUS de-asserts in CDP and DCP_Auto when load current is below ILIM_LO + 25 mA for 3s.

8.3.7.3 Implementing PPM in a System with Two Charging Ports

Figure 36 shows implementation of two charging ports, each with its own TPS2543-Q1. In this example 5-V power supply for the two charging ports is rated at < 3 A or <15 W max. Both devices have R_{LIM} chosen to correspond to the low (0.9 A) and high (1.5 A) current limit setting for the port. In this implementation the system can support only one of the two ports at 1.5-A charging current while the other port is set to SDP mode and I_{LIMIT} corresponding to 0.9 A.

Feature Description (continued)

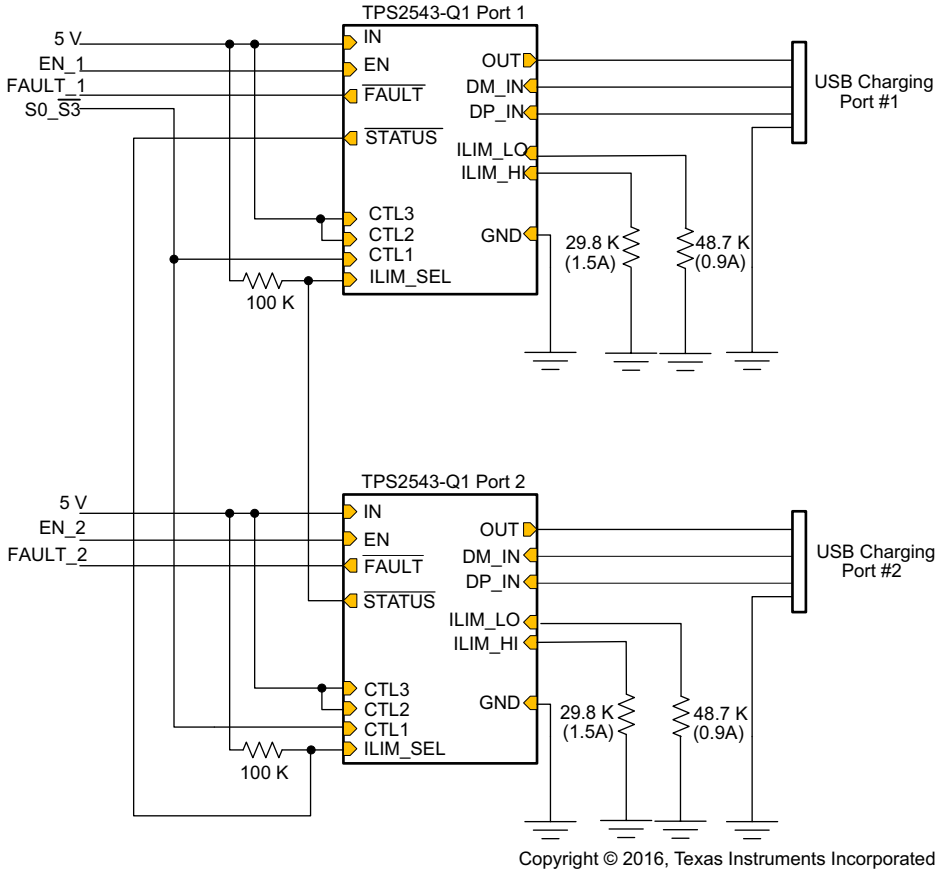


Figure 36. Implementing Port Power Management in a System Supporting Two Charging Ports

8.3.8 Over-Current Protection

When an over-current condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before VIN has been applied. The TPS2543-Q1 senses the short and immediately switches into a constant-current output. In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for nominally one to two microseconds before the current-limit circuit can react. The device operates in constant-current mode after the current-limit circuit has responded. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting. The device will remain off until the junction temperature cools approximately 20°C and will then re-start. The device will continue to cycle on/off until the over-current condition is removed.

8.3.9 FAULT Response

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an over-temperature or current limit condition. The output remains asserted until the fault condition is removed. The TPS2543-Q1 is designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal deglitch circuit for current limit conditions without the need for external circuitry. This ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. Over-temperature conditions are not deglitched and assert the $\overline{\text{FAULT}}$ signal immediately.

Feature Description (continued)

8.3.10 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted oscillations on the output due to input voltage drop from large current surges.

8.3.11 Thermal Sense

The TPS2543-Q1 protects itself with two independent thermal sensing circuits that monitor the operating temperature of the power distribution switch and disables operation if the temperature exceeds recommended operating conditions. The device operates in constant-current mode during an over-current condition, which increases the voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, so the junction temperature rises during an over-current condition. The first thermal sensor turns off the power switch when the die temperature exceeds 135°C and the part is in current limit. The second thermal sensor turns off the power switch when the die temperature exceeds 155°C regardless of whether the power switch is in current limit. Hysteresis is built into both thermal sensors, and the switch turns on after the device has cooled by approximately 20°C. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output $\overline{\text{FAULT}}$ is asserted (active low) during an over-temperature shutdown condition.

8.4 Device Functional Modes

Table 1 shows the differences between these ports.

Table 1. Operating Modes

PORT TYPE	SUPPORT USB 2.0 COMMUNICATION	MAX. ALLOWABLE CURRENT DRAW BY PORTABLE DEVICE (A)
SDP (USB 2.0)	Yes	0.5
SDP (USB 3.0)	Yes	0.9
CDP	Yes	1.5
DCP	No	1.5

8.4.1 DCP Auto Mode

As mentioned above the TPS2543-Q1 integrates an auto-detect state machine that supports all the above DCP charging schemes. It starts in Divider1 scheme, however if a BC1.2 or YD/T 1591-2009 compliant device is attached, the TPS2543-Q1 responds by discharging OUT, turning back on the power switch and then moving to BC1.2 DCP mode. It then stays in that mode until the device releases the data line, in which case it goes back to Divider1 scheme. When a Divider1 compliant device is attached the TPS2543-Q1 will stay in Divider1 state.

Also, the TPS2543-Q1 will automatically switch between the Divider1 and Divider2 schemes based on charging current drawn by the connected device. Initially the device will set the data lines to Divider1 scheme. If charging current of >750 mA is measured by the TPS2543-Q1, it discharges and then switches to Divider2 scheme and test to see if the peripheral device will still charge at a high current. If it does then it stays in Divider2 scheme otherwise it performs OUT discharge and will revert to Divider1 scheme.

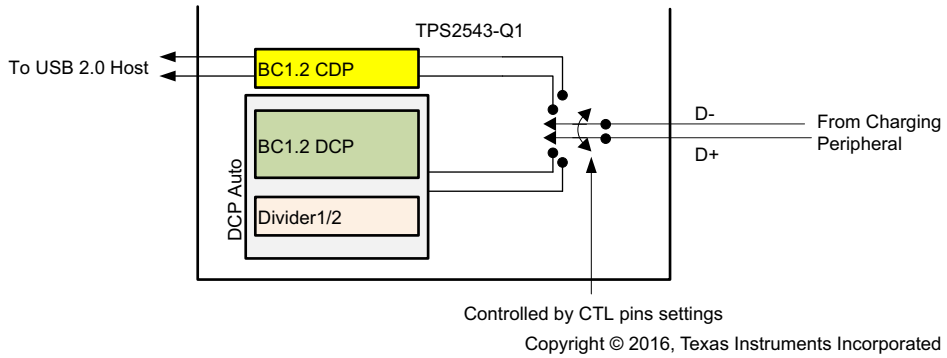


Figure 37. DCP Auto Mode

8.4.2 DCP Forced Shorted / DCP Forced Divider1

In this mode the device is permanently set to one of the DCP schemes (BC1.2/ YD/T 1591-2009 or Divider1) as commanded by its control pin setting per device truth table.

8.4.3 High-Bandwidth Data Line Switch

The TPS2543-Q1 passes the D+ and D- data lines through the device to enable monitoring and handshaking while supporting charging operation. A wide bandwidth signal switch is used, allowing data to pass through the device without corrupting signal integrity. The data line switches are turned on in any of CDP or SDP operating modes. The EN input also needs to be at logic High for the data line switches to be enabled.

NOTE

- While in CDP mode, the data switches are ON even while CDP handshaking is occurring
- The data line switches are OFF if EN or all CTL pins are held low, or if in DCP mode. They are not automatically turned off if the power switch (IN to OUT) is in current limit
- The data switches are for USB 2.0 differential pair only. In the case of a USB 3.0 host, the super speed differential pairs must be routed directly to the USB connector without passing through the TPS2543-Q1
- Data switches are OFF during OUT (VBUS) discharge

Table 2 can be used as an *aid* to program the TPS2543-Q1 per system states however not restricted to below settings only.

Table 2. Control Pin Settings Matched to System Power States

SYSTEM GLOBAL POWER STATE	TPS2543-Q1 CHARGING MODE	CTL1	CTL2	CTL3	ILIM_SEL	CURRENT LIMIT SETTING
S0	SDP1	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP2, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 75 mA thresholds or if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds	0	0	1	1	ILIM_HI
S3/S4/S5	Auto mode, no load detection	0	0	1	0	ILIM_HI
S3	Auto mode, keyboard/mouse wake up, load detection with ILIM_LO + 75 mA thresholds	0	1	1	1	ILIM_HI
S3	Auto mode, keyboard/mouse wake-up, no load detection	0	1	1	0	ILIM_HI
S3	SDP1, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

8.4.4 Device Truth Table (TT)

Device TT lists all valid bias combinations for the three control pins CTL1-3 and ILIM_SEL pin and their corresponding charging mode. It is important to note that the TT *purposely* omits matching charging modes of the TPS2543-Q1 with global power states (S0-S5) as device is agnostic to system power states. The TPS2543-Q1 monitors its CTL inputs and will transition to whatever charging state it is commanded to go to (except when LS HID device is detected). For example if sleep charging is desired when system is in standby or hibernate state then user must set TPS2543-Q1 CTL pins to correspond to DCP_Auto charging mode per below table. When system is put back to operation mode then set control pins to correspond to SDP or CDP mode and so on.

Table 3. Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	CURRENT LIMIT SETTING	STATUS OUTPUT (Active low)	COMMENT
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	0	1	1	DCP_Auto	I_{OS_PW} & ILIM_HI(1)	DCP load present(2)	Data Lines Disconnected and Load Detect Function Active
0	1	0	0	SDP1	ILIM_LO	OFF	Data Lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP load present(3)	Data Lines Disconnected and Load Detect Function Active
1	0	0	0	DCP _Shorted	ILIM_LO	OFF	Device Forced to stay in DCP BC1.2 charging mode
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	
1	0	1	0	DCP / Divider1	ILIM_LO	OFF	Device Forced to stay in DCP Divider1 Charging Mode
1	0	1	1	DCP / Divider1	ILIM_HI	OFF	
1	1	0	0	SDP1	ILIM_LO	OFF	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	OFF	
1	1	1	0	SDP2(4)	ILIM_LO	OFF	
1	1	1	1	CDP(4)	ILIM_HI	CDP load present(5)	Data Lines Connected and Load Detect Active

(1) TPS2543-Q1 : Current limit (I_{OS}) is automatically switched between I_{OS_PW} and the value set by ILIM_HI according to the Load Detect – Power Wake functionality.
(2) DCP Load present governed by the “Load Detection – Power Wake” limits.
(3) DCP Load present governed by the “Load Detection – Non Power Wake” limits.
(4) No OUT discharge when changing between 1111 and 1110.
(5) CDP Load present governed by the “Load Detection – Non Power Wake” limits and BC1.2 primary detection.

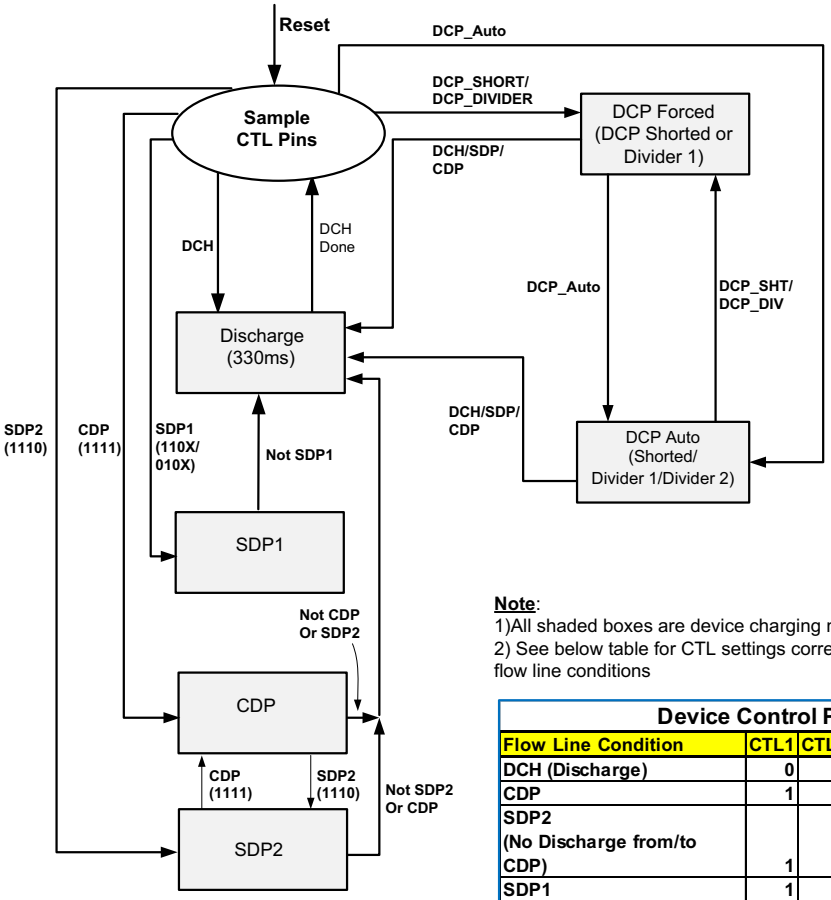
9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Refer to the simplified device state diagram in Figure 38. Power-on-reset (POR) holds device in initial state while output is held in discharge mode. Any POR event will take the device back to initial state. After POR clears, device goes to the next state depending on the CTL lines as shown in Figure 38.



Note:
1)All shaded boxes are device charging modes
2) See below table for CTL settings corresponding to flow line conditions

Device Control Pins				
Flow Line Condition	**CTL1**	**CTL2**	**CTL3**	**ILIM_SEL**
DCH (Discharge)	0	0	0	X
CDP	1	1	1	1
SDP2 (No Discharge from/to CDP)	1	1	1	0
SDP1	1	1	0	X
(Discharge from/to any charging state including CDP)	0	1	0	X
DCP_SHORT	1	0	0	X
DCP_DIVIDER	1	0	1	X
DCP_Auto	0	1	1	X
	0	0	1	X

Figure 38. TPS2543-Q1 Charging States

Application Information (continued)

9.1.1 Output Discharge

To allow a charging port to renegotiate current with a portable device, TPS2543-Q1 uses the OUT discharge function. It proceeds by turning off the power switch while discharging OUT, then turning back on the power switch to reassert the OUT voltage. This discharge function is automatically applied as shown in device state diagram.

9.2 Typical Application

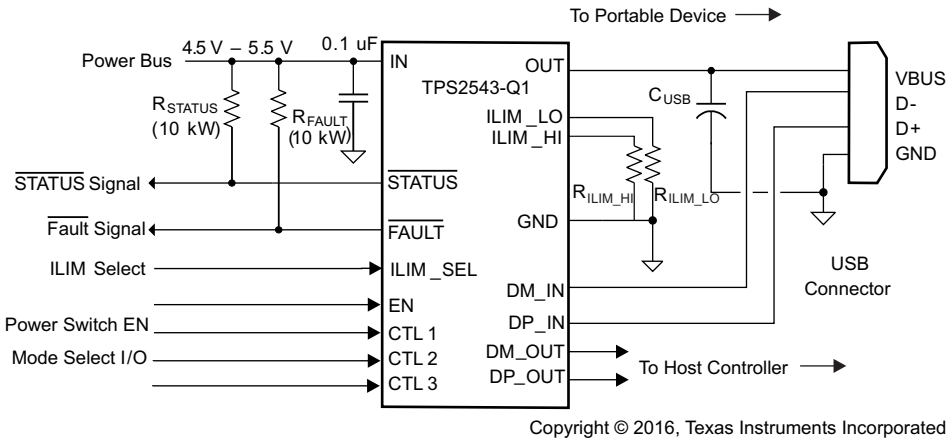


Figure 39. Typical Application Schematic USB Port Charging

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 4.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage, $V_{(IN)}$	5 V
Output voltage, $V_{(DC)}$	5 V
Maximum continuous output current, $I_{(OUT)}$	2.5 A
Current limit, $I_{(LIM\_LO)}$ at R_{ILIM_LO} = 80.6 kΩ	0.625 A
Current Limit, $I_{(LIM\_HI)}$ at R_{ILIM_HI} = 16.9 kΩ	2.97 A

9.2.2 Detailed Design Procedure

9.2.2.1 Current-Limit Settings

The TPS2543-Q1 has two independent current limit settings that are each programmed externally with a resistor. The ILIM_HI setting is programmed with R_{ILIM_HI} connected between ILIM_HI and GND. The ILIM_LO setting is programmed with RILIM_LO connected between ILIM_LO and GND. Consult the Device Truth Table (Table 3) to see when each current limit is used. Both settings have the same relation between the current limit and the programming resistor.

R_{ILIM_LO} is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:

1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used

If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use R_{ILIM_LO} < 80.6 kΩ.

Equation 1 programs the typical current limit:

$$I_{OS\_typ}(mA) = \frac{50{,}500}{(R_{ILIM\_XX}(k\Omega) + 0.1)} \quad (1)$$

R_{ILIM_XX} corresponds to either R_{ILIM_HI} or R_{ILIM_LO} as appropriate.

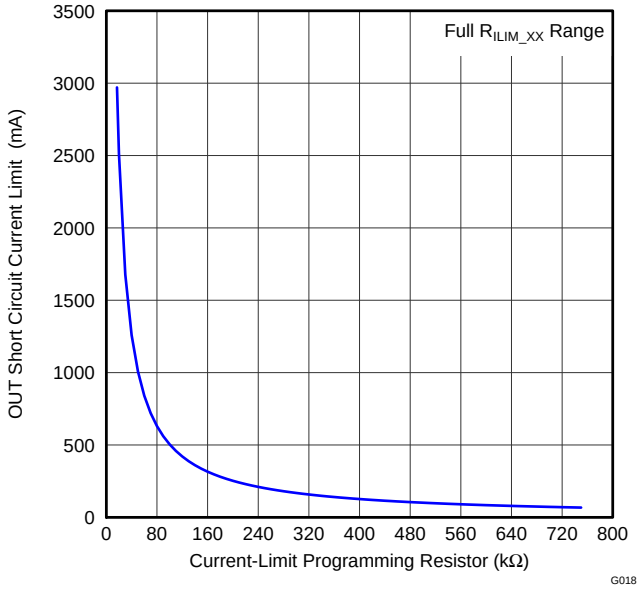


Figure 40. Typical Current Limit Setting vs Programming Resistor

Many applications require that the current limit meet specific tolerance limits. When designing to these tolerance limits, both the tolerance of the TPS2543-Q1 current limit and the tolerance of the external programming resistor must be taken into account. The following equations approximate the TPS2543-Q1 minimum / maximum current limits to within a few mA and are appropriate for design purposes. The equations do not constitute part of TI's published device specifications for purposes of TI's product warranty. These equations assume an ideal - no variation - external programming resistor. To take resistor tolerance into account, first determine the minimum / maximum resistor values based on its tolerance specifications and use these values in the equations. Because of the inverse relation between the current limit and the programming resistor, use the maximum resistor value in the I_{OS_min} equation and the minimum resistor value in the I_{OS_max} equation.

$$I_{OS\_min}(mA) = \frac{45{,}661}{(R_{ILIM\_XX}(k\Omega) + 0.1)^{0.98422}} - 30 \quad (2)$$

$$I_{OS\_max}(mA) = \frac{55{,}639}{(R_{ILIM\_XX}(k\Omega) + 0.1)^{1.0143}} + 30 \quad (3)$$

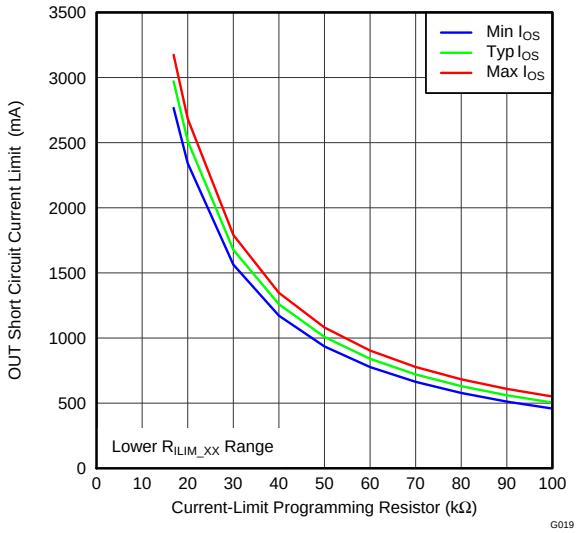


Figure 41. Current Limit Setting vs Programming Resistor

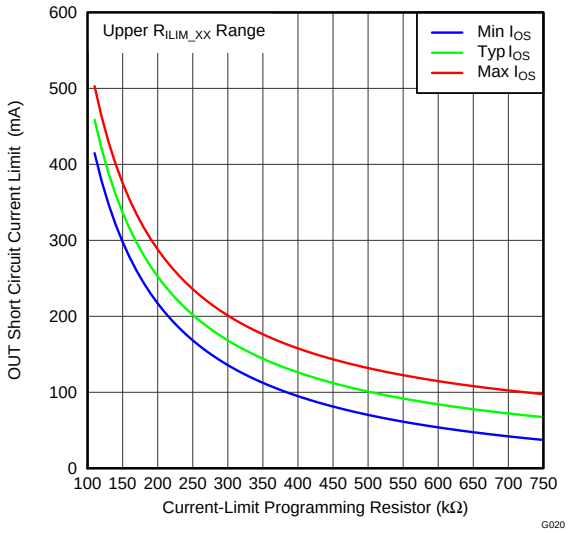


Figure 42. Current Limit Setting vs Programming Resistor

The traces routing the R_{ILIM_XX} resistors should be a sufficiently low resistance as to not affect the current-limit accuracy. The ground connection for the R_{ILIM_XX} resistors is also very important. The resistors need to reference back to the TPS2543-Q1 GND pin. Follow normal board layout practices to ensure that current flow from other parts of the board does not impact the ground potential between the resistors and the TPS2543-Q1 GND pin.

9.2.3 Application Curves

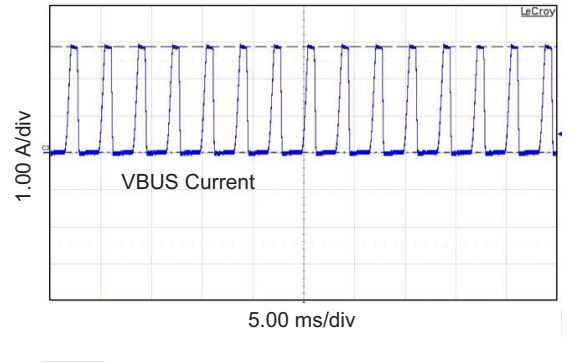


Figure 43. High-Current Limit

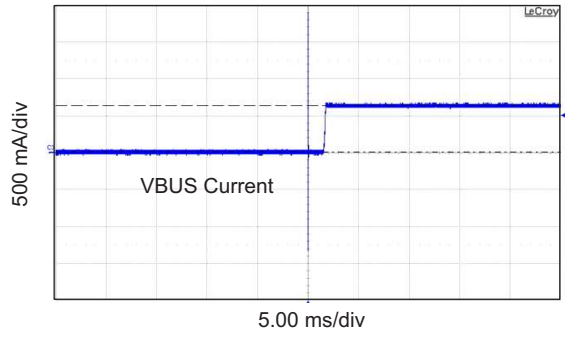


Figure 44. Low-Current Limit

10 Power Supply Recommendations

The TPS2543-Q1 device is designed for a supply-voltage range of 4.5 V ≤ VIN ≤ 5.5 V. If the input supply is located more than a few inches from the device, an input ceramic bypass capacitor higher than 0.1 µF is recommended. In order to avoid drops in voltage during overcurrent and short-circuit conditions, choose a power supply rated higher than the TPS2543-Q1 current-limit setting.

11 Layout

11.1 Layout Guidelines

For the trace routing of DP_IN, DM_IN, DP_OUT, and DM_OUT: route these traces as micro-strips with nominal differential impedance of 90 Ω. Minimize the use of vias in the high-speed data lines. Keep the reference GND plane devoid from cuts or splits above the differential pairs to prevent impedance discontinuities. For more information, see the *High-Speed USB Platform Design Guidelines* from Intel.

The trace routing from the upstream regulator to the TPS2543-Q1 IN pin must as short as possible to reduce the voltage drop and parasitic inductance.

In order to meet IEC61000-4-2 level 4 ESD, external circuitry is required. Refer to the guidelines provided in the *Related Documentation* section.

The traces routing from the RILIM_HI and RILIM_LO resistors to the device must be as short as possible to reduce parasitic effects on the current-limit accuracy.

The thermal pad must be directly connected to the PCB ground plane using wide and short copper trace.

11.2 Layout Example

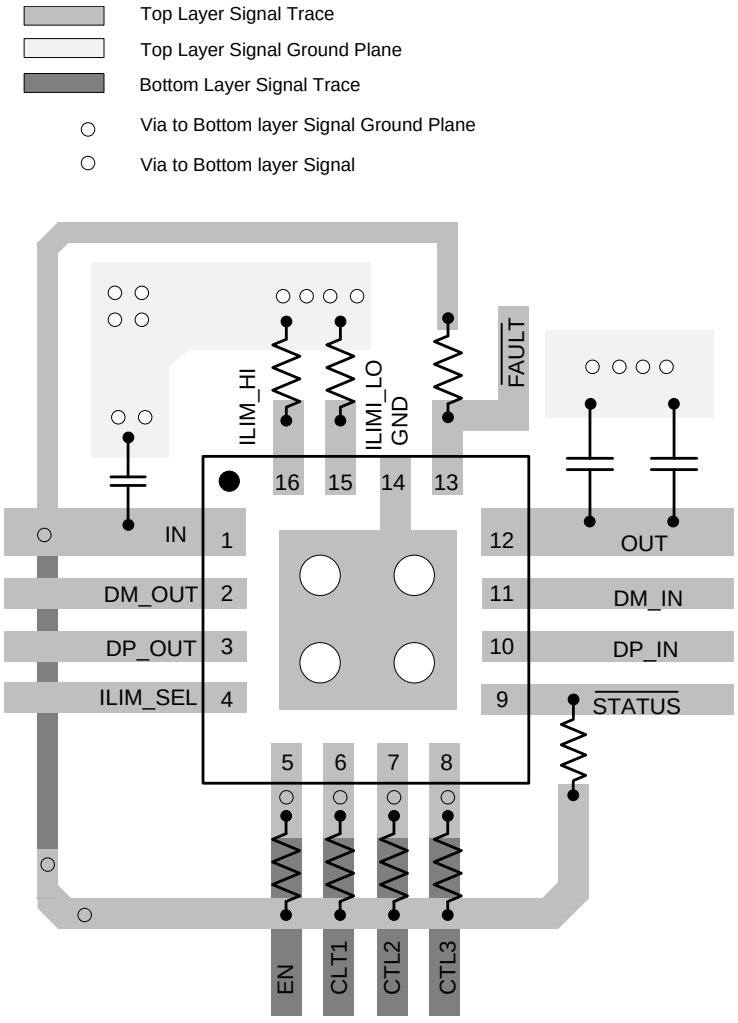


Figure 45. Layout Recommendation

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see:

Effective System ESD Protection for TPS254x USB Charging Port Controllers, SLVA796.

High Speed USB Platform Design Guidelines, Intel (www.usb.org/developers/docs/hs_usb_pdg_r1_0.pdf)

USB 2.0 Specifications (www.usb.org/developers/docs/usb20_docs/#usb20spec)

BC1.2 Battery Charging Specification (kinetis.pl/sites/default/files/BC1.2_FINAL.pdf)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2543QRTERQ1	NRND	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2543Q	
TPS2543QRTETQ1	NRND	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2543Q	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS2543-Q1 :

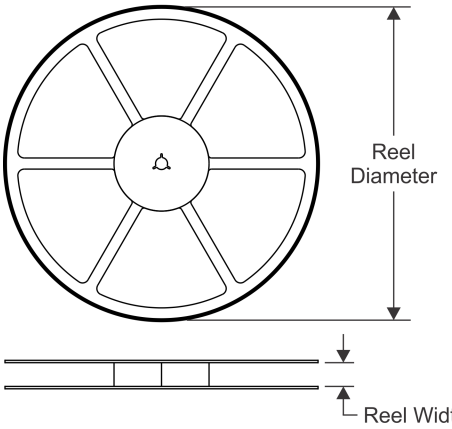
- Catalog: TPS2543

NOTE: Qualified Version Definitions:

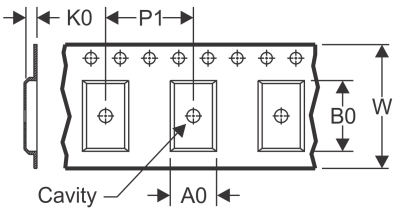
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

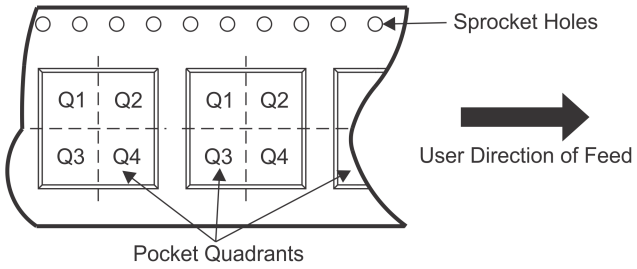


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

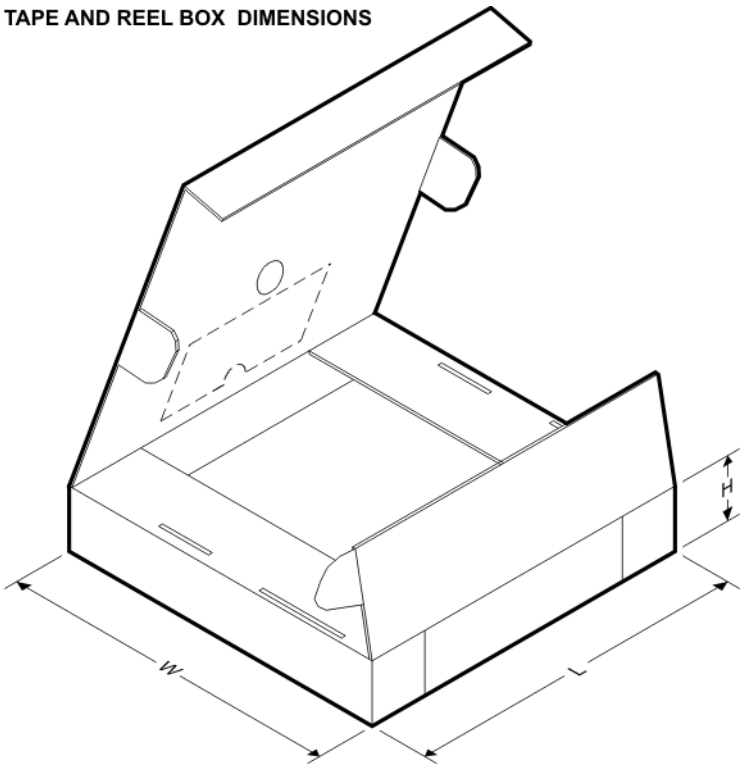
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2543QRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2543QRTETQ1	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

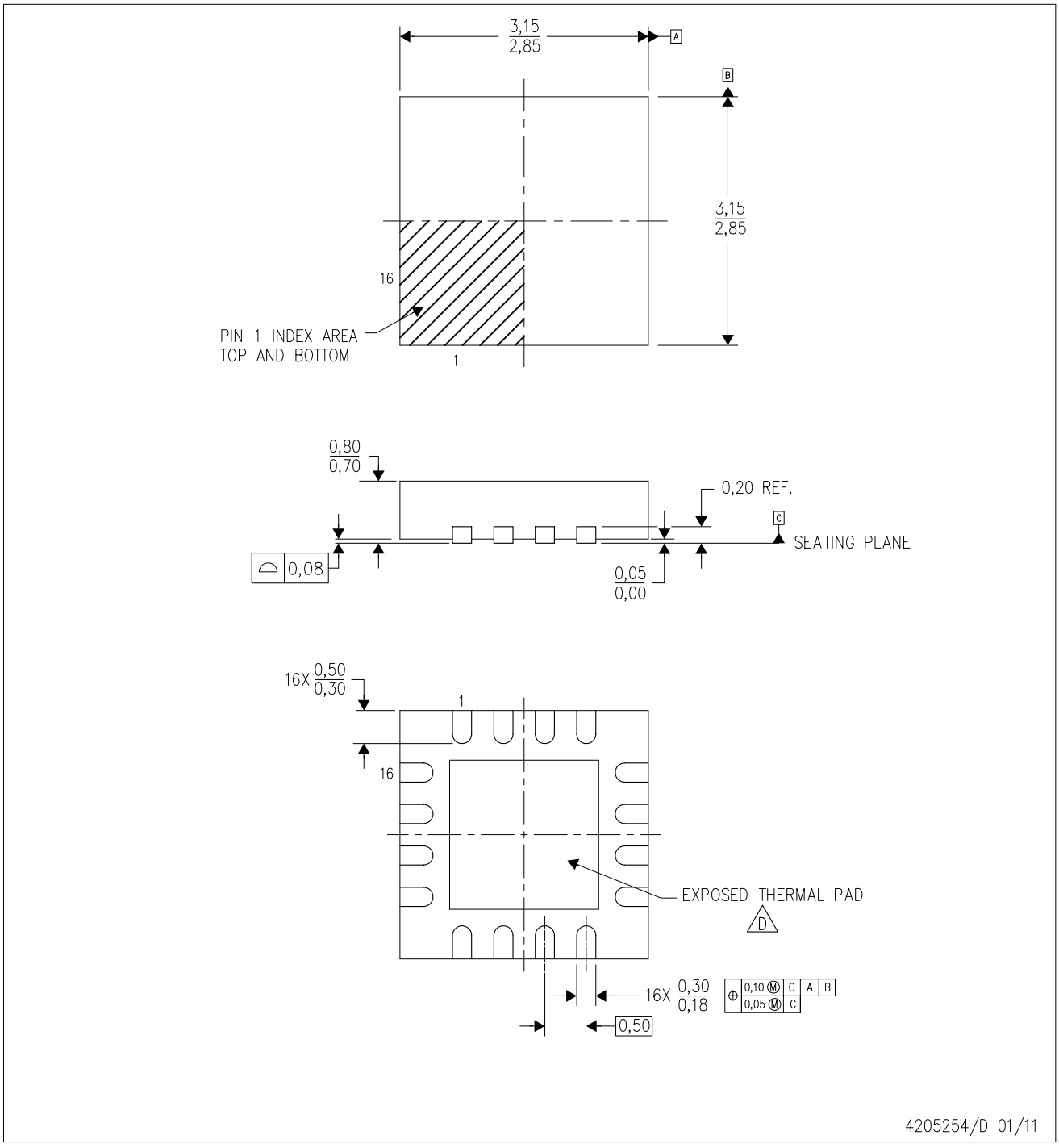
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2543QRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS2543QRTETQ1	WQFN	RTE	16	250	210.0	185.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

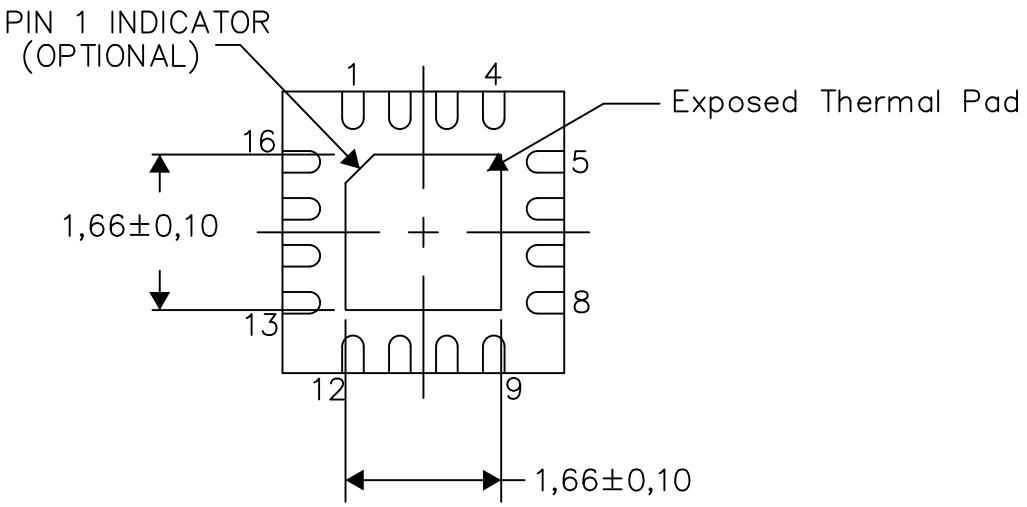
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



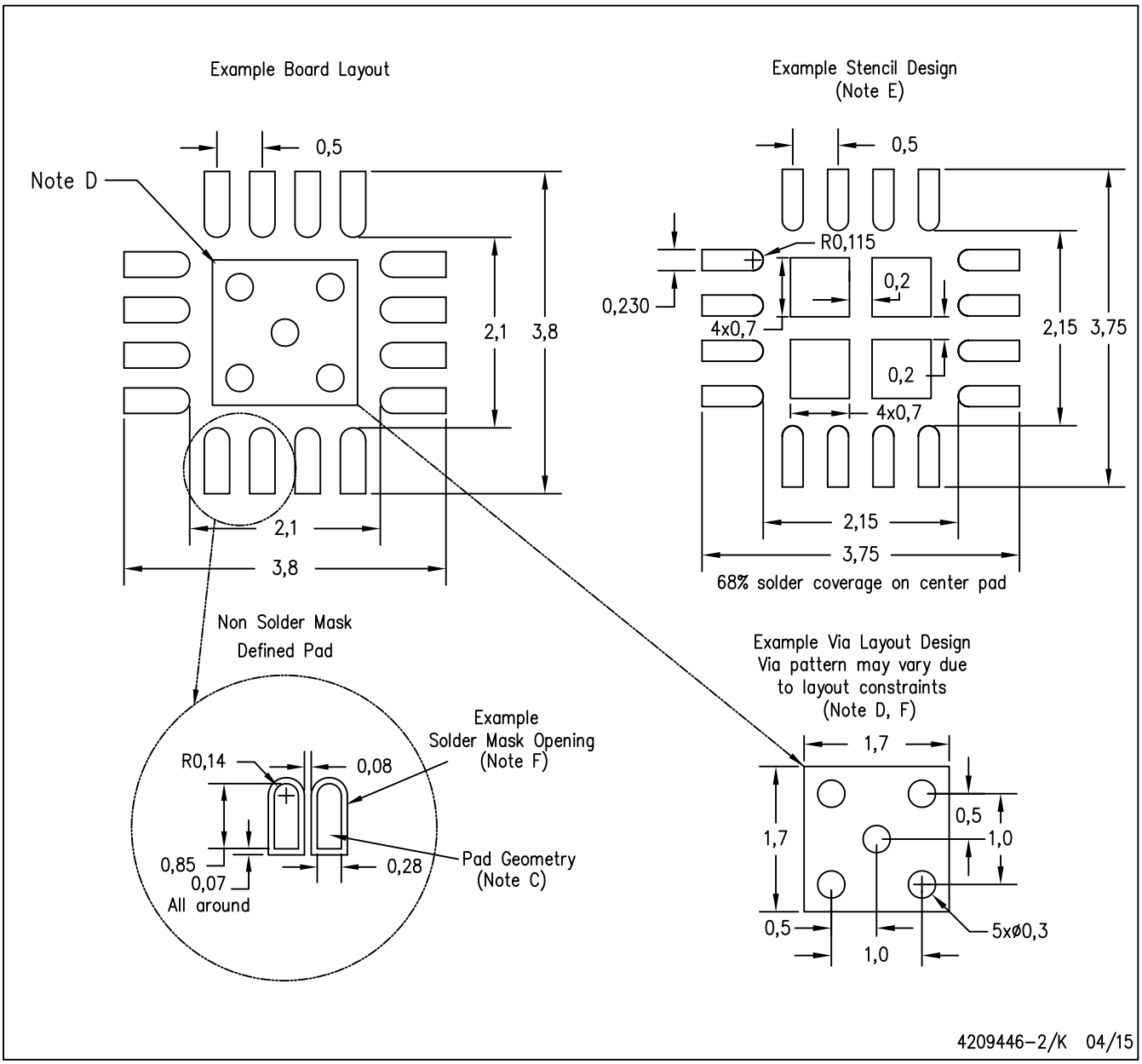
Bottom View

Exposed Thermal Pad Dimensions

4206446–8/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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