DLPC350 DLP® Digital Controller for DLP4500 and DLP4500NIR DMDs

1 Features

- Required for reliable operation of the DLP4500 and DLP4500NIR DMDs
- High-speed pattern display mode
  - 1-Bit binary pattern rates to 4225 Hz
  - 8-Bit grayscale pattern rates to 120 Hz
  - 1-to-1 input mapping to micromirrors
  - Multiple bit depths and LEDs in pattern sequences
- Easy synchronization with cameras and sensors
  - Two configurable input triggers
  - Two configurable output triggers
- 14 fully programmable GPIO signals
- 64 Mb internal RAM
  - Stores up to 48 1-bit patterns
  - No external volatile memory required
- Supports up to 32 MB external parallel flash for increased pattern storage
- Multiple configuration interfaces
  - One USB V1.1 slave port
  - Two I^2C ports
  - LED PWM generators
- Video display mode of operation
  - 10- to 120-Hz full color frame rates
  - YUV, YCrCb, or RGB input data formats
- Integrated micromirror drivers
- Integrated clock generation

2 Applications

- Machine vision
  - 3D depth measurement and capture
  - Robotic guidance
  - Inline surface inspection
  - Pick and place
- Spectrometers (chemical analysis)
  - Process analyzers
  - Laboratory equipment
  - Dedicated analyzers
- 3D printers
- Medical instruments
  - 3D dental scanners
  - Vascular imaging
  - Microscopes
- 3D biometrics
  - Fingerprint recognition
  - Facial recognition
- Single-pixel cameras
- Laser marking

3 Description

The DLPC350 digital controller is required for reliable operation of the DLP4500 or DLP4500NIR digital micromirror device (DMD). The DLPC350 controller provides a convenient, multi-functional interface between user electronics and the DMD, enabling high-speed pattern rates, along with LED control and data formatting for multiple input formats.

The DLPC350 controller provides input and output trigger signals for synchronizing displayed patterns with a camera, sensor, or other peripherals. The controller enables integration into small-form-factor and low-cost light steering applications. Applications include 3D scanning or metrology systems, spectrometers, interactive displays, chemical analyzers, medical instruments, and other end equipment that requires spatial light modulation (light steering and patterning).

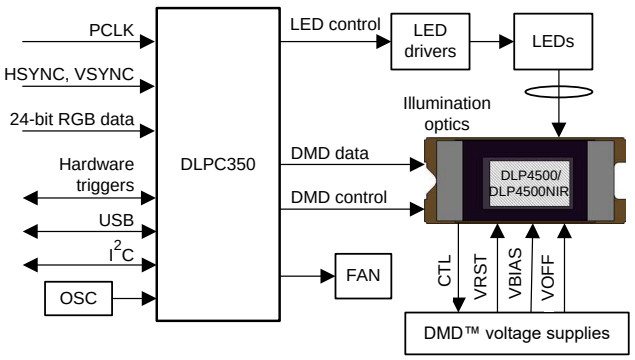
The DLPC350 controller is the data formatting and DMD controlling ASIC for either the visible or near-infrared (NIR) version of the DLP4500. For further details, please see the DLPR350 firmware homepage, the DLP4500 data sheet, and the DLP4500NIR data sheet.

Device Information[1]

ORDER NUMBER	PACKAGE	BODY SIZE
DLPC350	BGA (419)	23.4 mm × 23.4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (February 2018) to Revision F **Page**

- Added footnote specifying that signals are only captured at positive edge of P1A_CLK ... 16

Changes from Revision D (August 2016) to Revision E **Page**

- Corrected LEDx_PWM and LEDx_EN descriptions in *Pin Functions* table ... 9
- Added information about pullup resistor requirements on USB_DAT_P and other USB clarifying notes in *Pin Functions* table ... 9
- Changed FAN_LOCKED pin to indicate it is unimplemented and FAM_PWM pin to indicate it is not user controllable in *Pin Functions* table ... 10
- Corrected DMD interface setup and hold timings to be minimum values and updated the corresponding note ... 23
- Updated "pulse-duration modulation" to "pulse width modulation" in *Overview* subsection of *Detailed Description* ... 27
- Updated language concerning structured light applications related to the buffer, trigger modes, and video algorithms; also added additional requirements related to the maximum pattern speed in *Structured Light Applications* ... 31
- Added Table 7, which lists summaries of trigger modes, and updated corresponding descriptions ... 31
- Added DMD_TRC and DMD_LOADB to *Routing Priority* table ... 49
- Deleted mention of spread-spectrum clock, which is not supported ... 52
- Added MSL Peak Temp to *Packaging Information* ... 56

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Changes from Revision C (September 2013) to Revision D **Page**

- Changed title of datasheet to DLPC350 DLP Digital Controller for DLP4500 and DLP4500NIR DMDs ... 1
- Updated "High Speed Pattern Sequence Mode" to "High Speed Pattern Display Mode" in *Features* ... 1
- Corrected internal RAM space to 64 Mb and deleted redundant "Stores up to 48 1-Bit Patterns" ... 1
- Moved External Parallel Flash up to bullet point; changed 64 MB to 32 MB ... 1
- Changed "Video Projection Mode" to "Video Display Mode" ... 1
- Deleted "Extensive Video Processing Capability" ... 1
- Changed several phrases in description ... 1
- Changed "NIR" to "near-infrared (NIR)" ... 1
- Added direct links to DLPR350 firmware and DLP4500 data sheet ... 1
- Changed Description field of I2C_ADDR_SEL in Pin Function Descriptions ... 5
- Changed I2C bus max to reference *I^2C0 and I^2C1 Interface Timing Requirements*(1)(2)(3) in Pin Function Descriptions table ... 5
- Moved and changed "e.g. HDMI, BT656" in Pin Function Descriptions table ... 5
- Updated note on ICTSEN and TRST in description column of Pin Function Descriptions table ... 10
- Removed Machine Model ESD information from *ESD Ratings* ... 12
- Changed Operating junction temperature to 105°C in *Recommended Operating Conditions* ... 13
- Changed table notes for *I^2C0 and I^2C1 Interface Timing Requirements*(1)(2)(3) ... 15
- Added exception for 120 Hz source in *Source Input Blanking* ... 20
- Added VSYNC and HSYNC high value to Table 3 ... 20
- Added Table 4 ... 20
- Added Figure 7 ... 21
- Added clarification on putting DLPC350 in tri-state during JTAG boundary scan in *Board Level Test Support* ... 30
- Changed 48 bit-plane" to "48 1-bit planes ... 31
- Clarified wording about mapping options in *(LVDS) Receiver Supported Pixel Mapping Modes* ... 34
- Added Link to DLPR350 firmware page ... 36
- Corrected flash access read and write timing to fixed values ... 38
- Removed subsection Application Performance Plot and figure ... 40
- Changed Figure 23 to reference DLPC350 and INIT_BUSY timing to 2.3 s max ... 44
- Added DLPC350 Configuration and Support Firmware (DLPR350) in *Related Documentation* ... 55

Changes from Revision B (September 2013) to Revision C **Page**

- Updated to new TI standards and rearranged content for the new data sheet flow ... 1
- Clarified the description for POWER_ON_OFF pin in the Pin Function Descriptions ... 4
- Moved the pin descriptions as part of new data sheet flow ... 4
- Removed empty Conditions column from *Absolute Maximum Ratings* ... 12
- Separated the handling ratings from the absolute maximum ratings ... 12
- Removed empty Conditions column from the *Recommended Operating Conditions* table ... 13
- Added *Device and Documentation Support* section ... 54

Changes from Revision A (May 2013) to Revision B **Page**

- Added PIB_CLK and P1C_CLK to Pin Function Descriptions ... 5
- Deleted $\overline{\text{PM_CS_0}}$ from FLASH INTERFACE in Pin Function Descriptions ... 8
- Deleted Y16 and AB17 from the RESERVED PINS list in Pin Function Descriptions ... 10
- Added $\overline{\text{PM_CS_0}}$ to the RESERVED PINS LIST in Pin Function Descriptions ... 10

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- Deleted "PM_CS_0 - available for optional Flash device (≤ 128 Mb)" From the Program Memory Flash Interface section 38

Changes from Original (April 2013) to Revision A **Page**

- Changed the device From: Preview To: Production 1

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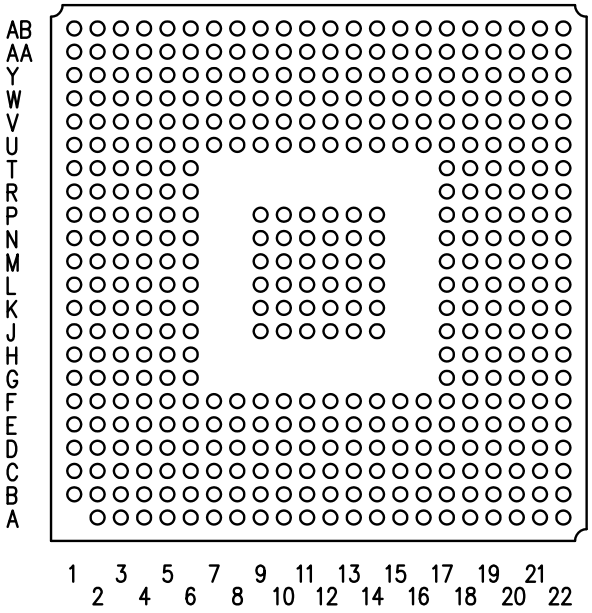
5 Pin Configuration and Functions

ZFF Package
419 Pins BGA
Bottom View



Pin Functions

PIN[1]		I/O POWER	I/O TYPE[2]	INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NUMBER					
CONTROL						
PWRGOOD	H19	VDDC	I_4 H		Async	PWRGOOD is an active high signal with hysteresis that is generated by an external power supply or voltage monitor. A high value indicates all power is within operating voltage specs and the system is safe to exit its reset state. A transition from high to low should indicate that the controller or DMD supply voltage will drop below their rated minimum level within the next 0.5 ms (POSENSE must remain active high during this interval). This is an early warning of an imminent power loss condition. This warning is required to enhance long-term DMD reliability. A DMD park sequence, followed by a full controller reset, is performed by the DLPC350 controller when PWRGOOD goes low for a minimum of 4 µs protecting the DMD. This minimum de-assertion time is used to protect the input from glitches. Following this, the DLPC350 controller is held in its reset state as long as PWRGOOD is low. PWRGOOD must be driven high for normal operation. The DLPC350 controller acknowledges PWRGOOD as active after it is driven high for a minimum of 625 ns. Utilizes hysteresis.
POSENSE	G21		I_4 H		Async	Power-On Sense is an active high input signal with hysteresis that is generated by an external voltage monitor circuit. POSENSE must be driven inactive (low) when any of the controller supply voltages are below minimum operating voltage specs. POSENSE must be active (high) when all controller supply voltages remain above minimum specs.
POWER_ON_OFF	N21	VDD33	B_2		Async	POWER_ON_OFF is an active high input signal which controls the DLPC350 standby feature. When this signal is externally driven high, the DLPC350 is commanded to active mode. When driven low, the DLPC350 is commanded to standby mode.

(1) See General Handling Guidelines for Unused CMOS-Type Pins in the Layout section for instructions on handling unused pins.
(2) I/O Type: I indicates input, O indicates output, B indicates bidirectional, and H indicates hysteresis. See Table 2 for subscript explanation.

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Pin Functions (continued)

PIN[1]		I/O POWER	I/O TYPE[2]	INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NUMBER					
EXT_PWR_ON	D21	VDD33	B_2		Async	Signal to host processor or power supply to indicate that the DLPC350 controller is powered on. Asserted just before INIT_DONE.
HOLD_IN_BOOT	D18	VDD33	B_2	External pullup required	N/A	
INIT_DONE	F19	VDD33	B_2		Async	Prior to transferring part of code from parallel flash content to internal memory, the internal memory is initialized and a memory test is performed. The result of this test (pass or fail) is recorded in the system status. If the memory test fails, the initialization process is halted. INIT_DONE is asserted twice to indicate an error situation. See Figure 23 and note that GPIO26 is the INIT_DONE signal.
I2C_ADDR_SEL	F21	VDD33	B_2		Async	This signal is sampled during power-up. If the signal is low, the I^2C slave addresses are 0x34 and 0x35. If the signal is high, the I^2C slave addresses are 0x3A and 0x3B. After the system has been initialized, this signal is available as a GPIO.
I2C1_SCL	J3	VDD33	B_2	Requires an external pullup to 3.3 V. The minimum acceptable pullup value is 1 kΩ.	N/A	I^2C clock. bidirectional, open-drain signal. I^2C slave clock input from the external processor. This bus supports the frequency as specified in *I^2C0 and I^2C1 Interface Timing Requirements*[3][4][5].
I2C1_SDA	J4	VDD33	B_2	Requires an external pullup to 3.3 V. The minimum acceptable pullup value is 1 kΩ.	I2C1_SCL	I^2C data. bidirectional, open drain signal. I^2C slave to accept command or transfer data to and from the external processor. This bus supports the frequency as specified in *I^2C0 and I^2C1 Interface Timing Requirements*[3][4][5].
I2C0_SCL	M2	VDD33	B_8	Requires an external pullup to 3.3 V. The minimum acceptable pullup value is 1 kΩ. This input is not 5-V tolerant.	N/A	I^2C Bus 0, Clock; I^2C master for on-board peripherals such as temperature sensor. This bus supports the frequency as specified in *I^2C0 and I^2C1 Interface Timing Requirements*[3][4][5].
I2C0_SDA	M3	VDD33	B_8	Requires an external pullup to 3.3 V. The minimum acceptable pullup value is 1 kΩ. This input is not 5-V tolerant.	I2C0_SCL	I^2C Bus 0, Data; I^2C master for on-board peripherals such as temperature sensor. This bus supports the frequency as specified in *I^2C0 and I^2C1 Interface Timing Requirements*[3][4][5].
SYSTEM CLOCK						
MOSC	A14	VDD33	I_{10}		N/A	System clock oscillator input (3.3-V LVCMOS). Note that the MOSC must be stable a maximum of 25 ms after POSENSE transitions from high to low.
MOSCN	A15	VDD33	O_{10}		N/A	MOSC crystal return
PORT 1: PARALLEL VIDEO/GRAPHICS INPUT[6] [7] [8]						
P1A_CLK	W15	VDD33	I_4	Includes an internal pulldown	N/A	Port 1 input data pixel write clock 'A'
P1B_CLK	AB17	VDD33	I_4	Includes an internal pulldown	N/A	Port 1 input data pixel write clock 'B'
P1C_CLK	Y16	VDD33	I_4	Includes an internal pulldown	N/A	Port 1 input data pixel write clock 'C'
P1_VSYNC	Y15	VDD33	B_1 H	Includes an internal pulldown	P1A_CLK	Port 1 vertical sync; utilizes hysteresis
P1_HSYNC	AB16	VDD33	B_1 H	Includes an internal pulldown	P1A_CLK	Port 1 horizontal sync; utilizes hysteresis

(3) Meets I^2C timing per the I^2C Bus Specification, unless otherwise noted. For reference see version 2.1 of the Phillips/NXP specification.
(4) The maximum clock frequency does not account for rise time, nor added capacitance of PCB or external components which may adversely impact this value.
(5) By definition, I^2C transactions operate at the speed of the slowest device on the bus and thus there is no requirement to match the speed grade of all devices in the system. However if Full-speed operation is desired, it will be necessary to ensure the other I^2C devices support full-speed operation as well. In addition to other devices slowing down bus operation, the length of the line (due to its capacitance) and the value of the I^2C pullup resistors will also influence the max achievable speed.
(6) Port 1 can be used to support multiple source options (e.g. HDMI, BT656) for a given product. To do so, the data bus from both source components must be connected to the same port 1 pins and control given to the DLPC350 to 3-state the "inactive" source. Tying them together like this will cause some signal degradation due to reflections on the 3-stated path.
(7) The A, B, and C input data channels of Port 1 can be internally swapped for optimum board layout.
(8) Sources feeding less than the full 10-bits per color component channel should be MSB justified when connected to the DLPC350 and LSBs tied off to zero. For example, an 8-bit per color input should be connected to bits 9:2 of the corresponding A, B, or C input channel. BT656 are 8 or 10 bits in width. If a BT656 type input is utilized, the data bits must be MSB justified as with the other types of input sources on either of the A, B, or C data input channels.

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Pin Functions (continued)

PIN[1]		I/O POWER	I/O TYPE[2]	INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NUMBER					
P1_DATEN	AA16	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 data enable
P1_FIELD	W14	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 field sync; required for interlaced sources only (and not progressive)
P1_A_9	AB20	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 128)
P1_A_8	AA19	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 64)
P1_A_7	Y18	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 32)
P1_A_6	W17	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 16)
P1_A_5	AB19	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 8)
P1_A_4	AA18	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 4)
P1_A_3	Y17	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 2)
P1_A_2	AB18	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 1)
P1_A_1	W16	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 0.5)
P1_A_0	AA17	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 0.25)
P1_B_9	U21	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 128)
P1_B_8	U20	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 64)
P1_B_7	V22	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 32)
P1_B_6	U19	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 16)
P1_B_5	V21	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 8)
P1_B_4	W22	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 4)
P1_B_3	W21	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 2)
P1_B_2	AA20	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 1)
P1_B_1	Y19	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 0.5)
P1_B_0	W18	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 0.25)
P1_C_9	P21	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 128)
P1_C_8	P22	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 64)
P1_C_7	R19	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 32)
P1_C_6	R20	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 16)
P1_C_5	R21	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 8)
P1_C_4	R22	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 4)
P1_C_3	T21	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 2)
P1_C_2	T20	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 1)
P1_C_1	T19	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 0.5)
P1_C_0	U22	VDD33	I_4	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 0.25)
PORT 2: FPD-LINK COMPATIBLE VIDEO/GRAPHICS INPUT[9]						
RCK_IN_P	Y9	VDD33_FPD	I_5	Includes weak internal pulldown	N/A	Positive differential input signal for Clock, FPD-Link receiver
RCK_IN_N	W9	VDD33_FPD	I_5	Includes weak internal pulldown	N/A	Negative differential input signal for Clock, FPD-Link receiver
RA_IN_P	AB10	VDD33_FPD	I_5	Includes weak internal pulldown	RCK_IN	Positive differential input signal for data channel A, FPD-Link receiver
RA_IN_N	AA10	VDD33_FPD	I_5	Includes weak internal pulldown	RCK_IN	Negative differential input signal for data channel A, FPD-Link receiver
RB_IN_P	Y11	VDD33_FPD	I_5	Includes weak internal pulldown	RCK_IN	Positive differential input signal for data channel B, FPD-Link receiver
RB_IN_N	W11	VDD33_FPD	I_5	Includes weak internal pulldown	RCK_IN	Negative differential input signal for data channel B, FPD-Link receiver
RC_IN_P	AB12	VDD33_FPD	I_5	Includes weak internal pulldown	RCK_IN	Positive differential input signal for data channel C, FPD-Link receiver

(9) Port 2 is a single-channel FPD-Link compatible input interface. FPD-Link is a defacto industry standard flat-panel display interface, which utilizes the high bandwidth capabilities of LVDS signaling to serialize video or graphics data down to a couple wires to provide a low wire count and low EMI interface. Port 2 supports sources rates up to a maximum effective clock of 90 MHz. The Port 2 input pixel data must adhere to one of four supported data mapping formats (see Table 9). Given that Port 2 inputs contain weak pulldown resistors, they can be left floating when not used.

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Pin Functions (continued)

PIN[1]		I/O POWER	I/O TYPE[2]	INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NUMBER					
RC_IN_N	AA12	VDD33_FPD	I_5	Includes weak internal pulldown	RCK_IN	Negative differential input signal for data channel C, FPD-Link receiver
RD_IN_P	Y13	VDD33_FPD	I_5	Includes weak internal pulldown	RCK_IN	Positive differential input signal for data channel D, FPD-Link receiver
RD_IN_N	W13	VDD33_FPD	I_5	Includes weak internal pulldown	RCK_IN	Negative differential input signal for data channel D, FPD-Link receiver
RE_IN_P	AB14	VDD33_FPD	I_5	Includes weak internal pulldown	RCK_IN	Positive differential input signal for data channel E, FPD-Link receiver
RE_IN_N	AA14	VDD33_FPD	I_5	Includes weak internal pulldown	RCK_IN	Negative differential input signal for data channel E, FPD-Link receiver
DMD INTERFACE						
DMD_D0	A8	VDD_DMD	O_7		DMD_DCLK	DMD data pins. DMD data pins are double data rate (DDR) signals that are clocked on both edges of DMD_DCLK. All 24 DMD data signals are use to interface to the DMD.
DMD_D1	B8					
DMD_D2	C8					
DMD_D3	D8					
DMD_D4	B11					
DMD_D5	C11					
DMD_D6	D11					
DMD_D7	E11					
DMD_D8	C7					
DMD_D9	B10					
DMD_D10	E7					
DMD_D11	D10					
DMD_D12	A6					
DMD_D13	A12					
DMD_D14	B12					
DMD_D15	C12					
DMD_D16	D12					
DMD_D17	B7					
DMD_D18	A10					
DMD_D19	D7					
DMD_D20	B6					
DMD_D21	E9					
DMD_D22	C10					
DMD_D23	C6					
DMD_DCLK	A9	VDD_DMD	O_7		N/A	DMD data clock (DDR)
$\overline{\text{DMD_LOADB}}$	B9	VDD_DMD	O_7		DMD_DCLK	DMD data load signal (active-low)
DMD_SCTRL	C9	VDD_DMD	O_7		DMD_DCLK	DMD data serial control signal
DMD_TRC	D9	VDD_DMD	O_7		DMD_DCLK	DMD data toggle rate control
DMD_DRC_BUS	D5	VDD_DMD	O_7		DMD_SAC_CLK	DMD reset control bus data
DMD_DRC_STRB	C5	VDD_DMD	O_7		DMD_SAC_CLK	DMD reset control bus strobe
$\overline{\text{DMD_DRC_OE}}$	B5	VDD_DMD	O_7	Requires a 30 to 51-kΩ external pullup resistor to VDD_DMD.	Async	DMD reset control enable (active-low)
DMD_SAC_BUS	D6	VDD_DMD	O7		DMD_SAC_CLK	DMD stepped-address control bus data
DMD_SAC_CLK	A5	VDD_DMD	O_7		N/A	DMD stepped-address control bus clock
DMD_PWR_EN	G20	VDD_DMD	O_2		Async	DMD Power Enable control. This signal indicates to an external regulator that the DMD is powered.
$\overline{\text{EXRES}}$	A3		O		Async	DMD drive strength adjustment precision reference. A ± 1% external precision resistor should be connected to this pin.

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Pin Functions (continued)

PIN[1]		I/O POWER	I/O TYPE[2]	INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NUMBER					
FLASH INTERFACE						
PM_CS_1	U2	VDD33	O_2		Async	Boot flash (active low). Required for boot memory
PM_CS_2	U1	VDD33	O_2		Async	Optional for additional flash (up to 128 Mb)
PM_ADDR_22	V3	VDD33	B_2		Async	Flash memory address bit
PM_ADDR_21	W1					
PM_ADDR_20	W2		O_2			
PM_ADDR_19	Y1					
PM_ADDR_18	AB2					
PM_ADDR_17	AA3					
PM_ADDR_16	Y4					
PM_ADDR_15	W5					
PM_ADDR_14	AB3					
PM_ADDR_13	AA4					
PM_ADDR_12	Y5					
PM_ADDR_11	W6					
PM_ADDR_10	AB4					
PM_ADDR_9	AA5					
PM_ADDR_8	Y6					
PM_ADDR_7	W7					
PM_ADDR_6	AB5					
PM_ADDR_5	AA6					
PM_ADDR_4	Y7					
PM_ADDR_3	AB6					
PM_ADDR_2	W8					
PM_ADDR_1	AA7					
PM_ADDR_0	AB7					
PM_WE	V2	VDD33	O_2		Async	Write enable (active low)
PM_OE	U4	VDD33	O_2		Async	Output enable (active low)
PM_BLS_1	AA8	VDD33	O_2		Async	Upper byte(15:8) enable
PM_BLS_0	AB8	VDD33	O_2		Async	Lower byte(7:0) enable
PM_DATA_15	M1	VDD33	B_2		Async	Data bits, upper byte
PM_DATA_14	N1					
PM_DATA_13	N2					
PM_DATA_12	N3					
PM_DATA_11	N4					
PM_DATA_10	P1					
PM_DATA_9	P2					
PM_DATA_8	P3					
PM_DATA_7	P4	VDD33	B_2		Async	Data bits, lower byte
PM_DATA_6	R2					
PM_DATA_5	R3					
PM_DATA_4	R4					
PM_DATA_3	T1					
PM_DATA_2	T2					
PM_DATA_1	T3					
PM_DATA_0	T4					
LED DRIVER INTERFACE						
HEARTBEAT	C16	VDD33	B_2		Async	LED blinks continuously (heartbeat) to indicate the system is operational. The period is one second with a 50% duty cycle.
FAULT_STATUS	B16	VDD33	B_2		Async	LED off indicates any system fault

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Pin Functions (continued)

PIN[1]		I/O POWER	I/O TYPE[2]	INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NUMBER					
LEDR_PWM	K2	VDD33	O_2		Async	LED red PWM output
LEDG_PWM	K3					LED green PWM output
LEDB_PWM	K4					LED blue PWM output
LEDR_EN	L3	VDD33	O_2		Async	LED red PWM output enable control
LEDG_EN	L4					LED green PWM output enable control
LEDB_EN	K1					LED blue PWM output enable control
TRIGGER CONTROL						
TRIG_IN_1	G19	VDD33	B_2		Async	In trigger mode 1, this signal is used to advance the pattern display. In trigger mode 2, the rising edge displays the pattern and the falling edge displays the next indexed pattern.
TRIG_IN_2	F22	VDD33	B_2		Async	In trigger mode 1, this signal is used to start (rising edge) and stop (falling edge) the pattern display. It works along with the software start and stop command. In trigger mode 2, this signal is used to advance the pattern by two indexes.
TRIG_OUT_1	C17	VDD33	B_2		Async	Active high trigger output signal during pattern exposure
TRIG_OUT_2	K21	VDD33	B_2		Async	Active high trigger output to indicate first pattern display
PERIPHERAL INTERFACE						
USB_DAT_N	E3	VDD33	B_9		Async	USB D– I/O for USB 1.1 full speed command interface. TI strongly recommends a 5.0-W external series resistance (of 22 Ω) to limit the potential impact of a continuous short circuit between USB_DAT_N and either V_{BUS}, GND, the other data line, or the cable. For additional protection, an optional 200-mA Shottky diode from USB_DAT_N to VDD33 can also be added.
USB_DAT_P	E2					USB D+ I/O for USB 1.1 full speed command interface. TI strongly recommends a 5.0-W external series resistance (of 22 Ω) to limit the potential impact of a continuous short circuit between USB_DAT_P and either V_{BUS}, GND, the other data line, or the cable. For additional protection, an optional 200-mA Shottky diode from USB_DAT_P to VDD33 can also be added. The pin is required to be pulled high to 3.3V through a 1.5 KΩ resistor after the USB is enabled for correct operation.
$\overline{\text{USB_EN}}$	C18	VDD33	B_2		Async	USB enable
UART_TXD	L19	VDD33	O_2		Async	Transmit data output. Reserved for debug messages
UART_RXD	L21	VDD33	I_4		Async	Receive data input. Reserved for debug messages
$\overline{\text{UART_RTS}}$	M19	VDD33	O_2		Async	Ready to send hardware flow control output. Reserved for debug messages
$\overline{\text{UART_CTS}}$	L20	VDD33	I_4		Async	Clear to send hardware flow control input. Reserved for debug messages
GPIOS [10]						**ALTERNATIVE MODE**
GPIO_36	G1	VDD33	B_2		Async	None
GPIO_35	H4	VDD33	B_2		Async	None
GPIO_34	H3	VDD33	B_2		Async	None
GPIO_33	H2	VDD33	B_2		Async	None
GPIO_29	F20	VDD33	B_2		Async	None
GPIO_28	E22	VDD33	B_2		Async	None
GPIO_27	E21	VDD33	B_2		Async	None
GPIO_25	D22	VDD33	B_2		Async	None
GPIO_24	E20	VDD33	B_2		Async	None
GPIO_21	N20	VDD33	B_2		Async	None
GPIO_20	N19	VDD33	B_2		Async	None

(10) GPIO signals must be configured via software for input, output, bidirectional, or open-drain. Some GPIOs have one or more "alternative use" modes which are also software configurable. The reset default for all optional GPIOs is as an input signal. However, any alternate function connected to these GPIO pins with the exception of General Purpose Clocks and PWM Generation, will be reset. An external pullup to the 3.3-V supply is required for each signal configured as open-drain. External pullup or pulldown resistors may be required to ensure stable operation before software is able to configure these ports.

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Pin Functions (continued)

PIN[1]		I/O POWER	I/O TYPE[2]	INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NUMBER					
GPIO_15	B19	VDD33	B_2		Async	None
GPIO_14	B18	VDD33	B_2		Async	None
GPIO_13	L2	VDD33	B_2		Async	None
GPIO_12	M4	VDD33	B_2		Async	OCLKD (Output)
GPIO_11	A19	VDD33	B_2		Async	OCLKC (Output)
GPIO_06	A18	VDD33	B_2		Async	PWM_IN_1 (Input)
GPIO_05	D16	VDD33	B_2		Async	PWM_IN_0 (Input)
GPIO_02	A17	VDD33	B_2		Async	PWM_STD_2 (Output)
GPIO_00	C15	VDD33	B_2		Async	PWM_STD_0 (Output)
FAN_LOCKED	B17	VDD33	B_2		Async	Feedback from fan to indicate fan is connected and running (unimplemented, pull high through 3.3 kΩ resistor)
FAN_PWM	D15	VDD33	B_2		Async	Fan PWM speed control (not user controllable, defaults to output 1% duty cycle to enable running fan near maximum speed)
CONTROLLER MANUFACTURER TEST SUPPORT						
HW_TEST_EN	V7	VDD33	I_4 H	Includes internal pulldown	N/A	Reserved for test. Should be connected directly to ground on the PCB for normal operation
BOARD LEVEL TEST AND DEBUG						
TDI	P18	VDD33	I_4	Includes internal pullup	TCK	JTAG serial data in.[11]
TCK	R18	VDD33	I_4	Includes internal pullup	N/A	JTAG serial data clock.[11]
TMS1	V15	VDD33	I_4	Includes internal pullup	TCK	JTAG test mode select.[11]
TDO1	L18	VDD33	O_1		TCK	JTAG serial data out.[11]
$\overline{\text{TRST}}$	V17	VDD33	I_4 H	Includes internal pullup	Async	JTAG, RESET (active-low). This pin should be pulled high (or left unconnected) when the JTAG interface is in use for boundary scan. Connect this pin to ground otherwise. Failure to tie this pin low during normal operation causes startup and initialization problems.[11]
RTCK	G18	VDD33	O_2		N/A	JTAG return clock.[12]
ICTSEN	V6	VDD33	I_4 H	Includes internal pulldown. External pulldown recommended for added protection.	Async	IC 3-State Enable (active high). Asserting high 3-states all outputs except the JTAG interface. ICTSEN and $\overline{\text{TRST}}$ should be electrically tied together to put IC pins in tri-state during JTAG boundary scan operations in case other chips exist on the board interfacing with DLPC350.
RESERVED PINS						
RESERVED	N22, M22, P19, P20	VDD33	I_4	Includes an internal pulldown	N/A	Reserved[12]
RESERVED	V16	VDD33	I_4	Includes an internal pullup	N/A	
RESERVED	D1, J2	VDD33	I_4		N/A	
RESERVED	F1, F2, G2, G3, G4	VDD33	O_2	Includes internal pulldown	N/A	Leave these pins unconnected[12]
RESERVED	F3, J1, M21, U3	VDD33	O_2		N/A	
RESERVED	H20, M18, M20	VDD33	O_1		N/A	
RESERVED	H21, H22, J19, J20, J21, J22, K19, K20	VDD33	B_2	Includes internal pulldown	N/A	Reserved[12]
RESERVED	C1, D2, F4	VDD33	B_2		N/A	

(11) All JTAG signals are LVCMOS compatible.
(12) See General Handling Guidelines for Unused CMOS-Type Pins in the Layout section for instructions on handling unused pins.

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Table 1. Power and Ground Pin Descriptions

POWER GROUP	PIN NUMBER	DESCRIPTION
PLLM_VSS	B15	Master clock generator PLL ground return
PLLM_VDD	E14	1.2-V master clock generator PLL digital power(1)
PLLM_VAD	D14	1.8-V master clock generator PLL analog power(1)
PLLM_VAS	C14	Master clock generator PLL ground return
PLLD_VSS	B14	DDR clock generator PLL ground return
PLLD_VDD	E13	1.2-V DDR clock generator PLL digital power
PLLD_VAD	D13	1.8-V DDR clock generator PLL analog power(1)
PLLD_VAS	C13	DDR clock generator PLL ground return
VSS	E5, D4, C3, B2, A2, N6, F11, J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14, H1, B1, C2, D3, E4, V5, W4, Y3, AA1, AA2, U8, U15, A21, A22, B21, B22, C20, D19, E18, V18, W19, Y20, AA21, AB22, M17, C22, C21, D20, E19, K22, L22, V19, V20, W20, Y21, R1, Y2, W3, V4, F9, A7, B3, B4, C4, A13, B13, B20, C19, Y14, Y12, W12, W10, Y10, AA13, AB13, AA11, AB11, Y8, AA9, F14, V14, V8	Common Ground (105)
VDDC	F12, F7, F6, G6, M6, F5, G5, M5, U6, U7, F17, G17, U16, U17, F18, N17, U18, U5, F16, E6, E12, E17, K6, L6, P6, R6, K17, L17, P17, R17	Core 1.2-V Power
VDD33	AB1, F15, T5, T6, AA22, H6, J6, L1, E1, H5, J5, K5, L5, N5, P5, U9, U14, H17, J17, T17, Y22, T22, G22, H18, J18, N18, R5, V1, A20, A16, E15, V9, AA15, AB15, AB21, AB9, T18, K18, F13	LVCMOS I/O 3.3-V Power
VDD_DMD	F10, F8, A4, A11, E8, E10	1.9-V DMD interface voltage
VDD12_FPD	U11, U12, V12, V11	FPD-Link LVDS interface 1.2-V power(1)
VDD33_FPD	U10, U13, V13, V10	FPD-Link LVDS interface 3.3-V power(1)
Spare	E16	TI recommends that this signal be tied to ground via an external pulldown resistor
VPGM	D17	Fuse programming pin (for manufacturing use only); this signal should be tied directly to ground for normal operation

(1) Special filter is required for proper operation. See *Recommended DLPC350 PLL Layout Configuration*.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
Supply Voltage(2) (3)	VDDC (Core 1.2-V Power)	–0.5	1.7	V
	VDD33	–0.5	3.8	V
	VDD_DMD	–0.5	2.3	V
	VDD12_FPD	–0.5	1.7	V
	VDD33_FPD	–0.5	3.8	V
	VDD12_PLLD	–0.5	1.7	V
	VDD12_PLLM	–0.5	1.7	V
	VDD_18_PLLD	–0.5	2.3	V
	VDD_18_PLLM	–0.5	2.3	V
Input Voltage (V_I)(4)	USB	–1.00	5.25	V
	OSC	–0.3	3.6	V
	LVCMOS	–0.5	3.6	V
	I^2C	–0.5	3.6	V
	LVDS	–0.5	3.6	V
Output Voltage (V_O)	USB	–1.00	5.25	V
	DMD LPDDR	–0.3	2.0	V
	LVCMOS	–0.5	3.6	V
	I^2C	–0.5	3.6	V
T_J	Junction temperature	0	105	ºC
T_{stg}	Storage temperature	-40	125	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to VSS (ground).
(3) All of the 3.3-V, 1.9-V, 1.8-V, and 1.2-V power should be applied and removed per the procedure defined in System Power and Reset.
(4) Applies to external input and bidirectional buffers.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD} (1)	Electrostatic discharge immunity	Human body model (HBM)(2)	±2000	V
		Charged device model (CDM)(3)	±500	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

		MIN	NOM	MAX	UNIT
VDD33	3.3 V supply voltage, I/O	3.135	3.300	3.465	V
VDD_DMD	1.9 V supply voltage, I/O	1.8	1.9	2.0	
VDD_18_PLLD	1.8 V supply voltage, PLL analog	1.71	1.80	1.89	
VDD_18_PLLM	1.8 V supply voltage, PLL analog	1.71	1.80	1.89	
VDD12	1.2 V supply voltage, core logic	1.116	1.200	1.26	
VDD12_PLLD	1.2 V supply voltage, PLL digital	1.116	1.200	1.26	
VDD12_PLLM	1.2 V supply voltage, PLL digital	1.116	1.200	1.26	
V_I	USB	0		VDD33	V
	OSC	0		VDD33	
	3.3-V LVCMOS	0		VDD33	
	3.3-V I^2C	0		VDD33	
	3.3-V LVDS	0.6		2.2	
V_O	USB	0		VDD33	V
	3.3-V LVCMOS	0		VDD33	
	3.3-V I^2C	0		VDD33	
	1.9-V LPDDR	0		VDD_DMD	
T_J	Operating junction temperature	0		105	ºC

6.4 Thermal Information

THERMAL METRIC		DLPC350 BGA (ZFF) 419 PINS	UNIT
$R_{\theta JC}$ (1)	Junction-to-case thermal resistance	6.6	°C/W
$R_{\theta JA}$ at 0 m/s of forced airflow (2)	Junction-to-air thermal resistance	19.4	°C/W
$R_{\theta JA}$ at 1 m/s of forced airflow (2)	Junction-to-air thermal resistance	16.7	°C/W
$R_{\theta JA}$ at 2 m/s of forced airflow (2)	Junction-to-air thermal resistance	15.8	°C/W
φ_{jt} (3)	Temperature variance from junction to package top center temperature, per unit power dissipation	0.33	°C/W

(1) $R_{\theta JC}$ analysis assumptions: The heat generated in the chip flows both into over-mold (top side) and into the package laminate (bottom side) and then into the PCB via package solder balls. This should be used for heat sink analysis only.
(2) Thermal coefficients abide by JEDEC Standard 51. $R_{\theta JA}$ is the thermal resistance of the package as measured using a JEDEC defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC350 PCB and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance.
(3) Example: (3 W) × (0.33 °C/W) = approximately a 1.00°C temperature rise.

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6.5 I/O Electrical Characteristics

Voltage and current characteristics for each I/O type signal. All inputs and outputs are LVCMOS. Over operating free-air temperature range (unless otherwise noted).

PARAMETER[1]			TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{IH}	High-level input voltage	USB (9)		2.0			V
		OSC (10)		2.0			
		3.3-V LVCMOS (1, 2, 3, 4)		2.0			
		3.3-V I^2C (8)		2.4			
V_{IL}	Low-level input voltage	USB (9)				0.8	V
		OSC (10)				0.8	
		3.3-V LVCMOS (1, 2, 3, 4)				0.8	
		3.3-V I^2C				1.0	
V_{OH}	High-level output voltage	USB (9)		2.8			V
		3.3-V LVCMOS (1, 2, 3)	I_{OH} = Max Rated	2.8			
		1.9-V DMD LPDDR (7)	I_{OH} = –0.1 mA	0.9 × VDD_DMD			
V_{OL}	Low-level output voltage	USB (9)				0.3	V
		3.3-V LVCMOS (1, 2, 3)	I_{OL} = Max Rated			0.4	
		1.9-V DMD LPDDR (7)	I_{OL} = +0.1 mA			0.1 × VDD_DMD	
		3.3-V I^2C (8)	I_{OL} = 3 mA sink			0.4	
V_{IDTH}	Input differential threshold	3.3-V LVDS (5)		–200		200	mV
$\|V_{ID}\|$	Absolute input differential voltage	USB (9)		200			mV
		3.3-V LVDS (5)		200		600	
V_{ICM}	Input Common Mode Voltage Range	USB (9)		0.8		2.5	V
		3.3-V LVDS (5)	At MIN absolute input differential voltage	0.7		2.1	
		3.3-V LVDS (5)	At MAX absolute input differential voltage	0.9		1.9	
V_{HYS}	Hysteresis ($V_{T+} – V_{T–}$)	3.3-V LVCMOS (1, 2, 3, 4)			400		mV
		3.3-V I^2C (8)			550		
		USB (9)			320		
R_I	Receiver input impedance	3.3-V LVDS (5)	VDDH = 3.3 V	90	110	132	Ω
I_{IH}	High-level input current (IPD = internal pulldown)	USB (9)				10	µA
		OSC (10)				10	
		3.3-V LVCMOS (1, 2, 3, 4) without IPD	V_{IH} = VDD33			10	
		3.3-V LVCMOS (1, 2, 3, 4) with IPD	V_{IH} = VDD33			200	
		3.3-V I^2C (8)	V_{IH} = VDD33			10	
I_{IL}	Low-level input current(IPU = internal pullup)	USB (9)				–10	µA
		OSC (10)				–10	
		3.3-V LVCMOS (1, 2, 3, 4) without IPU	V_{OH} = VDD33			–10	
		3.3-V LVCMOS (1, 2, 3, 4) with IPU	V_{OH} = VDD33			–200	
		3.3-V I^2C (8)	V_{OH} = VDD33			–10	

(1) Numbers in parentheses correspond with *I/O Type Definition*.

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I/O Electrical Characteristics (continued)

Voltage and current characteristics for each I/O type signal. All inputs and outputs are LVCMOS. Over operating free-air temperature range (unless otherwise noted).

PARAMETER[1]			TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{OH}	High-level output current	USB (9)		17.08			mA
		1.9-V DMD LPDDR (7)	V_O = 1.5 V	–4.0			
		3.3-V LVCMOS (1)	V_O = 2.4 V	–4.0			
		3.3-V LVCMOS (2)	V_O = 2.4 V	–8.0			
		3.3-V LVCMOS (3)	V_O = 2.4 V	–12.0			
I_{OL}	Low-level output current	USB (9)		–17.08			mA
		1.9-V DMD LPDDR (7)	V_O = 0.4 V	4.0			
		3.3-V LVCMOS (1)	V_O = 0.4 V	4.0			
		3.3-V LVCMOS (2)	V_O = 0.4 V	8.0			
		3.3-V LVCMOS (3)	V_O = 0.4 V	12.0			
		3.3-V I^2C (8)		3.0			
I_{OZ}	High-impedance leakage current	USB (9)		–10		10	µA
		3.3-V LVCMOS (1, 2, 3)		–10		10	
		3.3-V I^2C (8)		–10		10	
C_I	Input capacitance (including package)	USB (9)		11.3	12.8	14.7	pF
		3.3-V LVCMOS (2)		2.8	3.3	4.0	
		3.3-V LVCMOS (4)		2.7	3.4	4.2	
		3.3-V I^2C (8)		3.0	3.2	3.5	

Table 2. I/O Type Definition

I/O	
(NUMBER)	DEFINITION
1	3.3-V LVCMOS I/O buffer, with 4-mA drive
2	3.3-V LVCMOS I/O buffer, with 8-mA drive
3	3.3-V LVCMOS I/O buffer, with 12-mA drive
4	3.3-V LVCMOS receiver
5	3.3-V LVDS receiver (FPD-Link interface)
6	N/A
7	1.9-V LPDDR output buffer (DMD interface)
8	3.3-V I^2C with 12-mA sink
9	USB compatible (3.3 V)
10	OSC 3.3-V I/O compatible LVCMOS

6.6 I^2C0 and I^2C1 Interface Timing Requirements[1][2][3]

			MIN	MAX	UNIT
f_{clock}	Clock frequency, HOST_I^2C_SCL (50% reference points)	Fast-Mode		400[4]	kHz
		Standard Mode		100[4]	kHz

(1) Meets I^2C timing per the I^2C Bus Specification, unless otherwise noted. For reference see version 2.1 of the Phillips/NXP specification.
(2) The maximum clock frequency does not account for rise time, nor added capacitance of PCB or external components which may adversely impact this value.
(3) By definition, I^2C transactions operate at the speed of the slowest device on the bus and thus there is no requirement to match the speed grade of all devices in the system. However if Full-speed operation is desired, it will be necessary to ensure the other I^2C devices support full-speed operation as well. In addition to other devices slowing down bus operation, the length of the line (due to its capacitance) and the value of the I^2C pullup resistors will also influence the max achievable speed.
(4) The data setup time should be greater than 300 ns. This differs from the I^2C specification.

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6.7 Port 1 Input Pixel Interface Timing Requirements

See Figure 1

PARAMETER			MIN	MAX	UNIT
$f_{(clock)}$	Clock frequency, P1A_CLK		12	150	MHz
t_c	Cycle time, P1A_CLK		6.666	83.330	ns
t_{jp}	Clock jitter, P1A_CLK (deviation in period from ideal)(1)	Maximum $f_{(clock)}$			
$t_{w(L)}$	Pulse duration low, P1A_CLK	50% reference points	2.3		ns
$t_{w(H)}$	Pulse duration high, P1A_CLK	50% reference points	2.3		ns
t_{su}	Setup time – P1_(A-C)(9-0), P1_VSYNC, P1_HSYNC, P1_FIELD, P1_DATEN; Valid before P1A_CLK↑(2)	50% reference points	3		ns
t_h	Hold time – P1_(A-C)(9-0), P1_VSYNC, P1_HSYNC, P1_FIELD, P1_DATEN; Valid after P1A_CLK↑(2)	50% reference points	3		ns
t_t	Transition time – P1A_CLK	20% to 80% reference points	0.6	2.0	ns
t_t	Transition time – P1_A(9-0), P1_B(9-0), P1_C(9-0), P1_HSYNC, P1_VSYNC, P1_DATEN	20% to 80% reference points	0.6	3.0	ns

(1) For f_{clock} frequencies less than 150 MHz, calculate clock jitter (in ns) using this formula: Maxiimum Clock Jitter = ± [1 / f_{clock} – 5414 ps].
(2) All signals are sampled at the rising edge of P1A_CLK only.

6.8 Port 2 Input Pixel Interface (FPD-Link Compatible LVDS Input) Timing Requirements

See Figure 2, Figure 3 and Figure 4

PARAMETER(1)			MIN	MAX	UNIT
f_{clock}	Clock frequency, P2_CLK (LVDS input clock)		20	90	MHz
t_c	Cycle time, P2_CLK (LVDS input clock)		11.1	50.0	ns
t_{slew}	Clock or data slew rate	f_{pxck} < 90 MHz	0.3		V/ns
		f_{pxck} > 90 MHz	0.5		
$t_{startup}$	Link startup time (internal)			1	ms

(1) Extra Notes:
(a) Minimize cross-talk and match traces on PCB as close as possible.
(b) TI recommends to keep the common mode voltage as close to 1.2 V as possible.
(c) TI recommends to keep the absolute input differential voltage as high as possible.
(d) The LVDS open input detection is only related to a low common mode voltage; it is not related to a low differential swing.
(e) LVDS power 3.3-V supply (VDD33_FPD) noise level should be below 100 mV_{p-p}.
(f) LVDS power 1.2-V supply (VDD12_FPD) noise level should be below 60 mV_{p-p}.

6.9 System Oscillator Timing Requirements

See Figure 5

PARAMETER			MIN	MAX	UNIT
f_{clock}	Clock frequency, MOSC(1)		31.9968	32.0032	MHz
t_c	Cycle time, MOSC(1)		31.188	31.256	ns
$t_{w(H)}$	Pulse duration (high), MOSC(2)	50% reference points	12.5		ns
$t_{w(L)}$	Pulse duration (low), MOSC(2)		12.5		ns
t_t	Transition time, MOSC(2)	20% to 80% reference points		7.5	ns
t_{jp}	Period jitter, MOSC(2) (Deviation in period from ideal period solely due to high frequency jitter and not spectrum clocking)		–100	+100	ps

(1) The frequency range for MOSC is 32 MHz with ±100 PPM accuracy. This shall include impact to accuracy due to aging, temperature and trim sensitivity. The MOSC input cannot support spread spectrum clock spreading.
(2) Applies only when driven via an external digital oscillator.

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6.10 Reset Timing Requirements

PARAMETER			MIN	MAX	UNIT
$t_{w1(L)}$	Pulse duration, inactive low, PWRGOOD	50% reference points	4		µs
t_{t1}	Transition time, PWRGOOD	20% to 80% reference points		625	µs
$t_{w2(L)}$	Pulse duration, inactive low, POSENSE	50% reference points	500		µs
t_{t2}	Transition time, POSENSE	20% to 80% reference points		1	µs
t_{PH}	Power hold time, POSENSE remains active after PWRGOOD is de-asserted	20% to 80% reference points	500		µs

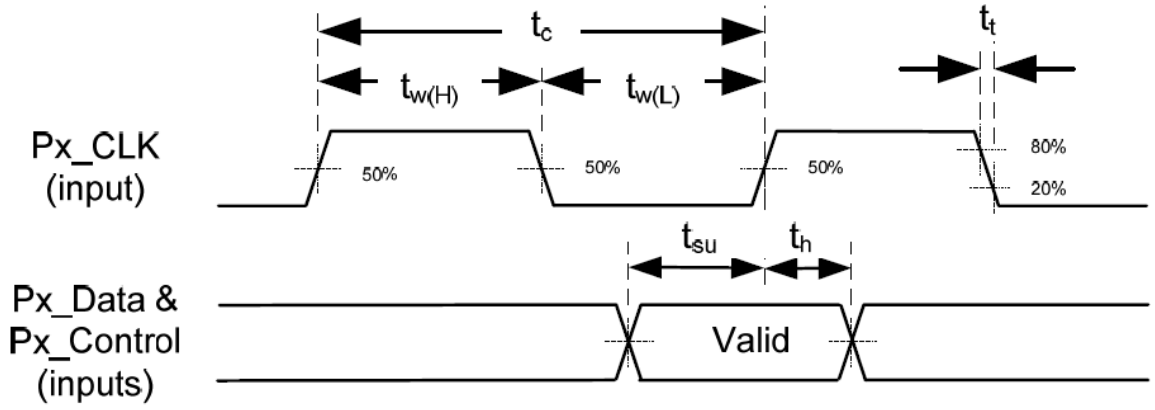

Figure 1. Port 1 Input Pixel Timing

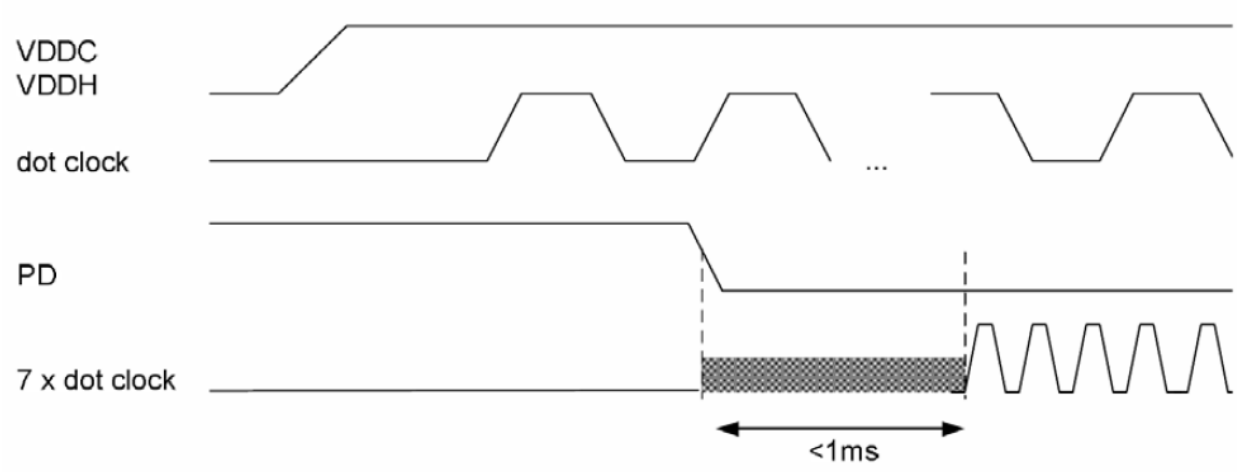

Figure 2. LVDS Timing Diagram

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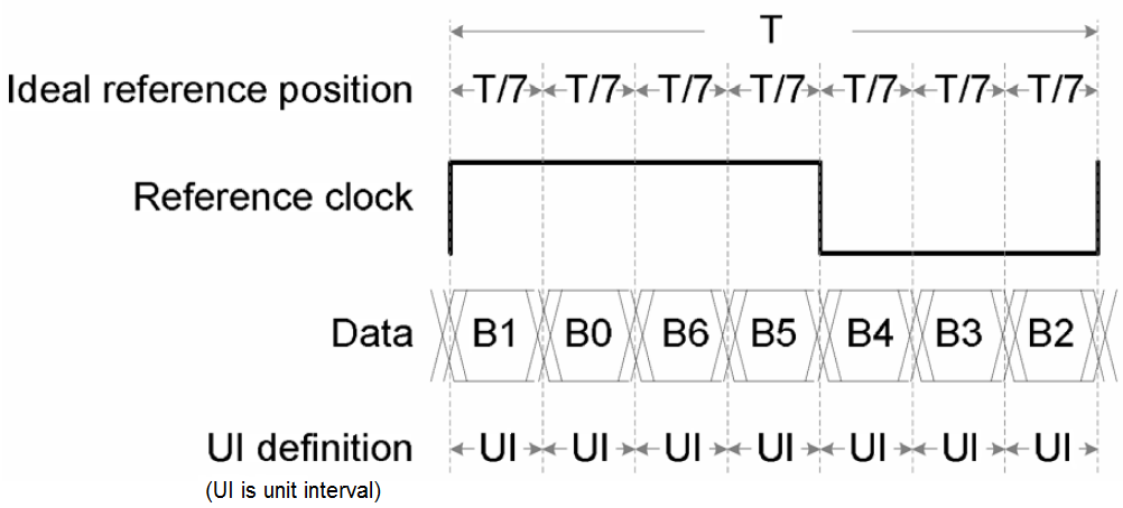

Figure 3. (LVDS) Link Start-up Timing

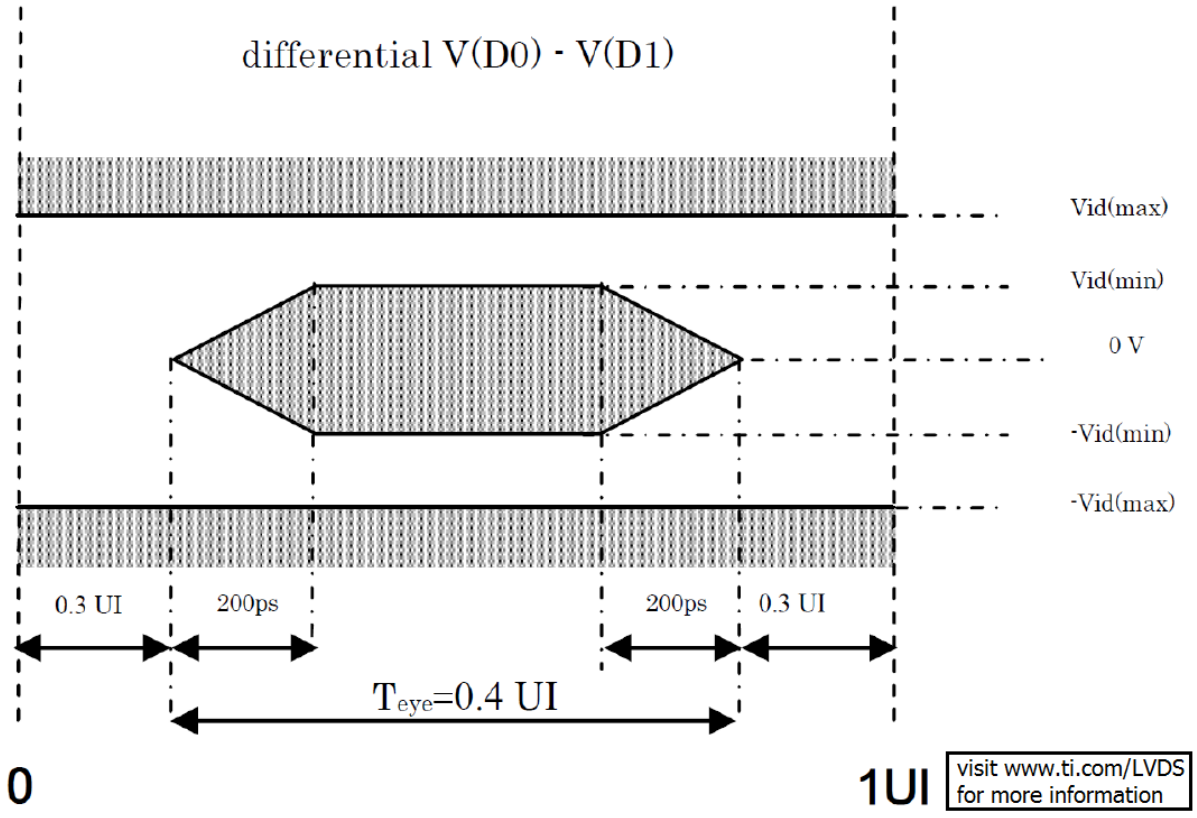

Figure 4. (LVDS) Clock: Data Skew Definition

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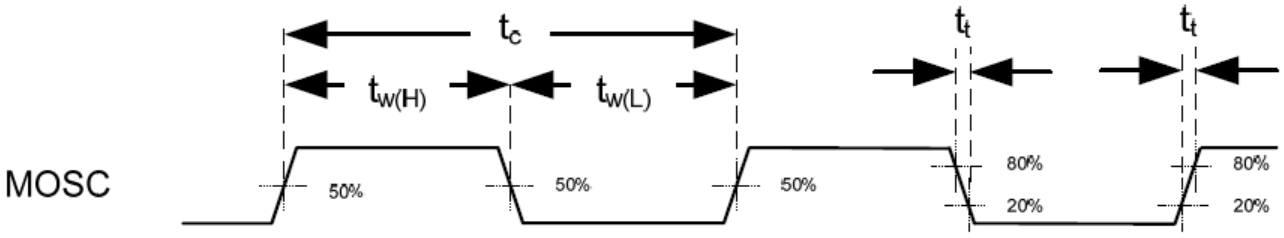

Figure 5. System Oscillators Timing

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6.11 Video Timing Input Blanking Specification

The DLPC350 controller requires a minimum horizontal and vertical blanking for both Port 1 and Port 2. These parameters indicate the time allocated to retrace the signal at the end of each line and field of a display. For the related parameter definitions, see *Video Timing Parameter Definitions*.

6.11.1 Source Input Blanking

The vertical and horizontal blanking requirements for both input ports are defined in Table 3, except when using a 120 Hz source. In this case, please use the source input blanking timing found in Table 4. Refer to the video timing parameter definitions listed in *Video Timing Parameter Definitions*. Also, see Figure 7 for Parallel I/F Frame Timing.

Table 3. Source Input Blanking Requirements

PORT	PARAMETER	MINIMUM BLANKING
Port 1 Vertical Blanking	VBP (tp_vbp)	370 µs
	VFP (tp_vfp)	2 lines
	Total vertical blanking	370 µs + 3 lines
	VSYNC high (tp_vsw)	1 line
Port 2 Vertical Blanking	VBP (tp_vbp)	370 µs
	VFP (tp_vfp)	0 lines
	Total vertical blanking	370 µs + 3 lines
	VSYNC high (tp_vsw)	1 line
Port 1 and 2 Horizontal Blanking	HBP (tp_hbp)	10 pixels
	HFP (tp_hfp)	0 pixels
	Total horizontal blanking for 0.45 WXGA DMD	154286 ÷ Source APPL pixels (round up)
	HSYNC high (tp_hsw)	16 pixels

Table 4. 120 Hz Source Input Blanking Timings on Port 1

PORT	PARAMETER	MINIMUM BLANKING
Vertical Blanking	VBP (tp_vbp)	3 lines
	VFP (tp_vfp)	17 lines
	Total vertical blanking	30 lines
	VSYNC high (tp_vsw)	10 lines
Horizontal Blanking	HBP (tp_hbp)	10 pixels
	HFP (tp_hfp)	56 pixels
	Total horizontal blanking	128 pixels
	HSYNC high (tp_vsw)	64 pixels
Pixel Clock		146.0 MHz

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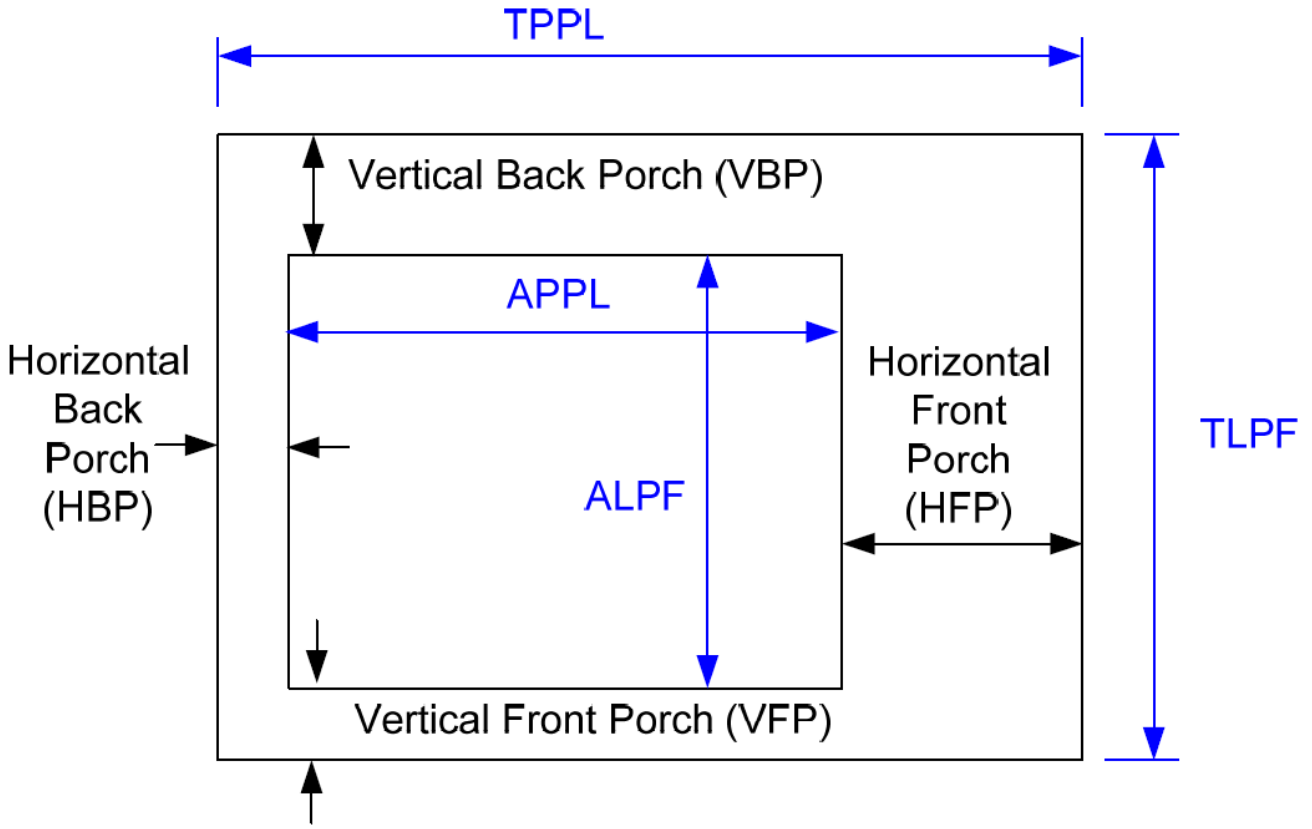

Figure 6. Horizontal and Vertical Blanking Diagram

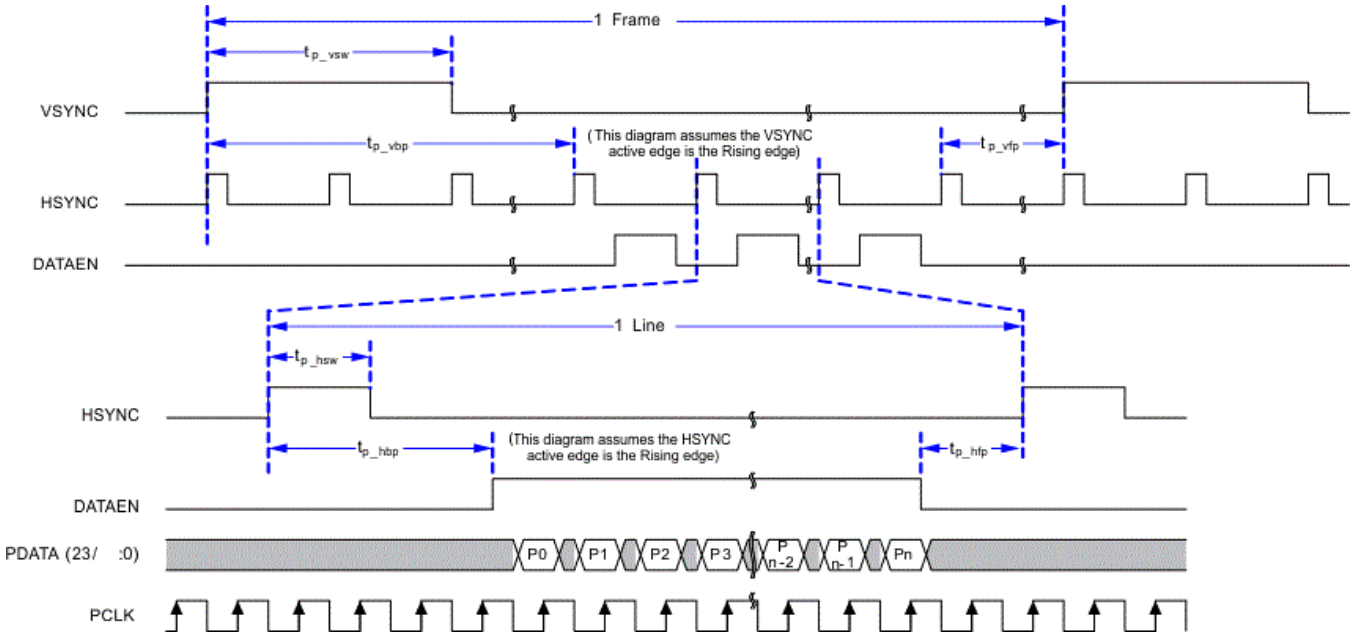

Figure 7. Parallel I/F Frame Timing

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6.12 Programmable Output Clocks Switching Characteristics

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{clock}	Clock frequency, OCLKC (1)	N/A	OCLKC	0.7759	48	MHz
t_c	Cycle time, OCLKC (2)	N/A	OCLKC	20.83	1288.80	ns
$t_{w(L)}$	Pulse duration low (50% reference points)	N/A	OCLKC	(t_c / 2) – 2		ns
$t_{w(H)}$	Pulse duration high (50% reference points)	N/A	OCLKC	(t_c / 2) – 2		ns
f_{clock}	Clock frequency, OCLKD (1)	N/A	OCLKD	0.7759	48	MHz
t_c	Cycle time, OCLKD (2)	N/A	OCLKD	20.83	1288.80	ns
$t_{w(L)}$	Pulse duration low (50% reference points)	N/A	OCLKD	(t_c / 2) – 2		ns
$t_{w(H)}$	Pulse duration high (50% reference points)	N/A	OCLKD	(t_c / 2) – 2		ns

(1) The frequency of OCLKC and OCLKD is programmable. See GPIO pins 11 and 12.
(2) The duty cycle of OCLKC and OCLKD will be within ±2 ns of 50%.

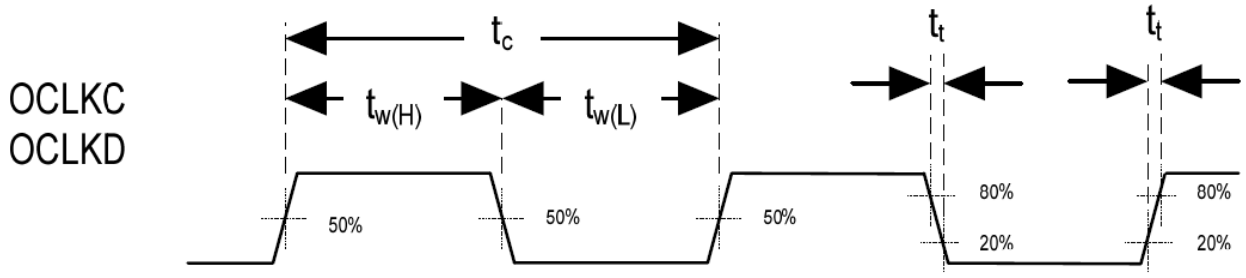

Figure 8. Programmable Output Clocks Timing Diagram

6.13 DMD Interface Switching Characteristics

The DLPC350 controller DMD interface is comprised of a combination of both single data rate (SDR) and double data rate (DDR), and output signals using LPDDR (as defined by JESD209A). SDR signals are referenced to DMD_SAC_CLK and DDR signals are referenced to DMD_DCLK.

Switching characteristics over recommended operating conditions, C_L (minimum timing) = 5 pF, C_L (maximum timing) = 25 pF (unless otherwise noted).

PARAMETER		TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{clock1}	Clock frequency(1) (2)		N/A	DMD_DCLK	79.992	120.012	MHz
t_{p1_clkper}	Clock period	50% reference points	N/A	DMD_DCLK	8.332	12.502	ns
t_{p1_cwh}	Clock pulse duration low	50% reference points	N/A	DMD_DCLK	3.75		ns
t_{p1_cwl}	Clock pulse duration high	50% reference points	N/A	DMD_DCLK	3.75		ns
f_{clock2}	Clock frequency(2)		N/A	DMD_SAC_CLK	74.659	74.675	MHz
t_{p2_clkper}	Clock period	50% reference points	N/A	DMD_SAC_CLK	13.391	13.394	ns
t_{p2_cwh}	Clock pulse duration low	50% reference points	N/A	DMD_SAC_CLK	6		ns
t_{p2_cwl}	Clock pulse duration high	50% reference points	N/A	DMD_SAC_CLK	6		ns
t_{slew}	Slew rate(3) (4) (5)		N/A	All	0.7		V/ns
t_{p1_su}	Output setup time(6)	50% reference points	Both rising and falling edges of DMD_DCLK	DMD_D(23:0), DMD_SCTRL, DMD_LOADB, DMD_TRC	1.10		ns
t_{p1_h}	Output hold time(6)	50% reference points	Both rising and falling edges of DMD_DCLK	DMD_D(23:0), DMD_SCTRL, DMD_LOADB, DMD_TRC	1.10		ns
t_{p1_skew}	DMD data skew	50% reference points	Relative to each other	DMD_D(23:0), DMD_SCTRL, DMD_LOADB, DMD_TRC, DMD_DCLK		0.2	ns
t_{p2_su}	Output setup time(6)	50% reference points	Rising edge of DMD_SAC_CLK	DMD_SAC_BUS, DMD_DRC_OE, DMD_DRC_BUS, DMD_DRC_STRB	2.35		ns
t_{p2_h}	Output hold time(6)	50% reference points	Rising edge of DMD_SAC_CLK	DMD_SAC_BUS, DMD_DRC_OE, DMD_DRC_BUS, DMD_DRC_STRB	2.35		
t_{p2_skew}	DRC/SAC data skew	50% reference points	Relative to each other	DMD_SAC_BUS, DMD_DRC_OE, DMD_DRC_BUS, DMD_DRC_STRB, DMD_SAC_CLK		0.2	ns

(1) The controller supports a fixed number of programmable clock rates with the min and max values as shown. The performance may be further limited by interface voltage and PCB routing.
(2) Note that these values do not include any tolerance variation of the external crystal or oscillator, nor do they include any associated jitter.
(3) LPDDR slew rate for the rising edge is measured between VILD(DC) to VIHD(AC) where VILD(DC) = 0.3 × VDDQ and VILD(AC) = 0.8 × VDDQ.
(4) LPDDR slew rate for the rising edge is measured between VILD(DC) to VIHD(AC) where VILD(DC) = 0.7 × VDDQ and VILD(AC) = 0.2 × VDDQ.
(5) The DMD setup and hold time window must be de-rated by 300 ps for each 0.1 V/ns reduction in slew rate below 1 V/ns. Thus a 0.7 V/ns slew rate increases this window by 900 ps from 1400 to 2300 ps.
(6) The minimum output setup and hold values of the controller already include clock jitter, DCD, SSO, ISI noise, and PCB variation. In order to meet the separate setup and hold timing minimums of the DMD, only routing skew needs to be considered in system timing analysis.

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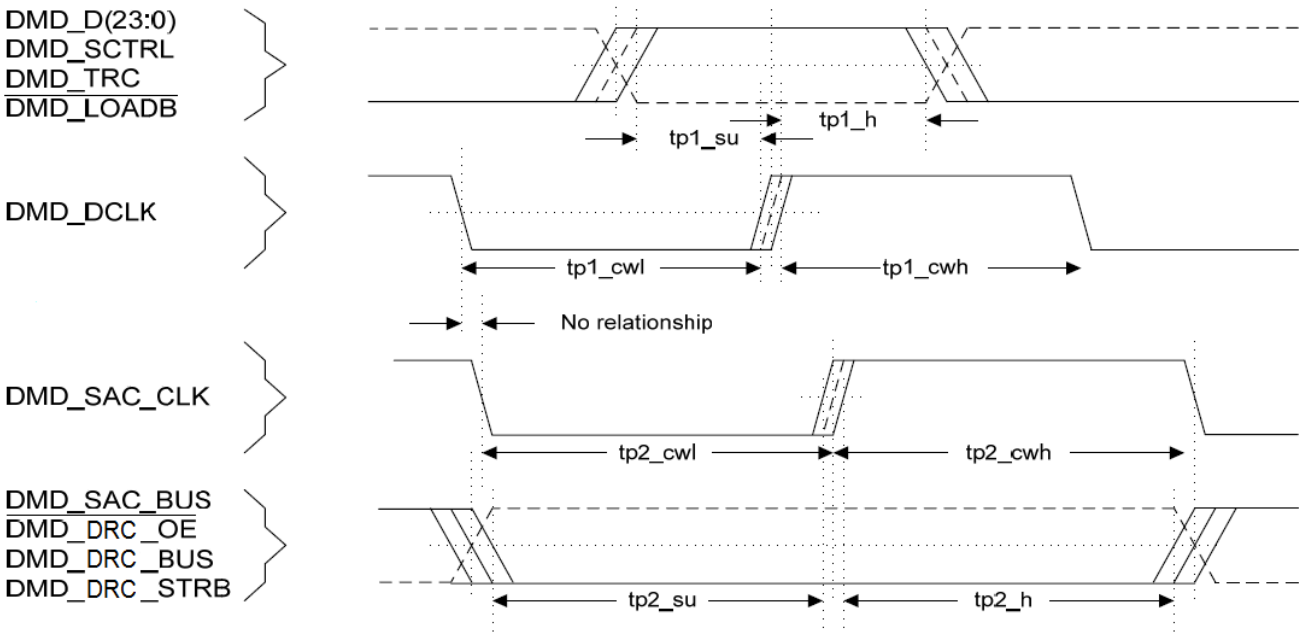

Figure 9. DMD Interface Timing

6.14 JTAG Interface: I/O Boundary Scan Application Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{(clock)}$	Clock frequency, TCK			10	MHz
t_c	Cycle time, TCK		100		ns
$t_{w(L)}$	Pulse duration low, PCLK	50% reference points	40		ns
$t_{w(H)}$	Pulse duration high, PCLK	50% reference points	40		ns
t_{su}	Setup time – TDI, TMS1; Valid before TCK↑↓	20% to 80% reference points	8		ns
t_h	Hold time – TDI, TMS1; Valid after TCK↑↓		2		ns
t_t	Transition time			5	ns
t_{pd} (1)	Output propagation, Clock to Q	From (Input) TCK↓ to (Output) TDO1	3	12	ns

(1) Switching characteristics over recommended operating conditions, C_L (minimum timing) = 5 pF, C_L (maximum timing) = 85 pF (unless otherwise noted).

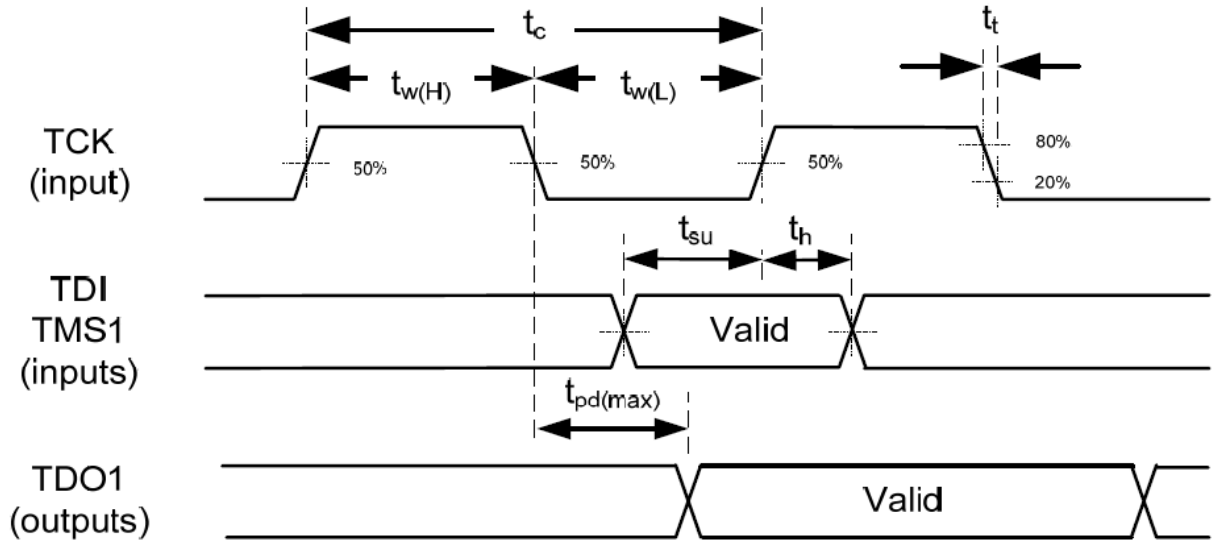

Figure 10. Boundary Scan Timing

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7 Parameter Measurement Information

7.1 Power Consumption

Table 5 lists the typical current and power consumption of the individual supplies.

Normal mode refers to operation during full functionality, active product operation. Typical values correspond to power dissipated on nominal process devices operating at nominal voltage and 70°C junction temperature (approximately 25°C ambient) displaying typical video-graphics content from a high frequency source. Maximum values correspond to power dissipated on fast process devices operating at high voltage and 105°C junction temperature (approximately 55°C ambient) displaying typical video-graphics content from a high-frequency source. The increased power dissipation observed on fast process devices operated at maximum recommended temperatures is primarily a result of increased leakage current. Maximum power values are estimates and may not reflect the actual final power consumption of the device.

Table 5. Power Consumption

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{CC12}	Supply voltage, 1.2-V core power	Normal Mode		600	1020	mA
I_{CC19_DMD}	Supply voltage, 1.9-V I/O power (DMD LPDDR)	Normal Mode		30	50	mA
I_{CC33}	Supply voltage, 3.3-V (I/O) power	Normal Mode		40	70	mA
I_{CC12_FPD}	FPD-Link LVDS interface supply voltage, 1.2-V power	Normal Mode		60	100	mA
I_{CC33_FPD}	FPD-Link LVDS interface supply voltage, 3.3-V power	Normal Mode		50	85	mA
I_{CC12_PLLD}	Supply voltage, PLL digital power (1.2 V)	Normal Mode		9	15	mA
I_{CC12_PLLM}	Supply voltage, master clock generator PLL digital power (1.2 V)	Normal Mode		9	15	mA
I_{CC18_PLLD}	Supply voltage, PLL analog power (1.8 V)	Normal Mode		10	15	mA
I_{CC18_PLLM}	Supply voltage, master clock generator PLL analog power (1.8 V)	Normal Mode		10	15	mA
Total Power		Normal Mode		1225	2200	mW

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8 Detailed Description

8.1 Overview

In DLP-based solutions, image data is 100% digital from the DLPC350 input port to the image on the DMD. The image stays in digital form and is not converted into an analog signal. The DLPC350 controller processes the digital input image and converts the data into a format needed by the DMD. The DMD steers light by using binary pulse width modulation (PWM) for each micromirror. For further details, refer to DMD data sheet (TI literature number DLPS028 for the DLP4500 and DLPS032 for the DLP4500NIR).

Figure 13 is the DLPC350 controller functional block diagram. As part of the pixel processing functions, the DLPC350 controller offers format conversion functions: chroma interpolation and color-space conversion. The DLPC350 controller also offers several image-enhancement functions. The DLPC350 controller also supports the necessary functions to format the input data to the DMD. The pixel processing functions allow the DLPC350 controller and DMD to support a wide variety of resolutions including NTSC, PAL, XGA, and WXGA. The pixel processing functions can be optionally bypassed with the native 912 × 1140 pixel resolution to support direct one-to-one pixel mapping.

When accurate pattern display is needed, the native 912 × 1140 input resolution pattern has a one-to-one association with the corresponding micromirror on the DMD. The DLPC350 controller enables high-speed display of these patterns. This functionality is well-suited for techniques such as structured light, additive manufacturing, or digital exposure.

Commands can be input to the DLPC350 controller over an I^2C interface.

The DLPC350 controller takes as input 24-, 27-, or 30-bit RGB data at up to 120-Hz frame rate. This frame rate is composed of three colors (red, green, and blue) with each color equally divided in the 120-Hz frame rate. Thus, each color has a 2.78-ms time slot allocated. Because each color has an 8-, 9-, or 10-bit depth, each color time slot is further divided into bit-planes. A bit-plane is the 2-dimensional arrangement of one-bit extracted from all the pixels in the full color 2D image to implement dynamic depth (see Figure 11).

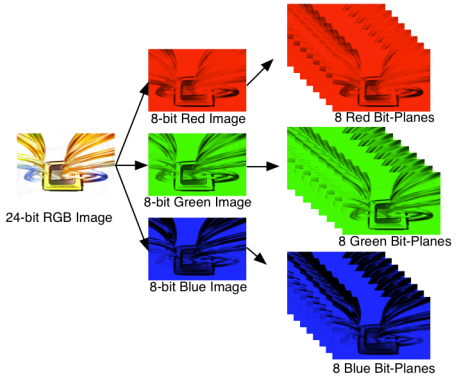

Figure 11. Bit Slices

The length of each bit-plane in the time slot is weighted by the corresponding power of two of its binary representation. This provides a binary pulse width modulation of the image. For example, a 24-bit RGB input has three colors with 8-bit depth each. Each color time slot is divided into eight bit-planes, with the sum of the weight of all bit planes in the time slot equal to 256. See Figure 12 for an illustration of this partition of the bits in a frame.

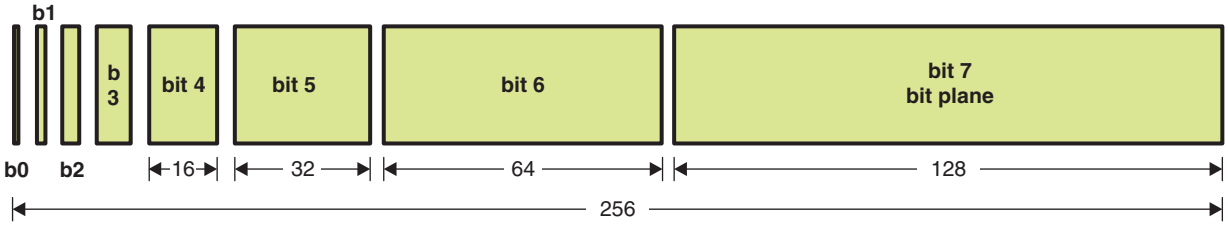

Figure 12. Bit Partition in a Frame for an 8-Bit Color

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Overview (continued)

Therefore, a single video frame is composed of a series of bit-planes. Because the DMD mirrors can be either on or off, an image is created by turning on the mirrors corresponding to the bit set in a bit-plane. With binary pulse width modulation, the intensity level of the color is reproduced by controlling the amount of time the mirror is on. For a 24-bit RGB frame image input to the DLPC350 controller, the DLPC350 controller creates 24 bit-planes, stores them in a double-buffered eDRAM embedded in the chip, and sends them to the DMD, one bit-plane at a time. Depending on the bit weight of the bit-plane, the DLPC350 controller controls the time this bit-plane is illuminated, controlling the intensity of the bit-plane. To improve image quality in video frames, these bit-planes, time slots, and color frames are shuffled and interleaved with spatial-temporal algorithms by the DLPC350 controller.

8.2 Functional Block Diagram

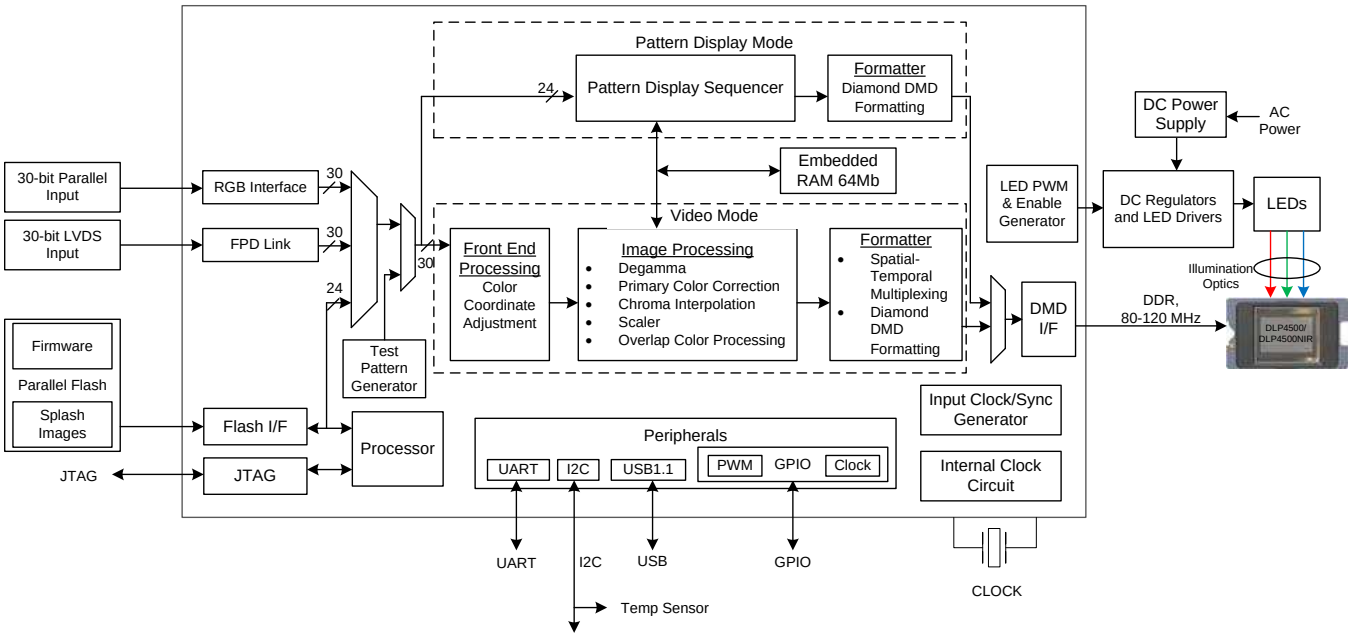

Figure 13. DLPC350 Functional Block Diagram

Functional Block Diagram (continued)

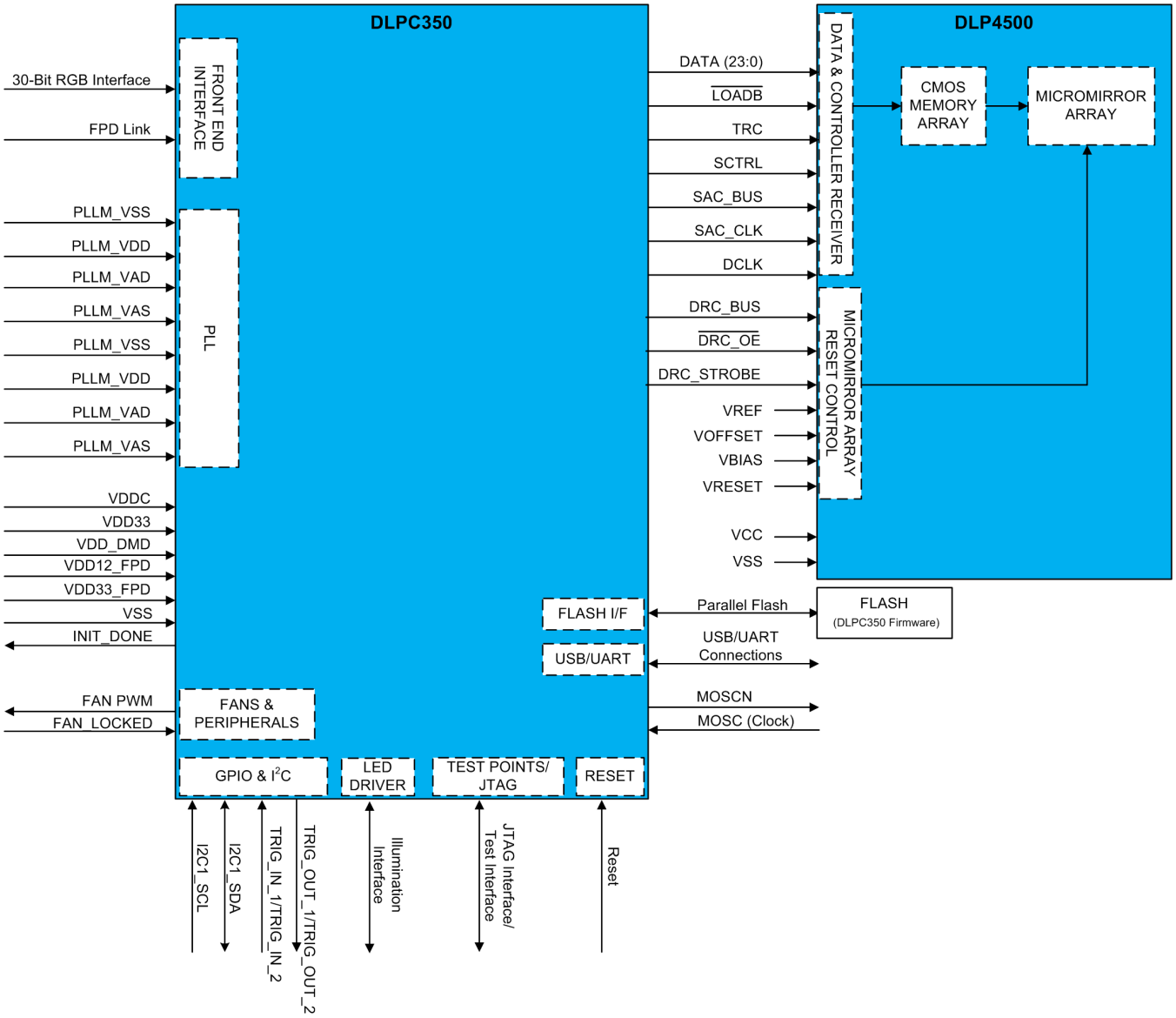

Figure 14. Chipset Block Diagram

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8.3 Feature Description

8.3.1 Board Level Test Support

The In-Circuit Three-State Enable signal (ICTSEN) is a board-level test control signal. By driving ICTSEN to a logic high state, all controller outputs (except TDO1) are 3-stated.

The ICTSEN and TRST should be electrically tied together to put DLPC350 pins in tri-state during JTAG boundary scan operation in case other chips exist on the board interfacing with DLPC350.

The DLPC350 controller also provides JTAG boundary scan support on all I/O signals, non-digital I/O, and a few special signals. Exceptions are defined in Table 6.

Table 6. Signals Not Covered by JTAG

SIGNAL NAME	PKG BALL
USB_DAT_N	E3
USB_DAT_P	E2
HW_TEST_EN	V7
VPGM	D17
EXRES	A3
MOSC	A14
MOSCN	A15
RA_IN_P	AB10
RA_IN_N	AA10
RB_IN_P	Y11
RB_IN_N	W11
RC_IN_P	AB12
RC_IN_N	AA12
RD_IN_P	Y13
RD_IN_N	W13
RE_IN_P	AB14
RE_IN_N	AA14
RCK_IN_P	Y9
RCK_IN_N	W9

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8.4 Device Functional Modes

8.4.1 Structured Light Applications

For applications where video enhancement is not desired, the video processing algorithms can be bypassed and replaced with a specific set of bit-planes. The pattern image is then allocated into the corresponding time slots. Furthermore, an output trigger signal is synchronized with these time slots to indicate when the image is displayed. For structured light applications, this mechanism provides the capability to display a set of patterns and signal a camera to capture these patterns overlaid on an object.

The DLPC350 controller stores two 24-bit frames in its internal memory buffer. This display buffer, composed of 48 1-bit planes, allows the DLPC350 controller to send one 24-bit buffer to the DMD array while the second 24-bit buffer is filled from the flash or streamed in through the 24-bit RGB interface. In streaming mode, the DMD array displays the previous 24-bit frame while the current 24-bit frame fills the second display buffer. After a 24-bit frame is displayed, the buffer rotates, accessing the next 24-bit frame to the DMD. Thus, the displayed image is a 24-bit frame behind the data streamed through the 24-bit RGB parallel interface.

In structured light mode, the maximum pattern rate can be achieved by pre-loading the 48 1-bit planes from flash memory, and sequencing them in the desired order with different bit depths. In order to achieve this maximum pre-loaded pattern rate shown in Table 8, it is required to display all the patterns from one 24-bit frame buffer before displaying patterns from the second 24-bit frame buffer. If all displayed patterns cannot fit inside the 48 1-bit plane buffer, the maximum pattern rate cannot be achieved as a load penalty will be incurred when loading one side of the buffer as the other is displayed. To synchronize a camera to the displayed patterns, the DLPC350 controller supports three trigger modes: mode 0, mode 1, and mode 2. An overview of the modes can be found in Table 7.

Table 7. Trigger Modes

	TRIG_IN_1	TRIG_IN_2	TRIG_OUT_1	TRIG_OUT_2
Mode 0	Unused (uses VSYNC)	Starts and stops pattern sequence	Asserted during exposure time	Start of the pattern sequence
Mode 1	Advances to next pattern	Starts and stops pattern sequence	Asserted during exposure time	Start of the pattern sequence
Mode 2	Alternates between two patterns	Advances to next pair of patterns	Asserted during exposure time	Start of the pattern sequence

In mode 0, the vertical sync (VSYNC) acts as the trigger input (TRIG_IN_1 is unused), and TRIG_IN_2 starts and stops the pattern sequence on the rising and falling edge respectively. In mode 1, a TRIG_IN_1 pulse indicates to the DLPC350 controller to advance to the next pattern, while TRIG_IN_2 starts and stops the pattern sequence on the rising and falling edge respectively. In mode 2, the TRIG_IN_1 signal toggles between two consecutive patterns, while a TRIG_IN_2 pulse advances to the next pair of patterns. In all modes, TRIG_OUT_1 is asserted during the exposure time of the pattern, while TRIG_OUT_2 pulses at the start of the pattern sequence .

An example of mode 0 is shown in Figure 15, where the VSYNC signal starts the pattern sequence display. The pattern sequence consists of a series of three consecutive patterns. The first pattern sequence consists of P1, P2, and P3. Because P3 is an RGB pattern, it is shown with its time sequential representation of P3.1, P3.2, and P3.3. The second pattern sequence consists of three patterns: P4, P5, and P6. The third sequence consists of P7, P8, and P9. TRIG_OUT_1 is high for each pattern exposure period, while TRIG_OUT_2 indicates the start of each of the three pattern sequences.

An example of mode 1 is shown in Figure 16, where pattern sequences of four are displayed. TRIG_OUT_1 is asserted for each pattern exposure period, while TRIG_OUT_2 indicates the start of each four-pattern sequence. TRIG_IN_1 pulses advance the pattern.

Another example of mode 1 is shown in Figure 17, where pattern sequences of three are displayed. TRIG_OUT_1 is asserted during each pattern exposure, while TRIG_OUT_2 indicates the start of each three-pattern sequence. TRIG_IN_2 serves as a start and stop signal. When high, the pattern sequence starts or continues. Note that in the middle of displaying the P4 pattern, TRIG_IN_2 is low, so the sequence stops displaying P4. When TRIG_IN_2 is raised, the pattern sequence continues where it stopped by re-displaying P4.

An example of mode 2 is shown in Figure 18, where TRIG_IN_1 alternates between two patterns, while TRIG_IN_2 advances to the next pair of patterns.

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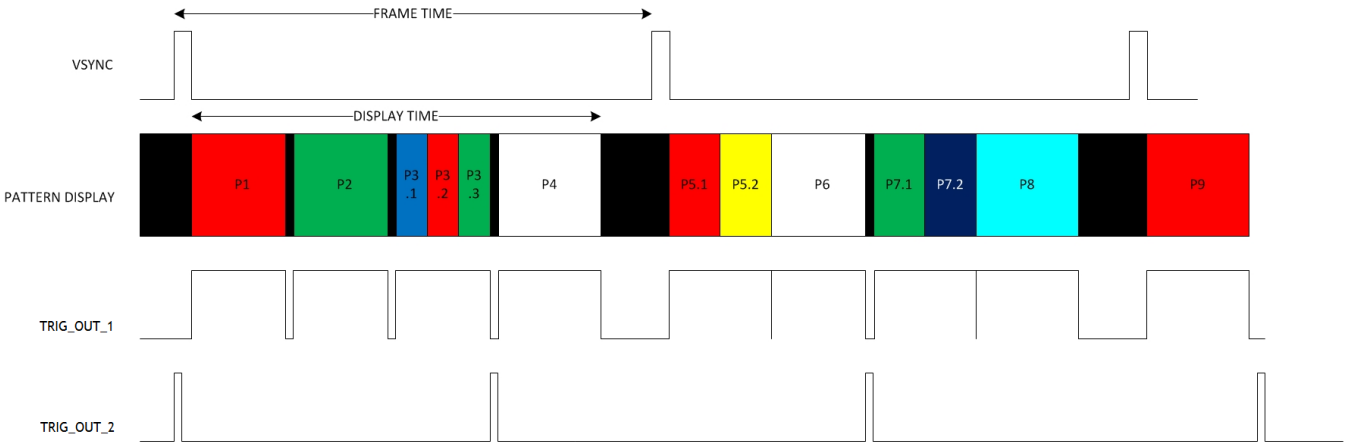

Figure 15. Mode 0 Trigger Timing Diagram

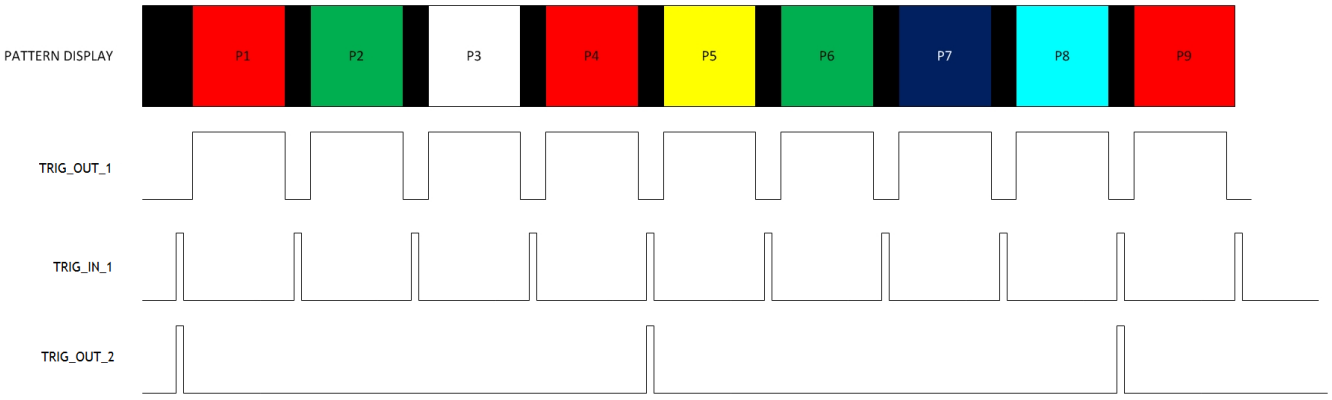

Figure 16. Mode 1 Triggers Timing Diagram for 6-bit Patterns

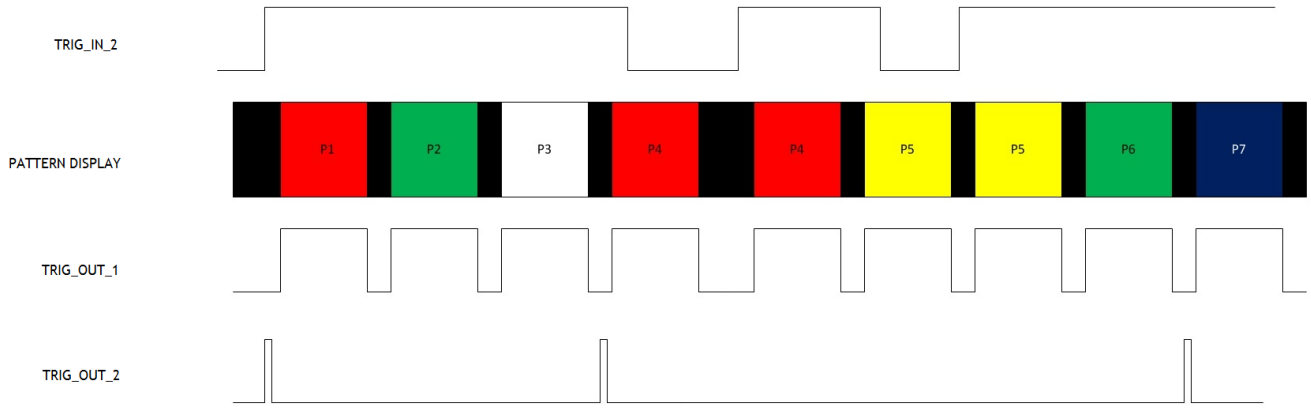

Figure 17. Mode 1 Trigger Timing Diagram

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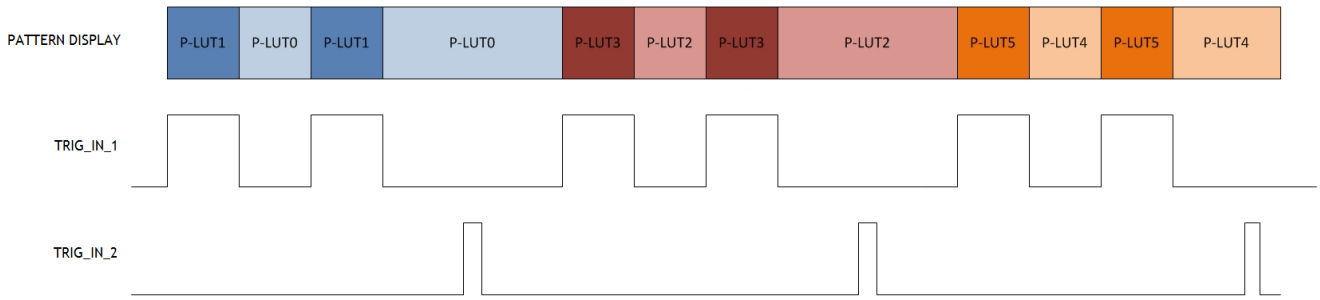

Figure 18. Mode 2 Trigger Timing Diagram

Table 8. Allowed Pattern Combinations

BIT DEPTH	EXTERNAL RGB INPUT PATTERN RATE (Hz)	PRE-LOADED PATTERN RATE (Hz)	MAXIMUM NUMBER OF PATTERNS (PRE-LOADED)
1	2880	4225	48
2	1428	1428	24
3	636	636	16
4	588	588	12
5	480	500	8
6	400	400	8
7	222	222	6
8	120	120	6

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8.4.2 (LVDS) Receiver Supported Pixel Mapping Modes

Table 9. (LVDS) Receiver Supported Pixel Mapping Modes

LVDS Receiver Input	Mapping Selection 1	Mapping Selection 2	Mapping Selection 3	Mapping Selection 4 (18-bit Mode)
RA Input Channel				
RDA(6)	map to GRN(4)	map to GRN(2)	map to GRN(0)	map to GRN(4)
RDA(5)	map to RED(9)	map to RED(7)	map to RED(5)	map to RED(9)
RDA(4)	map to RED(8)	map to RED(6)	map to RED(4)	map to RED(8)
RDA(3)	map to RED(7)	map to RED(5)	map to RED(3)	map to RED(7)
RDA(2)	map to RED(6)	map to RED(4)	map to RED(2)	map to RED(6)
RDA(1)	map to RED(5)	map to RED(3)	map to RED(1)	map to RED(5)
RDA(0)	map to RED(4)	map to RED(2)	map to RED(0)	map to RED(4)
RB Input Channel				
RDB(6)	map to BLU(5)	map to BLU(3)	map to BLU(1)	map to BLU(5)
RDB(5)	map to BLU(4)	map to BLU(2)	map to BLU(0)	map to BLU(4)
RDB(4)	map to GRN(9)	map to GRN(7)	map to GRN(5)	map to GRN(9)
RDB(3)	map to GRN(8)	map to GRN(6)	map to GRN(4)	map to GRN(8)
RDB(2)	map to GRN(7)	map to GRN(5)	map to GRN(3)	map to GRN(7)
RDB(1)	map to GRN(6)	map to GRN(4)	map to GRN(2)	map to GRN(6)
RDB(0)	map to GRN(5)	map to GRN(3)	map to GRN(1)	map to GRN(5)
RC Input Channel				
RDC(6)	map to DEN			
RDC(5)	map to VSYNC			
RDC(4)	map to HSYNC			
RDC(3)	map to BLU(9)	map to BLU(7)	map to BLU(5)	map to BLU(9)
RDC(2)	map to BLU(8)	map to BLU(6)	map to BLU(4)	map to BLU(8)
RDC(1)	map to BLU(7)	map to BLU(5)	map to BLU(3)	map to BLU(7)
RDC(0)	map to BLU(6)	map to BLU(4)	map to BLU(2)	map to BLU(6)
RD Input Channel				
RDD(6)	map to Field (option 1 if available)			
RDD(5)	map to BLU(3)	map to BLU(9)	map to BLU(7)	NO MAPPING
RDD(4)	map to BLU(2)	map to BLU(8)	map to BLU(6)	NO MAPPING
RDD(3)	map to GRN(3)	map to GRN(9)	map to GRN(7)	NO MAPPING
RDD(2)	map to GRN(2)	map to GRN(8)	map to GRN(6)	NO MAPPING
RDD(1)	map to RED(3)	map to RED(9)	map to RED(7)	NO MAPPING
RDD(0)	map to RED(2)	map to RED(8)	map to RED(6)	NO MAPPING
RE Input Channel				
RDE(6)	map to Field (option 2 if available)			
RDE(5)	map to BLU(1)		map to BLU(9)	NO MAPPING
RDE(4)	map to BLU(0)		map to BLU(8)	NO MAPPING
RDE(3)	map to GRN(1)		map to GRN(9)	NO MAPPING
RDE(2)	map to GRN(0)		map to GRN(8)	NO MAPPING
RDE(1)	map to RED(1)		map to RED(9)	NO MAPPING
RDE(0)	map to RED(0)		map to RED(8)	NO MAPPING

Mapping options are selected via software. If only 18-bit mode is used (mapping selection number 4 in Table 9), and if a Field 1 or Field 2 input is not needed, then the LVDS RD Input Channel (RDD) and RE Input Channel (RDE) may be omitted in the board layout.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DLP4500 family of DMDs must be coupled with the DLPC350 controller to provide a reliable solution for many different structured light and video applications. The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC350. Applications of interest include 3D measurement systems, spectrometers, medical systems, and compressive sensing.

9.2 Typical Applications

9.2.1 Typical Chipset Application

Figure 19 shows a typical embedded system application using the DLPC350 controller and DMD. In this configuration, the DLPC350 controller supports a 24-bit parallel RGB input, typical of LCD interfaces, from an external source or processor. This system supports both still and motion video sources. However, the controller only supports sources with periodic synchronization pulses. This is ideal for motion video sources, but can also be used for still images by maintaining periodic syncs and only sending a new frame of data when needed. The still image must be fully contained within a single video frame and meet the frame timing constraints. The DLPC350 controller refreshes the displayed image at the source frame rate and repeats the last active frame for intervals in which no new frame has been received.

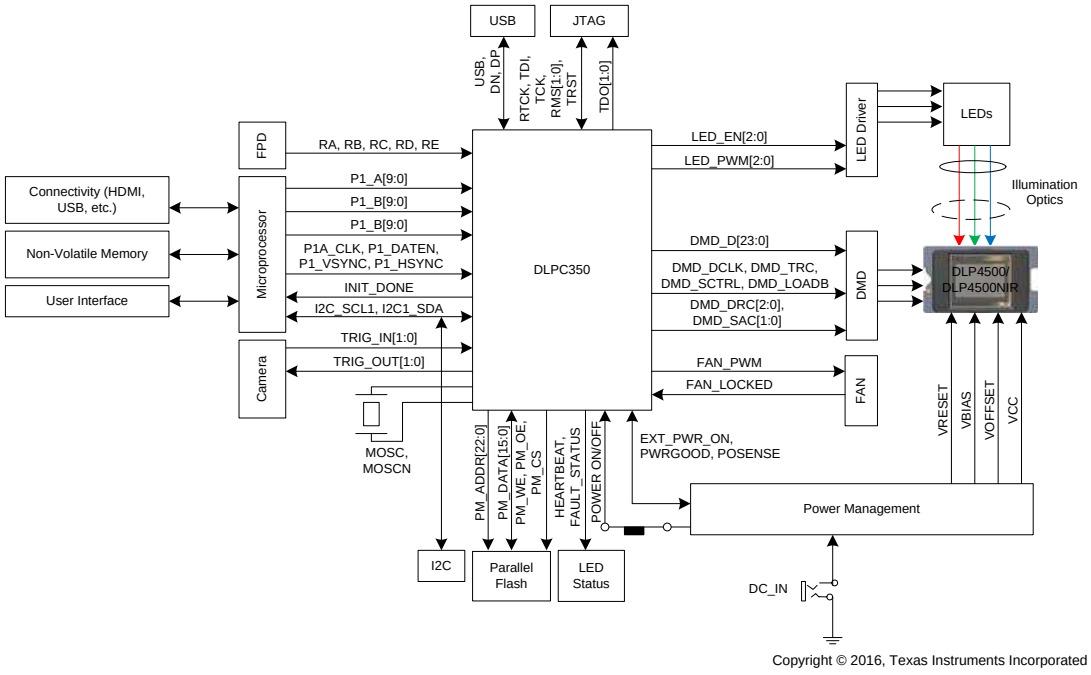

Figure 19. Typical Application Schematic

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Typical Applications (continued)

9.2.1.1 Design Requirements

All applications using the DLP4500 and DLP4500NIR chipset require both the controller and DMD components for operation. The system also requires an external parallel flash memory device loaded with the DLPC350 configuration and support firmware. The chipset has several system interfaces and requires some support circuitry. The following interfaces and support circuitry are required:

- DLPC350 system interfaces:
  - Control interface
  - Trigger interface
  - Input data interface
  - Illumination interface
- DLPC350 support circuitry and interfaces:
  - Reference clock
  - PLL
  - Program memory flash interface
- DMD interfaces:
  - DLPC350 to DMD digital data
  - DLPC350 to DMD control interface
  - DLPC350 to DMD micromirror reset control interface

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 DLPC350 System Interfaces

The DLPC350 supports a 30-bit parallel RGB interface for image data transfers from another device and a 30-bit interface for video data transfers. The system input requires proper generation of the PWRGOOD and POSENSE inputs to ensure reliable operation. The two primary output interfaces are the illumination driver control interface and sync outputs.

9.2.1.2.1.1 Control Interface

The DLPC350 supports I^2C or USB commands through the control interface. The control interface allows another master processor to send commands to the DLPC350 to query system status or perform realtime operations such as LED driver current settings.

The DLPC350 controller offers two different sets of slave addresses. The I2C_ADDR_SEL pin provides the ability to select an alternate set of 7-bit I^2C slave address only during power-up. If I2C_ADDR_SEL is low, then the DLPC350 slave addresses are 0x34 and 0x35. If I2C-ADDR_SEL is high, then the DLPC350 slave address is 0x3A and 0x3B. This signal also changes the serial number for the USB device so that two DLPC350s can be connected to one computer through USB. Once the system initialization is complete, this pin will be available as a GPIO. See the DLPC350 Programmer's Guide (TI literature number DLPU010) for detailed information about these operations.

Table 10 lists a description for active signals used by the DLPC350 to support the I^2C interface.

Table 10. Active Signals – I^2C Interface

Signal Name	Description
I2C1_SCL	I^2C clock. Bidirectional open-drain signal. I^2C slave clock input from the external processor.
I2C1_SDA	I^2C data. Bidirectional open-drain signal. I^2C slave to accept command or transfer data to and from the external processor.
I2C0_SCL	I^2C bus 0, clock; I^2C master for on-board peripherals
I2C0_SDA	I^2C bus 0, data; I^2C master for on-board peripherals

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9.2.1.2.1.2 Input Data Interface

The data interface has two components: a parallel RGB-input port and an FPD-Link LVDS input port. Both components can support up to 30 bits and have a nominal I/O voltage of 3.3 V. The *Interface Timing Requirements* in *Specifications* list the maximum and minimum input timing specifications for both components.

The parallel RGB port can support up to 30 bits in video mode. In pattern mode, the upper 8-bits of each color convert the 30-bit input into a 24-bit RGB input.

The FPD-Link input port can be configured to connect to a video decoder device or an external processor through a 24-, 27-, or 30-bit interface.

Table 11 provides a description of the signals associated with the data interface.

Table 11. Active Signals – Data Interface

Signal Name	Description
RGB Parallel Interface	
P1_(A, B, C)_[0:9]	30-bit data inputs 10 bits for each of the red, green, and blue channels). If interfacing to a system with less than 10-bits per color, connect the bus of the red, green, and blue channels to the upper bits of the DLPC350 10-bit bus.
P1A_CLK	Pixel clock; all input signals on data interface are synchronized with this clock.
P1_VSYNC	Vertical sync
P1_HSYNC	Horizontal sync
P1_DATAEN	Input data valid
FPD-Link LVDS Input	
RCK	Differential input signal for clock
RA_IN	Differential input signal for data channel A
RB_IN	Differential input signal for data channel B
RC_IN	Differential input signal for data channel C
RD_IN	Differential input signal for data channel D
RE_IN	Differential input signal for data channel E

The A, B, and C input data channels of Port 1 can be internally swapped for optimum board layout.

9.2.1.2.2 DLPC350 System Output Interfaces

9.2.1.2.2.1 Illumination Interface

An illumination interface is provided that supports up to a 3-channel LED driver.

The illumination interface provides signals that support LED driver enable, LED enable, LED enable select, and PWM signals to control the LED current. Table 12 describes the active signals for the illumination interface.

Table 12. Active Signals – Illumination Interface

Signal Name	Description
HEARTBEAT	LED blinks continuously to indicate system is running fine
FAULT_STATUS	LED off indicates system fault
LEDR_EN	Red LED enable
LEDG_EN	Green LED enable
LEDB_EN	Blue LED enable
LEDR_PWM	Red LED PWM signal used to control the LED current
LEDG_PWM	Green LED PWM signal used to control the LED current
LEDB_PWM	Blue LED PWM signal used to control the LED current

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9.2.1.2.2.2 Trigger Interface (Sync Outputs)

The DLPC350 controller outputs a trigger signal for synchronizing displayed patterns with a camera, sensor, or other peripherals.

The signals that support sync-output are horizontal sync, vertical sync, two input triggers, and two output triggers. Depending on the application, these signals control how the pattern is displayed.

Table 13. Active Signals – Trigger and Sync Interface

Signal Name	Description
P1_HSYNC	Horizontal sync
P1_VSYNC	Vertical sync
TRIG_IN_1	Advances the pattern display or displays two alternating patterns, depending on the mode
TRIG_IN_2	Pauses the pattern display or advances the pattern by two, depending on the mode
TRIG_OUT_1	Active high during pattern exposure
TRIG_OUT_2	Active high to indicate first pattern display

9.2.1.2.3 DLPC350 System Support Interfaces

9.2.1.2.3.1 Reference Clock

The DLPC350 controller requires a 32-MHz 3.3-V external input from an oscillator. This signal serves as the DLPC350 reference clock from which the majority of the interfaces derive their timing. This includes DMD interfaces and serial interfaces.

9.2.1.2.3.2 PLL

The DLPC350 controller contains two PLLs (PLLM and PLLD), each of which have dedicated 1.2-V digital and 1.8-V analog supplies. These 1.2-V PLL pins should be individually isolated from the main 1.2-V system supply via a ferrite bead. The impedance of the ferrite bead should be much greater than the capacitor at frequencies where noise is expected. The impedance of the ferrite bead must also be less than 0.5 Ω in the frequency range of 100 to 300 kHz and greater than 10 Ω at frequencies greater than 100 MHz.

As a minimum, the 1.8-V analog PLL power and ground pins should be isolated using an LC filter with a ferrite bead serving as the inductor and a 0.1-µF capacitor on the DLPC350 side of the ferrite bead. TI recommends that this 1.8-V PLL power be supplied from a dedicated linear regulator and each PLL should be individually isolated from the regulator. The same ferrite recommendations described for the 1.8-V analog PLL supply apply to the 1.2-V digital PLL supply.

When designing the overall supply filter network, care must be taken to ensure that no resonances occur. Take special care when using the 1- to 2-MHz band because this coincides with the PLL natural loop frequency.

9.2.1.2.3.3 Program Memory Flash Interface

The DLPC350 controller provides two external program memory chip selects:

- $\overline{\text{PM_CS_1}}$ is mandatory CS for boot flash device (Standard *NOR* Flash ≤ 128 Mb).
- $\overline{\text{PM_CS_2}}$ is available for an optional flash device (≤128 Mb).

The flash access timing is fixed at 100.5 ns for read timing, and 154.1 ns for write timing. In standby mode, these values change to 803.5 ns for read timing and 1232.1 ns for write timing.

These timing values assume a maximum single direction trace length of 75 mm. When an additional flash is used in conjunction with the boot flash, stub lengths must be kept short and located as close as possible to the flash end of the route.

The DLPC350 controller provides enough program memory address pins to support a flash device up to 128 Mb. PM_ADDR_22 and PM_ADDR_21 are GPIO pins on reset, so they require board-level pulldown resistors to prevent the flash address bits from floating during initial bootload.

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9.2.1.2.4 DMD Interfaces

9.2.1.2.4.1 DLPC350 to DMD Digital Data

The DLPC350 controller provides the pattern data to the DMD over a double data rate (DDR) interface.

Table 14 describes the signals used for this interface.

Table 14. Active Signals – DLPC350 to DMD Digital Data Interface

DLPC350 Signal Name	DMD Signal Name
DMD_D(23:0)	DATA(23:0)
DMD_DCLK	DCLK

9.2.1.2.4.2 DLPC350 to DMD Control Interface

The DLPC350 controller provides the control data to the DMD over a serial bus.

Table 15 describes the signals used for this interface.

Table 15. Active Signals – DLPC350 to DMD Control Interface

DLPC350 Signal Name	DMD Signal Name	Description
DMD_SAC_BUS	SAC_BUS	DMD stepped-address control (SAC) bus data
DMD_SAC_CLK	SAC_CLK	DMD stepped-address control (SAC) bus clock
$\overline{\text{DMD_LOADB}}$	$\overline{\text{LOADB}}$	DMD data load signal
DMD_SCTRL	SCTRL	DMD data serial control signal
DMD_TRC	TRC	DMD data toggle rate control

9.2.1.2.4.3 DLPC350 to DMD Micromirror Reset Control Interface

The DLPC350 controls the micromirror clock pulses in a manner to ensure proper and reliable operation of the DMD.

Table 16 describes the signals used for this interface.

Table 16. Active Signals – DLPC350 to DMD Micromirror Reset Control Interface

DLPC350 Signal Name	DMD Signal Name	Description
DMD_DRC_BUS	DRC_BUS	DMD reset control serial bus
$\overline{\text{DMD_DRC_OE}}$	$\overline{\text{DRC_OE}}$	DMD reset control output enable
DMD_DRC_STRB	DRC_STRB	DMD reset control strobe

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10 Power Supply Recommendations

10.1 System Power and Reset

There are several factors related to system power and reset, which affect the DC error (offset) and AC noise at the DLPC350 power pins.

10.1.1 Default Conditions

At system power-up, the DLPC350 controller performs a power-up initialization routine that defaults the controller to its normal power mode, enables related clocks at their full rate, and releases associated resets. Most other clocks default to disabled with associated resets asserted until released by the processor. These same defaults are also applied as part of all system reset events that occur without removing or recycling power.

Following power-up or system reset initialization, the system boots from an external flash memory after which it enables the rest of the controller clocks. After system initialization is complete, application software determines if and when to enter standby mode.

10.1.1.1 1.2-V System Power

The controller supports a low-cost power delivery system with a single 1.2-V power source derived from a switching regulator. The main core should receive 1.2-V power directly from the regulator output, and the internal DLPC350 PLLs (VDD_12_PLLM, VDD_12_PLLD) should receive individually filtered versions of this 1.2-V power. For specific filter recommendations, see *Recommended DLPC350 PLL Layout Configuration*.

10.1.1.2 1.8-V System Power

A single 1.8-V power source should be used to supply both internal PLLs (VDD_18_PLLM, VDD_18_PLLD). To keep the power as clean as possible, TI recommends that this power be sourced via a linear regulator that is individually filtered for each PLL. For specific filter recommendations, see *Recommended DLPC350 PLL Layout Configuration*.

10.1.1.3 1.9-V System Power

To maximize signal integrity, TI recommends that an independent linear regulator be used to source the 1.9-V supply that supports the DMD interface (VDD_DMD). To achieve maximum performance, this supply must be tightly regulated to operating within a 1.9 V ±0.1 V range.

10.1.1.4 3.3-V System Power

The DLPC350 controller supports a low-cost power delivery system with a single 3.3-V power source derived from a switching regulator. This 3.3-V power supplies all LVCMOS I/O. 3.3-V power (VDD33) should remain active in all power modes for which the 1.2-V core power is applied.

10.1.1.5 FPD-Link Input LVDS System Power

The controller supports an FPD-Link compatible LVDS input for an additional method of inputting video or graphics data for display. This interface has some special controller power considerations that are separate from the other controller 1.2- or 3.3-V power rails. An FPD-Link 1.2-V power pin configuration example is shown in Figure 20.

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System Power and Reset (continued)

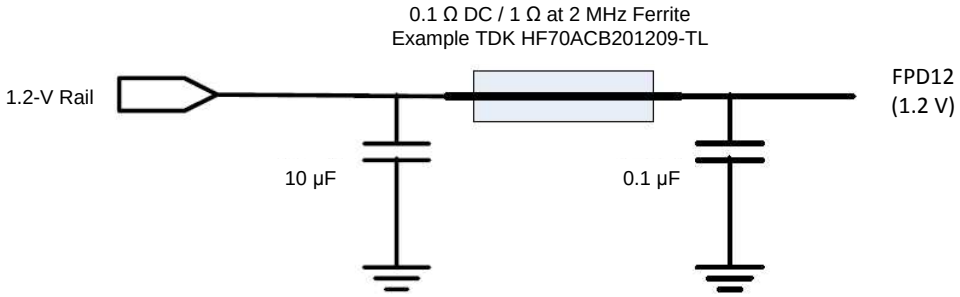

Figure 20. FPD-Link 1.2-V Power Pin Configuration

In addition, TI recommends to place the 0.1-µF low equivalent series resistance (ESR) capacitors to ground as close to the FPD-Link power pins of the DLPC350 controller as possible. FPD-Link 3.3-V power pins should also use external capacitors in the same manner as the 1.2-V pins. When FPD-Link is not utilized, the filtering can be omitted. However, the corresponding voltages must still be provided in order to avoid potential long-term reliability issues.

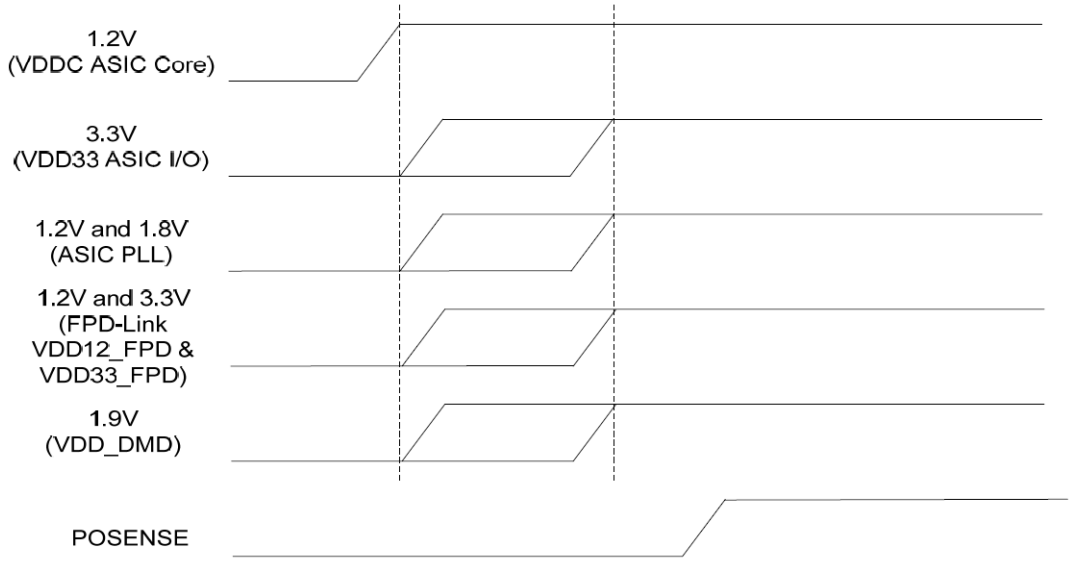

Figure 21. Initialization Timeline

10.1.2 System Power-up and Power-down Sequence

Although the DLPC350 controller requires an array of power supply voltages, (for example, VDDC, VDD_1X_PLLX, VCC_18, VCC_DMD, and VCCXX_FPD), there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the DLPC350 controller. This is true for both power-up and power-down. Similarly, there is no minimum time between powering-up or powering-down the different supplies of the DLPC350 controller. Note that it is not uncommon for there to be power-sequencing requirements for other devices that share power supplies with the DLPC350 controller.

Although there is no risk of damaging the DLPC350 controller as a result of a given power sequence, from a functional standpoint there are a few specific power-sequencing recommendations to ensure proper operation.

- 1.2-V core power should be applied whenever any I/O power is applied. This ensures that the powered I/O pins are set to a known state. Thus, TI recommends that core power be applied first. Other supplies should be applied only after the 1.2-V DLPC350 core has ramped up.
- All controller power should be applied before POSENSE is asserted to ensure proper power-up initialization is

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System Power and Reset (continued)

performed. 1.8-V PLL power, 1.9-V I/O power, and 3.3-V I/O power should remain applied as long as 1.2-V core power is applied and POSENSE is asserted.

It is assumed that all DLPC350 power-up sequencing is handled by external hardware. It is also assumed that an external power monitor will hold the DLPC350 controller in system reset during power-up (that is, POSENSE = 0). It should continue to assert system reset until all DLPC350 voltages have reached minimum specified voltage levels. During this time, all controller I/O are either 3-stated or driven low. The master PLL (PLLM) is released from reset upon the low-to-high transition of POSENSE, but the DLPC350 controller keeps the rest of the controller in reset for an additional 100 ms to allow the PLL to lock and stabilize its outputs. After this 100-ms delay, internal resets are de-asserted causing the microprocessor to begin its boot-up routine.

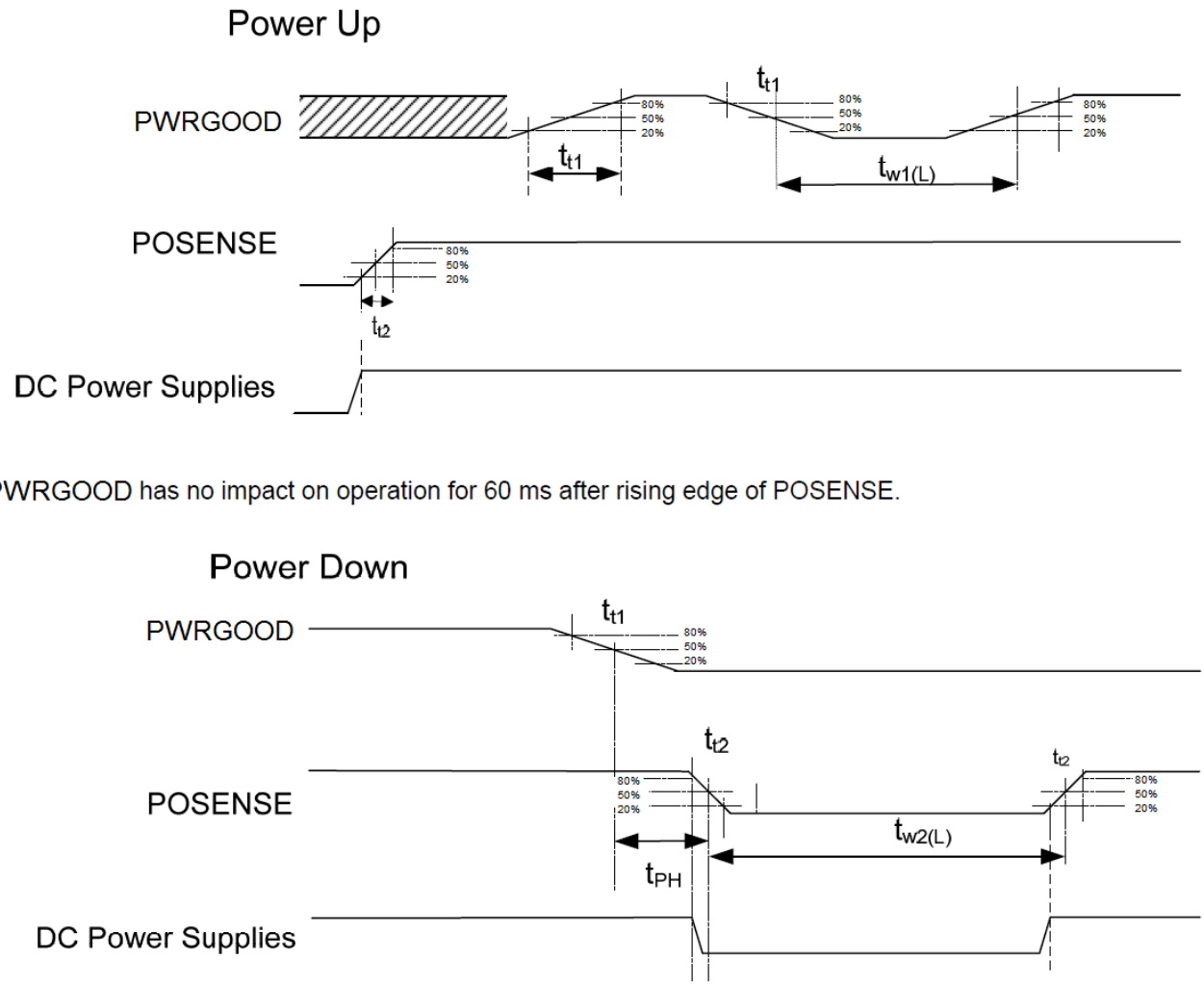

Figure 22. Power-up and Power-down Timing

10.1.3 Power-On Sense (POSENSE) Support

It is difficult to set up a power monitor to trip exactly on the DLPC350 controller minimum supply voltages specifications. Thus, TI recommends that the external power monitor generating POSENSE target its threshold to 90% of the minimum supply voltages and ensure that POSENSE remain low for a sufficient amount of time to allow all supply voltages to reach minimum controller requirements and stabilize. Note that the trip voltage for detecting the loss of power is not critical for POSENSE and thus may be as low as 50% of rated supply voltages. In addition, the reaction time to respond to a low voltage condition is not critical for POSENSE. INIT_DONE has much more critical requirements in these areas.

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System Power and Reset (continued)

10.1.4 Power-Good (PWRGOOD) Support

The PWRGOOD signal is defined to be an early warning signal that should alert the controller 500 µs before DC supply voltages have dropped below specifications. This allows the controller time to park the DMD, ensuring the integrity of future operation. TI recommends that monitor sensing PWRGOOD be on the input side of the supply regulators.

10.1.5 5-V Tolerant Support

With the exception of USB_DAT, the DLPC350 controller does not support any other 5-V tolerant I/O.

10.1.6 Power Reset Operation

Immediately following a power-up event, the DLPC350 hardware automatically brings up the master PLL and places the controller in NORMAL power mode. It then follows the standard system reset procedure (see *System Reset Operation*).

10.1.7 System Reset Operation

Immediately following any type of system reset (power-up reset, PWRGOOD reset, and so forth), the DLPC350 controller automatically returns to NORMAL power mode and returns to the following state:

- All GPIO 3-state and as a result all GPIO-controlled voltage switches default to enabling power to all the DLPC350 supply lines (assuming that these outputs are externally pulled-high).
- The master PLL remains active (it is only reset on a power-up reset) and most of the derived clocks are active. However, only those resets associated with the internal processor and its peripherals are released.
- The internal processor associated clocks default to their full clock rates, as boot-up occurs at full speed.
- The PLL feeding the DDR DMD interface (PLLD) defaults to its power-down mode, and all derived clocks are inactive with the corresponding resets asserted.
- The DMD interface (except $\overline{\text{DMD_DRC_OE}}$) default outputs to a logic low state. $\overline{\text{DMD_DRC_OE}}$ defaults to 3-state, but should be pulled high via an external 30- to 51-kΩ pullup resistor on the PCB.
- All resets output by the DLPC350 controller remain asserted until released by the internal processor (after boot-up).
- The DLPC350 controller boots-up from external flash. After the DLPC350 controller boots, it:
  - Configures the programmable DDR clock generator (DCG) clock rates (that is, the DMD LPDDR interface rate).
  - Enables the DCG PLL (PLLD) while holding the divider logic in reset.
  - After the DCG PLL locks, the firmware sets the DMD clock rates.
  - The DLPC350 firmware then releases the DCG divider logic resets, which in turn, enables all derived DCG clocks.
- After the clocks are configured, an internal memory test is performed. See Figure 23 and note that GPIO26 is the INIT_DONE signal.

Application software should wait for a wake-up command from the user. After the controller is requested to wake-up, the software should place the controller back in NORMAL mode and re-initialize clocks and resets as required. See reset timing requirements in *Reset Timing Requirements*.

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System Power and Reset (continued)

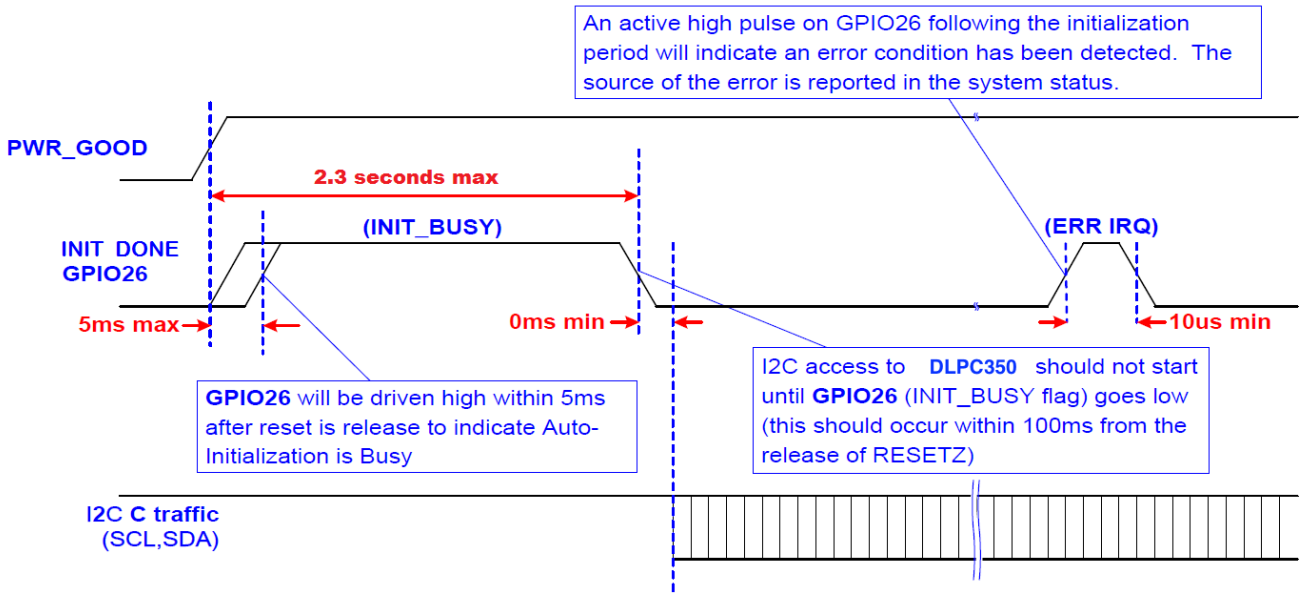

Figure 23. Internal Memory Test Diagram

11 Layout

11.1 Layout Guidelines

11.1.1 DMD Interface Design Considerations

The DMD interface is modeled after the low-power DDR-memory (LPDDR) interface. To minimize power dissipation, the LPDDR interface is defined to be unterminated. As a result, PCB signal-integrity management is imperative. Impedance control and crosstalk mitigation is critical to robust operation. LPDDR board design recommendations include trace spacing that is three times the trace width, impedance control within 10%, and signal routing directly over a neighboring reference plane (ground or 1.9-V plane).

DMD interface performance is also a function of trace length; therefore the length of the trace limits performance. The DLPC350 controller only works over a narrow range of DMD signal routing lengths at 120 MHz. Ensuring positive timing margins requires attention to many factors.

As an example, the DMD interface system timing margin can be calculated as follows.

Setup Margin = (DLPC350 Output Setup) – (DMD Input Setup) – (PCB Routing Mismatch) – (PCB SI Degradation) (1)

Hold-Time Margin = (DLPC350 Output Hold) – (DMD Input Hold) – (PCB Routing Mismatch) – (PCB SI Degradation) (2)

PCB signal integrity degradation can be minimized by reducing the affects of simultaneously switching output (SSO) noise, crosstalk, and inter-symbol interface (ISI). Additionally, PCB routing mismatch can be budgeted via controlled PCB routing.

In an attempt to minimize the need for signal integrity analysis that would otherwise be required, the following PCB design guidelines are provided. They describe an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Variation from these recommendations may also work, but should be confirmed with PCB signal integrity analysis or lab measurements.

11.1.2 DMD Termination Requirements

Table 17 lists the termination requirements for the DMD interface. These series resistors should be placed as close to the DLPC350 pins as possible while following all PCB guidelines.

Table 17. Termination Requirements for DMD Interface

SIGNALS	SYSTEM TERMINATION
DMD_D(23:0), DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_DRC_STRB, DMD_DRC_BUS, DMD_SAC_CLK, and DMD_SAC_BUS	External 5-Ω series termination at the transmitter
DMD_DCLK	External 5-Ω series termination at the transmitter
$\overline{\text{DMD_DRC_OE}}$	External 0-Ω series termination. This signal must be externally pulled-up to VDD_DMD via a 30-kΩ to 51-kΩ resistor

DMD_CLK and DMD_SAC_CLK clocks should be equal lengths, as shown in Figure 24.

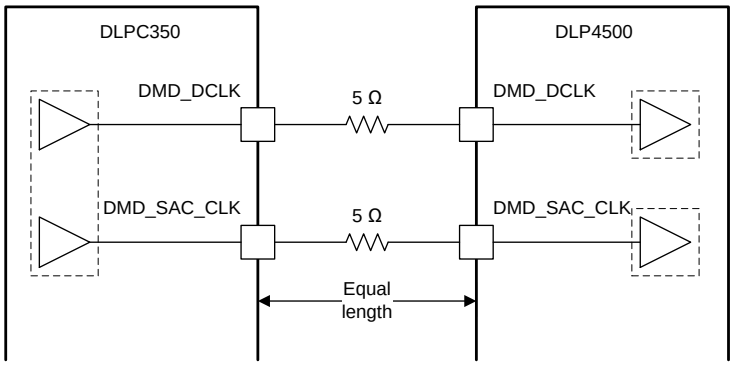

Figure 24. Series-Terminated Clocks

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11.1.3 Decoupling Capacitors

The decoupling capacitors should be given placement priority. The supply voltage pin of the capacitor should be located close to the DLPC350 supply voltage pin or pins. Decoupling capacitors should have two vias connecting the capacitor to ground and two vias connecting the capacitor to the power plane, but if the trace length is less than 0.05 inches, the device can be connected directly to the decoupling capacitor. The vias should be located on opposite sides of the long side of the capacitor, and those connections should be less than 0.05 inches as well.

11.1.4 Power Plane Recommendations

For best performance, TI recommends the following:

- Two power planes
  - One solid plane for ground (GND)
  - One split plane for other voltages with no signal routing on the power planes
- Power and ground pins should be connected to these planes through a via for each pin.
- All device pin and via connections to these planes should use a thermal relief with a minimum of four spokes.
- Trace lengths for the component power and ground pins should be minimized to 0.03 inches or less.
- Vias should be spaced out to avoid forming slots on the power planes.
- High speed signals should not cross over a slot in the adjacent power planes.
- Vias connecting all the digital layers should be placed around the edge of the rigid PCB regions 0.03 inches from the board edges with 0.1 inch spacing prior to routing.
- Placing extra vias is not required if there are sufficient ground vias due to normal ground connections of devices.
- All signal routing and signal vias should be inside the perimeter ring of ground vias.

11.1.5 Signal Layer Recommendations

The PCB signal layers should follow typical good practice guidelines including:

- Layer changes should be minimized for single-ended signals.
- Individual differential pairs can be routed on different layers, but the signals of a given pair should not change layers.
- Stubs should be avoided.
- Only voltage or low-frequency signals should be routed on the outer layers, except as noted previously in this document.
- Double data rate signals should be routed first for best impedance and trace length matching.

The PCB should have a solder mask on the top and bottom layers. The mask should not cover the vias.

- Except for fine pitch devices (pitch ≤ 0.032 inches), the copper pads and the solder mask cutout should be of the same size.
- Solder mask between pads of fine pitch devices should be removed.
- In the BGA package, the copper pads and the solder mask cutout should be of the same size.

11.1.6 General Handling Guidelines for CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends that unused input pins be tied through a pullup resistor to its associated power supply, or a pulldown to ground. For inputs with internal pullup or pulldown resistors, adding an external pullup or pulldown resistor is unnecessary unless specified in the Pin Configuration and Functions section. Note that internal pullup and pulldown resistors are weak and should not be expected to drive an external line.

After power-up or device reset, bidirectional pins are configured as inputs as a reset default until directed otherwise.

Unused output-only pins can be left open.

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11.1.7 PCB Manufacturing

The DLPC350 Controller and DMD are a high-performance (high-frequency and high-bandwidth) set of components. This section provides PCB guidelines to help ensure proper operation of these components.

The DLPC350 controller board will be a multi-layer PCB with surface mount components on both sides. The majority of large surface mount components are placed on the top side of the PCB. Circuitry is high speed digital logic. The high speed interfaces include:

- 120-MHz DDR interface from DLPC350 to DMD
- 150-MHz LVTTL interface from a video decoder to the DLPC350
- 150-MHz pixel clock supporting 30-bit parallel RGB interface
- LVTTL parallel memory interface between the DLPC350 controller and flash with 70-ns access time
- LVDS flat panel display port to DLPC350

The PCB should be designed to IPC2221 and IPC2222, Class 2, Type Z, at level B producibility and built to IPC6011 and IPC6012, Class 2.

11.1.7.1 General Guidelines

Table 18. PCB General Recommendations

DESCRIPTION	RECOMMENDATION
Configuration	Asymmetric dual stripline
Etch thickness (T)	1.0-oz. (1.2-mil thick) copper
Single-ended signal impedance	50 Ω (±10%)
Differential signal impedance	100 Ω differential (±10%)

11.1.7.2 Trace Widths and Minimum Spacings

For best performance, TI recommends the trace widths and minimum spacings shown in Table 19.

Table 19. Trace Widths and Minimum Spacings

SIGNAL NAME	TRACE WIDTH (inches)	MINIMUM TRACE SPACING (inches)
P1P2, P1P2V_PLLM, P1P2V_PLLD, P2P5V, P3P3V, P1P9V, A1P8V, A1P8V_PLLD, A1P8V_PLLM	0.02	0.010
VRST, VBIAS, VOFFSET	0.02	0.010
VSS (GND)	0.02	0.005
FANx_OUT	0.02	0.020
DMD_DCLK		0.030
P1A_CLK, P1B_CLK, P1C_CLK		0.030
MOSC, MOSCN		0.030

11.1.7.3 Routing Constraints

In order to meet the specifications listed in the following tables, typically the PCB designer must route these signals manually (not using automated PCB routing software). In case of length matching requirements, routing traces in a serpentine fashion may be required. Keep the number of turns to a minimum and the turn angles no sharper than 45°. Traces must be 0.1 inches from board edges when possible; otherwise they must be 0.05 inches minimum from the board edges. Avoid routing long traces all around the PCB. PCB layout assumes adjacent trace spacing is twice the trace width. However, three times the trace width will reduce crosstalk and significantly help performance.

The maximum and minimum signal routing trace lengths include escape routing.

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Table 20. Signal Length Routing Constraints for DMD Interface

SIGNALS	MINIMUM SIGNAL ROUTING LENGTH(1)	MAXIMUM SIGNAL ROUTING LENGTH(2)
DMD_D(23:0), DMD_DCLK, DMD_TRC, DMD_SCTRL, DMD_LOADB,	2480 mil (63 mm)	2953 mil (75 mm)
DMD_OE, DMD_DRC_STRB, DMD_DRC_BUS, DMD_SAC_CLK, and DMD_SAC_BUS	512 mil (13 mm)	5906 mil (150 mm)

(1) Signal lengths below the stated minimum will likely result in overshoot or undershoot.
(2) DMD-DDR maximum signal length is a function of the DMD_DCLK rate.

Each high-speed, single-ended signal should be routed in relation to its reference signal, such that a constant impedance is maintained throughout the routed trace. Avoid sharp turns and layer switching while keeping total trace lengths to a minimum. The following signals should follow the signal matching requirements described in Table 21.

Table 21. High-Speed Signal Matching Requirements for DMD Interface

SIGNALS	REFERENCE SIGNAL	MAX MISMATCH	UNIT
DMD_D(23:0), DMD_TRC, DMD_SCTRL, DMD_LOADB	DMD_DCLK	±200 (±5.08)	mil (mm)
DMD_DRC_STRB, DMD_DRC_BUS, DMD_SAC_BUS, DMD_OE	DMD_SAC_CLK	±200 (±5.08)	mil (mm)

The values in Table 21 apply to the PCB routing only. They do not include any internal package routing mismatch associated with the DLPC350 or DMD. Additional margin can be attained if internal DLPC350 package skew is taken into account. Additionally, to minimize EMI radiation, serpentine routes added to facilitate trace length matching should only be implemented on signal layers *between* reference planes.

Both the DLPC350 output timing parameters and the DMD input timing parameters include a timing budget to account for their respective internal package routing skew. Thus, additional system margin can be attained by comprehending the package variations and compensating for them in the PCB layout. To increase the system timing margin, TI recommends that the DLPC350 package variation be compensated for (by signal group), but it may not be desirable to compensate for DMD package skew. This is due to the fact that each DMD has a different skew profile, making the PCB layout DMD specific. To use a common PCB design for different DMDs, TI recommends that either the DMD package skew variation not be compensated for on the PCB, or the package lengths for all applicable DMDs being considered. Table 22 provides the DLPC350 package output delay at the package ball for each DMD interface signal.

The total length of all the traces in Table 22 should be matched to the DMD_DCLK trace length. Total trace length includes package skews, PCB length, and DMD flex cable length.

Table 22. DLPC350 Package Skew and Routing Trace Length for the DMD Interface

SIGNAL	TOTAL DELAY (Package Skews)		PACKAGE PIN
	(ps)	(mil)	
DMD_D0	25.9	152.35	A8
DMD_D1	19.6	115.29	B8
DMD_D2	13.4	78.82	C8
DMD_D3	7.4	43.53	D8
DMD_D4	18.1	106.47	B11
DMD_D5	11.1	65.29	C11
DMD_D6	4.4	25.88	D11
DMD_D7	0.0	0.00	E11
DMD_D8	14.8	87.06	C7
DMD_D9	18.4	108.24	B10
DMD_D10	6.4	37.65	E7
DMD_D11	4.8	28.24	D10
DMD_D12	29.8	175.29	A6

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Table 22. DLPC350 Package Skew and Routing Trace Length for the DMD Interface (continued)

SIGNAL	TOTAL DELAY (Package Skews)		PACKAGE PIN
	(ps)	(mil)	
DMD_D13	25.7	151.18	A12
DMD_D14	19.0	111.76	B12
DMD_D15	11.7	68.82	C12
DMD_D16	4.7	27.65	D12
DMD_D17	21.5	126.47	B7
DMD_D18	24.8	145.88	A10
DMD_D19	8.3	48.82	D7
DMD_D20	23.9	140.59	B6
DMD_D21	1.6	9.41	E9
DMD_D22	10.7	62.94	C10
DMD_D23	16.7	98.24	C6
DMD_DCLK	24.8	145.88	A9
$\overline{\text{DMD_LOADB}}$	18.0	105.88	B9
DMD_SCTRL	11.4	67.06	C9
DMD_TRC	4.6	27.06	D9

Table 23. Routing Priority

SIGNAL	ROUTING PRIORITY	ROUTING LAYER	MATCHING REFERENCE SIGNAL	TOLERANCE
DMD_DCLK(1) (2) (3)	1	3	–	–
DMD_D[23:0], DMD_SCTRL, DMD_TRC, DMD_LOADB(1) (2) (3) (4)	1	3, 4	DMD_DCLK	±150 mils
P1_A[9:0], P1_B[9:0], P1_C[9:0], P1_HSYNC, P1_VSYNC, P1_DATAEN, P1X_CLK	1	3, 4	P1X_CLK	±0.1 inches
R[A-E]_IN_P, R[A-E]_IN_N, RCK_IN_P, RCK_IN_N	2	3, 4	RCK	±150 mils Differential signals need to be matched within ±12 mils

(1) Total signal length from the DLPC350 and the DMD, including flex cable traces and PCB signal trace lengths must be held to the lengths specified in Table 20.
(2) Switching routing layers is not permitted except at the beginning and end of a trace.
(3) Minimize vias on DMD traces.
(4) Matching includes PCB trace length plus the DLPC350 package length plus the DMD flex cable length.

11.1.7.4 Fiducials

Fiducials for automatic component insertion should be 0.05 inch diameter copper with a 0.1-inch cutout (antipad). Fiducials for optical auto insertion are placed on three corners of both sides of the PCB.

11.1.7.5 Flex Considerations

Table 24 shows the general DMD flex design recommendations. Table 25 lists the minimum flex design requirements.

Table 24. Flex General Recommendations

DESCRIPTION	RECOMMENDATION
Configuration	Two-layer micro strip
Reference plane 1	Ground plan for proper return
Vias	Maximum two per signal
Single trace width	4-mil minimum
Etch thickness (T)	0.5-oz. (0.6 mil thick) copper

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Table 24. Flex General Recommendations (continued)

DESCRIPTION	RECOMMENDATION
Single-ended signal impedance	50 Ω (± 10%)

Table 25. Minimum Flex Design Requirements

PARAMETER	APPLICATION	SINGLE-ENDED SIGNALS	UNIT
Line width (W)(1)	Escape routing in ball field	4 (0.1)	mil (mm)
	PCB etch data and control	5 (0.13)	mil (mm)
	PCB etch clocks	7 (0.18)	mil (mm)
Minimum line spacing to other signals (S)	Escape routing in ball field	4 (0.1)	mil (mm)
	PCB etch data and control	2x the line width(2)	mil (mm)
	PCB etch clocks	3x the line width	mil (mm)

(1) Line width is expected to be adjusted to achieve impedance requirements.
(2) Three times the line spacing is recommended for all signals to help achieve the desired signal integrity.

11.1.7.6 DLPC350 Thermal Considerations

The underlying thermal limitation for the DLPC350 controller is that the maximum operating junction temperature (T_J) must not be exceeded (see *Recommended Operating Conditions* in *Specifications*). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC350 controller, and power dissipation of surrounding components. The DLPC350 package is designed to extract heat through the power and ground planes of the PCB, thus copper content and airflow over the PCB are important factors.

11.2 Layout Example

11.2.1 Printed Circuit Board Layer Stackup Geometry

The DLPC350 PCB is targeted at six layers with layer stack up shown in Figure 25. The PCB layer stack may vary depending on system design. However, careful attention is required to meet design considerations. Layers one and six should consist of the components layers. Low-speed routing and power splits are allowed on these layers. Layer two should consist of a solid ground plane. Layer five should be a split voltage plane. Layers three and four should be used as the primary routing layers. Routing on external layers should be less than 0.25 inches for priority one and two signals. Refer to Table 23 for signal priority groups.

Board material should be FR-370HR or similar. PCB should be designed for lead-free assembly with the stackup geometry shown in Figure 25.

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Layout Example (continued)

Controlled Impedance Stack-up form

Material: FR370HR

Layer	Thickness	Stack-up	Descript	Cu Oz	SE Trace	SE Calculated	SE Target	SE Ref Pln	Diff Pairs Trace	Diff Pairs Space	Diff Pairs (Pitch)	Diff Pairs Calculated	Diff Pairs Target	Diff Pairs Ref Pln
	0.7	soldermask												
	1.2	plating												
1	0.6		sig	0.5	10.5	50.25	50	2	4.5	4.5	9	102.01	100	2
					4	74.93	75	2	5.25	4.75	10	99.14	100	2
	6	6.0 prepreg												
2	2.6		pln	2										
	5	5.0 core												
3	1.2		sig	1	7	50.36	50	2,5	4.25	5.75	10	99.11	100	2,5
	5	5.0	blank											
	18	18.0	blank	Filler to meet overall thickness										
	5	5.0 prepreg												
4	1.2		sig	1	7	50.36	50	2,5	4.25	5.75	10	99.11	100	2,5
	5	5.0 core												
5	2.6		pln	2										
	6	6.0 prepreg												
6	0.6		sig	0.5	10.5	50.25	50	5	4.5	4.5	9	102.01	100	5
	1.2	plating			4	74.93	75	5	5.25	4.75	10	99.14	100	5
	0.7	soldermask												

8.8 =copper
28 =core
22 =prepreg
3.8 =plating, s/m

62.6 =total thickness	Target thickness: .062 +-10%	Calculated using Apsim RLGC (Impedance calculator) +-10%	5/5/08

Figure 25. Layer Stackup

Table 26. PCB Layer Stackup Geometry

PARAMETER	DESCRIPTION	RECOMMENDATION
Reference plane 1	Ground plane for proper return	
Reference plane 2	1.9-V DMD I/O power plane or ground	
Er	Dielectric FR4	4.3 at 1 GHz (nominal)
H1	Signal trace distance to reference plane 1	5 mil (0.127 mm)
H2	Signal trace distance to reference plane 2	30.4 mil

11.2.2 Recommended DLPC350 MOSC Crystal Oscillator Configuration

The DLPC350 controller requires an external reference clock to feed its internal PLL. This reference may be supplied via a crystal or oscillator. The DLPC350 controller accepts a reference clock of 32 MHz with a maximum frequency variation of 100 ppm (including aging, temperature, and trim component variation). When a crystal is used, several discrete components are also required, as shown in Figure 26.

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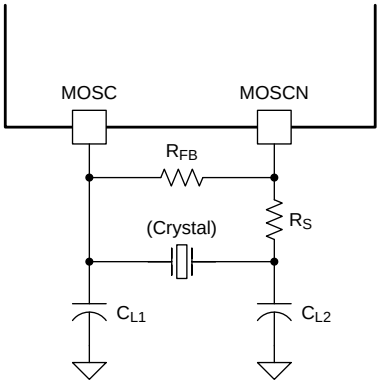

C_L = crystal load capacitance in F

$C_{L1} = 2 \times (C_L - C_{stray\text{-}MOSC})$

$C_{L2} = 2 \times (C_L - C_{stray\text{-}MOSCN}$

$C_{stray\text{-}MOSC}$ = sum of package and PCB capacitance at the crystal pin associated withe ASIC signal MOSC

$C_{stray\text{-}MOSCN}$ = sum of package and PCB capacitance at the crystal pin associated withe ASIC signal MOSCN

Figure 26. Recommended Crystal Oscillator Configuration

Table 27. Crystal Port Electrical Characteristics

PARAMETER	NOM	UNIT
MOSC to GND capacitance	3.9	pF
MOSCN to GND capacitance	3.8	pF

Table 28. Recommended Crystal Configuration

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	32	MHz
Crystal frequency tolerance (including accuracy, temperature, aging and trim sensitivity)	±100	PPM
Crystal equivalent series resistance (ESR)	50 maximum	Ω
Crystal load	10	pF
Crystal shunt load	7 maximum	pF
Crystal frequency temperature stability	±30	PPM
R_S drive resistor (nominal)	100	Ω
R_{FB} feedback resistor (nominal)	1	MΩ
C_{L1} external crystal load capacitor (MOSC)	Typical drive level with TCX9C3207001 crystal (ESRmax = 30 Ω) = 160 µW. See Figure 26	pF
C_{L2} external crystal load capacitor (MOSCN)	Typical drive level with TCX9C3207001 crystal (ESRmax = 30 Ω) = 160 µW. See Figure 26	pF
PCB layout	A ground isolation ring around the crystal	

If an external oscillator is used, then the oscillator output must drive the MOSC pin on the DLPC350 controller, and the MOSCN pin should be left unconnected. Note that the DLPC350 controller can only accept a triangular waveform.

Similar to the crystal option, the oscillator input frequency is limited to 32 MHz.

It is assumed that the external crystal or oscillator stabilizes within 50 ms after stable power is applied.

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11.2.3 Recommended DLPC350 PLL Layout Configuration

High-frequency decoupling is required for both 1.2-V and 1.8-V PLL supplies and should be provided as close as possible to each of the PLL supply package pins as shown in the example layout in Figure 27. TI recommends that decoupling capacitors be placed under the package on the opposite side of the board. High quality, low-ESR, monolithic, surface mount capacitors should be used. Typically 0.1 µF for each PLL supply should be sufficient. The length of a connecting trace increases the parasitic inductance of the mounting and thus, where possible, there should be no trace, allowing the via to butt up against the land itself. Additionally, the connecting trace should be made as wide as possible. Further improvement can be made by placing vias to the side of the capacitor lands or doubling the number of vias.

The location of bulk decoupling depends on the system design. Typically, a good ceramic capacitor in the 10-µF range is adequate.

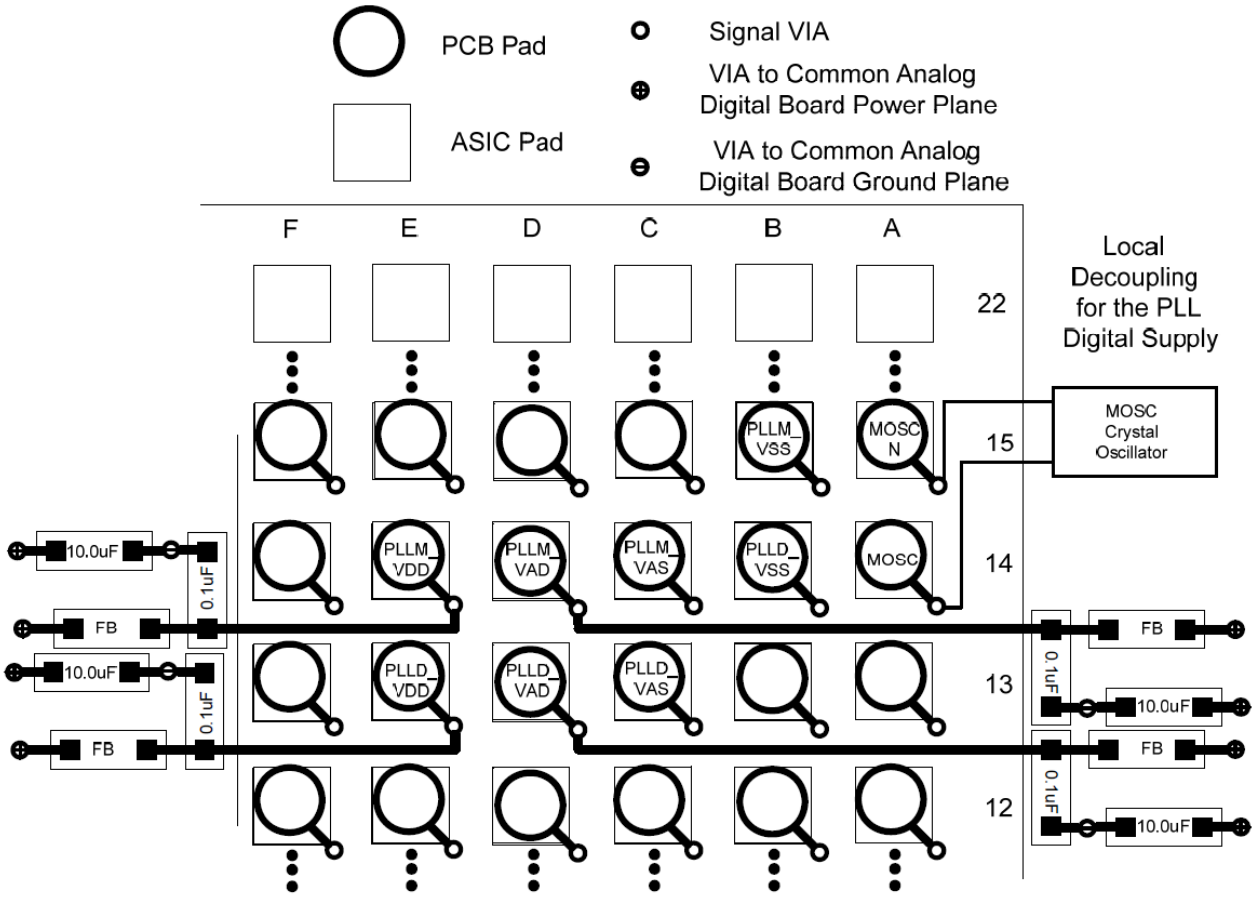

Figure 27. PLL Filter Layout

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Video Timing Parameter Definitions

The following is a list of the typical input video timing parameters and their definitions.

Active Lines Per Frame (ALPF) Number of lines in a frame containing displayable data. This is a subset of the TLPF

Active Pixels Per Line (APPL) Number of pixel clocks in a line containing displayable data. This is a subset of the TPPL

Horizontal Back Porch (HBP) Blanking Number of blank pixel clocks after Horizontal Sync but before the first active pixel. HBP times are in reference to the leading (active) edge of the respective sync signal

Horizontal Front Porch (HFP) Blanking Number of blank pixel clocks after the last active pixel but before horizontal sync

Horizontal Sync (HS) Timing reference point that indicates the start of the horizontal interval (line). The absolute reference point is defined by the active edge of the HS signal. This active edge is the reference from which all horizontal blanking parameters are measured

Total Lines (Active and Inactive) Per Frame (TLPF) Defines the vertical period (or frame time) in lines

Total Pixel Per Line (TPPL) Horizontal line period in pixel clocks. Total number of active and inactive pixel clocks per line

Vertical Back Porch (VBP) Blanking Number of blank lines after Vertical Sync but before the first active line

Vertical Front Porch (VFP) Blanking Number of blank lines after the last active line but before vertical sync

Vertical Sync (VS) Timing reference point that indicates the start of the vertical interval (frame). The absolute reference point is defined by the active edge of the VS signal. This active edge is the reference from which all vertical blanking parameters are measured

12.1.2 Device Nomenclature

Figure 28 provides a legend for reading the complete device name for any DLP® catalog device.

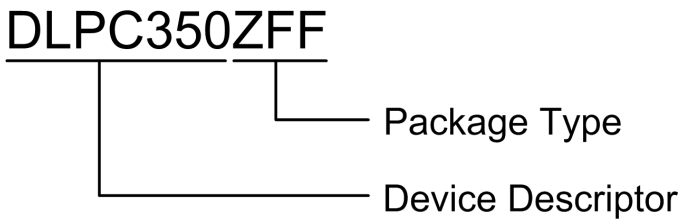

Figure 28. Device Nomenclature

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Device Support (continued)

12.1.3 Device Marking

The device marking consists of the fields shown in Figure 29.

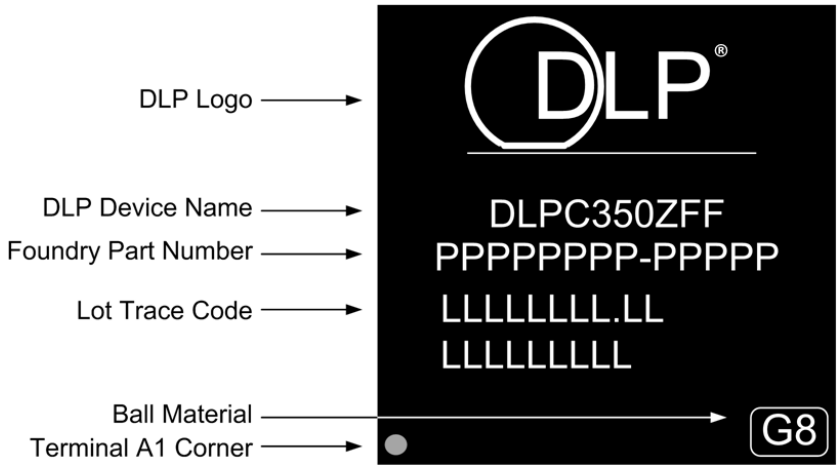

Figure 29. Device Marking

12.2 Documentation Support

12.2.1 Related Documentation

- *DLP4500 0.45 WXGA DMD Datasheet* (DLPS028)
- *DLP4500NIR 0.45 WXGA DMD Datasheet* (DLPS032)
- *DLPC350 Programmer's Guide* (DLPU010)
- *DLPC350 Configuration and Support Firmware* (DLPR350)

12.3 Trademarks

DLP is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
DLPC350ZFF	ACTIVE	BGA	ZFF	419	5	Call TI	Call TI	Level-3-255C-168 HRS		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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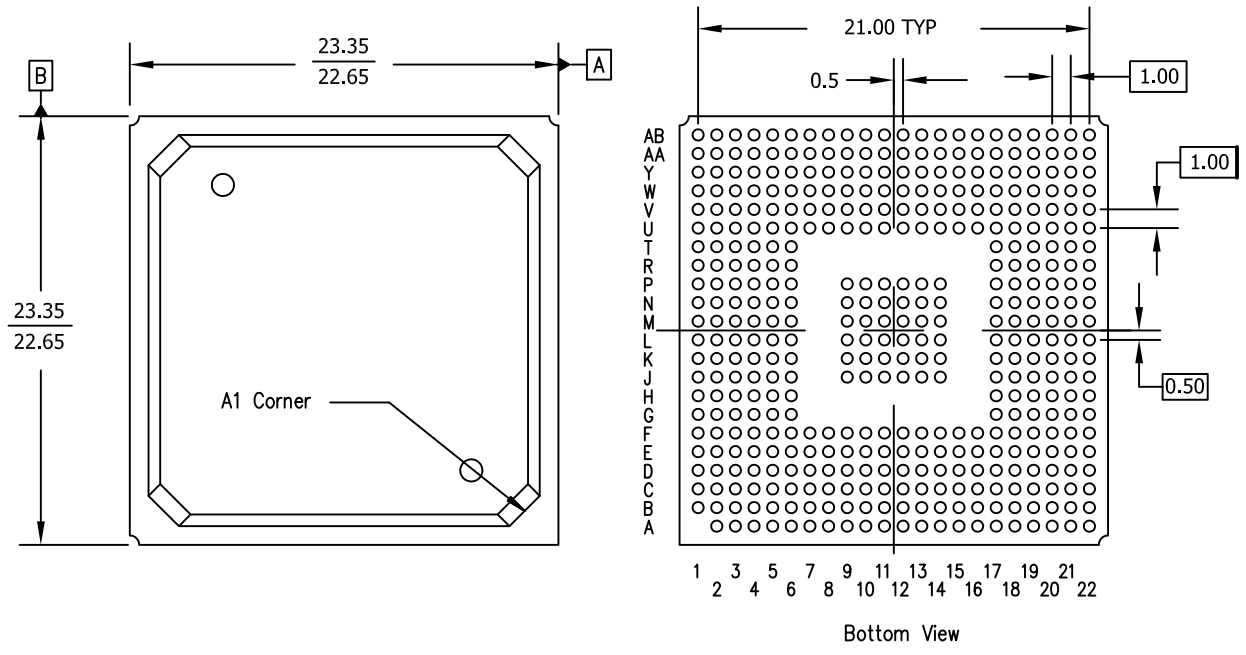
ZFF (S–PBGA–N419) PLASTIC BALL GRID ARRAY



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This package is Pb–free.

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