# Single Channel Operational Amplifier

# LM321

LM321 is a general purpose, single channel op amp with internal compensation and a true differential input stage. This op amp features a wide supply voltage ranging from 3 V to 32 V for single supplies and ±1.5 to ±16 V for split supplies, suiting a variety of applications. LM321 is unity gain stable even with large capacitive loads up to 1.5 nF. LM321 is available in a space-saving TSOP−5/SOT23−5 package.

### Features

- Wide Supply Voltage Range: 3 V to 32 V
- Short Circuit Protected Outputs
- True Differential Input Stage
- Low Input Bias Currents
- Internally Compensated
- Single and Split Supply Operation
- Unity Gain Stable with 1.5 nF Capacitive Load
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

### Typical Applications

- Gain Stage
- Active Filter
- Signal Processing

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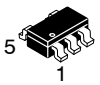
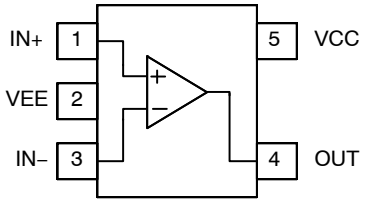
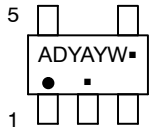



**TSOP−5**
**CASE 483**

### PIN CONNECTION




### MARKING DIAGRAM




ADY = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| LM321SN3T1G | TSOP−5 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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**Table 1. ABSOLUTE MAXIMUM RATINGS** (Over operating free-air temperature, unless otherwise stated)

| Parameter | Rating | Unit |
|---|---|---|
| Supply Voltage | 36 | V |
| **INPUT AND OUTPUT PINS** | | |
| Input Voltage | $V_{EE}$ – 0.3 to 32 | V |
| Input Current | ±10 | mA |
| Output Short Circuit Duration (Note 1) | Continuous | |
| **TEMPERATURE** | | |
| Operating Temperature | –40 to +125 | °C |
| Storage Temperature | –65 to +150 | °C |
| Junction Temperature | –65 to +150 | °C |
| **ESD RATINGS** (Note 2) | | |
| Human Body Model (HBM) | 200 | V |
| Charged Device Model (CDM) | 800 | V |
| Machine Model (MM) | 100 | V |
| **OTHER RATINGS** | | |
| Latch-Up Current (Note 3) | 100 | mA |
| MSL | Level 1 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Short circuits can cause excessive heating and eventual destruction.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JEDEC standard: JESD22–A114
   ESD Machine Model tested per JEDEC standard: JESD22–A115
3. Latch-up Current tested per JEDEC standard: JESD78

**Table 2. THERMAL INFORMATION** (Note 4)

| Parameter | Symbol | Package | Value | Unit |
|---|---|---|---|---|
| Junction to Ambient | $\theta_{JA}$ | TSOP–5/SOT23–5 | 235 | °C/W |

4. As mounted on an 80 × 80 × 1.5 mm FR4 PCB with 650 $mm^2$ and 2 oz (0.034 mm) thick copper heat spreader. Following JEDEC JESD/EIA 51.1, 51.2, 51.3 test guidelines.

**Table 3. RECOMMENDED OPERATING CONDITIONS**

| Parameter | Symbol | Range | Unit |
|---|---|---|---|
| Supply Voltage ($V_{CC}$ – $V_{EE}$) | $V_S$ | 3 to 32 | V |
| Specified Operating Range | $T_A$ | –40 to 85 | °C |
| Common Mode Input Voltage Range | $V_{CM}$ | $V_{EE}$ to $V_{CC}$–1.7 | V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 4. ELECTRICAL CHARACTERISTICS – $V_S$ = 5 V**

(At $T_A$ = +25°C, $R_L$ = 10 kΩ connected to mid-supply, $V_{CM}$ = $V_{OUT}$ = mid-supply, unless otherwise noted.
**Boldface** limits apply over the specified temperature range, $T_A$ = –40°C to 85°C, guaranteed by characterization and/or design.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| Offset Voltage | $V_{OS}$ | $V_S$ = 5 V, $V_{CM}$ = $V_{EE}$ to $V_{CC}$ – 1.7 V<br>$T_A$ = 25°C<br>$T_A$ = –40°C to 85°C | <br>–<br>– | <br>0.3<br>– | <br>7<br>**9** | mV |
| Offset Voltage Drift vs Temp | $\Delta V_{OS}/\Delta T$ | $T_A$ = –40°C to 85°C | – | **7** | – | μV/°C |
| Input Bias Current | $I_{IB}$ | $T_A$ = 25°C<br>$T_A$ = –40°C to 85°C | –<br>– | –10<br>– | –<br>**–500** | nA |
| Input Offset Current | $I_{OS}$ | $T_A$ = 25°C<br>$T_A$ = –40°C to 85°C | –<br>– | 1<br>– | –<br>**150** | nA |
| Common Mode Rejection Ratio | CMRR | $V_{CM}$ = $V_{EE}$ to $V_{CC}$ – 1.7 V | 65 | 85 | – | dB |
| Input Resistance | $R_{IN}$ | Differential<br>Common Mode | –<br>– | 85<br>300 | –<br>– | GΩ |
| Input Capacitance | $C_{IN}$ | Differential<br>Common Mode | –<br>– | 0.6<br>1.6 | –<br>– | pF |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| Open Loop Voltage Gain | $A_{VOL}$ | | – | 100 | – | dB |
| Open Loop Output Impedance | $Z_{OUT_OL}$ | f = UGBW, $I_O$ = 0 mA | – | 1,200 | – | Ω |
| Output Voltage High | $V_{OH}$ | $R_L$ = 2 kΩ to $V_{EE}$<br>$R_L$ = 10 kΩ to $V_{EE}$ | **$V_{CC}$–1.8**<br>**$V_{CC}$–1.8** | $V_{CC}$–1.4<br>$V_{CC}$–1.4 | –<br>– | V |
| Output Voltage Low | $V_{OL}$ | $R_L$ = 10 kΩ to $V_{CC}$ | – | $V_{EE}$+0.8 | **$V_{EE}$+1.0** | V |
| Output Current Capability | $I_O$ | Sinking Current<br>$V_S$ = 5 V<br>$V_S$ = 15 V | <br>**10**<br>**10** | <br>20<br>20 | <br>–<br>– | mA |
| Output Current Capability | $I_O$ | Sourcing Current<br>$V_S$ = 5 V<br>$V_S$ = 15 V | <br>**20**<br>**20** | <br>40<br>40 | <br>–<br>– | mA |
| Capacitive Load Drive | $C_L$ | Phase Margin = 15° | – | 1,500 | – | pF |
| **NOISE PERFORMANCE** | | | | | | |
| Voltage Noise Density | $e_N$ | $f_{IN}$ = 1 kHz | – | 40 | – | nV/√Hz |
| **DYNAMIC PERFORMANCE** | | | | | | |
| Gain Bandwidth Product | GBWP | $C_L$ = 25 pF, $R_L$ to $V_{CC}$ | – | 750 | – | kHz |
| Gain Margin | $A_M$ | $C_L$ = 25 pF, $R_L$ to $V_{CC}$ | – | 14 | – | dB |
| Phase Margin | $\alpha_M$ | $C_L$ = 25 pF, $R_L$ to $V_{CC}$ | – | 60 | – | ° |
| Slew Rate | SR | $C_L$ = 25 pF, $R_L$ = ∞ | – | 0.3 | – | V/μs |
| **POWER SUPPLY** | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_S$ = 5 V to 32 V | **62** | 100 | – | dB |
| Quiescent Current | $I_Q$ | No Load | – | 0.25 | **0.5** | mA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Table 5. ELECTRICAL CHARACTERISTICS – $V_S$ = 32 V**

(At $T_A$ = +25°C, $R_L$ = 10 kΩ connected to mid-supply, $V_{CM}$ = $V_{OUT}$ = mid-supply, unless otherwise noted.
**Boldface** limits apply over the specified temperature range, $T_A$ = –40°C to 85°C, guaranteed by characterization and/or design.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| Offset Voltage | $V_{OS}$ | $V_S$ = 32 V, $V_{CM}$ = $V_{EE}$ to $V_{CC}$ – 1.7 V<br>$T_A$ = 25°C<br>$T_A$ = –40°C to 85°C | <br>–<br>– | <br>0.3<br>– | <br>7<br>**9** | mV |
| Offset Voltage Drift vs Temp | $\Delta V_{OS}/\Delta T$ | $T_A$ = –40°C to 85°C | – | **7** | – | μV/°C |
| Common Mode Rejection Ratio | CMRR | $V_{CM}$ = $V_{EE}$ to $V_{CC}$ – 1.7 V | – | 100 | – | dB |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| Open Loop Voltage Gain | $A_{VOL}$ | $T_A$ = 25°C<br>$T_A$ = –40°C to 85°C | –<br>**84** | 100<br>– | –<br>– | dB |
| Open Loop Output Impedance | $Z_{OUT_OL}$ | f = UGBW, $I_O$ = 0 mA | – | 2,000 | – | Ω |
| Output Voltage High | $V_{OH}$ | $R_L$ = 2 kΩ to $V_{EE}$<br>$R_L$ = 10 kΩ to $V_{EE}$ | **$V_{CC}$–2.5**<br>**$V_{CC}$–2.5** | $V_{CC}$–2.0<br>$V_{CC}$–1.5 | –<br>– | V |
| Output Voltage Low | $V_{OL}$ | $R_L$ = 10 kΩ to $V_{CC}$ | – | $V_{EE}$+1.0 | **$V_{EE}$+1.5** | V |
| Capacitive Load Drive | $C_L$ | Phase Margin = 15° | – | 1,500 | – | pF |
| **NOISE PERFORMANCE** | | | | | | |
| Voltage Noise Density | $e_N$ | $f_{IN}$ = 1 kHz | – | 40 | – | nV/√Hz |
| Total Harmonic Distortion + Noise | THD+N | $V_S$ = 30 V, $f_{IN}$ = 1 kHz, $R_L$ to $V_{CC}$ | – | 0.02 | – | % |
| **DYNAMIC PERFORMANCE** | | | | | | |
| Gain Bandwidth Product | GBWP | $C_L$ = 25 pF, $R_L$ to $V_{CC}$ | – | 900 | – | kHz |
| Gain Margin | $A_M$ | $C_L$ = 25 pF, $R_L$ to $V_{CC}$ | – | 18 | – | dB |
| Phase Margin | $\alpha_M$ | $C_L$ = 25 pF, $R_L$ to $V_{CC}$ | – | 66 | – | ° |
| Slew Rate | SR | $C_L$ = 25 pF, $R_L$ = ∞ | – | 0.4 | – | V/μs |
| **POWER SUPPLY** | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_S$ = 5 V to 32 V | **62** | 100 | – | dB |
| Quiescent Current | $I_Q$ | No Load, $V_S$ = 32 V | – | 0.3 | **1.2** | mA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## TYPICAL CHARACTERISTICS

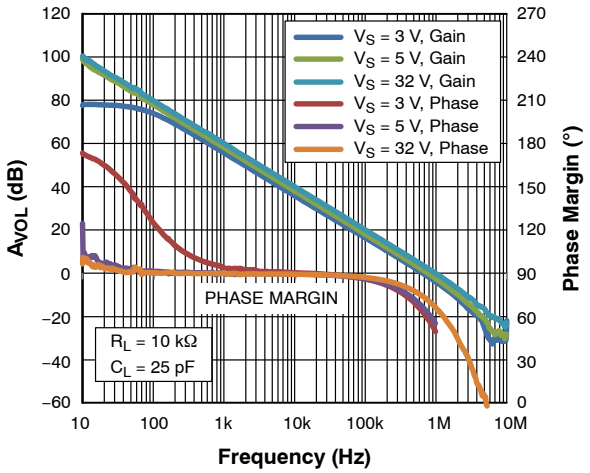



**Figure 1. Open Loop Gain and Phase Margin vs. Frequency**

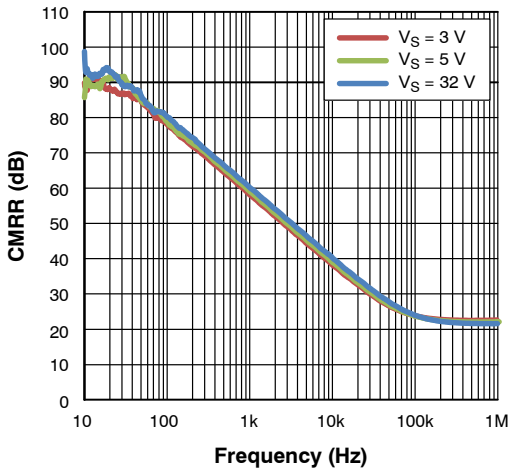



**Figure 2. CMRR vs. Frequency**

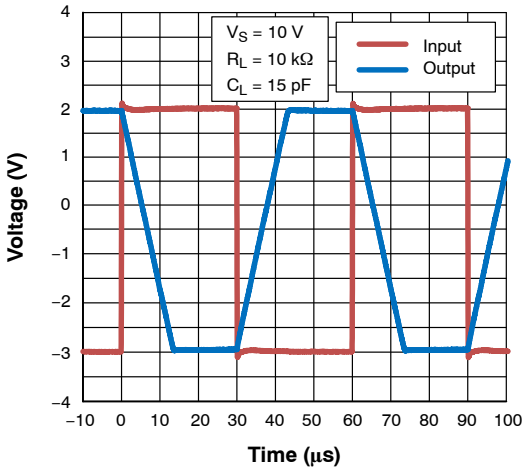



**Figure 3. Inverting Large Signal Step Response**

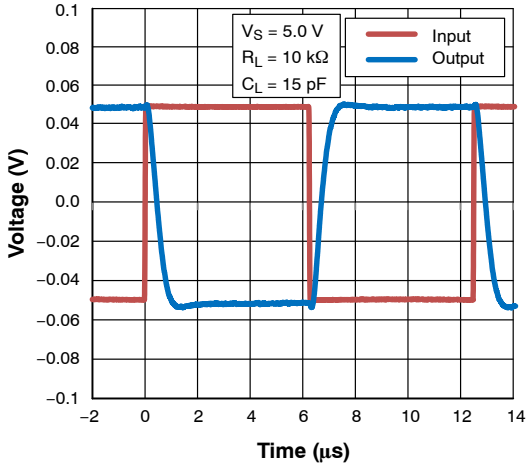



**Figure 4. Inverting Small Signal Step Response**

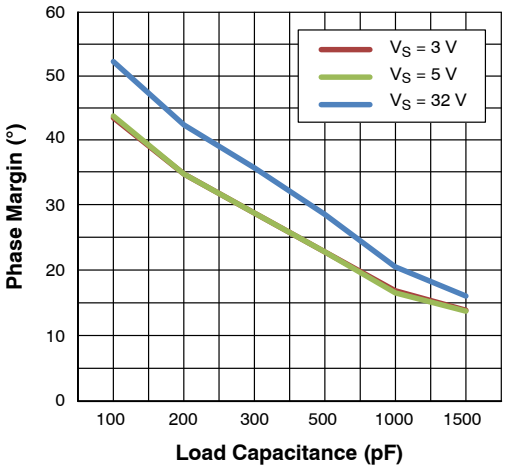



**Figure 5. Phase Margin vs. Load Capacitance**

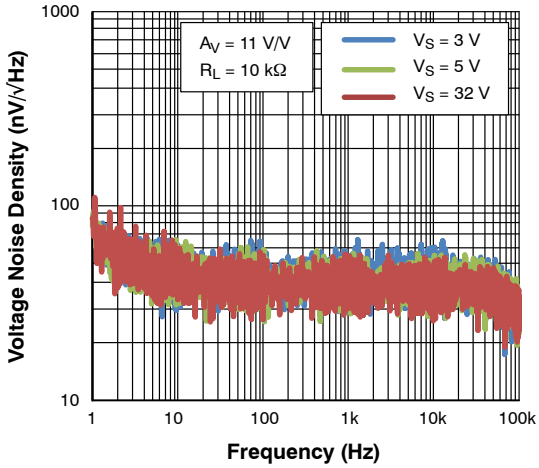



**Figure 6. Voltage Noise Density vs. Frequency**

## TYPICAL CHARACTERISTICS

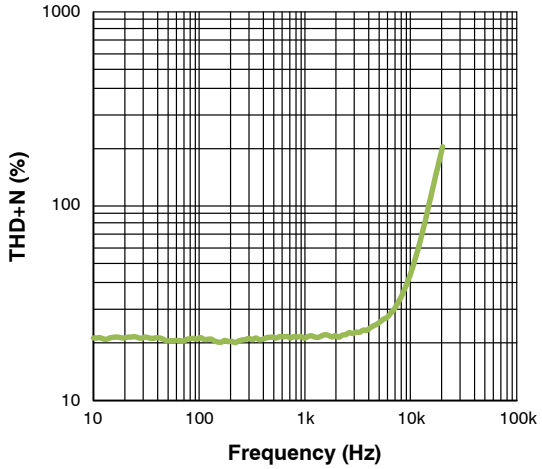



Figure 7. THD+N vs. Frequency

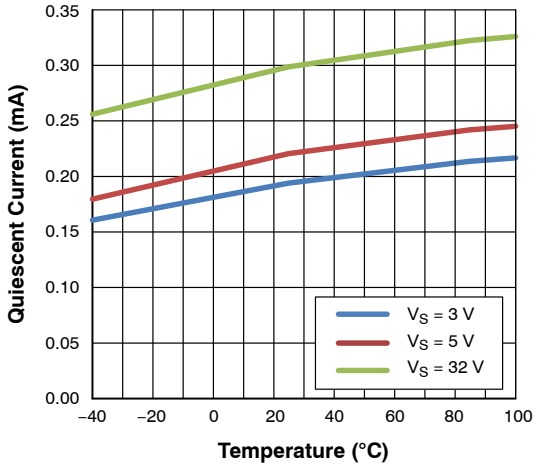



Figure 8. Quiescent Current vs. Temperature

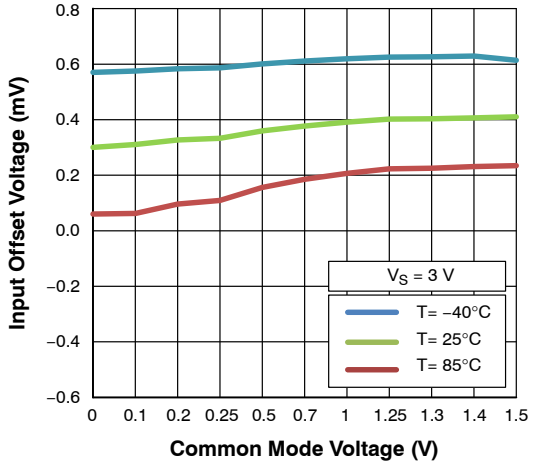



Figure 9. Input Offset Voltage vs. Common Mode Voltage at 3 V Supply

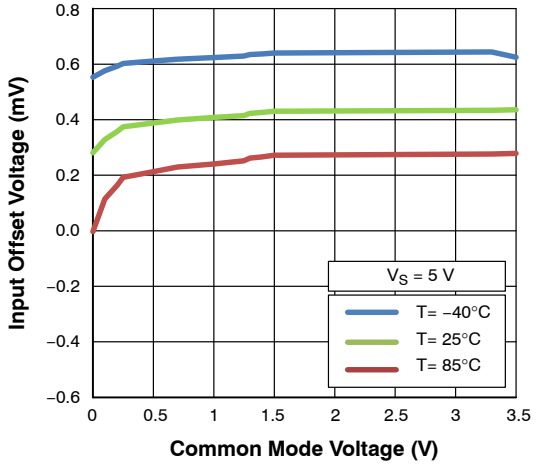



Figure 10. Input Offset Voltage vs. Common Mode Voltage at 5 V Supply

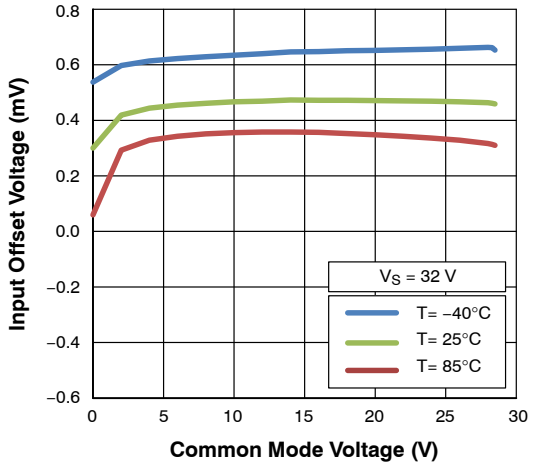



Figure 11. Input Offset Voltage vs. Common Mode Voltage at 32 V Supply

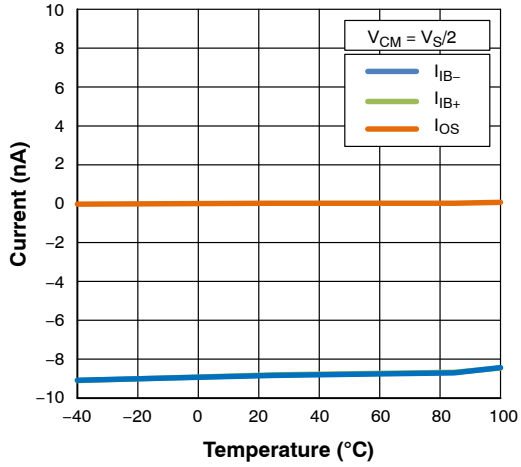



Figure 12. Input Bias and Offset Current vs. Temperature

## TYPICAL CHARACTERISTICS

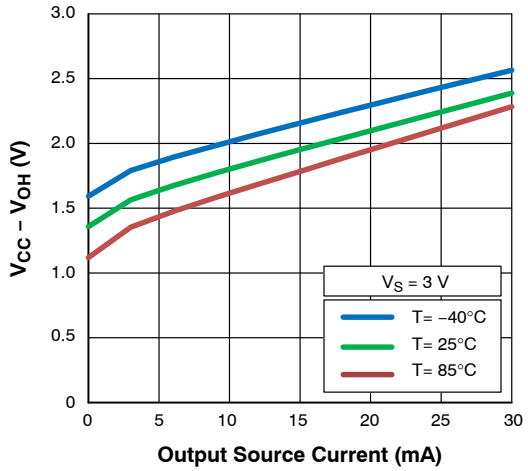



**Figure 13. High Level Output Voltage Swing vs. Output Current at 3 V Supply**

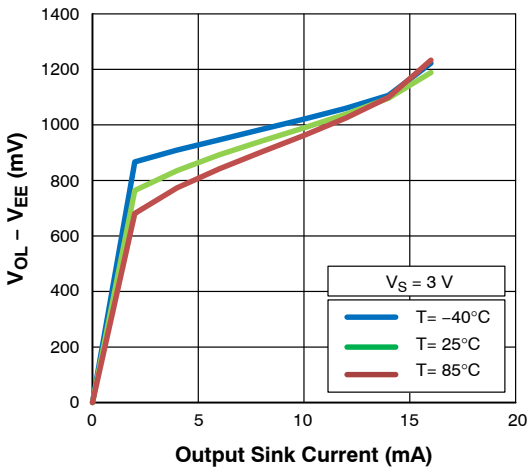



**Figure 14. Low Level Output Voltage Swing vs. Output Current at 3 V Supply**

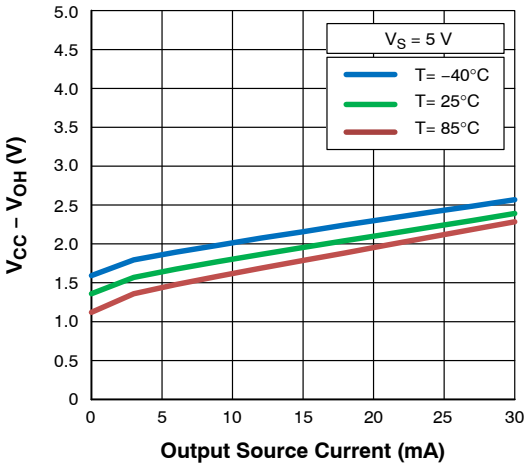



**Figure 15. High Level Output Voltage Swing vs. Output Current at 5 V Supply**

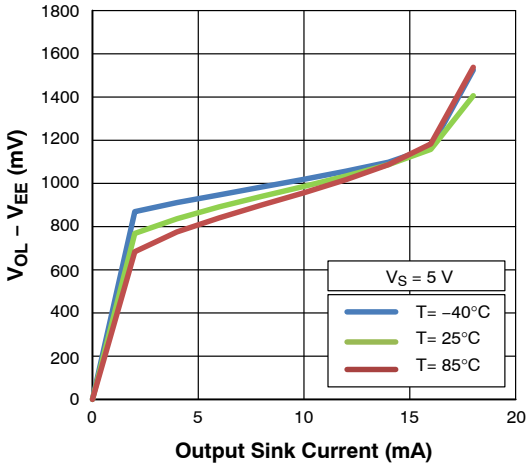



**Figure 16. Low Level Output Voltage Swing vs. Output Current at 5 V Supply**

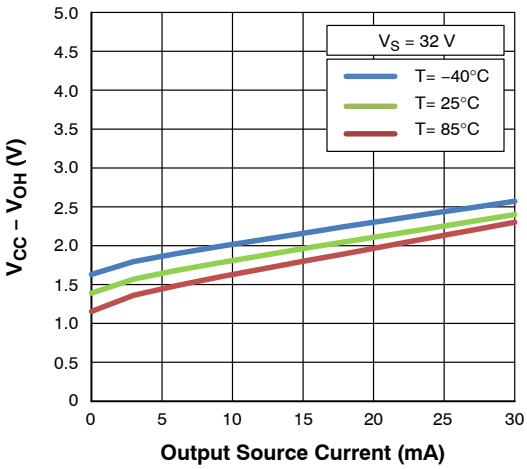



**Figure 17. High Level Output Voltage Swing vs. Output Current at 32 V Supply**

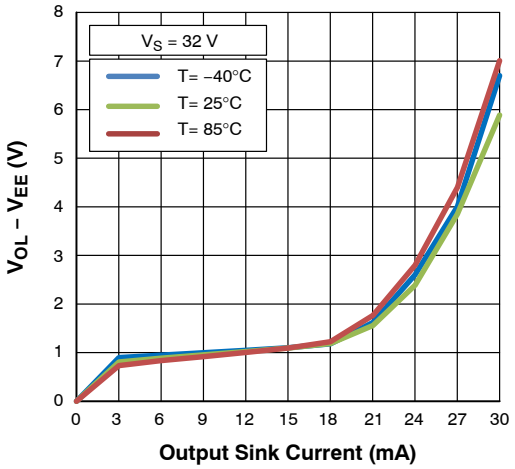



**Figure 18. Low Level Output Voltage Swing vs. Output Current at 32 V Supply**

## APPLICATION INFORMATION

### CIRCUIT DESCRIPTION

The LM321 is made using two internally compensated, two−stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single−ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal−voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

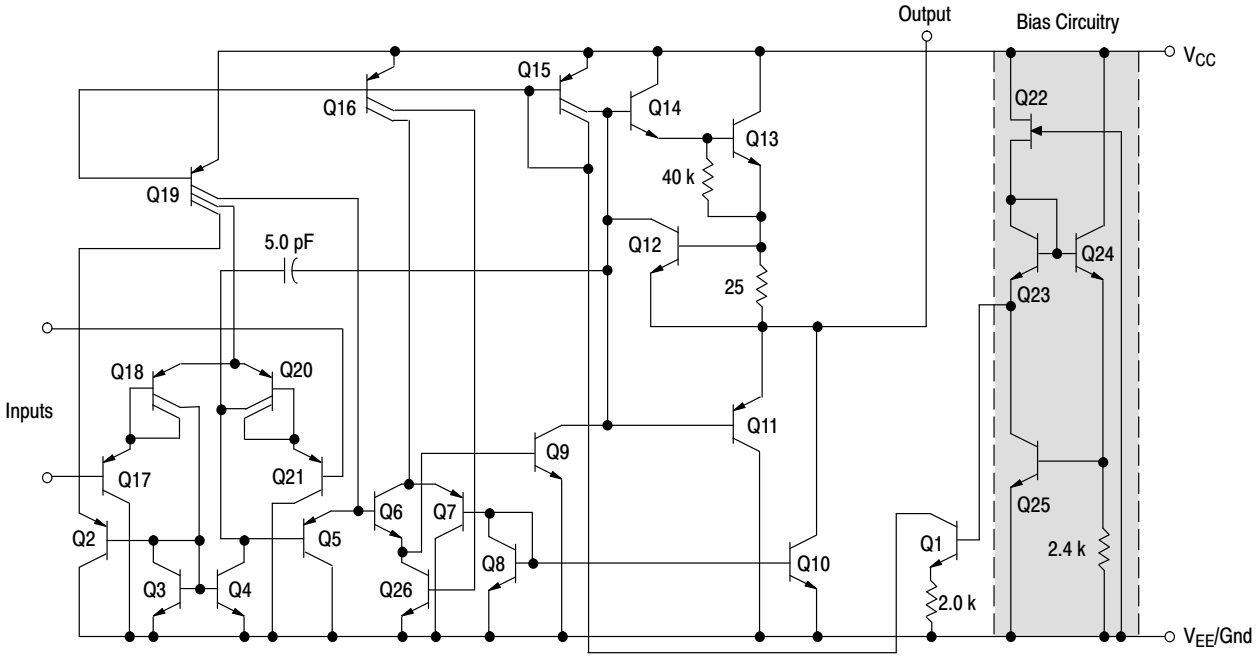



**Figure 19. LM321 Representative Schematic Diagram**

LM321 has a class B output stage, which is comprised of push−pull transistors. This type of output is inherently subject to crossover distortion near mid−rail where neither push or pull transistors are conducting. Several techniques can be used to minimize crossover distortion. Connecting the output load to either the positive or negative supply rail instead of mid−rail can reduce the crossover distortion. Additionally, increasing the load resistance relatively decreases the amount of crossover distortion.

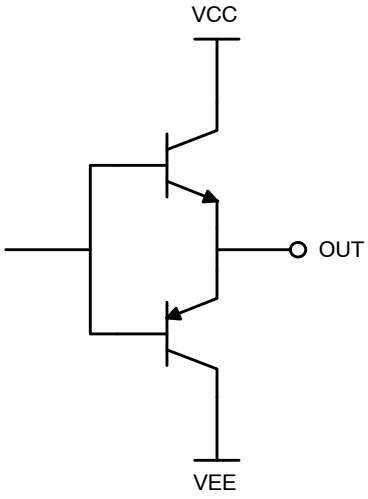



**Figure 20. Simplified Class B Output**

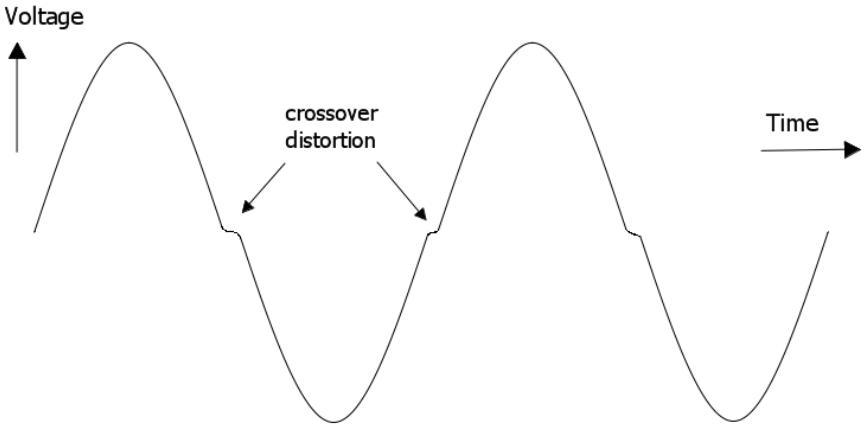


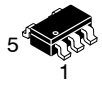

**Figure 21. Sine wave with crossover distortion**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

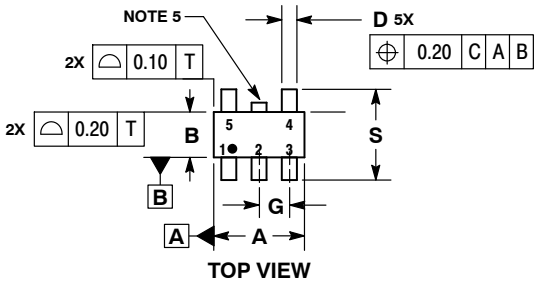
ON Semiconductor®

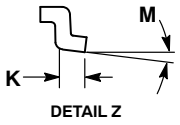
**TSOP−5**
CASE 483
ISSUE M

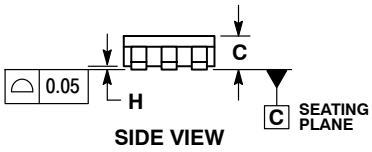
DATE 17 MAY 2016

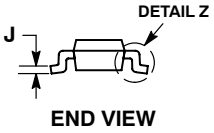



**SCALE 2:1**



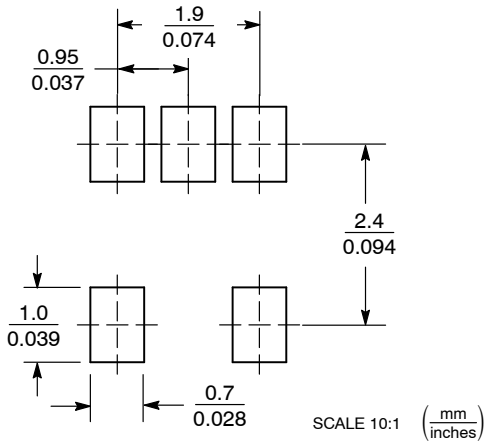




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

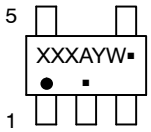
| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.85 | 3.15 |
| B | 1.35 | 1.65 |
| C | 0.90 | 1.10 |
| D | 0.25 | 0.50 |
| G | 0.95 BSC | |
| H | 0.01 | 0.10 |
| J | 0.10 | 0.26 |
| K | 0.20 | 0.60 |
| M | 0 ° | 10 ° |
| S | 2.50 | 3.00 |

### SOLDERING FOOTPRINT*

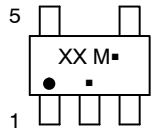



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




**Analog**




**Discrete/Logic**

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

| | | |
|---|---|---|
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