Digital Isolator Design Guide

This design guide helps system designers of galvanically isolated systems to begin designing with TI's broad portfolio of digital isolators and isolated functions in the shortest time possible. This portfolio includes the ISO78xx family of 5.7-kVrms reinforced digital isolators, the ISO77xx family of 5-kVrms digital isolators, the ISO73xx family of 3-kVrms digital isolators, and the ISO71xx family of 2.5-kVrms digital isolators, among others. This document explains the basic operating principle of an isolator, suggests where to place it within a system design, and recommends guidelines for an electromagnetic compatible (EMC) circuit-board design.

Further information is available in the respective product data sheets and the EVM manuals.

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1   Operating Principle

Isolation is a means of preventing dc and unwanted ac currents between two parts of a system, while allowing signal and power transfer between those two parts. Electronic devices and semiconductor ICs used for isolation are called isolators. In general, an isolator can be abstracted as comprising of a high-voltage isolation component or barrier, a transmitter (TX) to couple signal into one side of the isolation component, and a receiver (RX) to convert the signal available on the other side of the isolation component into digital levels.

TI's isolators use SiO_2 (silicon dioxide) based, high-voltage capacitors to serve as the isolation component. For the TX and RX circuits, two different architectures are used: Edge based and On-Off Keying (OOK) based. These architectures are explained in Section 1.1 and Section 1.2.

1.1   Edge-Based Communication

The conceptual block diagram of edge-based communication is shown in Figure 1. The isolators of ISO73xx, ISO74xx, ISO71xx, ISO76xx, ISO75xx, and ISO72xx families use this architecture in some form.

The device consists of at least two data channels, a high-frequency channel (HF) with a bandwidth from 100kbps up to 150Mbps, and a low-frequency channel (LF) covering the range from 100kbps down to dc.

In principle, a single-ended input signal entering the HF-channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into small and narrow transients, which then are converted into rail-to-rail differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit (*as in the case of a low-frequency signal*) the DCL forces the output-multiplexer to switch from the high-frequency to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.
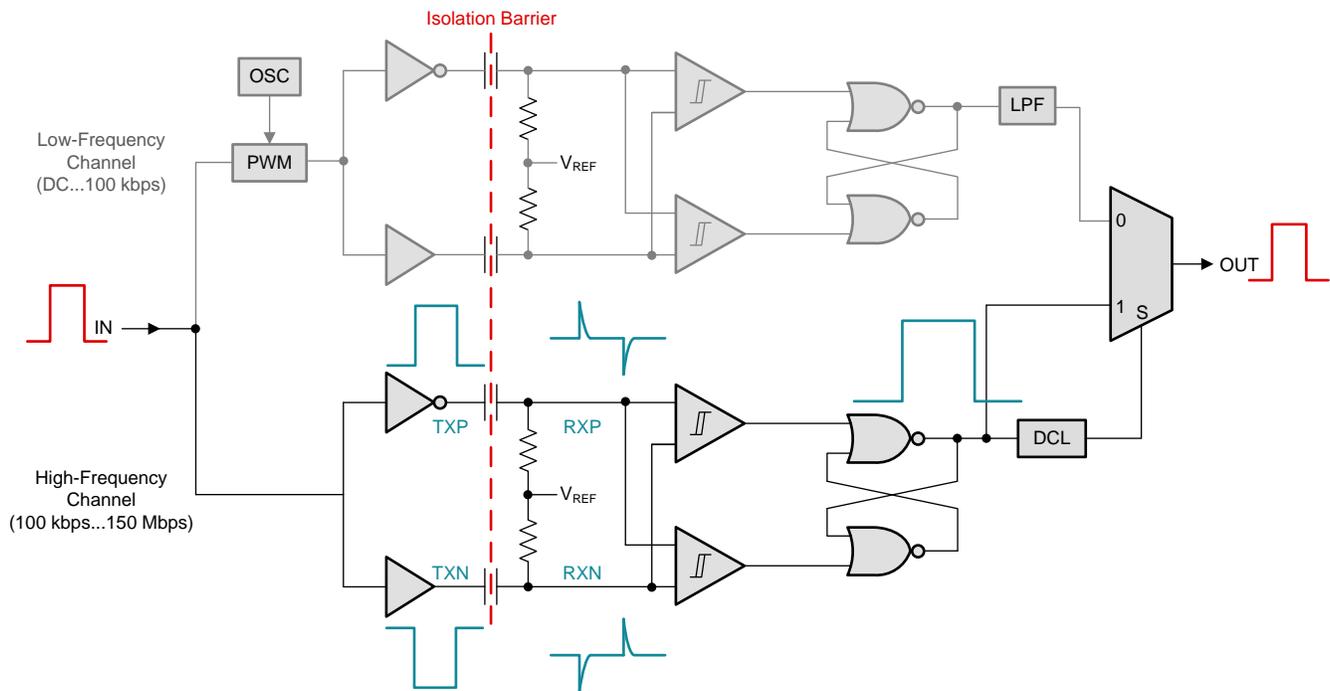
Figure 1. Conceptual Block Diagram of Edge-Based Architecture

1.2 On-Off Keying (OOK) Based Communication

The conceptual operation of OOK-based communication is shown in Figure 2. The corresponding signaling is shown in Figure 3. The isolators in both the ISO78xx family and ISO77xx family use this architecture.

In this architecture, the incoming digital bit stream is modulated with an internal spread spectrum oscillator clock to generate OOK signaling, such that one of the input states is represented by transmission of a carrier frequency, and the other state by no transmission. This modulated signal is coupled to the isolation barrier and appears in an attenuated form on the receive side. The receive path consists of a pre-amplifier to gain up the incoming signal followed by an envelope detector that serves as a demodulator to regenerate the original digital pattern. The TX and RX signal conditioning circuits are used to improve the common mode rejection of the channel resulting in better Common Mode Transient Immunity (CMTI).
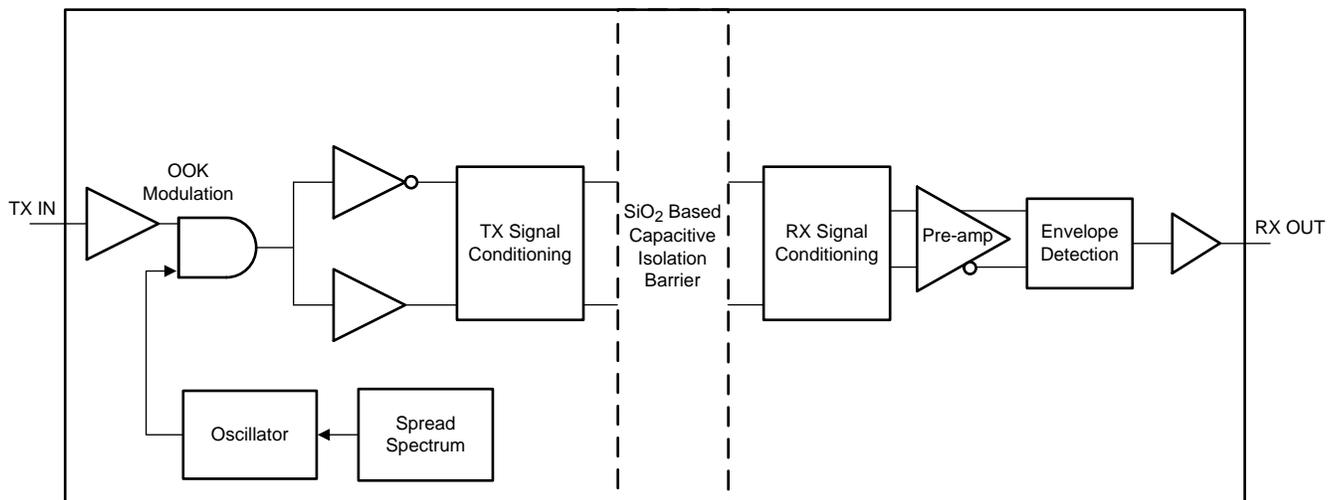

**Figure 2. Conceptual Block Diagram of On-Off Keying (OOK) Architecture**
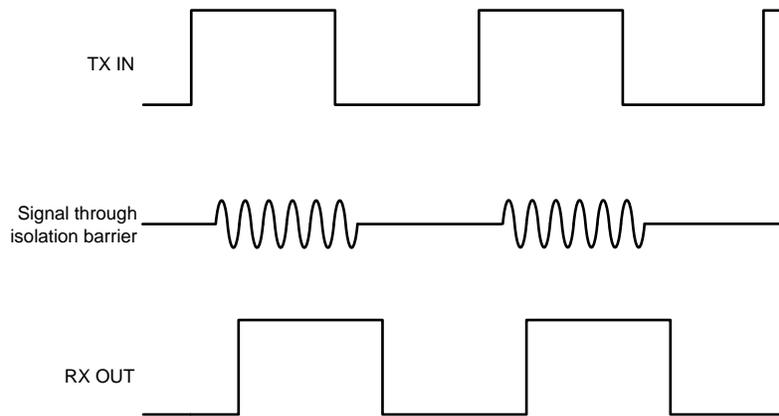
Figure 3. Representative Signal in OOK Architecture

2   Typical Applications for Digital Isolators and Isolated Functions


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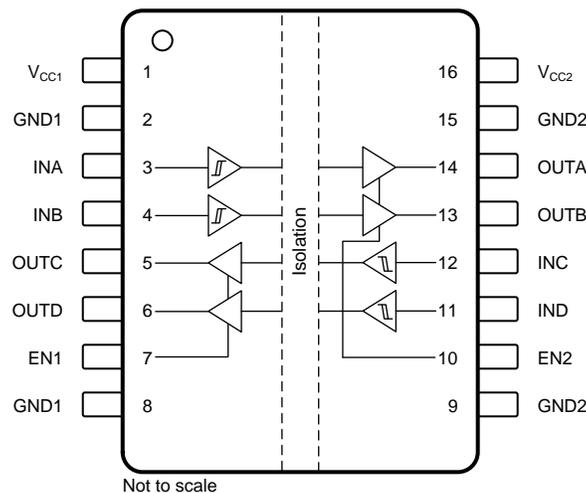
Figure 4. Example Isolator in a 16-Pin Package

A pin diagram of a typical digital isolator is shown in Figure 4. It consists of two supplies: V_{CC1} and V_{CC2} , two grounds: GND1 and GND2, and input and output pins on either side referred to the respective grounds. That is, in Figure 4, pins 1 through 8 are referred to GND1 and pins 9 through 16 are referred to GND2.

Digital isolators use single-ended, CMOS or TTL logic, switching technology. The voltage range normally ranges 3 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}, though some devices may support a larger supply voltage range. For example, ISO78xx devices can work with supplies down to 2.25 V. When designing with digital isolators, it is important to keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended digital signal lines.

Isolated functions are devices where additional functionality, such as a transceiver or a gate-driver is integrated along with an isolator. An example is the integrated isolated-RS485 described later on in this section. Unlike digital isolators, an isolated function may need to conform to certain standards. For example, an isolated-I²C buffer will be compatible to the I²C standard. Also, an isolated function may run off higher supplies, for example, an isolated gate-driver may use ±15 V to be able to drive an IGBT gate.

Isolation is required in modern electrical systems for a variety of reasons. Some examples are to protect human operators from high voltage transients and preventing damage to expensive processors, ASICs or FPGAs in high-voltage systems, breaking the ground loop in communication networks and communication to high-side devices in motor drive or power converter systems. Examples of applications that need isolation include industrial automation systems, motor drives, medical equipment, solar inverters, power supplies, and hybrid electric vehicles (HEV).

Some example applications of digital isolators and isolated functions are presented in this section. For more examples, detailed application diagrams and use cases, please refer the respective product datasheets.

Figure 5 presents the most simple isolator application. Here the entire circuit constitutes a single-ended, low-voltage system in which a digital isolator connects the SPI interface of a controller with the SPI interface of a data converter. The most commonly applied isolators in SPI interfaces are ISO7x31 and ISO7x41, hence often designated as 3- and 4-channel SPI isolators.
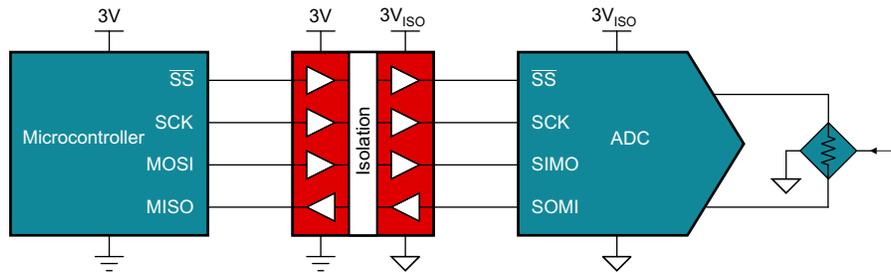
Figure 5. Isolated SPI Interface

The full-blown, isolated RS-232 interface in Figure 6 requires two quad isolators due to the six control signals required in addition to the actual data lines, RX and TX. Although the entire system is single-ended, the high-voltage requirements of the symmetric, 13-V bus supply make it necessary to galvanically isolate the data link between the UART and the low-voltage side of the bus transceiver. Also, the 13-V dc bus may be in turn generated from a higher supply, in which case the isolation also serves as a means of protection against high-voltage transients on the system supply lines.
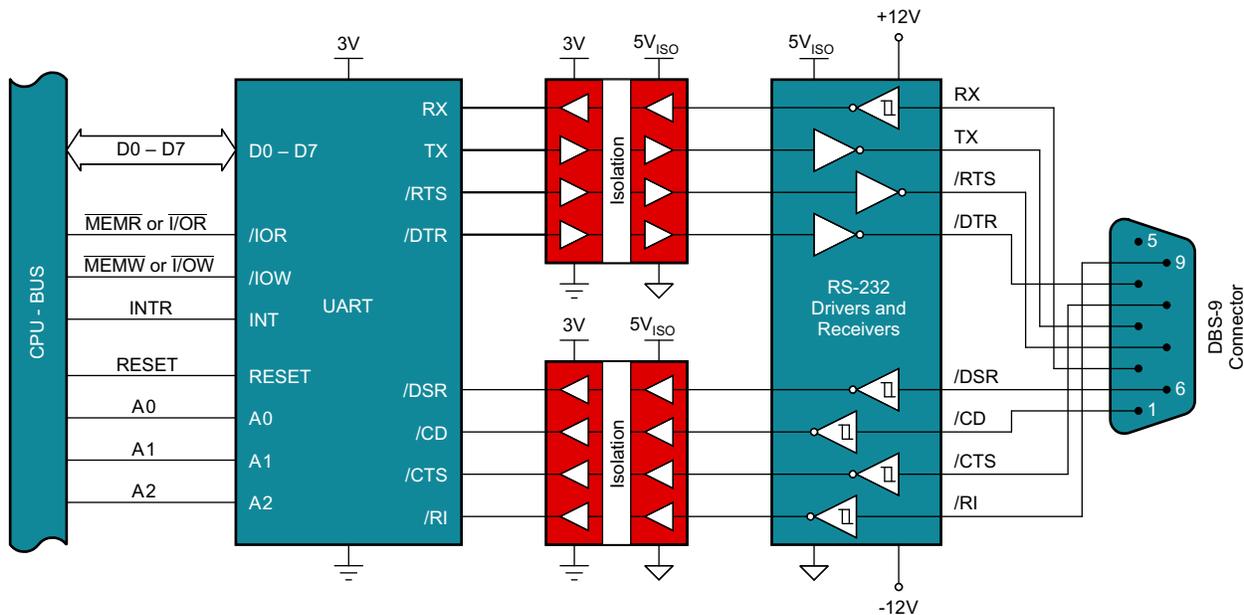

Figure 6. Isolated RS-232 Interface

As in the example in Figure 6, the isolation of the RS-485 interface in Figure 7 occurs between the controller and the bus transceiver. Despite the entire interface circuit being a low-volt system, the differential nature of the transmission bus requires prior isolation on the single-ended side. In a multi-node distributed RS-485 network, different nodes may be referenced to grounds at different potential, in which case isolation enables communication by level shifting between those ground potentials.
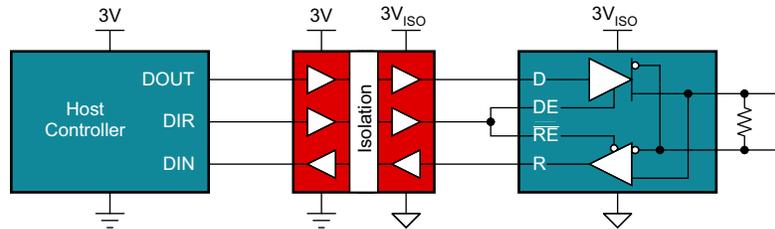

Figure 7. Isolated RS-485 Interface

Due to the simplicity of the interface shown in Figure 8, it is possible to integrate the isolator function into the transceiver circuit, thus providing an application-specific isolator device featuring low-cost and low component count. Figure 8 is an example of an isolated function.
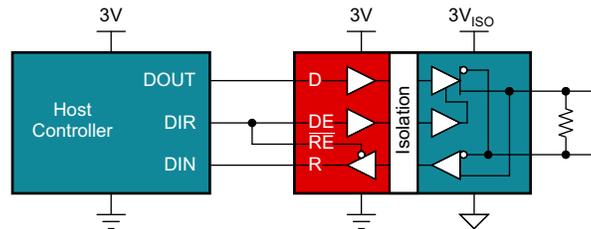

Figure 8. Integrated Isolated RS-485 Interface

Not all applications of digital isolators and isolated functions are covered here. These are just examples to understand how the isolator is placed in a system. For more examples, detailed application diagrams, and use cases, please refer the respective product data sheets.

3   Digital Isolator Selection Guide

This section first describes key parameters to look for while choosing a digital isolator or isolated function, and then gives a brief introduction to families of isolators and isolated functions currently available from TI. Please refer the following links for a comprehensive isolator selection guide.

For an overview of all isolation products, with links to different parameterized product selection guides, please visit:
http://www.ti.com/isolation/overview.html

For a parameterized selection guide for digital isolators please visit:
http://www.ti.com/lsds/ti/isolators/digital-isolator-products.page

For a parameterized selection guide for isolated RS485 transceivers please visit:
http://www.ti.com/lsds/ti/isolators/isolated-rs-485-products.page

3.1   *Parameters of Interest*

This section briefly describes some of the parameters that are present in a typical isolator datasheet and their relevance to system design.

Isolation Performance:

1. Maximum transient isolation voltage (V_{IOTM}) and isolation withstand voltage (V_{ISO}) indicate an isolator's ability to withstand temporary (less than 60 seconds) high voltage.
2. Maximum repetitive peak voltage (V_{IORM}) and working voltage (V_{IOWM}) indicate the continuous voltage that the isolator can withstand throughout its lifetime.

3. Maximum surge isolation voltage (V_{IOSM}) indicates the maximum impulse voltage (waveform with 1.2-μs rise and 50-μs decay time) that the isolator can withstand.

Timing Parameters:

1. Data rate.
2. Propagation delay is important in systems where the round trip delay adds to the timing budget (for example, SPI interface) or if the delay is part of a control loop.
3. Propagation delay skew is important if timing budget relies on matching between channels; for example, if clock is transmitted on one channel and data on another channel in the same direction.
4. Glitch filter: Some digital isolators come with an integrated glitch filter that helps them operate well, even in noisy environments. However, the glitch filter increases propagation delay and reduces data rate.

Common Mode Transient Immunity (CMTI):

CMTI indicates the isolator's ability to tolerate fast changes in the potential difference between its grounds, or in other words, fast changes in common mode, without causing bit errors. High CMTI indicates a robust isolation channel.

Power Consumption:

Power consumption per channel at data rate of interest.

Package:

1. Creepage and Clearance: Distance along the surface of the package and through the air between pins on one side of the isolator to the pins on the other side. System level standards mandate minimum values of these parameters based on the working voltage, the peak transient voltage, and the surge voltage.
2. Comparative Tracking Index (CTI) indicates the ability of the package mold compound to handle steady high voltage without surface degradation. A higher CTI allows the use of smaller packages for the same working voltage.

3.2 Isolator Families

Table 1 briefly describes the key features of a few digital isolator families and isolated functions from TI. For a more exhaustive listing of devices please visit:
http://www.ti.com/lsds/ti/analog/isolators/overview.page

Table 1. Digital Isolator Families and Isolated Functions

Isolator Type	Device	Isolation Performance	Timing Performance	CMTI	Package	Power per Channel (5 typ, 1Mbps)
Digital Isolator	ISO78xx	V_{IOTM} = 8000 Vpk V_{IORM} = 2121 Vpk Surge = 12.8 kV	Data rate = 100Mbps Prop delay = 11 ns typ Skew = 2.5 ns max Glitch filter not required	10 kV/µs min	CTI > 600 16-SOIC	1.7 mA
Digital Isolator	ISO77xx	V_{IOTM} = 8000 Vpk V_{IORM} = 1414 Vpk Surge = 12.8 kV	Data rate = 100Mbps Prop delay = 10.7 ns typ Skew = 4.1 ns max Glitch filter not required	100 kV/µs typ 85 kV/µs min	CTI > 600 16-SOIC, 8-SOIC, 16-SSOP	1.4 mA
Digital Isolator	ISO73xx	V_{IOTM} = 4242 Vpk V_{IORM} = 1414 Vpk Surge = 6 kV	Data rate = 25Mbps Prop delay = 35 ns typ Skew = 3 ns max Integrated glitch filter	50 kV/µs typ 25 kV/µs min	400 < CTI < 600 8-SOIC, 16-SOIC	1.1 mA (5 V) 0.85 mA (3.3 V)
Digital Isolator	ISO71xx	V_{IOTM} = 4242 Vpk V_{IORM} = 566 Vpk Surge = 4 kV	Data rate = 50Mbps Prop delay = 21 ns typ Skew = 2 ns max Integrated glitch filter	50 kV/µs typ 25 kV/µs min	400 < CTI < 600 16-QSOP	1.65 mA (5 V) 1.3 mA (3.3 V)
Isolated CAN	ISO1050	V_{IOTM} = 4000 Vpk V_{IORM} = 1200 Vpk Surge = 4 kV	Loop delay = 150 ns typ	50 kV/µs typ 25 kV/µs min	400 < CTI < 600 16-SOIC, 8-SOP	State dependent
Isolated RS-485	ISO3082	V_{IOTM} = 4000 Vpk V_{IORM} = 560 Vpk Surge = 4 kV	Prop delay = 700 ns	50 kV/µs typ 25 kV/µs min	175 < CTI < 400 16-SOIC	State dependent
Isolated I²C	ISO1540 ISO1541	V_{IOTM} = 4000 Vpk V_{IORM} = 566 Vpk Surge = 4 kV	Clock freq max = 1 MHz Loop delay = 110 ns typ	50 kV/µs typ 25 kV/µs min	400 < CTI < 600 8-SOIC	State dependent
Isolated IGBT Gate Driver	ISO5500	V_{IOTM} = 4000 Vpk V_{IORM} = 679 Vpk Surge = 6 kV	Prop delay = 200 ns typ	50 kV/µs typ 25 kV/µs min	400 < CTI < 600 16-SOIC	15 mA

4 PCB Design Guidelines

4.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as printed-circuit board (PCB) material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0 and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing, flammability characteristics.

4.2 Layer Stack

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 9). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.
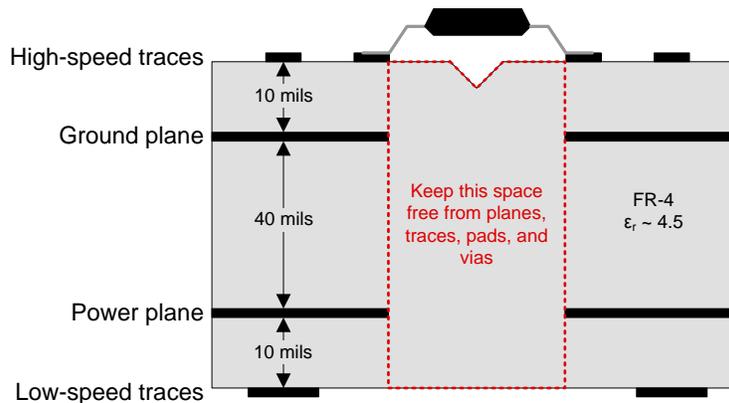
Figure 9. Recommended Layer Stack

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power/ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also, the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

4.3 Creepage Distance

Creepage distance is the shortest path between two conductive parts measured along the surface of the insulation. An adequate creepage distance protects against tracking, a process that produces a partially conducting path of localized deterioration on the surface of an insulating material as a result of the electric discharges on or close to an insulation surface.

The degree of tracking occurring depends on the comparative tracking index (CTI) of the material and the degree of pollution in the environment. Used for electrical insulating materials, the CTI provides a numerical value of the voltage that will cause failure by tracking during standard testing. IEC 112 provides a fuller explanation of tracking and CTI.

Tracking damaging the insulating material normally occurs because of one or more of the following reasons: humidity in the atmosphere, presence of contamination, corrosive chemicals, and altitude at which equipment is to be operated.

As isolation voltage levels continue to rise, it is more important than ever to have a robust PCB design that not only reduces electromagnetic interference emissions, but also reduces creepage problems. In addition to wide isolator packaging, techniques such as grooves can be used to attain a desired creepage distance (see Figure 10).
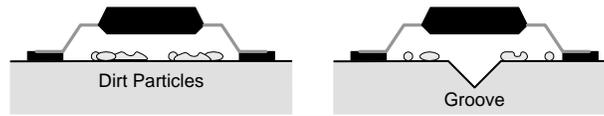
Figure 10. Groove Cutting Extends Effective Creepage Distance

For a groove (>1 mm wide), the only depth requirement is that the existing creepage distance plus the width of the groove and twice the depth of the groove must equal or exceed the required creepage distance. The groove must not weaken the substrate to a point that it fails to meet mechanical test requirements.

Also, on all layers keep the space under the isolator free from traces, vias, and pads to maintain maximum creepage distance (see Figure 9).

4.4 *Controlled Impedance Transmission Lines*

A controlled impedance transmission line is a trace whose characteristic impedance, Z_0, is tightly controlled by the trace geometries. In general, these traces match the differential impedance of the transmission medium, such as cables and line terminators, to minimize signal reflections. Around digital isolators, controlled impedance traces must match the isolator output impedance, $Z_0 \sim r_O$, which is known as source-impedance matching.
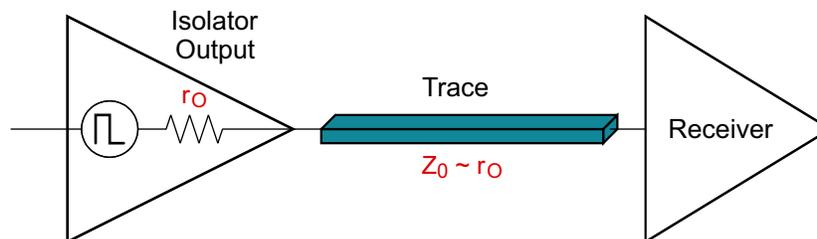
Figure 11. Source Impedance Matching: $Z_0 \sim r_O$

To determine Z_0, the dynamic output impedance of the isolator, $r_O = \Delta V_{OUT}/\Delta I_{OUT}$, needs to be established. For that purpose the output characteristic in Figure 12, (*taken from the ISO7240 data sheet*), is approximated by two linear segments indicating an $r_O \sim 260\ \Omega$ at low voltages, while for the majority of the curve, (*and thus the transition region of the output*), $r_O \sim 70\ \Omega$.
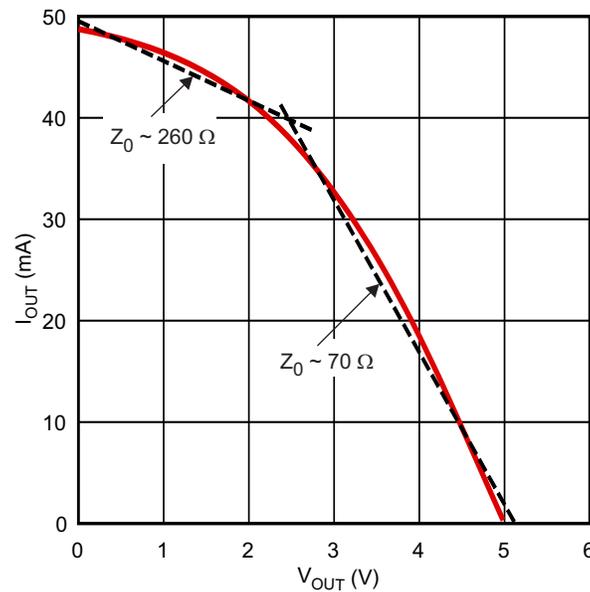
Figure 12. Isolator Output Characteristic

The required trace geometries, such as trace thickness (t) and width (w), the distance between trace and an adjacent ground layer (d), and the PCB dielectric (ε_r), are partially dictated by the copper-plating capabilities of the board manufacturing process and the dielectric of the chosen board material. Typical values are 1 and 2 oz of copper-plating, resulting in trace thicknesses of t = 1.37 mils and t = 2.74 mils, respectively. Dielectric values for FR-4 epoxy-glass vary between ε_r = 2.8 to 4.5 for microstrip, and ε_r = 4.5 for stripline traces.

With t and ε_r given, the designer has the freedom to define Z_0 through trace width w, and distance d. For PCB designs, however, the most critical dimensions are not the absolute values of w and d, but their ratio w/d. Easing the designer's task, Figure 13 plots the characteristic trace impedance as a function of the width-to-height (w/h) for a trace thickness of 2.74 mils (2-oz copper plating), an FR-4 dielectric of 4.5, and a trace-height of 10 mils above the ground plane.
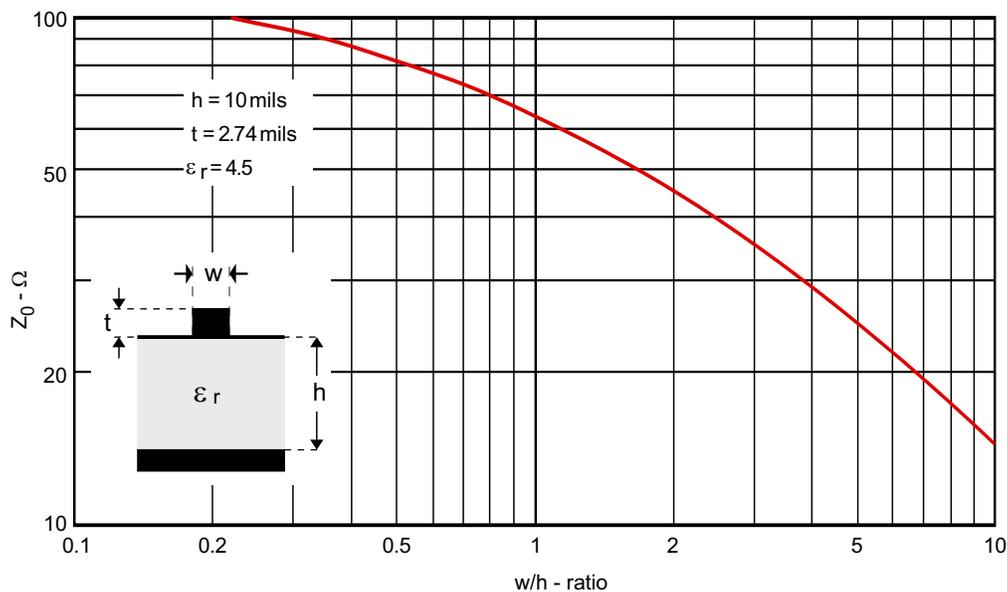
Figure 13. Characteristic Impedance as a Function of the w/h Ratio

From Figure 13 it is apparent that a 70-Ω design requires a w/h ratio of about 0.8. As described in the following section, *Reference Planes*, designing a low EMI board requires close electric coupling between signal trace and ground plane, which is accomplished by ensuring that h = 10 mils. The corresponding trace-width is therefore 8 mils. This width must be maintained across the entire trace length. Otherwise, variations in trace width cause discontinuities in the characteristic impedance, thus leading to increased reflections and EMI.

Note, that the preceding design example is only one of many possibilities to achieve the desired Z_0. Different trace thickness due to higher or lower copper plating, or different PCB material can be used, but require the w/d ratio to change. The rather complex, mathematic equations for calculating the characteristic impedance Z_0, while taking trace thickness, width, and dielectric into account, are presented in Table 2.

Table 2. Microstrip Equations for 0.2 < w/d < 1 [1]

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \times \left[\frac{1}{\sqrt{1 + \frac{12 \times h}{w}}} + 0.04 \times \left(1 - \frac{w}{h}\right)^2 - \frac{t}{2.3 \times \sqrt{w \times h}} \right]$$	ε_{eff} = effective dielectric, taking into account: • dielectric of air • dielectric of PCB material • height above ground • nominal trace width
$$w_{eff} = w + \frac{1.25 \times t}{\pi} \times \left[1 + \ln\left(\frac{2 \times h}{t}\right) \right]$$	w_{eff} = effective trace width, taking into account: • nominal trace width • trace thickness • height above ground
$$Z_0 = \frac{60 \times \ln\left(\frac{8 \times h}{w_{eff}} + \frac{w_{eff}}{4 \times h}\right)}{\sqrt{\varepsilon_{eff}}}$$	Z_0 = characteristic impedance, taking into account: • effective trace width • height above ground • effective dielectric

[1] Keep all dimensions in inch, or mils (1 in = 1000 mils), or mm (1 in = 25.4 mm).

4.5 Reference Planes

The power and ground planes of a high-speed PCB design usually must satisfy a variety of requirements.

At dc and low frequencies, they must deliver stable reference voltages, such as V_{CC} and ground, to the supply terminals of integrated circuits (IC).

At high frequencies reference planes, and in particular ground planes, serve numerous purposes. For the design of controlled impedance transmission systems, the ground plane must provide strong electric coupling with the signal traces of an adjacent signal layer.

Consider a single, ac-carrying conductor with its associated electric and magnetic fields, shown in Figure 14. Loose or no electric coupling allows the transversal electromagnetic (TEM) wave, created by the current flow, to freely radiate into the outside environment, causing severe electromagnetic interference (EMI).
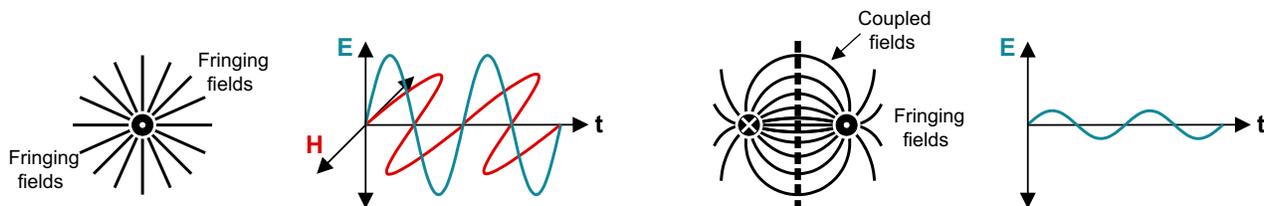

Figure 14. Reducing Field Fringing Through Close Electric Coupling Between Conductors

Now imagine a second conductor in close proximity, carrying a current of equal amplitude but opposite polarity. In this case, the conductors' opposing magnetic fields cancel, while their electric fields tightly couple. The TEM waves of the two conductors, now being robbed of their magnetic fields, cannot radiate into the environment. Only the far smaller fringing fields might be able to couple outside, thus yielding significantly lower EMI.

Figure 15 shows the same effect occurring between a ground plane and a closely coupled signal trace. High-frequency currents follow the path of least inductance, not the path of least impedance. Because the return path of least inductance lies directly under a signal trace, returning signal currents tend to follow this path. The confined flow of return current creates a region of high current density in the ground plane, right below the signal trace. This ground plane region then acts as a single return trace, allowing the magnetic fields to cancel while providing tight electric coupling to the signal trace above.

Figure 15. Ground Plane Acting as a Single Return Trace

To provide a continuous, low-impedance path for return currents, reference planes (power and ground planes) must be of solid copper sheets and free from voids and crevices. For reference planes, it is important that the clearance sections of vias do not interfere with the path of the return current. In the case of an obstacle, the return current finds its way around it. However, by doing so, the current's electromagnetic fields will most likely interfere with the fields of other signal traces introducing crosstalk. Moreover, this obstacle adversely affects the impedance of the traces passing over it, thus leading to discontinuities and increased EMI.
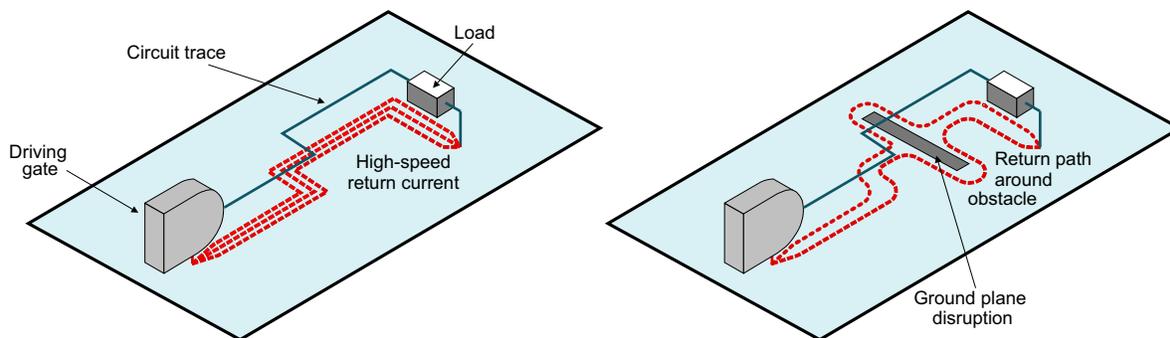
Figure 16. Return Current Paths in Solid Versus Slotted Ground Planes

4.6   Routing

Guidelines for routing PCB traces and placing components are necessary when trying to maintain signal integrity, avoiding noise pick-up, and lower EMI. Although an endless number of precautions seems to be taken, this section provides only a few main recommendations as layout guidance.

1. Keep signal traces 3 times the trace-to-ground height, (d = 3h), apart to reduce crosstalk down to 10%. Because the return current density under a signal trace diminishes via a $1/[1+(d/h)^2]$ function, its density at a point $d > 3h$, is sufficiently small to avoid causing significant crosstalk in an adjacent trace.
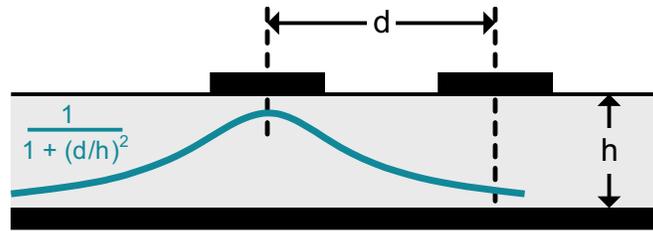
Figure 17. Separate Traces to Minimize Crosstalk

2. Use 45° bends (chamfered corners), instead of right-angle (90°) bends. Right-angle bends increase the effective trace width, and thus the trace impedance. This creates additional impedance mismatch, which may lead to higher reflections.

Figure 18. Use 45° Bends Instead of 90° Bends

3. For permanent operation in noisy environments, connect the Enable inputs of an isolator through a via to the appropriate reference plane, that is, High-Enable inputs to the V_{CC} plane and Low-Enable inputs to the ground plane.

4. When routing traces next to a via or between an array of vias, ensure that the via clearance section does not interrupt the path of the return current on the ground plane below. If a via clearance section lies in the return path, the return current finds a path of least inductance around it. By doing so, it may cross below other signal traces, thus generating cross-talk and increase EMI.
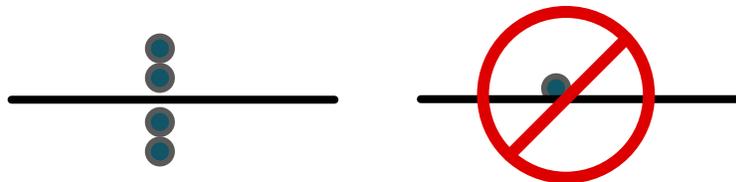
Figure 19. Avoiding Via Clearance Sections

5. Avoid changing layers with signal traces as this causes the inductance of the signal path to increase.

6. If, however, signal trace routing over different layers is unavoidable, accompany each signal trace via with a return-trace via. In this case, use the smallest via size possible to keep the increase in inductance at a minimum.

7. Use solid power and ground planes for impedance control and minimum power noise.

8. Use short trace lengths between isolator and surrounding circuits to avoid noise pick-up. Digital isolators are usually accompanied by isolated dc-to-dc converters, providing supply power across the isolation barrier. Because single-ended transmission signaling is sensitive to noise pick-up, the switching frequencies of close-by dc-to-dc converters can be easily picked up by long signal traces.

9. Place bulk capacitors, (i.e., 10 μF), close to power sources, such as voltage regulators or where the power is supplied to the PCB.

10. Place smaller 0.1-μF or 0.01-μF bypass capacitors at the device by connecting the power-side of the capacitor directly to the supply terminal of the device and through two vias to the V_{cc} plane, and the ground-side of the capacitor through two vias to the ground plane.

Ground plane vias

V_{CC}

V_{CC} plane vias
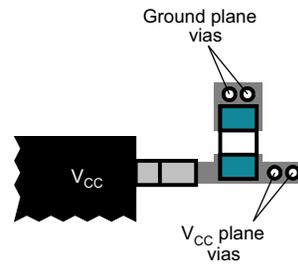
Figure 20. Connect Bypass Capacitor Directly to V_{CC} Terminal

4.7 *Vias*

The term via commonly refers to a plated hole in a printed-circuit board. Although some applications require through-hole vias to be wide enough to accommodate the leads of through-hole components, high-speed board designs mainly use them as trace routing vias when changing signal layers, or as connecting vias to connect SMT components to the required reference plane, and also to connect reference planes of the same potential to each other.

Layers connecting to a via do so by making direct contact with a pad surrounding the via, (the via pad). Layers that must not connect are separated by a clearance ring. Every via has a capacitance to ground which can be approximated using the following equation:

$$C = \frac{1.41 \times \varepsilon_r \times T \times D_1}{D_2 - D_1}$$

where

- D_2 = diameter of clearance hole in ground planes, [in.].
- D_1 = diameter of pad surround via, [in.].
- T = thickness of printed circuit board, [in.].
- ε_r = dielectric constant of the circuit board.
- C = parasitic via capacitance, [pF]. 　　　　　　　　　　　　　　　　　　　　(1)

Because the capacitance increases proportional with size, trace vias in high-speed designs must be as small as possible to avoid signal degradation caused by heavy capacitive loading.

When connecting decoupling capacitors to a ground plane or interconnecting ground planes, the via inductance becomes more important than its capacitance. The magnitude of this inductance is approximately:

$$L = 5.08 \times h \times \left[\ln\left(\frac{4 \times h}{d} \right) + 1 \right]$$

where

- L = via inductance, [nH].
- h = via length, [in.].
- d = via diameter, [in.]. 　　　　　　　　　　　　　　　　　　　　　　　　　(2)

Because this equation involves a logarithm, changing the via diameter does little to influence the inductance. A big change may be effected by changing the via length or by using multiple vias in parallel. Therefore, connect decoupling capacitors to ground by using two paralleled vias per device terminal. For low inductance connections between ground planes, use multiple vias in regular intervals across the board.

Although it is highly recommended not to change layers of high-speed traces, if the necessity still occurs, ensure a continuous return current path. Figure 21 on the left shows the flow of the return current for a single layer change and on the right for a multiple layer change.
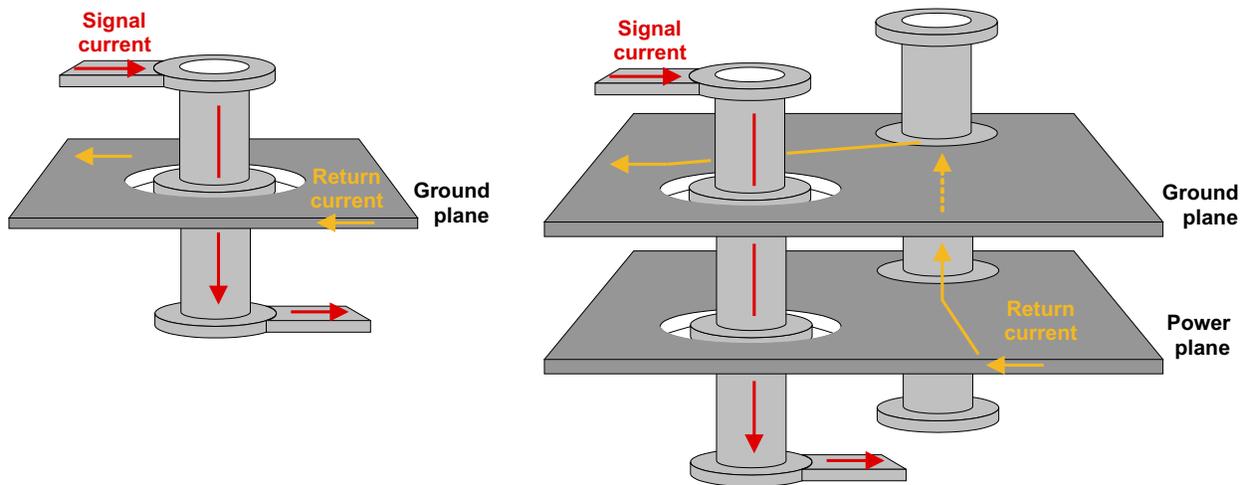
Figure 21. Return Current Paths for a Single and a Multiple Layer Change

The ability for the current flow to change from the bottom to the top of the ground plane is provided by a metallic laminate of the inner clearance ring. Thus, when a signal passes through a via and continues on the opposite side of the same plane, a return current discontinuity does not exist.

Changing a signal trace from one layer to another by crossing multiple reference planes complicates the design of the return current path. In the case of two ground planes, a ground-to-ground via must be placed near the signal via to ensure a continuous return current path, (right diagram in Figure 21).

If the reference planes are of different voltage potentials, such as the power and ground planes in Figure 22, the design of the return path becomes messy as it requires a third via and a decoupling capacitor. The return current flow begins at the bottom of the power plane, where it is closest to the signal current. It then flows through the power via, across the decoupling capacitor into the ground via and returns on top of the ground plane.
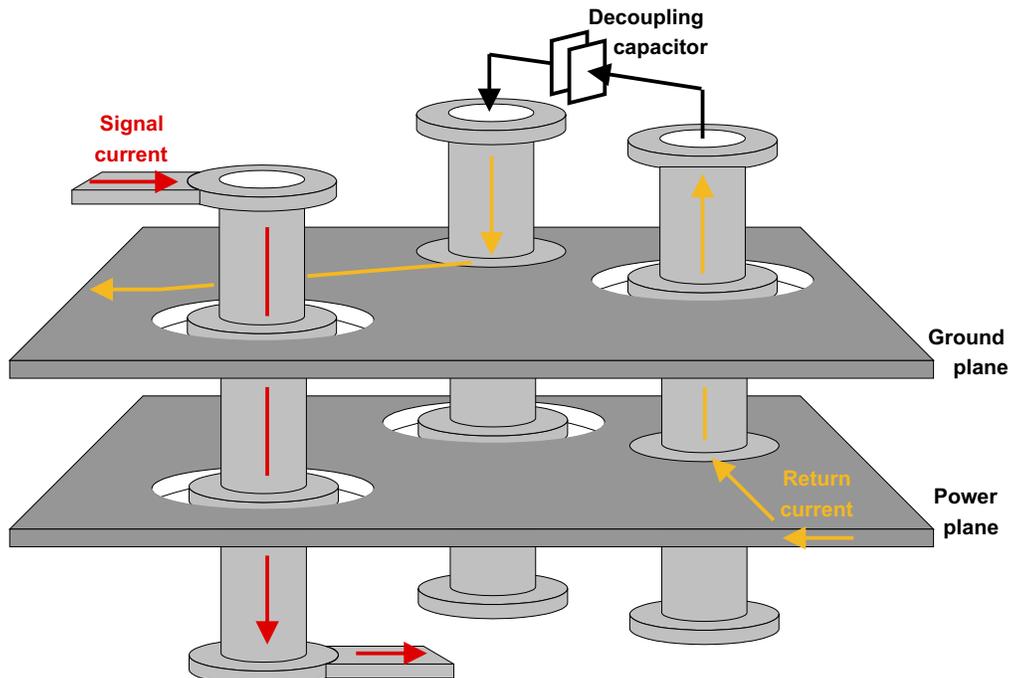
Figure 22. Return Current Paths for a Single and a Multiple Layer Change

Current return paths comprising multiple vias and decoupling capacitors possess high inductance, thus compromising signal integrity and increasing EMI. If possible, avoid changing layers during high-speed trace routing, as it usually worsens board performance, complicates design, and increases manufacturing cost.

4.8   *Decoupling Capacitors*

Decoupling capacitors provide a local source of charge for ICs requiring a significant amount of supply current in response to internal switching. Insufficient decoupling causes a lack of supply current required which may prevent the IC from working properly, resulting in signal integrity data errors to occur. This requires them to provide low impedance across the frequency range of interest. To accomplish that, a common approach is to distribute an array of decoupling capacitors evenly across the board. In addition to maintaining signal integrity, decoupling capacitors serve as EMC filters preventing high-frequency RF signals from propagating throughout the PCB.

When connecting a capacitor between the power and ground planes, the power supply is actually loaded with a series resonant circuit, whose frequency dependent R-L-C components represent the equivalent circuit of a real capacitor. Figure 23 shows the parasitic components of an initial equivalent circuit and their conversion into a series resonant circuit.
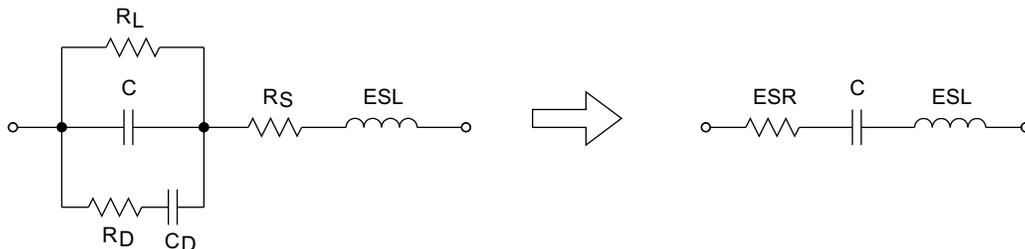
Figure 23. Capacitor Losses Modeled by a Series Resonance Circuit

The leakage resistance R_L represents the loss through leakage current at low frequencies. R_D and C_D indicate the losses due to molecular polarization, (R_D), and dielectric absorption, (C_D). R_S depicts the resistance in the leads and the plates of the capacitor. The three resistive losses are combined into one equivalent series resistance (ESR). As in the ESR case, the equivalent series inductance (ESL) combines the inductance of the capacitor plates and the internal leads.

Note that the capacitor connecting vias, although low in impedance, contribute a significant amount to the series inductance. Therefore, reduce via inductance by using two vias per capacitor terminal.

Figure 24 shows the progression of capacitor impedance (Z) versus frequency for a 10-nF capacitor. At frequencies far below the self-resonance frequency (SRF), the capacitive reactance is dominant. Closer to SRF, the inductive reactance gains influence trying to neutralize the capacitive component. At SRF, the capacitive and inductive reactance cancel, and only the ESR is effective. Note that the ESR is frequency dependent, and contrary to popular belief, does not reach its minimum at SRF. The impedance Z, however, does.
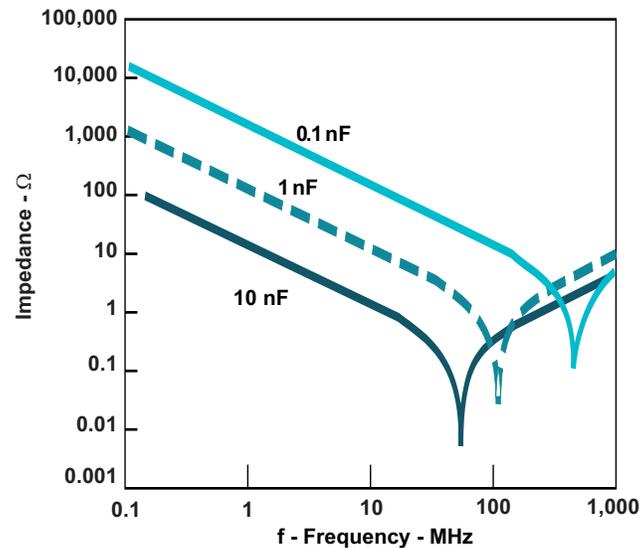
Figure 24. Capacitor Impedance Versus Frequency

The reason why the paralleling of capacitors in a distributed decoupling network works is because the total capacitance increases to $C_{TOT} = C \times n$, where n is the number of decoupling capacitors used. And with $X_c = 1/(\omega \times C)$, the capacitor impedance is reduced to $X_c = 1/(n \times \omega \times C)$ for frequencies below SRF. Similarly, this holds true for the inductance. Here $L_{TOT} = L/n$, and because $X_L = \omega \times L$, the impedance decreases to $X_L = \omega \times L/n$ for frequencies above SRF.

Designing a solid decoupling network must include lower frequencies down to dc, which requires the implementation of large bypass capacitors. Therefore, to provide sufficient low impedance at low frequencies, place 1-μF to 10-μF tantalum capacitors at the output of voltage regulators and at the point where power is supplied to the PCB. For the higher frequency range, place several 0.1-μF or 0.01-μF ceramic capacitors next to every high-speed switching IC.

5 Summary

This design guide helps system designers of galvanically isolated systems to begin designing with TI's broad portfolio of digital isolators and isolated functions in the shortest time possible. This document explains the basic operating principle of an isolator, suggests where to place it within a system design, and recommends guidelines for an EMC-compatible circuit-board design. Despite the enormous amount of technical literature, seminars, newsletters, and internet forums on PCB design, this document provides designers with layout guidelines in a comprehensive way. By following the recommendations presented herein, designers can accomplish EMC-compliant board design in the shortest time possible.

6 References

1. High-speed Digital Design, Johnson/Graham, 1993
2. Noise Reduction Techniques in Electronic Systems, Ott, 1988
3. Eliminating the myths about printed circuit board power/ground plane decoupling, Archambeault, 2001.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.