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FPF1015/6/7/8 IntelliMAX™ 1V Rated Advanced Load Management Products

Features

- 0.8 to 1.8V Input Voltage Range
- Typical $R_{DS(ON)} = 34m\Omega$ @ $V_{ON} - V_{IN} = 2.0V$
- Output Discharge Function
- Internal Pull down at ON Pin
- Accurate Slew Rate Controlled Turn-on time
- Low < 1 μ A Quiescent Current
- ESD Protected, above 8000V HBM, 2000V CDM
- RoHS Compliant
- Free from Halogenated Compounds and Antimony Oxides

Applications

- PDAs
- Cell Phones
- GPS Devices
- MP3 Players
- Digital Cameras
- Notebook Computers

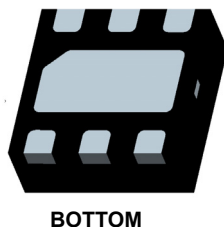


General Description

The FPF1015/6/7/8 series is an IntelliMAX advanced slew rate loadswitch offering a very low operating voltage. These devices consist of a 34m Ω N-channel MOSFET that supports an input voltage up to 2.0V. These slew rate devices control the switch turn-on and prevent excessive in-rush current from the supply rails. The input voltage range operates from 0.8V to 1.8V to fulfill today's lowest Ultraportable Device's supply requirements. Switch control is via a logic input (ON) capable of interfacing directly with low voltage control signals.

The FPF1016 and FPF1018 have an On-Chip pull down allowing for quick and controlled output discharge when switch is turned off. The FPF1015/6/7/8 series is available in a space-saving 2X2 MLP-6L package.

PIN 1

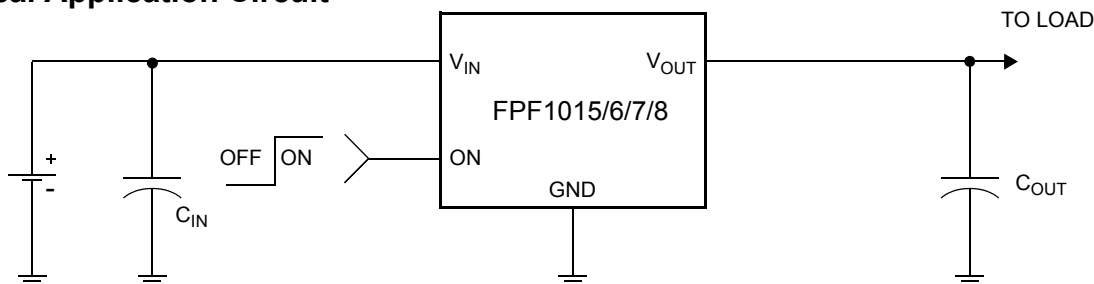


BOTTOM



TOP

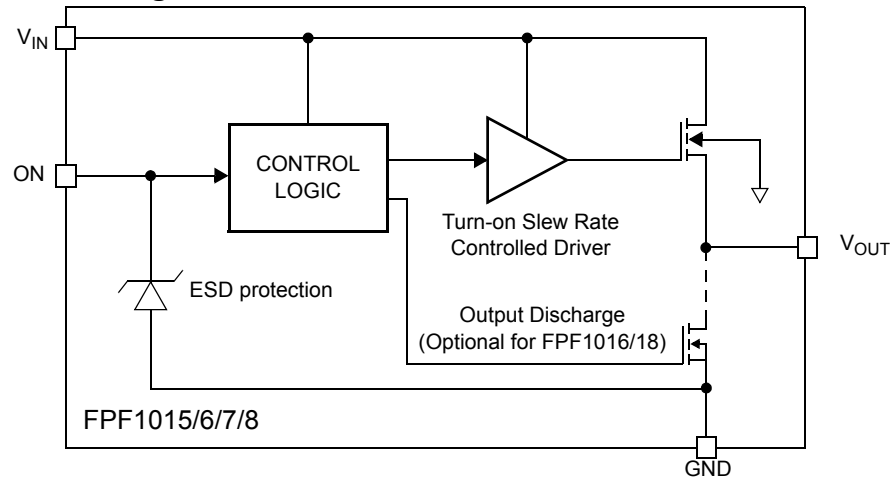
Typical Application Circuit



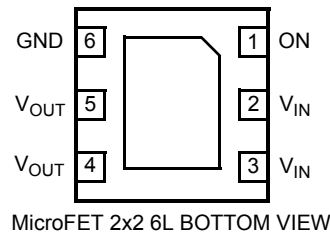
Ordering Information

Part	Switch	Turn-on Time	Output Discharge	ON Pin Activity	Package
FPF1015	34m Ω , NMOS	43us	NA	Active HI	MLP 2x2
FPF1016	34m Ω , NMOS	43us	60 Ω	Active HI	MLP 2x2
FPF1017	34m Ω , NMOS	165us	NA	Active HI	MLP 2x2
FPF1018	34m Ω , NMOS	165us	60 Ω	Active HI	MLP 2x2

Functional Block Diagram



Pin Configuration



Pin Description

Pin	Name	Function
1	ON	ON/OFF Control Input, 2nd Supply
2, 3	V _{IN}	Supply Input: Input to the power switch
4, 5	V _{OUT}	Switch Output.
6	GND	Ground

Absolute Maximum Ratings

Parameter	Min	Max	Unit
V _{IN} , V _{OUT} to GND	-0.3	2	V
V _{ON} to GND	-0.3	4.2	V
Maximum Continuous Switch Current		1.5	A
Power Dissipation @ T _A = 25°C (Note 1)		1.2	W
Operating Temperature Range	-40	85	°C
Storage Temperature	-65	150	°C
Thermal Resistance, Junction to Ambient		86	°C/W
Electrostatic Discharge Protection	HBM	8000	V
	CDM	2000	V

Recommended Operating Range

Parameter	Min	Max	Unit
V _{IN}	0.8	1.8	V
Ambient Operating Temperature, T _A	-40	85	°C

Note 1: Package power dissipation on 1square inch pad, 2 oz. copper board

Electrical Characteristics

$V_{IN} = 0.8$ to $1.8V$, $T_A = -40$ to $+85^\circ C$ unless otherwise noted. Typical values are at $V_{IN} = 1.8V$ and $T_A = 25^\circ C$.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Basic Operation						
Operating Voltage	V_{IN}		0.8		1.8	V
ON input Voltage	$V_{ON(MIN)}$	$V_{IN} = 0.8V$	1.8	2.8	4.0	V
	$V_{ON(MAX)}$	$V_{IN} = 1.8V$ (Note2)	2.8	3.8	4.0	V
Operating Current	I_{CC}	$V_{IN} = 1V$, $V_{ON} = 3.3V$, $V_{OUT} = \text{Open}$			1	μA
Quiescent Current	I_Q	$V_{IN} = 1V$, $V_{ON} = V_{OUT} = \text{Open}$			2	μA
Off Switch Current	I_{SWOFF}	$V_{IN} = 1.8V$, $V_{ON} = GND$, $V_{OUT} = GND$			2	μA
On-Resistance	R_{ON}	$V_{IN} = 1V$, $V_{ON} = 3V$, $I_{LOAD} = 1A$, $T_A = 25^\circ C$		34	45	m Ω
		$V_{IN} = 1V$, $V_{ON} = 2.3V$, $I_{LOAD} = 1A$, $T_A = 25^\circ C$		41	55	
Output Pull Down Resistance	R_{PD}	$V_{IN} = 1V$, $V_{ON} = 0V$, $T_A = 25^\circ C$, $I_{LOAD} = 1mA$, FPF1016, FPF1018		60	120	Ω
ON Input Logic Low Voltage	V_{IL}	$V_{IN} = 0.8V$, $R_{LOAD} = 1K\Omega$			0.3	V
		$V_{IN} = 1.8V$, $R_{LOAD} = 1K\Omega$			0.8	
ON Input Leakage		$V_{ON} = V_{IN}$ or GND	-1		1	μA
Dynamic ($V_{IN} = 1.0V$, $V_{ON} = 3.0V$, $T_A = 25^\circ C$)						
V_{OUT} Rise Time	T_R	FPF1015, FPF1016, $R_L = 500\Omega$, $C_L = 0.1\mu F$		28		μs
		FPF1017, FPF1018, $R_L = 500\Omega$, $C_L = 0.1\mu F$		114		
		FPF1015, FPF1016, $R_L = 3.3\Omega$, $C_L = 10\mu F$		38		
		FPF1017, FPF1018, $R_L = 3.3\Omega$, $C_L = 10\mu F$		155		
Turn ON	T_{ON}	FPF1015, FPF1016, $R_L = 500\Omega$, $C_L = 0.1\mu F$		43		μs
		FPF1017, FPF1018, $R_L = 500\Omega$, $C_L = 0.1\mu F$		165		
		FPF1015, FPF1016, $R_L = 3.3\Omega$, $C_L = 10\mu F$		58		
		FPF1017, FPF1018, $R_L = 3.3\Omega$, $C_L = 10\mu F$		228		
V_{OUT} Fall Time	T_F	FPF1015, FPF1017, $R_L = 500\Omega$, $C_L = 0.1\mu F$		105		μs
		FPF1016, FPF1018, $R_{PD} = 60\Omega$, $R_L = 500\Omega$, $C_L = 0.1\mu F$		15		
		FPF1015, FPF1017, $R_L = 3.3\Omega$, $C_L = 10\mu F$		80		
		FPF1016, FPF1018, $R_{PD} = 60\Omega$, $R_L = 3.3\Omega$, $C_L = 10\mu F$		74		
Turn Off	T_{OFF}	FPF1015, FPF1017, $R_L = 500\Omega$, $C_L = 0.1\mu F$		150		μs
		FPF1016, FPF1018, $R_{PD} = 60\Omega$, $R_L = 500\Omega$, $C_L = 0.1\mu F$		53		
		FPF1015, FPF1017, $R_L = 3.3\Omega$, $C_L = 10\mu F$		102		
		FPF1016, FPF1018, $R_{PD} = 60\Omega$, $R_L = 3.3\Omega$, $C_L = 10\mu F$		96		

Note 2: $V_{ON(MAX)}$ is limited by the absolute rating.

Typical Characteristics

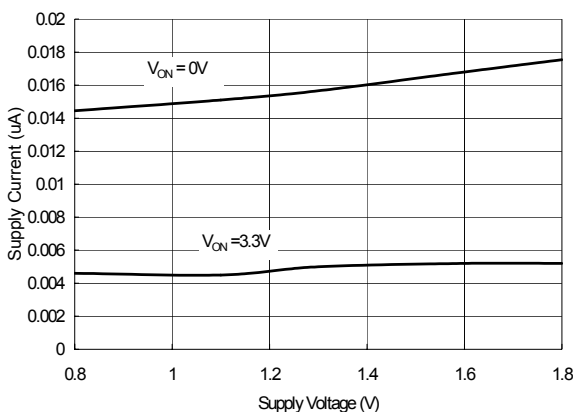


Figure 1. Supply Current vs. V_{IN}

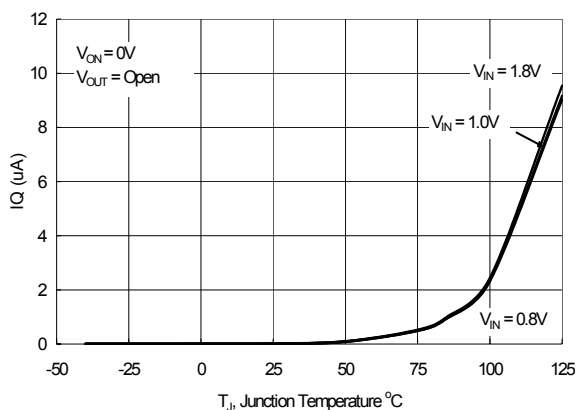


Figure 2. Quiescent Current vs. Temperature

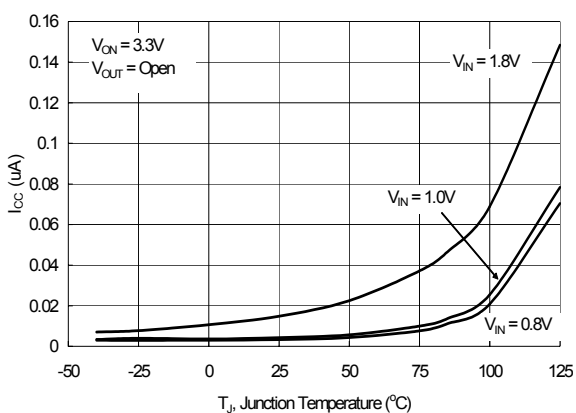


Figure 3. Operating Current vs. Temperature

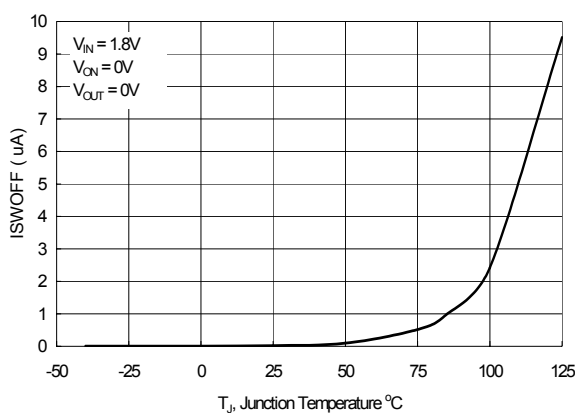


Figure 4. Off Switch Current vs. Temperature

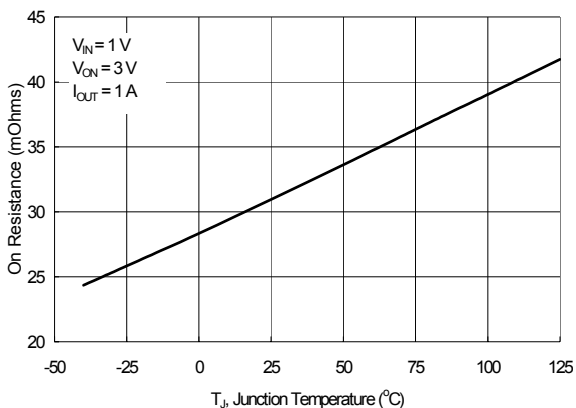


Figure 5. R_{ON} vs. Temperature

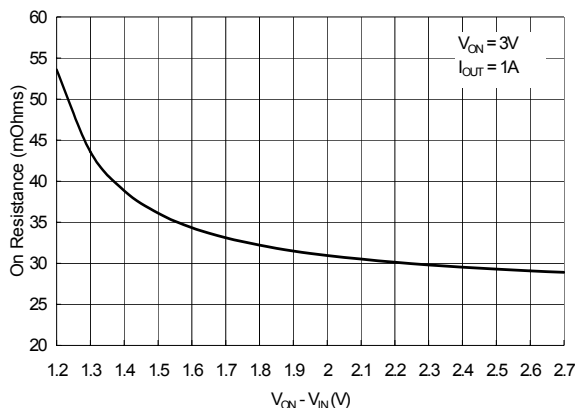


Figure 6. R_{ON} vs. $V_{ON} - V_{IN}$

Typical Characteristics

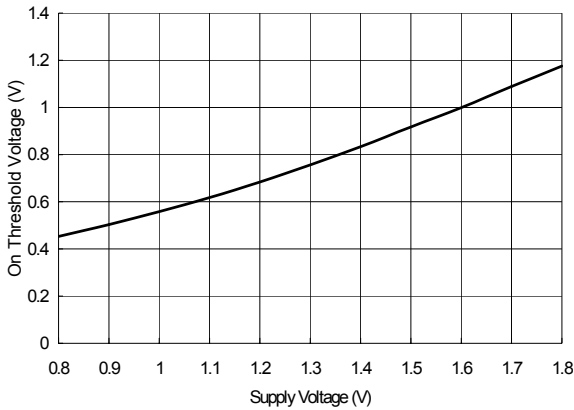


Figure 7. V_{IL} vs. V_{IN}

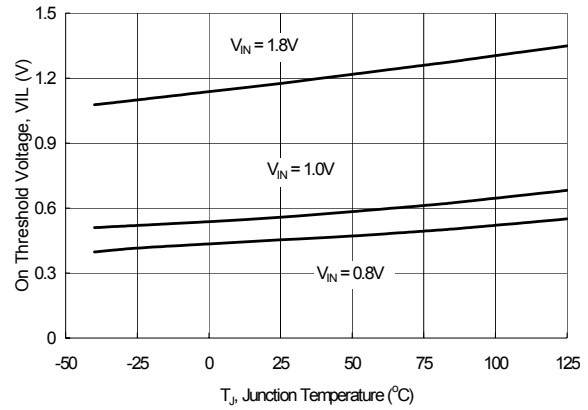


Figure 8. V_{IL} vs. Temperature

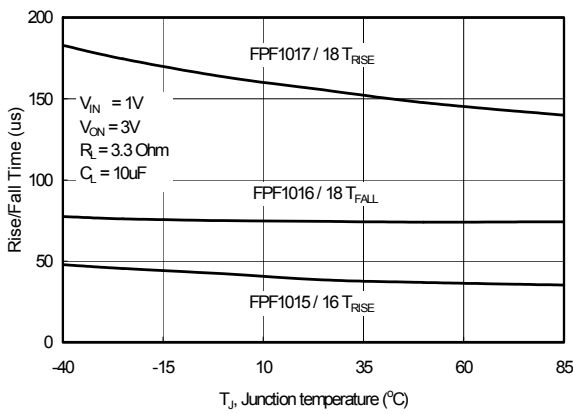


Figure 9. T_{RISE}/T_{FALL} vs. Temperature

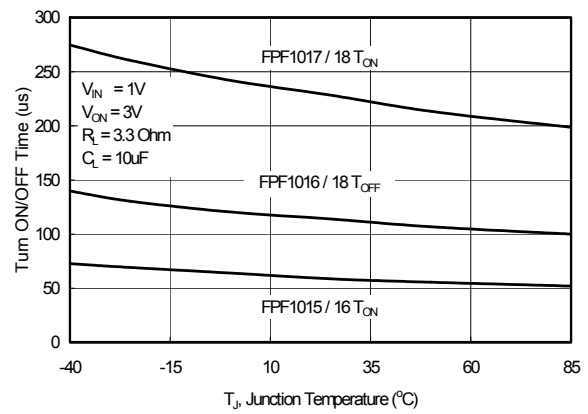


Figure 10. T_{ON}/T_{OFF} vs. Temperature

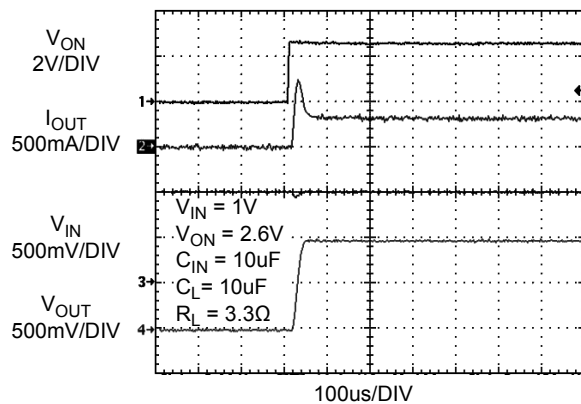


Figure 11. FPF1015 / 16 Turn ON response

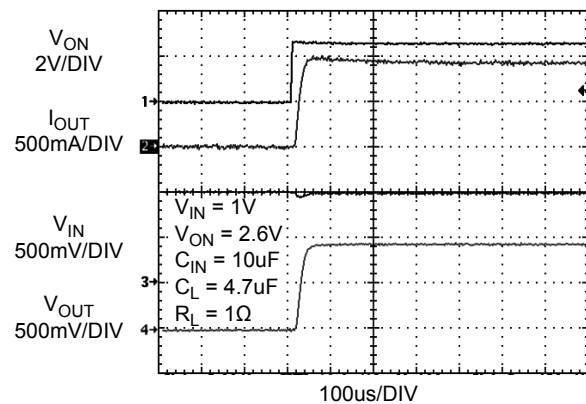


Figure 12. FPF1015 / 16 Turn ON response

Typical Characteristics

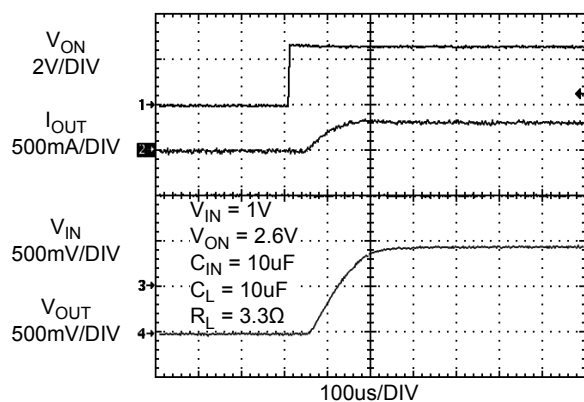


Figure 13. FPF1017 / 18 Turn On response

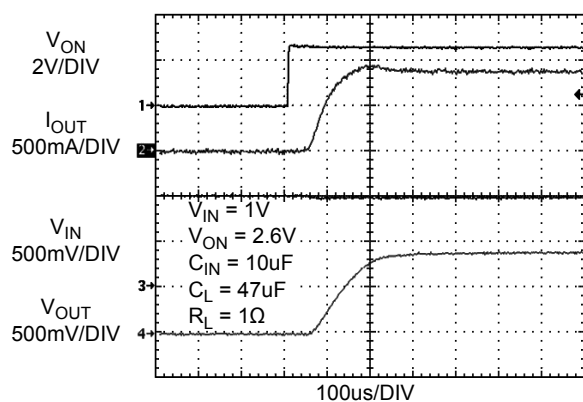


Figure 14. FPF1017 / 18 Turn On response

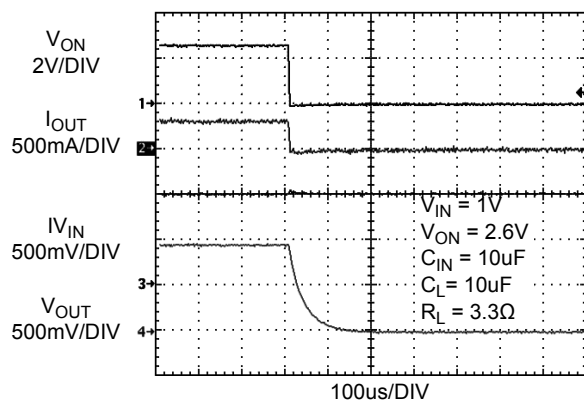


Figure 15. FPF1015 / 17 Turn OFF response

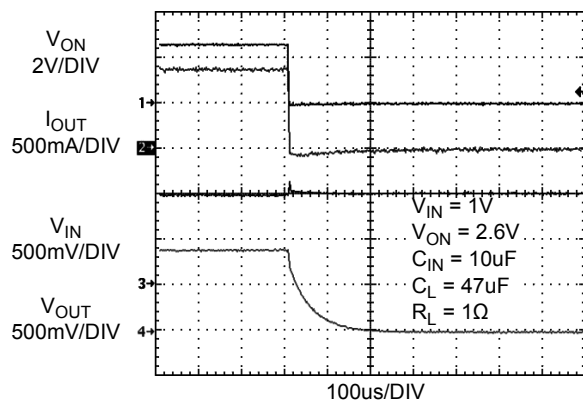


Figure 16. FPF105 / 17 Turn OFF response

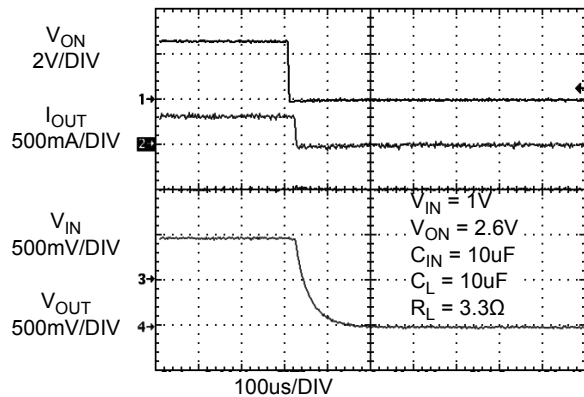


Figure 17. FPF1016 / 18 Turn OFF response

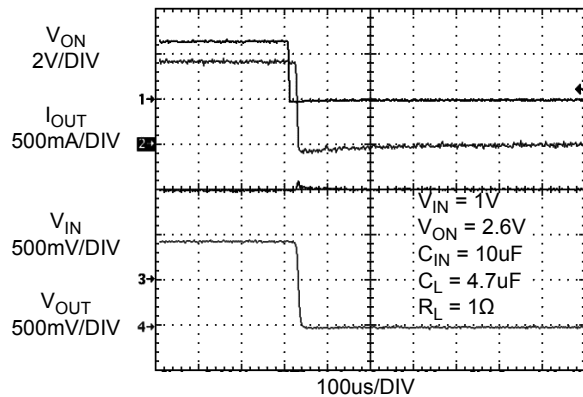


Figure 18. FPF1016 / 18 Turn OFF response

Typical Characteristics

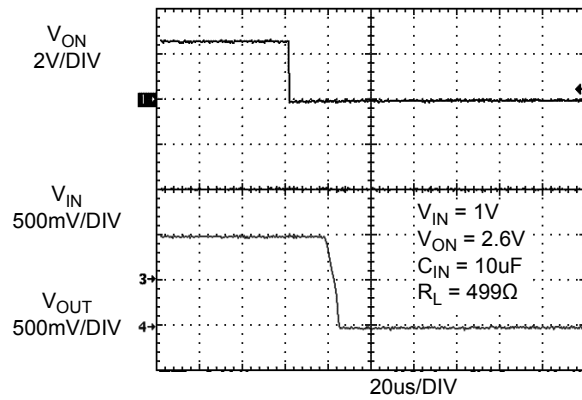


Figure 19. FPF1016 / 18 Output Pull Down response

Description of Operation

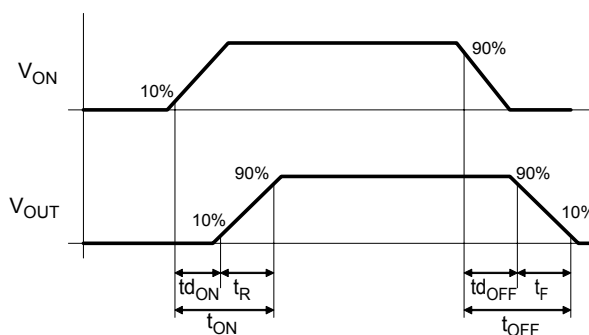
The FPF1015/6/7/8 are low $R_{DS(ON)}$ N-Channel load switches with controlled turn-on. The core of each device is a 34mΩ ($V_{IN} = 1V$, $V_{ON} = 3V$) N-Channel MOSFET and is customized for a low input operating range of 0.8 to 1.8V. The ON pin controls the state of the switch.

The FPF1016 and FPF1018 contain a 60Ω(typ) on-chip resistor which is connected internally from V_{OUT} to GND for quick output discharge when the switch is turned off.

On/Off Control

The ON pin is active high and it controls the state of the switch. Applying a continuous high signal will hold the switch in the ON state. In order to minimize the switch on resistance, the ON pin voltage should exceed the input voltage by 2V. This device is compatible with a GPIO (General Purpose Input/Output) port, where the logic voltage level can be configured to $4V \geq V_{ON} \geq V_{IN} + 2V$ and power consumed is less than 1μA in steady state.

Timing Diagram

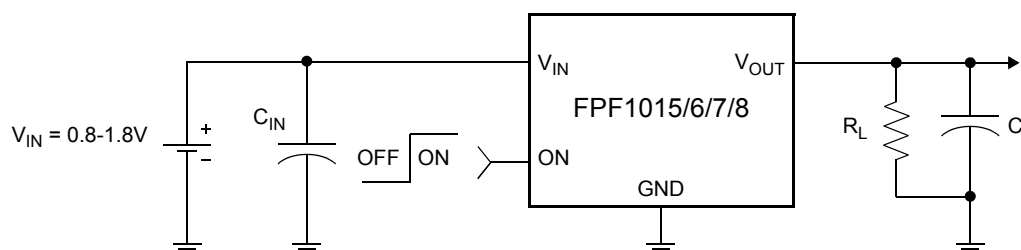


where:

- t_{dON} = Delay On Time
- t_R = V_{OUT} Rise Time
- t_{ON} = Turn On Time
- t_{dOFF} = Delay Off Time
- t_F = V_{OUT} Fall Time
- t_{OFF} = Turn Off Time

Application Information

Typical Application



Input Capacitor

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns-on, a capacitor must be placed between V_{IN} and GND. For minimized voltage drop, especially when the operating voltage approaches 1V and a fast slew rate part (FPF1015 and FPF1016) is selected, a 10μF ceramic capacitor should be placed close to the V_{IN} pins. Higher values of C_{IN} can be used to further reduce the voltage drop during higher current modes of operation.

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces or large copper planes for all pins (V_{IN} , V_{OUT} , ON and GND) will help minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

Output Capacitor

A 0.1μF capacitor, C_L , should be placed between V_{OUT} and GND. This capacitor will prevent parasitic board inductance from forcing V_{OUT} below GND when the switch turns-off. If the application has a capacitive load, the FPF1016 and FPF1018 can be used to discharge that load through an on-chip output discharge path.

Improving Thermal Performance

An improper layout could result in higher junction temperature. This concern applies when the current is at its continuous maximum value and is then switched into a large capacitive load that introduces a large transient current. Since the FPF1015/6/7/8 does not have thermal shutdown capability, a proper layout is essential to improving power dissipation of the switch in transient events and prevents the switch from exceeding the maximum absolute power dissipation of 1.2W.

The following techniques have been identified to improve the thermal performance of this family of devices. These techniques are listed in order of the significance of their impact.

1. Thermal performance of the load switch can be improved by connecting pin7 of the DAP (Die Attach Pad) to the GND plane of the PCB.
2. Embedding two exposed through-hole vias into the DAP (pin7) provides a path for heat to transfer to the back GND plane of the PCB. A drill size of Round, 14 mils (0.35mm) with 1-ounce copper plating is recommended to result in appropriate solder reflow. A smaller size hole prevents the solder from penetrating into the via, resulting in device lift-up. Similarly, a larger via-hole consumes excessive solder, and may result in voiding of the DAP.

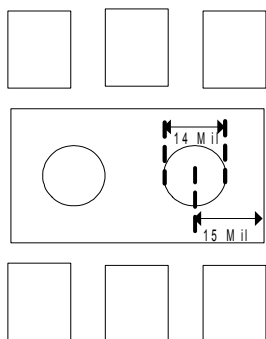


Figure 19: Two through hole open vias embedded in DAP

3. The V_{IN} , V_{OUT} and GND pins will dissipate most of the heat generated during a high load current condition. The layout suggested in Figure 20 provides each pin with adequate copper so that heat may be transferred as efficiently as possible out of the device. The ON pin trace may be laid-out diagonally from the device to maximize the area available to the ground pad. Placing the input and output capacitors as close to the device as possible also contributes to heat dissipation, particularly during high load currents.

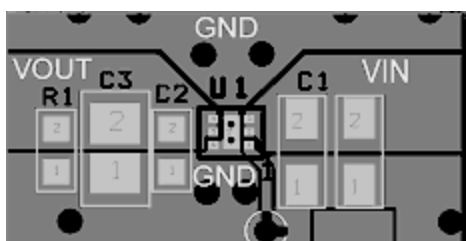


Figure 20: Proper layout of output, input and ground copper area

Demo Board Layout

FPF1015/6/7/8 Demo board has the components and circuitry to demonstrate FPF1015/6/7/8 load switches functions. Thermal performance of the board is improved using a few techniques recommended in the layout recommendations section of datasheet.

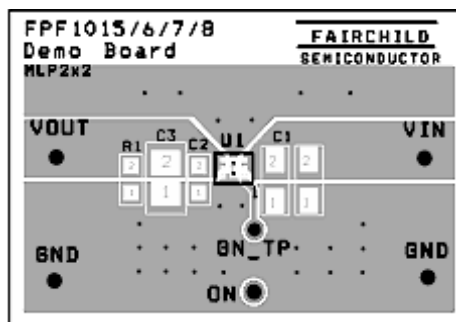
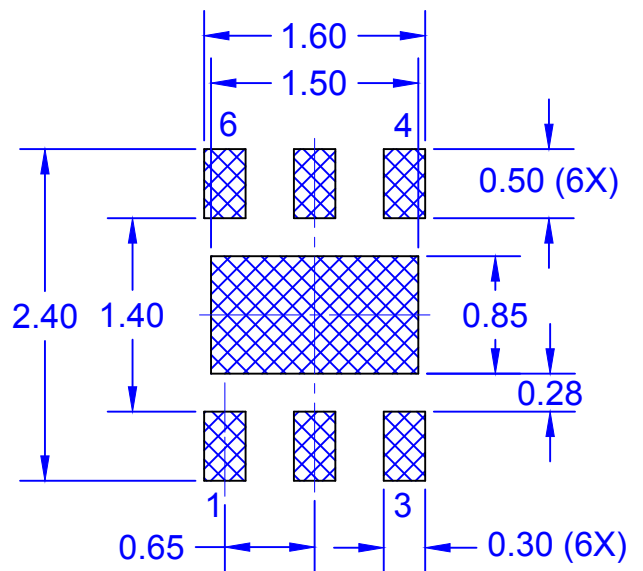
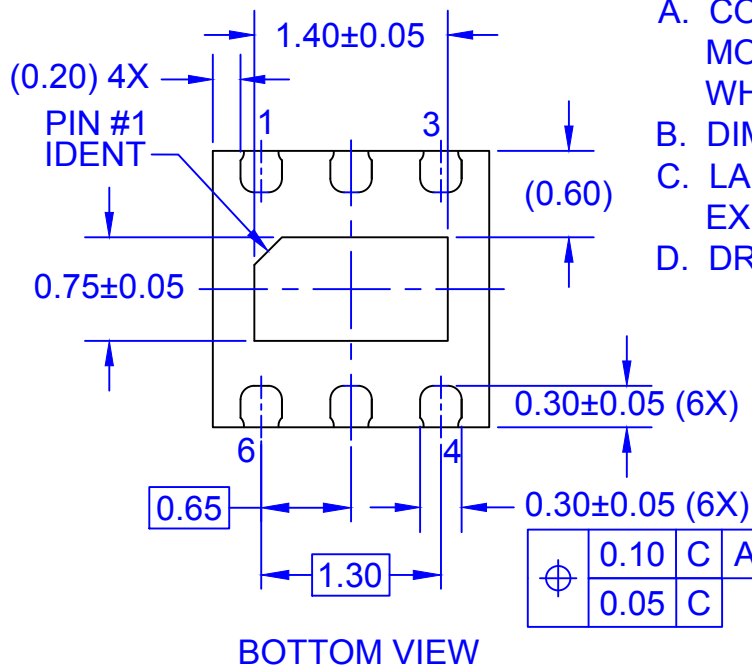
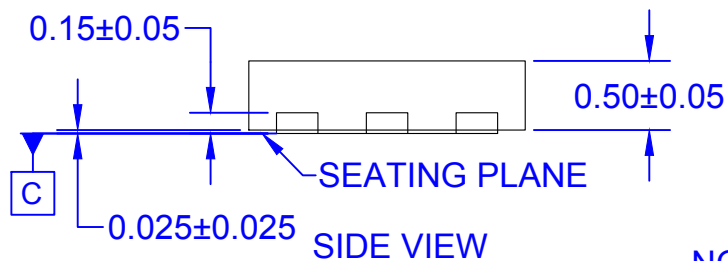
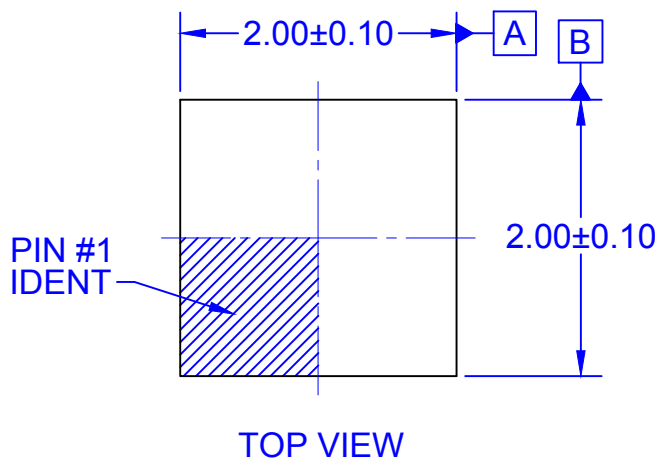


Figure 21. FPF1015/6/7/8 Demo board TOP, SST, ASTOP and DRL layers



RECOMMENDED LAND PATTERN

NOTES:

- CONFORM TO JEDEC REGISTRATIONS MO-229,VARIATION VCCC, EXCEPT WHERE NOTED.
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