50-MHz Low-Distortion High-CMRR Rail-to-Rail I/O, Single-Supply Operational Amplifier

Check for Samples: OPA365-EP

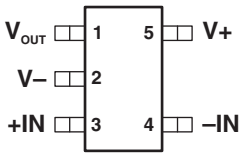
FEATURES

- **Gain Bandwidth: 50 MHz**
- **Zero-Crossover Distortion Topology**
  - **Excellent THD+N: 0.0004%**
  - **CMRR: 96.5 dB (Min)**
  - **Rail-to-Rail Input and Output**
  - **Input 100 mV Beyond Supply Rail**
- **Low Noise: 4.5 nV/√Hz at 100 kHz**
- **Slew Rate: 25 V/µs**
- **Fast Settling: 0.3 µs to 0.01%**
- **Precision**
  - **Low Offset: 100 µV (Typical at 25°C)**
  - **Low Input Bias Current: 0.2 pA (Typical at 25°C)**
- **2.2-V to 5.5-V Operation**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C), Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

DBV PACKAGE
(TOP VIEW)



(1) Additional temperature ranges available - contact factory

DESCRIPTION

The OPA365 zero-crossover series, rail-to-rail, high-performance, CMOS operational amplifier is optimized for very low voltage, single-supply applications. Rail-to-rail input/output, low-noise (4.5 nV/√Hz) and high-speed operation (50-MHz gain bandwidth) make this device ideal for driving sampling analog-to-digital converters (ADCs). The OPA365 supports audio, signal conditioning, sensor amplification, defense, aerospace and medical applications. The OPA365 is also well-suited for cell phone power amplifier control loops.

Special features include an excellent common-mode rejection ratio (CMRR), no input stage crossover distortion, high input impedance, and rail-to-rail input and output swing. The input common-mode range includes both the negative and positive supplies. The output voltage swing is within 10mV of the rails.

The OPA365 is available in the SOT23-5 package and is specified for operation from −55°C to 125°C.

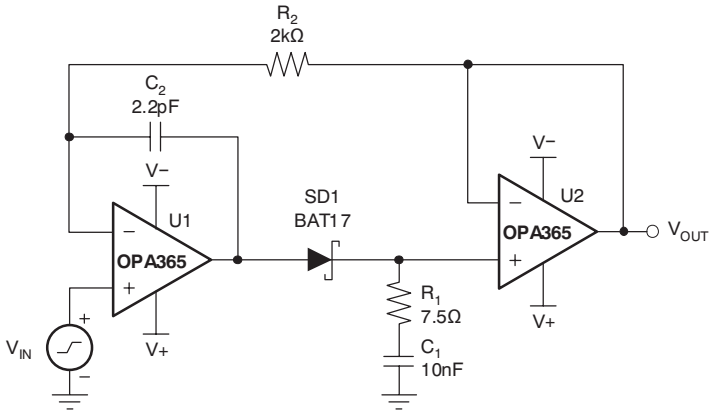


Figure 1. Fast Settling Peak Detector

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2011, Texas Instruments Incorporated

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOT23 – DBV	OPA365AMDBVTEP	OUNM

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

V_{CC}	Supply voltage		5.5 V
V_I	Signal input terminals, voltage(2)		(V−) − 0.5V to (V+) + 0.5 V
I_I	Signal input terminals, current(2)		±10 mA
t_{OSC}	Output short-circuit duration(3)(4)		Continuous
T_{OP}	Operating temperature		−55°C to 125°C
T_{stg}	Storage temperature		−65°C to 150°C
T_J	Junction temperature		150°C
ESD	Electrostatic discharge rating	Human Body Model	4000V
		Charged Device Model	1000V
		Machine Model	200V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package
(4) Continuous output current greater than 20 mA for extended periods may affect product reliability.

Copyright © 2011, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS

V_S = 2.2 V to 5.5 V, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage		25°C		100	200	µV
			Full range			450	
dV_{OS}/dT	Input offset voltage drift		Full range		3		µV/°C
PSRR	Input offset voltage vs power supply	V_S = +2.2V to +5.5V	Full range		10	100	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current		25°C		±0.2	±10	pA
			Full range	See Typical Characteristics			
I_{OS}	Input offset current		25°C		±0.2	±10	pA
NOISE							
e_n	Input voltage noise	f = 0.1Hz to 10Hz	25°C		5		$µV_{PP}$
e_n	Input voltage noise density	f = 100kHz	25°C		4.5		nV/√Hz
i_n	Input current noise density	f = 10kHz	25°C		4		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range		Full range	(V-) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V-) – 0.1V ≤ V_{CM} ≤ (V+) + 0.1V	Full range	96.5	120		dB
INPUT CAPACITANCE							
	Differential		25°C		6		pF
	Common-mode		25°C		2		pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	R_L = 10kΩ, 100mV < V_O < (V+) – 100mV	Full range	96.5	120		dB
		R_L = 600Ω, 200mV < V_O < (V+) – 200mV	25°C	100	120		
		R_L = 600Ω, 200mV < V_O < (V+) – 200mV	Full range	91			
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product		25°C		50		MHz
SR	Slew rate	V_S = 5V, G = +1	25°C		25		V/µs
t_S	Settling time	0.1%, V_S = 5V, 4V Step, G = +1	25°C		200		ns
		0.01%, V_S = 5V, 4V Step, G = +1	25°C		300		
	Overload recovery time	V_S = 5V, V_{IN} x Gain > V_S	25°C		< 0.1		µs
THD+N	Total harmonic distortion + noise (2)	V_S = 5V, R_L = 600Ω, V_O = 4VPP, G = +1, f = 1kHz	25°C		0.0004		%
OUTPUT							
	Voltage output swing from rail	R_L = 10kΩ, V_S = 5.5V	Full range		10	20	mV
I_{SC}	Short-circuit current (3)		25°C		±65		mA
C_L	Capacitive load drive		25°C	See Typical Characteristics			
	Open-loop output impedance	f = 1MHz, I_O = 0	25°C		30		Ω
POWER SUPPLY							
V_S	Specified voltage range		Full range	2.2		5.5	V
I_Q	Quiescent current per amplifier	I_O = 0	25°C		4.6	5	mA
			Full range			5.5	

(1) Full range T_A = −55°C to +125°C
(2) Third-order filter, bandwidth 80kHz at −3dB.
(3) Continuous output current greater than 20 mA for extended periods may affect product reliability.

Copyright © 2011, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

V_S = 2.2 V to 5.5 V, R_L = 10 kΩ connected to $V_S/2$, V_{CM} = $V_S/2$, and V_{OUT} = $V_S/2$ (unless otherwise noted)

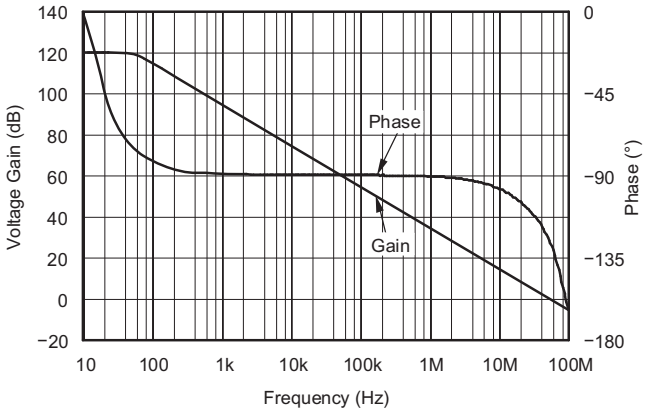
PARAMETER		TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
TEMPERATURE RANGE							
	Specified range			–55		125	°C
θ_{JA}	Thermal resistance				200		°C/W

Copyright © 2011, Texas Instruments Incorporated

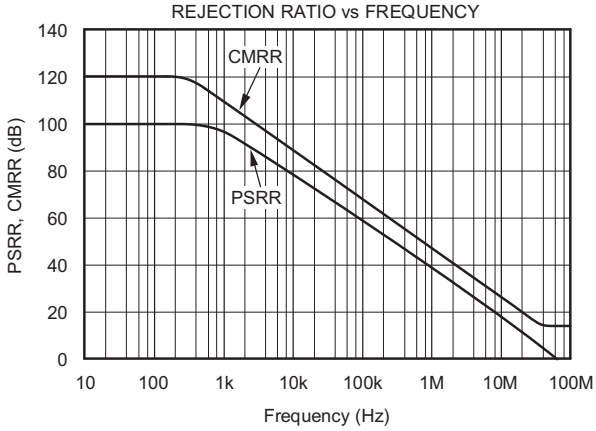
TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5 V, C_L = 0 pF (unless otherwise noted)

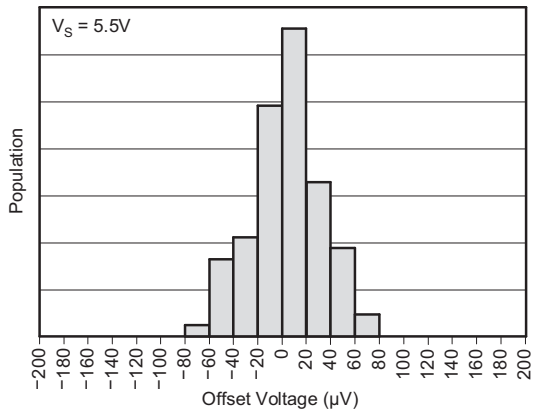
OPEN−LOOP GAIN/PHASE vs FREQUENCY



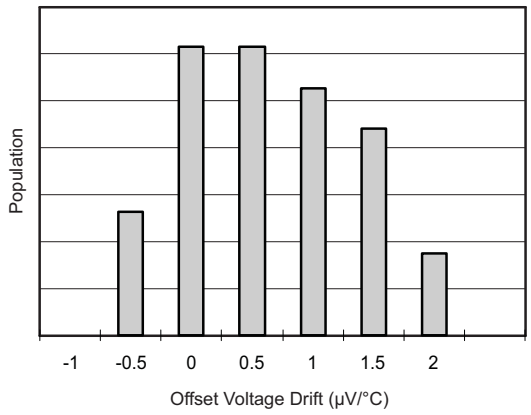
POWER SUPPLY AND COMMON−MODE REJECTION RATIO vs FREQUENCY



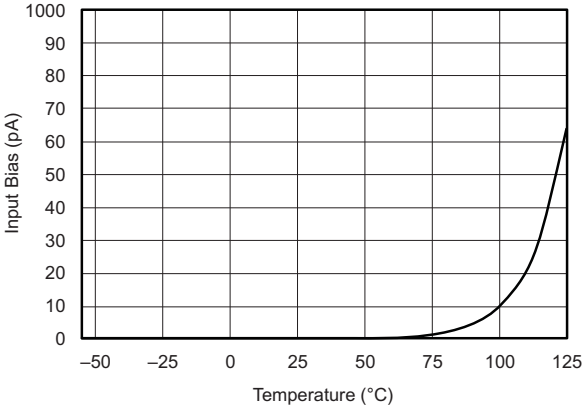
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



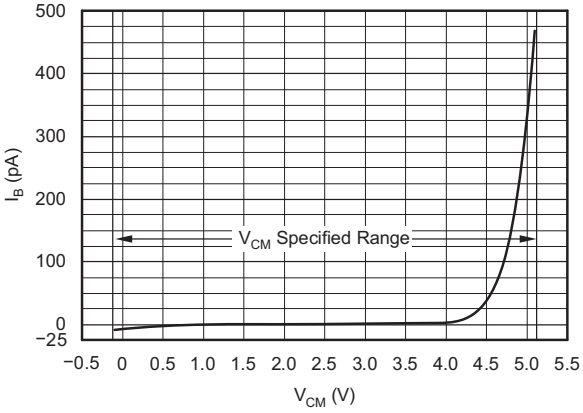
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



INPUT BIAS CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs COMMON−MODE VOLTAGE

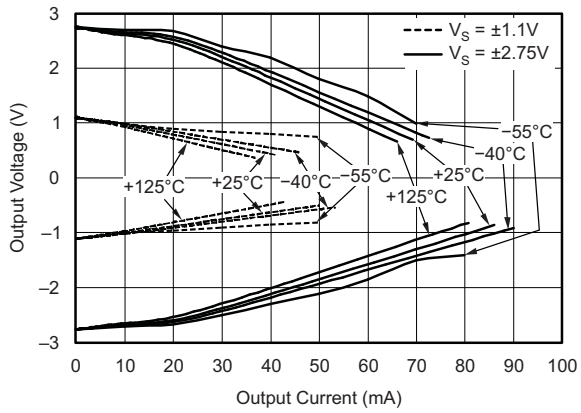


Copyright © 2011, Texas Instruments Incorporated

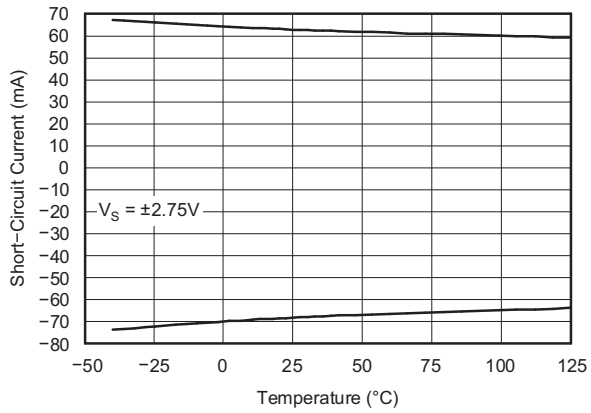
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_S = 5 V, C_L = 0 pF (unless otherwise noted)

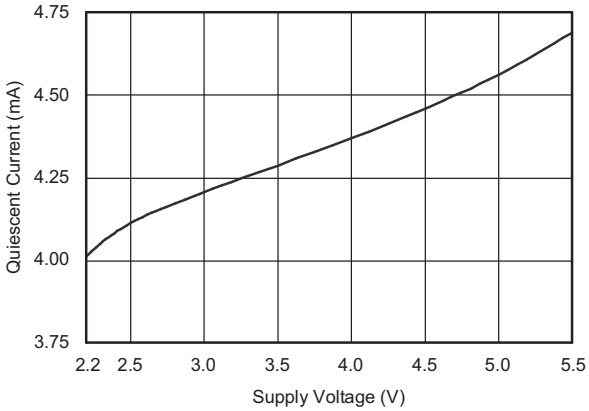
OPA365 OUTPUT VOLTAGE vs OUTPUT CURRENT



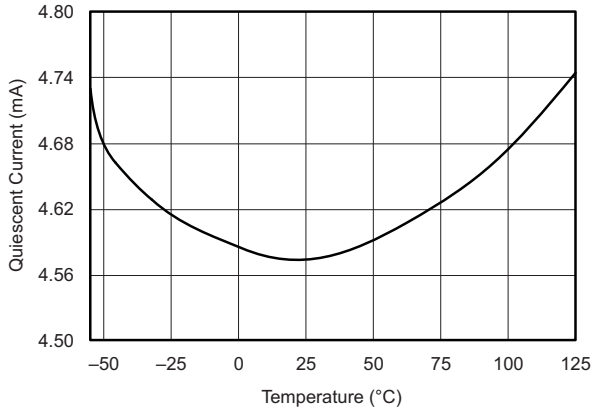
SHORT−CIRCUIT CURRENT vs TEMPERATURE



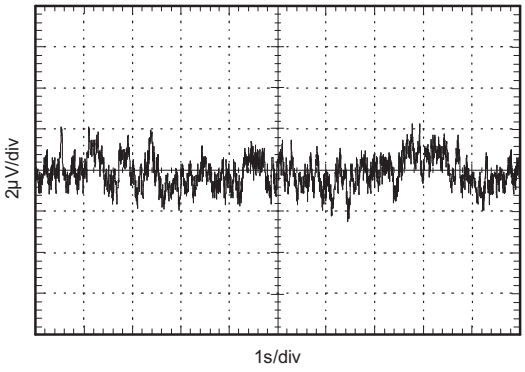
QUIESCENT CURRENT vs SUPPLY VOLTAGE



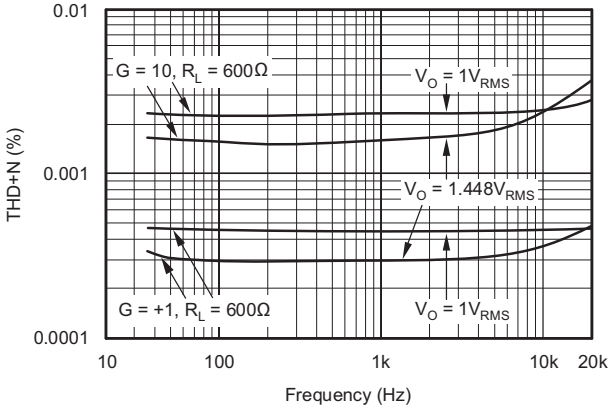
QUIESCENT CURRENT vs TEMPERATURE



0.1Hz to 10Hz
INPUT VOLTAGE NOISE



TOTAL HARMONIC DISTORTION + NOISE
vs FREQUENCY

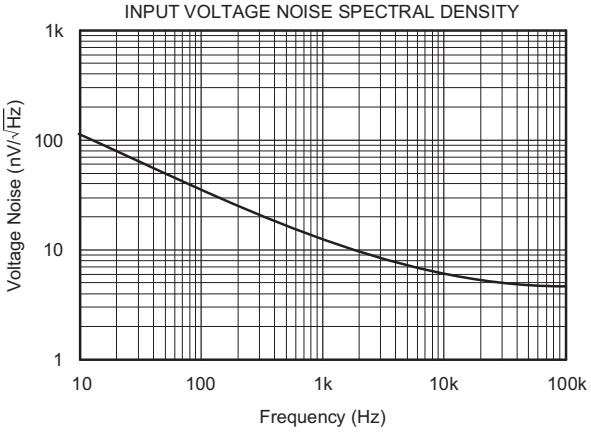


Copyright © 2011, Texas Instruments Incorporated

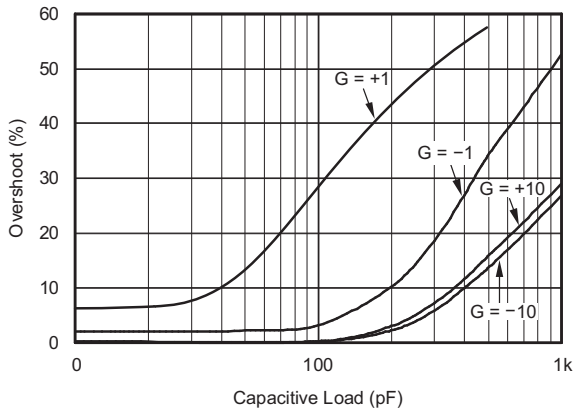
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_S = 5 V, C_L = 0 pF (unless otherwise noted)

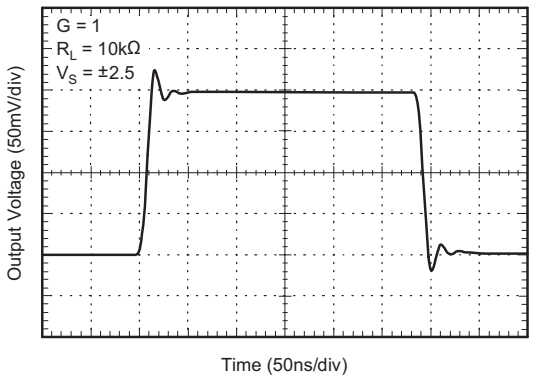
INPUT VOLTAGE NOISE SPECTRAL DENSITY



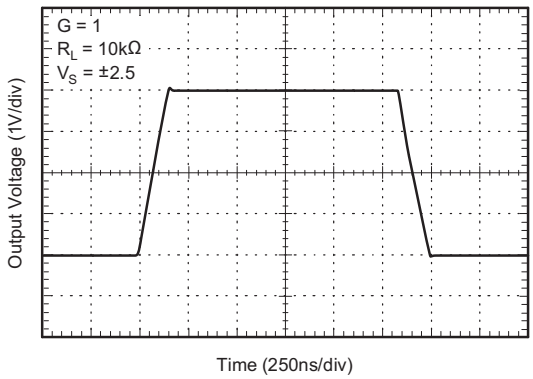
OVERSHOOT vs CAPACITIVE LOAD



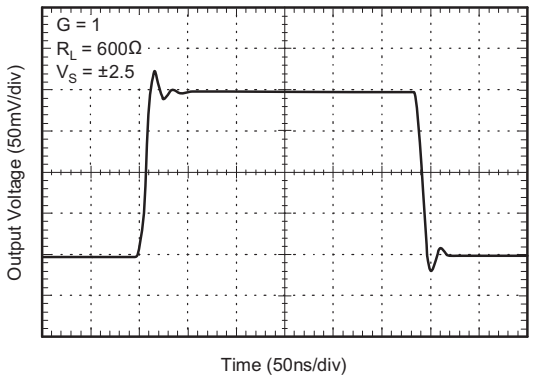
SMALL−SIGNAL STEP RESPONSE



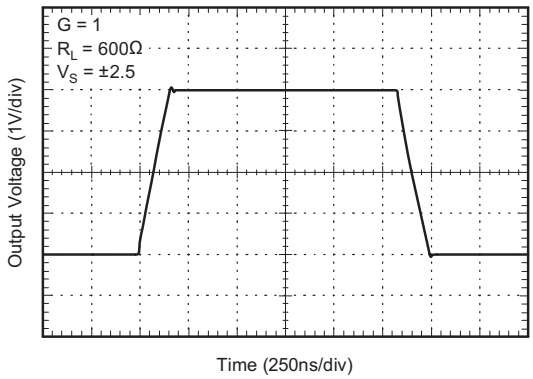
LARGE−SIGNAL STEP RESPONSE



SMALL−SIGNAL STEP RESPONSE



LARGE−SIGNAL STEP RESPONSE



Copyright © 2011, Texas Instruments Incorporated

APPLICATION INFORMATION

Operating Characteristics

The OPA365 amplifier parameters are fully specified from 2.2 V to 5.5 V. Many of the specifications apply from −55°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

General Layout Guidelines

The OPA365 is a wideband amplifier. To realize the full operational performance of the device, good high-frequency printed circuit board (PCB) layout practices are required. Low-loss 0.1-µF bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces should be designed for minimum inductance.

Basic Amplifier Configurations

As with other single-supply op amps, the OPA365 may be operated with either a single supply or dual supplies (see Figure 2). A typical dual-supply connection is shown in Figure 2, which is accompanied by a single-supply connection. The OPA365 is configured as a basic inverting amplifier with a gain of −10 V/V. The dual-supply connection has an output voltage centered on zero, while the single−supply connection has an output centered on the common-mode voltage V_{CM}. For the circuit shown, this voltage is 1.5 V, but may be any value within the common-mode input voltage range. The OPA365 V_{CM} range extends 100 mV beyond the power-supply rails.

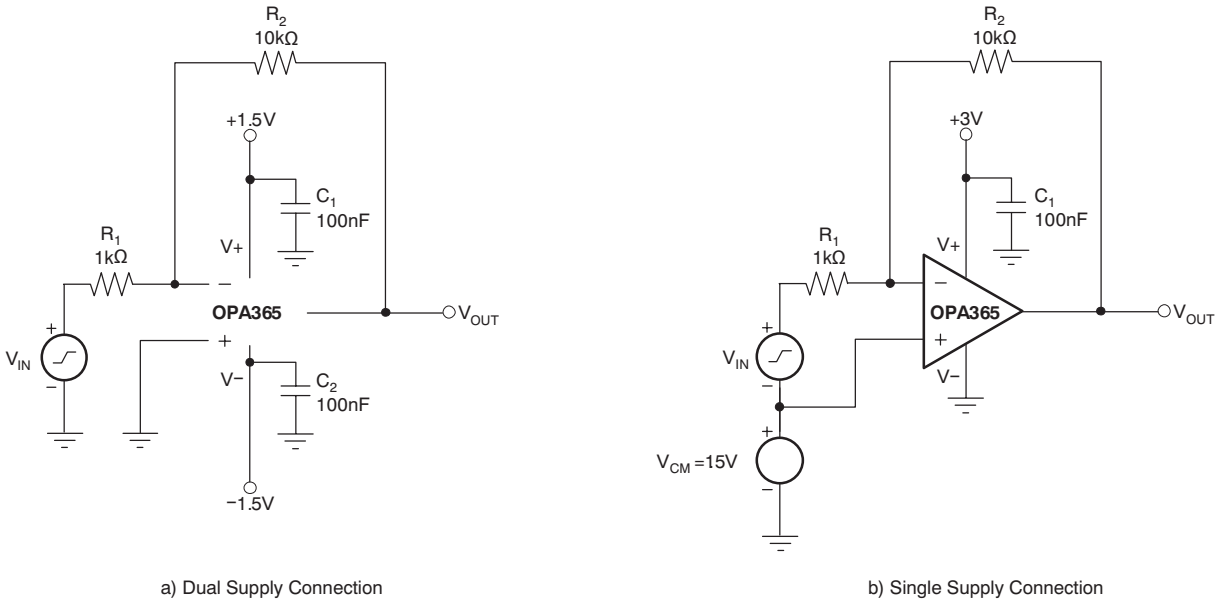


Figure 2. Basic Circuit Connections

Copyright © 2011, Texas Instruments Incorporated

Figure 3 shows a single-supply, electret microphone application where V_{CM} is provided by a resistive divider. The divider also provides the bias voltage for the electret element.

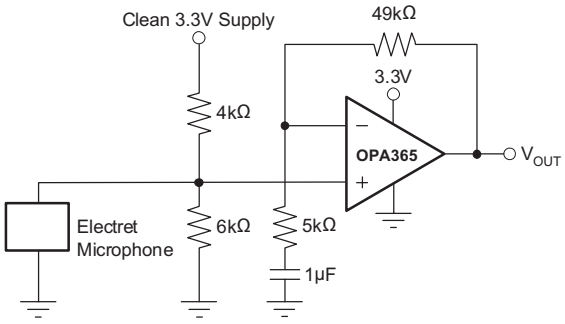


Figure 3. Microphone Preamplifier

Input and ESD Protection

The OPA365 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, provided that the current is limited to 10 mA as stated in the Absolute Maximum Ratings. Figure 4 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to the minimum in noise-sensitive applications.

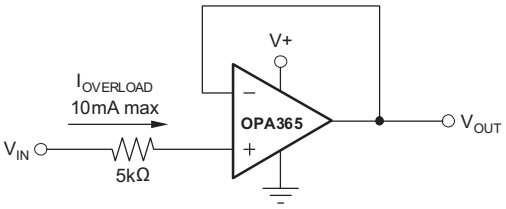


Figure 4. Input Current Protection

Rail-to-Rail Input

The OPA365 features true rail-to-rail input operation, with supply voltages as low as ±1.1 V (2.2 V). A unique zero-crossover input topology eliminates the input offset transition region typical of many rail-to-rail, complementary stage operational amplifiers. This topology also allows the OPA365 to provide superior common-mode performance over the entire input range, which extends 100 mV beyond both power-supply rails, as shown in Figure 5. When driving ADCs, the highly linear VCM range of the OPA365 assures that the op amp/ADC system linearity performance is not compromised.

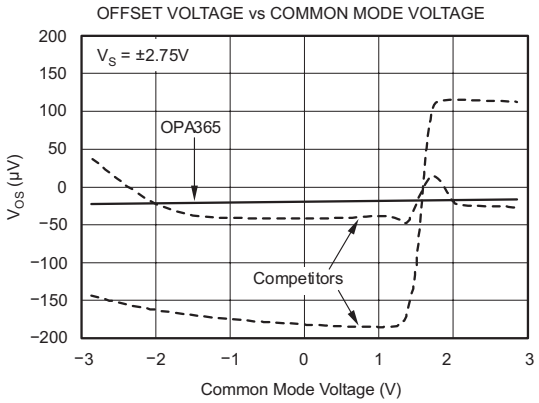


Figure 5. OPA365 has Linear Offset Over the Entire Common-Mode Range

A simplified schematic illustrating the rail-to-rail input circuitry is shown in Figure 6.

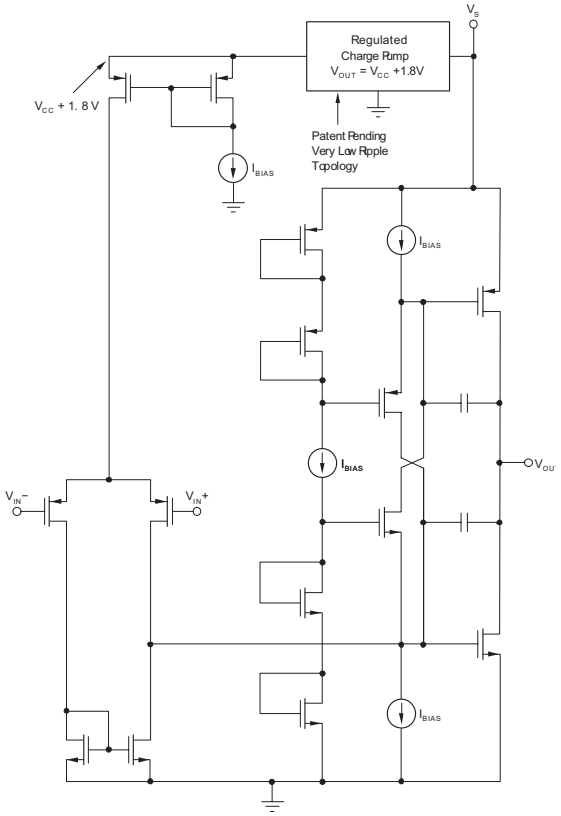


Figure 6. Simplified Schematic

Copyright © 2011, Texas Instruments Incorporated

Capacitive Loads

The OPA365 may be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPA365 can become unstable, leading to oscillation. The particular op amp circuit configuration, layout, gain and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation. An op amp in the unity-gain (1 V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases.

When operating in the unity-gain configuration, the OPA365 remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some very large capacitors (C_L > 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains. See the typical characteristic graph, Small-Signal Overshoot vs. Capacitive Load.

One technique for increasing the capacitive load drive capability of the amplifier operating in unity gain is to insert a small resistor, typically 10 Ω to 20 Ω, in series with the output; see Figure 7. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. A possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing. The error contributed by the voltage divider may be insignificant. For instance, with a load resistance, R_L = 10 kΩ, and R_S = 20 Ω, the gain error is only about 0.2%. However, when R_L is decreased to 600 Ω, which the OPA365 is able to drive, the error increases to 7.5%.

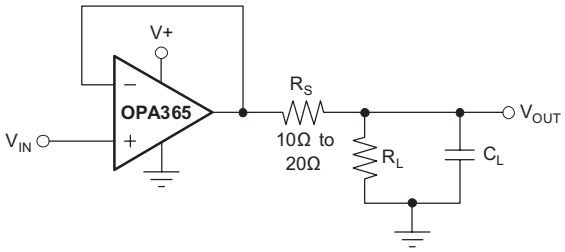


Figure 7. Improving Capacitive Load Drive

Achieving an Output Level of Zero Volts (0V)

Certain single-supply applications require the op amp output to swing from 0 V to a positive full-scale voltage and have high accuracy. An example is an op amp employed to drive a single-supply ADC having an input range from 0 V to 5 V. Rail-to-rail output amplifiers with very light output loading may achieve an output level within millivolts of 0 V (or $+V_S$ at the high end), but not 0 V. Furthermore, the deviation from 0V only becomes greater as the load current required increases. This increased deviation is a result of limitations of the CMOS output stage.

When a pulldown resistor is connected from the amplifier output to a negative voltage source, the OPA365 can achieve an output level of 0 V, and even a few millivolts below 0 V. Below this limit, nonlinearity and limiting conditions become evident. Figure 8 illustrates a circuit using this technique.

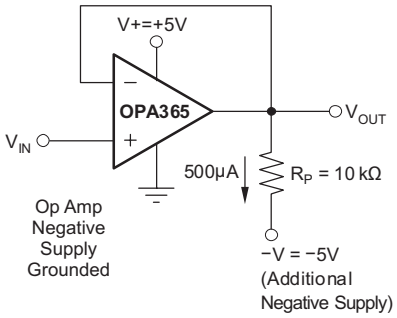


Figure 8. Swing-to-Ground

A pulldown current of approximately 500 µA is required when OPA365 is connected as a unity-gain buffer. A practical termination voltage (V_{NEG}) is −5 V, but other convenient negative voltages also may be used. The pulldown resistor R_L is calculated from $R_L = [(V_O - V_{NEG})/(500\ \mu A)]$. Using a minimum output voltage (V_O) of 0 V, $R_L = [0\ V-(-5\ V)]/(500\ \mu A)] = 10\ k\Omega$. Keep in mind that lower termination voltages result in smaller pulldown resistors that load the output during positive output voltage excursions.

Note that this technique does not work with all op amps and should only be applied to op amps such as the OPA365 that have been specifically designed to operate in this manner. Also, operating the OPA365 output at 0 V changes the output stage operating conditions, resulting in somewhat lower open-loop gain and bandwidth. Keep these precautions in mind when driving a capacitive load because these conditions can affect circuit transient response and stability.

Copyright © 2011, Texas Instruments Incorporated

Active Filtering

The OPA365 is well-suited for active filter applications requiring a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 9 shows a 500-kHz, 2nd-order, low-pass filter utilizing the multiple-feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is −40 dB/dec. The Butterworth response is ideal for applications requiring predictable gain characteristics such as the anti-aliasing filter used ahead of an ADC.

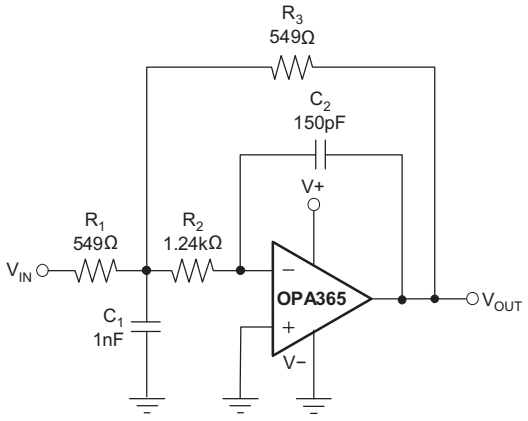


Figure 9. Second-Order Butterworth 500kHz Low-Pass Filter

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of these options: 1) adding an inverting amplifier; 2) adding an additional 2nd-order MFB stage; or 3) using a noninverting filter topology such as the Sallen-Key (shown in Figure 10). MFB and Sallen-Key, low-pass and high-pass filter synthesis is quickly accomplished using TI's FilterPro program. This software is available as a free download at www.ti.com.

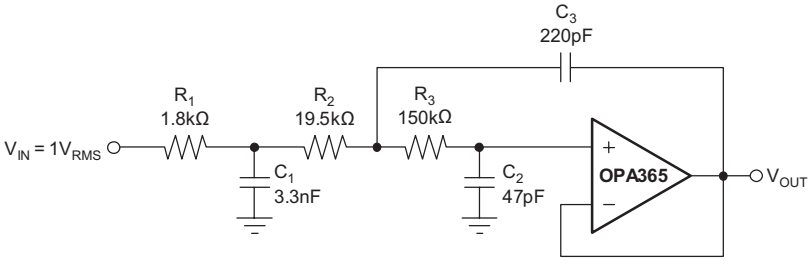


Figure 10. Configured as a 3-Pole, 20kHz, Sallen-Key Filter

Driving an Analog-to-Digital Converter

Very wide common-mode input range, rail-to-rail input and output voltage capability and high speed make the OPA365 an ideal driver for modern ADCs. Also, because it is free of the input offset transition characteristics inherent to some rail-to-rail CMOS op amps, the OPA365 provides low THD and excellent linearity throughout the input voltage swing range. Figure 11 shows the OPA365 driving an ADS8326, 16-bit, 250kSPS converter. The amplifier is connected as a unity-gain, noninverting buffer and has an output swing to 0 V, making it directly compatible with the ADC minus full-scale input level. The 0-V level is achieved by powering the OPA365 V−pin with a small negative voltage established by the diode forward voltage drop. A small, signal-switching diode or Schottky diode provides a suitable negative supply voltage of −0.3 V to −0.7 V. The supply rail-to-rail is equal to V+, plus the small negative voltage.

Copyright © 2011, Texas Instruments Incorporated

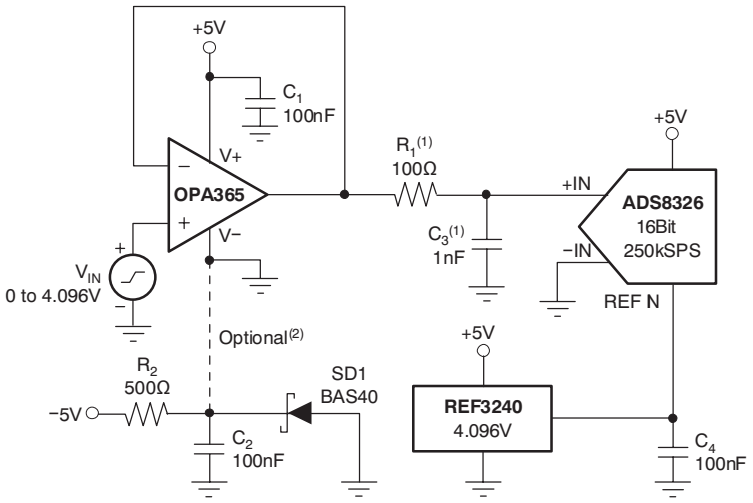


Figure 11. Driving the ADS8326

One method for driving an ADC that negates the need for an output swing down to 0 V uses a slightly compressed ADC full-scale input range (FSR). For example, the 16-bit ADS8361 (shown in Figure 12) has a maximum FSR of 0 V to 5 V, when powered by a 5-V supply and V_{REF} of 2.5 V. The idea is to match the ADC input range with the op amp full linear output swing range; for example, an output range of 0.1 V to 4.9 V. The reference output from the ADS8361 ADC is divided down from 2.5 V to 2.4 V using a resistive divider. The ADC FSR then becomes $4.8V_{PP}$ centered on a common-mode voltage of 2.5 V. Current from the ADS8361 reference pin is limited to about ±10 µA. Here, 5 µA was used to bias the divider. The resistors must be precise to maintain the ADC gain accuracy. An additional benefit of this method is the elimination of the negative supply voltage; it requires no additional power-supply current.

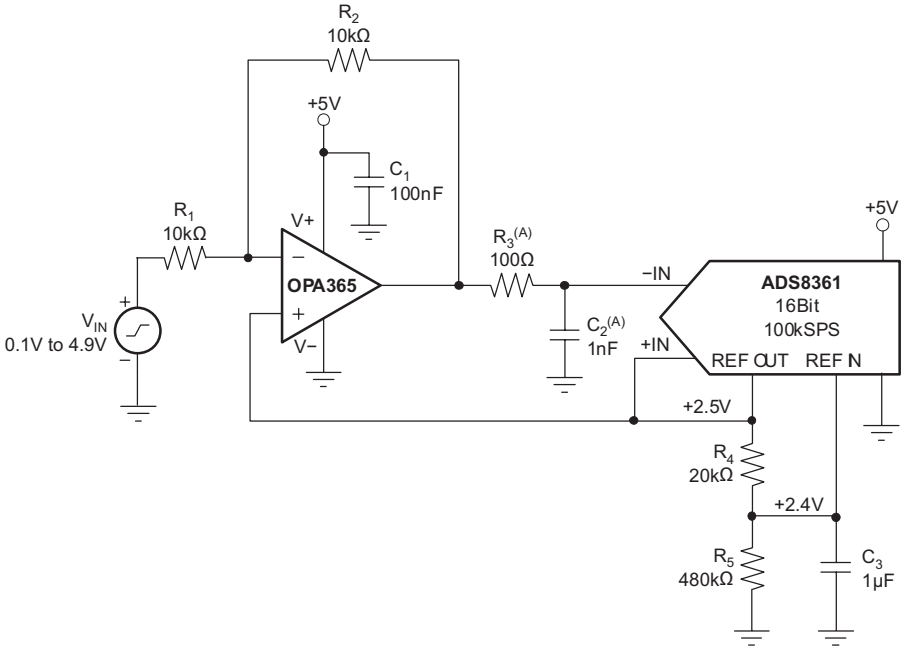


Figure 12. Driving the ADS8361

Copyright © 2011, Texas Instruments Incorporated

An RC network, consisting of R1 and C1, is included between the op amp and the ADS8361. It not only provides a high-frequency filter function, but more importantly serves as a charge reservoir used for charging the converter internal hold capacitance. This capability assures that the op amp output linearity is maintained as the ADC input characteristics change throughout the conversion cycle. Depending on the particular application and ADC, some optimization of the R1 and C1 values may be required for best transient performance.

Copyright © 2011, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA365AMDBVTEP	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	OUNM	Samples
V62/11610-01XE	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	OUNM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA365-EP :

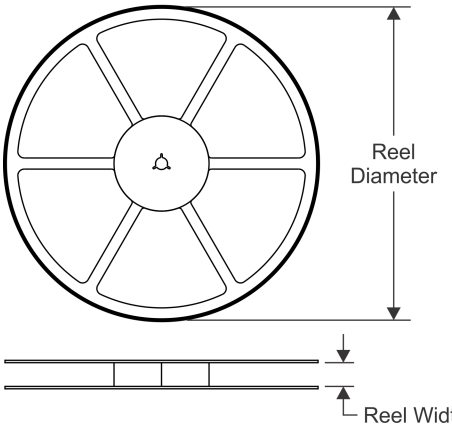
- Catalog: OPA365
- Automotive: OPA365-Q1

NOTE: Qualified Version Definitions:

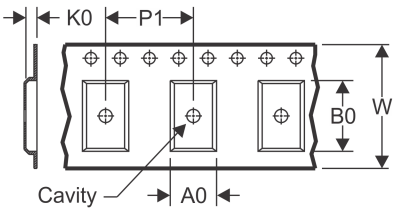
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

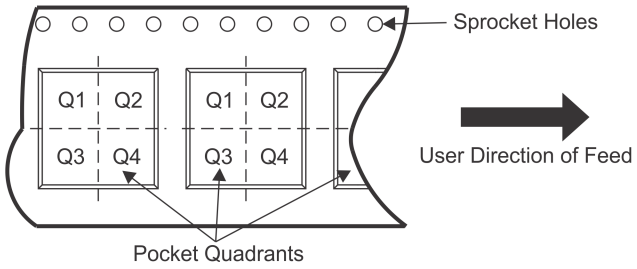


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

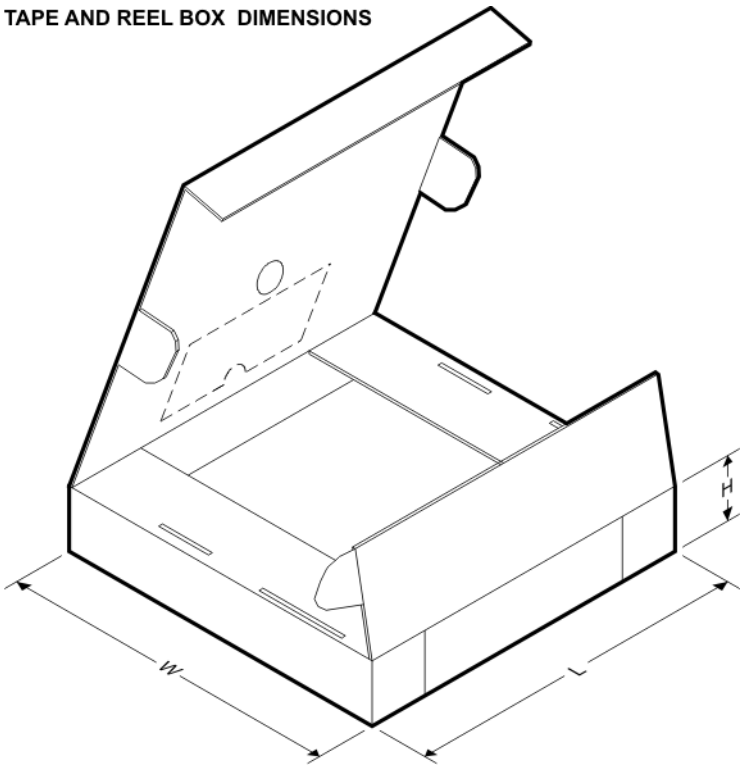
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA365AMDBVTEP	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

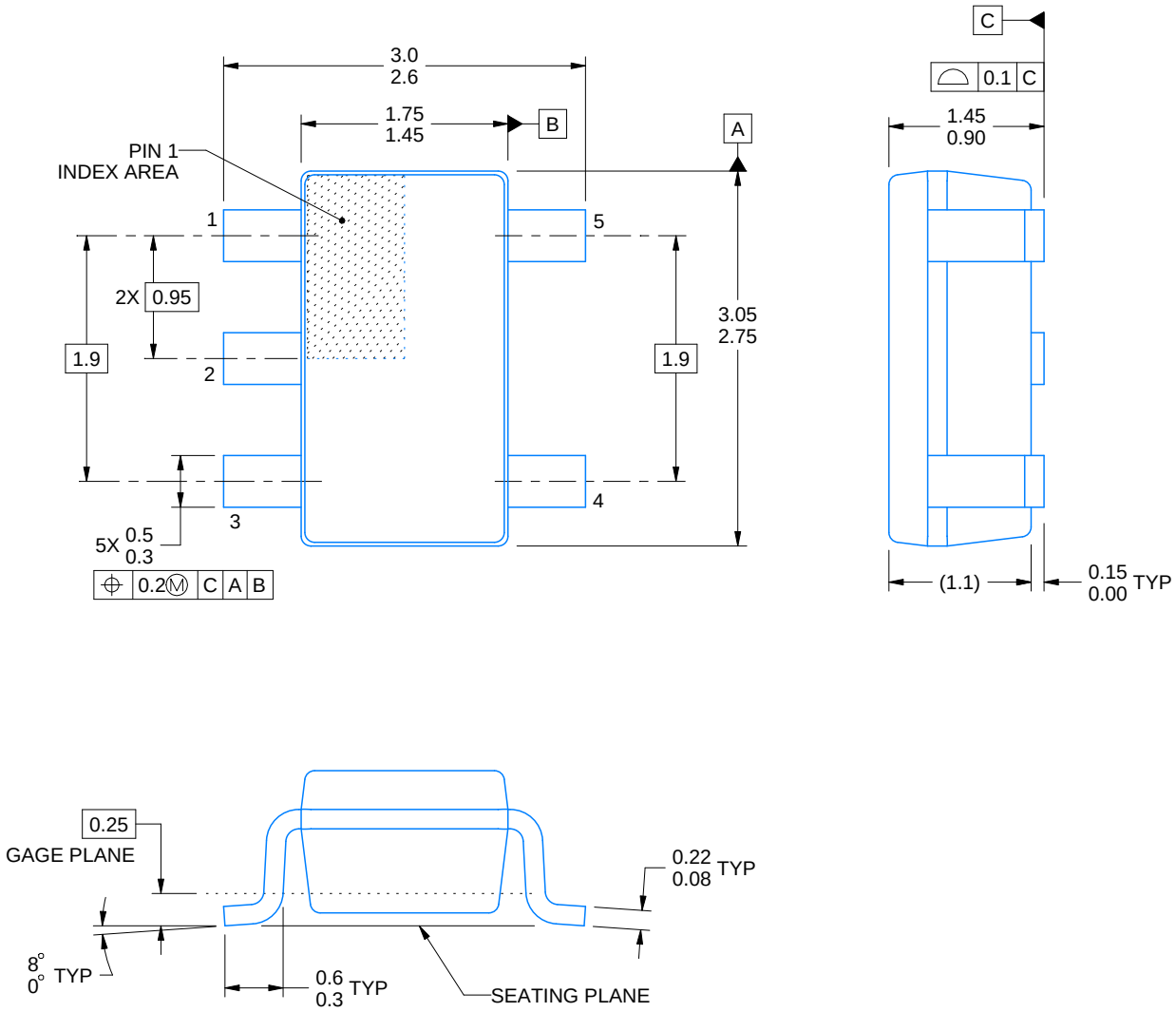
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA365AMDBVTEP	SOT-23	DBV	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

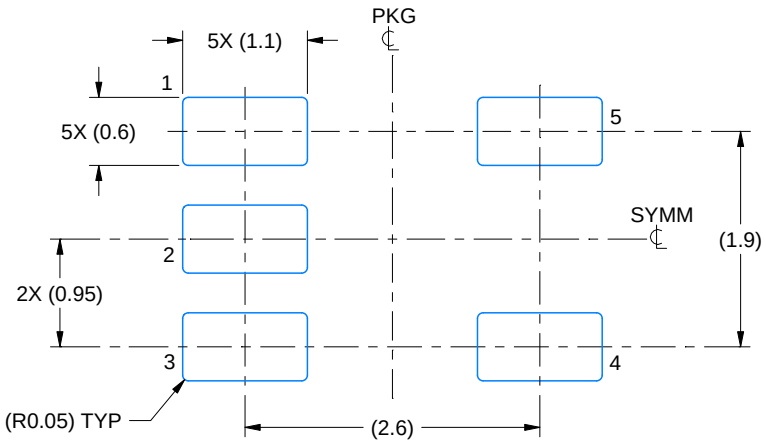
SMALL OUTLINE TRANSISTOR



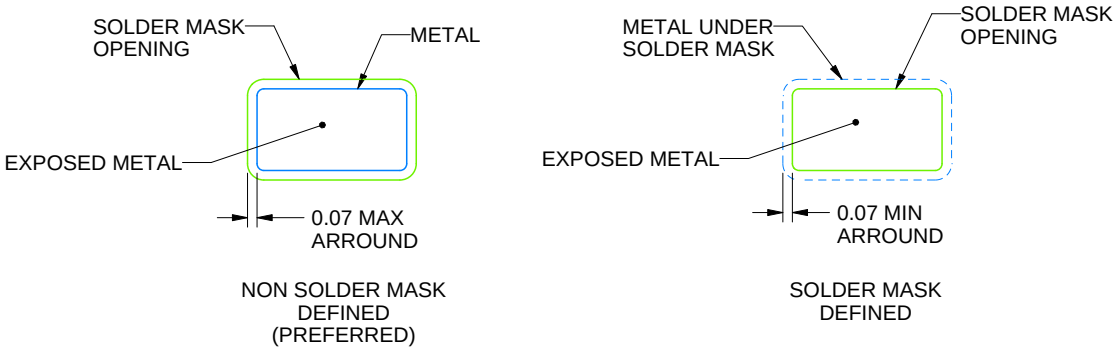
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

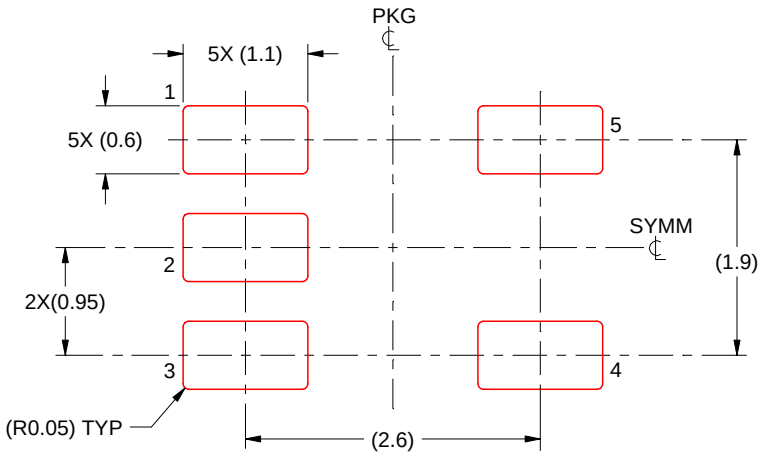


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated