# DisplayPort™ Quad Equalizer

**Check for Samples: DS32EV400**

## FEATURES

- **Equalizes up to 14 dB Loss at 3.2 Gbps**
- **8 Levels of Programmable Equalization**
- **Settable Through Control Pins or SMBus Interface**
- **Operates up to 3.2 Gbps With 40” FR4 Traces**
- **0.12 UI Residual Deterministic Jitter at 3.2 Gbps With 40” FR4 Traces**
- **Single 2.5V or 3.3V Power Supply**
- **Signal Detect for Individual Channels**
- **Standby Mode for Individual Channels**
- **Supports AC or DC-Coupling With Wide Input Common-Mode**
- **Low Power Consumption: 375 mW Typ at 2.5V**
- **Small 7 mm x 7 mm 48-pin WQFN Package**
- **9 kV HBM ESD Rating**
- **-40 to 85°C Operating Temperature Range**

## APPLICATIONS

- **DisplayPort**
- **XAUI**
- **InfiniBand**
- **Other 8b10b Applications**

## DESCRIPTION

The DS32EV400 programmable quad equalizer provides compensation for transmission medium losses and reduces the medium-induced deterministic jitter for four NRZ data channels. The DS32EV400 is optimized for operation up to 3.2 Gbps for both cables and FR4 traces. Each equalizer channel has eight levels of input equalization that can be programmed by three control pins, or individually through a Serial Management Bus (SMBus) interface. The device equalizes up to 14 dB of loss at 3.2 Gbps.

The equalizer supports both AC and DC-coupled data paths for long run length data patterns such as PRBS-31, and balanced codes such as 8b/10b. The device uses differential current-mode logic (CML) inputs and outputs.

Each channel has an independent signal detect output and independent enable input. The SD output maybe tied to the EN to automatically control the power up and down of the channel.

The DS32EV400 can be used in a variety of applications that include DisplayPort, XAUI, InfiniBand and other high-speed data transmission applications.

The DS32EV400 is available in a 7 mm x 7 mm 48-pin leadless WQFN package. Power is supplied from either a 2.5V or 3.3V supply.

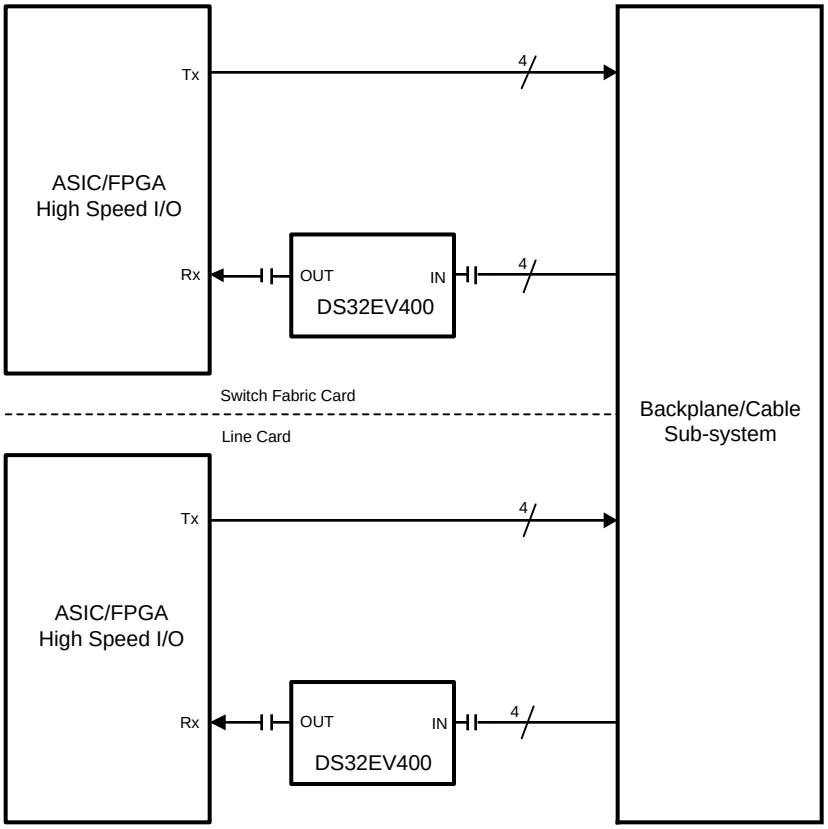
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## Simplified Application Diagram





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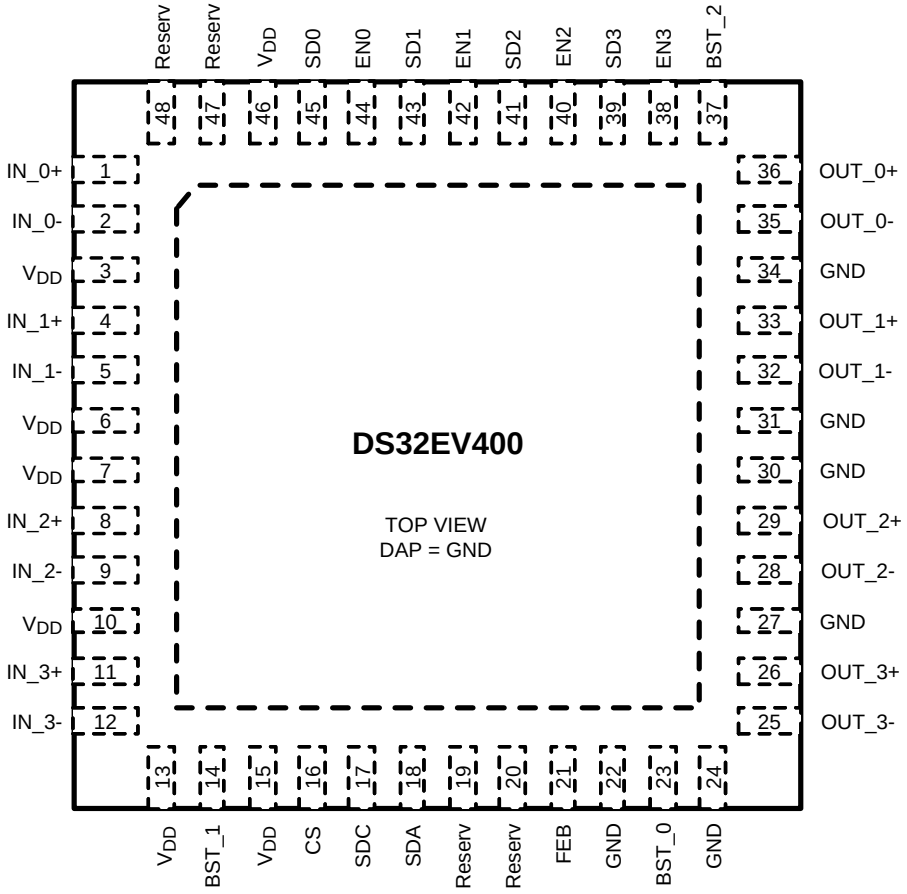
## PIN DESCRIPTIONS

| Pin Name | Pin # | I/O, Type[1] | Description |
|---|---|---|---|
| **HIGH SPEED DIFFERENTIAL I/O** | | | |
| IN_0+<br>IN_0– | 1<br>2 | I, CML | Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor is connected between IN_0+ and IN_0-. Refer to Figure 6. |
| IN_1+<br>IN_1– | 4<br>5 | I, CML | Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor is connected between IN_1+ and IN_1-. Refer to Figure 6. |
| IN_2+<br>IN_2– | 8<br>9 | I, CML | Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor is connected between IN_2+ and IN_2-. Refer to Figure 6. |
| IN_3+<br>IN_3– | 11<br>12 | I, CML | Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor is connected between IN_3+ and IN_3-. Refer to Figure 6. |
| OUT_0+<br>OUT_0– | 36<br>35 | O, CML | Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_0+ to $V_{DD}$ and OUT_0- to $V_{DD}$. |
| OUT_1+<br>OUT_1– | 33<br>32 | O, CML | Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_1+ to $V_{DD}$ and OUT_1- to $V_{DD}$. |
| OUT_2+<br>OUT_2– | 29<br>28 | O, CML | Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_2+ to $V_{DD}$ and OUT_2- to $V_{DD}$. |
| OUT_3+<br>OUT_3– | 26<br>25 | O, CML | Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_3+ to $V_{DD}$ and OUT_3- to $V_{DD}$. |
| **EQUALIZATION CONTROL** | | | |
| BST_2<br>BST_1<br>BST_0 | 37<br>14<br>23 | I, LVCMOS | BST_2, BST_1, and BST_0 select the equalizer strength for all EQ channels. BST_2 is internally pulled high. BST_1 and BST_0 are internally pulled low. |
| **DEVICE CONTROL** | | | |
| EN0 | 44 | I, LVCMOS | Enable Equalizer Channel 0 input. When held High, normal operation is selected. When held Low, standby mode is selected. EN is internally pulled High. |
| EN1 | 42 | I, LVCMOS | Enable Equalizer Channel 1 input. When held High, normal operation is selected. When held Low, standby mode is selected. EN is internally pulled High. |
| EN2 | 40 | I, LVCMOS | Enable Equalizer Channel 2 input. When held High, normal operation is selected. When held Low, standby mode is selected. EN is internally pulled High. |
| EN3 | 38 | I, LVCMOS | Enable Equalizer Channel 3 input. When held High, normal operation is selected. When held Low, standby mode is selected. EN is internally pulled High. |
| FEB | 21 | I, LVCMOS | Force External Boost. When held high, the equalizer boost setting is controlled by BST_[2:0] pins. When held low, the equalizer boost setting is controlled by SMBus (see Table 1) register bits. FEB is internally pulled High. |
| SD0 | 45 | O, LVCMOS | Equalizer Ch0 Signal Detect Output. Produces a High when signal is detected. |
| SD1 | 43 | O, LVCMOS | Equalizer Ch1 Signal Detect Output. Produces a High when signal is detected. |
| SD2 | 41 | O, LVCMOS | Equalizer Ch2 Signal Detect Output. Produces a High when signal is detected. |
| SD3 | 39 | O, LVCMOS | Equalizer Ch3 Signal Detect Output. Produces a High when signal is detected. |
| **POWER** | | | |
| $V_{DD}$ | 3, 6, 7,<br>10, 13,<br>15, 46 | Power | $V_{DD}$ = 2.5V ± 5% or 3.3V ± 10%. $V_{DD}$ pins should be tied to $V_{DD}$ plane through low inductance path. A 0.01µF bypass capacitor should be connected between each $V_{DD}$ pin to GND planes. |
| GND | 22, 24,<br>27, 30,<br>31, 34 | Power | Ground reference. GND should be tied to a solid ground plane through a low impedance path. |
| DAP | PAD | Power | Ground reference. The exposed pad at the center of the package must be connected to ground plane of the board. |
| **SERIAL MANAGEMENT BUS (SMBus) INTERFACE CONTROL PINS** | | | |
| SDA<br>SDC<br>CS | 18<br>17<br>16 | I/O, LVCMOS<br>I, LVCMOS<br>I, LVCMOS | Data input/output (bi-directional). Internally pulled high.<br>Clock input. Internally pulled high.<br>Chip select. When pulled high, access to the equalizer SMBus registers are enabled. When pulled low, access to the equalizer SMBus registers are disabled. Please refer to System Management Bus (SMBus) and Configuration Registers for detailed information. |
| **Other** | | | |
| Reserv | 19, 20<br>47,48 | | Reserved. Do not connect. |

(1) I = Input, O = Output

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## Connection Diagram





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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings (1)(2)

| | | |
|---|---|---|
| Supply Voltage ($V_{DD}$) | | -0.5V to +4.0V |
| CMOS Input Voltage | | -0.5V + 4.0V |
| CMOS Output Voltage | | -0.5V to 4.0V |
| CML Input/Output Voltage | | -0.5V to 4.0V |
| Junction temperature | | +150°C |
| Storage temperature | | -65°C to +150°C |
| Lead temperature (Soldering, 4 Seconds) | | +260°C |
| ESD rating | HBM, 1.5 kΩ, 100 pF | > 9 kV |
| | EIAJ, 0Ω, 200pF | > 250 V |
| Thermal Resistance — $\theta_{JA}$, no airflow | | 30°C/W |

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are ensured for a junction temperature range of –40°C to +125°C. Models are validated to Maximum Operating Voltages only.

(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

## Recommended Operating Conditions

| | Min | Typ | Max | Units |
|---|---|---|---|---|
| Supply Voltage (1) | | | | |
| $V_{DD2.5}$ to GND | 2.375 | 2.5 | 2.625 | V |
| $V_{DD3.3}$ to GND | 3.0 | 3.3 | 3.6 | V |
| Ambient Temperature | -40 | 25 | +85 | °C |

(1) The $V_{DD2.5}$ is $V_{DD}$ = 2.5V ± 5% and $V_{DD3.3}$ is $V_{DD}$ = 3.3V ± 10%.

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## Electrical Characteristics[1]

Over recommended operating supply and temperature ranges with default register settings unless other specified.

| Symbol | Parameter | Conditions | Min | Typ[2] | Max | Units |
|---|---|---|---|---|---|---|
| **POWER** | | | | | | |
| P | Power Supply Consumption | Device Output Enabled (EN [0–3] = High), $V_{DD3.3}$ | | 490 | 700 | mW |
| | | Device Output Disable (EN [0–3] = Low), $V_{DD3.3}$ | | | 100 | mW |
| P | Power Supply Consumption | Device Output Enabled (EN [0–3] = High), $V_{DD2.5}$ | | 360 | 490 | mW |
| | | Device Output Disable (EN [0–3] = Low), $V_{DD2.5}$ | | 30 | | |
| N | Supply Noise Tolerance [3] | 50 Hz — 100 Hz<br>100 Hz — 10 MHz<br>10 MHz — 1.6 GHz | | 100<br>40<br>10 | | $mV_{P-P}$<br>$mV_{P-P}$<br>$mV_{P-P}$ |
| **LVCMOS DC SPECIFICATIONS** | | | | | | |
| $V_{IH}$ | High Level Input Voltage | $V_{DD3.3}$ | 2.0 | | $V_{DD3.3}$ | V |
| | | $V_{DD2.5}$ | 1.6 | | $V_{DD2.5}$ | V |
| $V_{IL}$ | Low Level Input Voltage | | -0.3 | | 0.8 | V |
| $V_{OH}$ | High Level Output Voltage | $I_{OH}$ = -3mA, $V_{DD3.3}$ | 2.4 | | | V |
| | | $I_{OH}$ = -3mA, $V_{DD2.5}$ | 2.0 | | | |
| $V_{OL}$ | Low Level Output Voltage | $I_{OL}$ = 3mA | | | 0.4 | V |
| $I_{IN}$ | Input Leakage Current | $V_{IN} = V_{DD}$ | | | +15 | µA |
| | | $V_{IN}$ = GND | -15 | | | µA |
| $I_{IN-P}$ | Input Leakage Current with Internal Pull-Down/Up Resistors | $V_{IN} = V_{DD}$, with internal pull-down resistors | | | +120 | µA |
| | | $V_{IN}$ = GND, with internal pull-up resistors | -20 | | | µA |
| **SIGNAL DETECT** | | | | | | |
| SDH | Signal Detect ON Threshold Level | Default input signal level to assert SD pin, 3.2 Gbps | | 70 | | $mV_{p-p}$ |
| SDI | Signal Detect OFF Threshold Level | Default input signal level to de-assert SD, 3.2Gbps | | 40 | | $mV_{p-p}$ |
| **CML RECEIVER INPUTS (IN_n+, IN_n-)** | | | | | | |
| $V_{TX}$ | Source Transmit Launch Signal Level (IN diff) | AC-Coupled or DC-Coupled Requirement, Differential measurement at point A. Figure 1 | 400 | | 1600 | $mV_{P-P}$ |
| $V_{INTRE}$ | Input Threshold Voltage | Differential measurement at point B. Figure 1 | | 120 | | $mV_{P-P}$ |
| $V_{DDTX}$ | Supply Voltage of Transmitter to EQ | DC-Coupled Requirement ([4]) | 1.6 | | $V_{DD}$ | V |
| $V_{ICMDC}$ | Input Common Mode Voltage | DC-Coupled Requirement, Differential measurement at point A. Figure 1, ([5]) | $V_{DDTX}$ – 0.8 | | $V_{DDTX}$ – 0.2 | V |
| $R_{LI}$ | Differential Input Return Loss | 100MHz – 1.6GHz, with fixture's effect de-embedded | | 10 | | dB |
| $R_{IN}$ | Input Resistance | Differential across IN+ and IN-, Figure 6. | 85 | 100 | 115 | Ω |

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at $V_{DD}$ = 3.3V, $T_A$ = 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(3) Allowed supply noise ($mV_{P-P}$ sine wave) under typical conditions.
(4) Recommended value. Parameter not tested.
(5) Measured with clock like {11111 00000} pattern.


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## Electrical Characteristics[1] (continued)

Over recommended operating supply and temperature ranges with default register settings unless other specified.

| Symbol | Parameter | Conditions | Min | Typ[2] | Max | Units |
|---|---|---|---|---|---|---|
| **CML OUTPUTS (OUT_n+, OUT_n-)** | | | | | | |
| $V_{OD}$ | Output Differential Voltage Level (OUT diff) | Differential measurement with OUT+ and OUT- terminated by 50Ω to GND, AC-Coupled Figure 2 | 500 | 620 | 725 | $mV_{P-P}$ |
| $V_{OCM}$ | Output Common Mode Voltage | Single-ended measurement DC-Coupled with 50Ω terminations (6) | $V_{DD}$– 0.2 | | $V_{DD}$– 0.1 | V |
| $t_R$, $t_F$ | Transition Time | 20% to 80% of differential output voltage, measured within 1" from output pins. Figure 2, (6) | 20 | | 60 | ps |
| $R_O$ | Output Resistance | Single ended to $V_{DD}$ | 42 | 50 | 58 | Ω |
| $R_{LO}$ | Differential Output Return Loss | 100 MHz – 1.6 GHz, with fixture's effect de-embedded. IN+ = static high. | | 10 | | dB |
| $t_{PLHD}$ | Differential Low to High Propagation Delay | Propagation delay measurement at 50% VO between input to output, 100 Mbps. Figure 3, (6) | | 240 | | ps |
| $t_{PHLD}$ | Differential High to Low Propagation Delay | | | 240 | | ps |
| $t_{CCSK}$ | Inter Pair Channel to Channel Skew | Difference in 50% crossing between channels | | 7 | | ps |
| $t_{PPSK}$ | Part to Part Output Skew | Difference in 50% crossing between outputs | | 20 | | ps |
| **EQUALIZATION** | | | | | | |
| DJ1 | Residual Deterministic Jitter at 3.2 Gbps | 40" of 6 mil microstrip FR4, EQ Setting 0x07, PRBS-7 ($2^7$-1) pattern. ((7) (8)) | | 0.12 | 0.20 | $UI_{P-P}$ |
| DJ2 | Residual Deterministic Jitter at 2.5 Gbps | 40" of 6 mil microstrip FR4, EQ Setting 0x07, PRBS-7 ($2^7$-1) pattern. ((7) (8)) | | 0.1 | 0.16 | $UI_{P-P}$ |
| DJ3 | Residual Deterministic Jitter at 1 Gbps | 40" of 6 mil microstrip FR4, EQ Setting 0x07, PRBS-7 ($2^7$-1) pattern. ((7) (8)) | | 0.05 | | $UI_{P-P}$ |
| RJ | Random Jitter | (6) (9) | | 0.5 | | psrms |
| **SIGNAL DETECT and ENABLE TIMING** | | | | | | |
| $t_{ZISD}$ | Input OFF to ON detect — SD Output High Response Time | Response time measurement at $V_{IN}$ to SD output, $V_{IN}$ = 800 $mV_{P-P}$, 100 Mbps, 40" of 6 mil microstrip FR4 See Figure 1 and Figure 4 (6) | | 35 | | ns |
| $t_{IZSD}$ | Input ON to OFF detect — SD Output Low Response Time | | | 400 | | ns |
| $t_{OZOED}$ | EN High to Output ON Response Time | Response time measurement at EN input to $V_O$, $V_{IN}$ = 800 $mV_{P-P}$, 100 Mbps, 40" of 6 mil microstrip FR4 See Figure 1 and Figure 5 (6) | | 150 | | ns |
| $t_{ZOED}$ | EN Low to Output OFF Response Time | | | 5 | | ns |

(6) Measured with clock like {11111 00000} pattern.
(7) Specification is ensured by characterization and is not tested in production.
(8) Deterministic jitter is measured at the differential outputs (point C of Figure 1), minus the deterministic jitter before the test channel (point A of Figure 1). Random jitter is removed through the use of averaging or similar means.
(9) Random jitter contributed by the equalizer is defined as sqrt ($J_{OUT}^2 - J_{IN}^2$). $J_{OUT}$ is the random jitter at the equalizer outputs in ps-rms, see point C of Figure 1; $J_{IN}$ is the random jitter at the input of the equalizer in ps-rms, see Figure 1.

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## Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **SERIAL BUS INTERFACE DC SPECIFICATIONS** | | | | | | |
| $V_{IL}$ | Data, Clock Input Low Voltage | | | | 0.8 | V |
| $V_{IH}$ | Data, Clock Input High Voltage | | 2.1 | | $V_{DD}$ | V |
| $I_{PULLUP}$ | Current through pull-up resistor or current source | High Power Specification | 4 | | | mA |
| $V_{DD}$ | Nominal Bus Voltage | | 2.375 | | 3.6 | V |
| $I_{LEAK-Bus}$ | Input Leakage per bus segment | (1) | -200 | | +200 | µA |
| $I_{LEAK-Pin}$ | Input Leakage per device pin | | | -15 | | µA |
| $C_I$ | Capacitance for SDA and SDC | (1) (2) | | | 10 | pF |
| $R_{TERM}$ | External Termination Resistance pull to $V_{DD}$ = 2.5V ± 5% OR 3.3V ± 10 | $V_{DD3.3}$ (1) (2) (3) | | 2000 | | Ω |
| | | $V_{DD2.5}$ (1) (2) (3) | | 1000 | | Ω |
| **SERIAL BUS INTERFACE TIMING SPECIFICATIONS (Figure 7)** | | | | | | |
| FSMB | Bus Operating Frequency | (4) | 10 | | 100 | kHz |
| TBUF | Bus Free Time Between Stop and Start Condition | | 4.7 | | | µs |
| THD:STA | Hold Time After (Repeated) Start Condition. After this period, the first clock is generated. | At $I_{PULLUP}$, Max | 4.0 | | | µs |
| TSU:STA | Repeated Start Condition Setup Time | | 4.7 | | | µs |
| TSU:STO | Stop Condition Setup Time | | 4.0 | | | µs |
| THD:DAT | Data Hold Time | | 300 | | | ns |
| TSU:DAT | Data Setup Time | | 250 | | | ns |
| $T_{TIMEOUT}$ | Detect Clock Low Timeout | (4) | 25 | | 35 | ms |
| $T_{LOW}$ | Clock Low Period | | 4.7 | | | µs |
| $T_{HIGH}$ | Clock High Period | (4) | 4.0 | | 50 | µs |
| $T_{LOW}$:SEXT | Cumulative Clock Low Extend Time (Slave Device) | (4) | | | 2 | ms |
| $t_F$ | Clock/Data Fall Time | (4) | | | 300 | ns |
| $t_R$ | Clock/Data Rise Time | (4) | | | 1000 | ns |
| $t_{POR}$ | Time in which a device must be operational after power-on reset | (4) | | | 500 | ms |

(1) Recommended value. Parameter not tested.
(2) Recommended maximum capacitance load per bus segment is 400pF.
(3) Maximum termination voltage should be identical to the device supply voltage.
(4) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 *SMBus Common AC Specifications* for details.


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## SYSTEM MANAGEMENT BUS (SMBUS) AND CONFIGURATION REGISTERS

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. The use of the Chip Select signal is **required**. Holding the CS pin High enables the SMBus port allowing access to the configuration registers. Holding the CS pin Low disables the device's SMBus allowing communication from the host to other slave devices on the bus. In the STANDBY state, the System Management Bus remains active. When communication to other devices on the SMBus is active, the CS signal for the DS32EV400s must be driven Low.

The address byte for all DS32EV400s is AC'h. Based on the SMBus 2.0 specification, the DS32EV400 has a 7-bit slave address of 1010110'b. The LSB is set to 0'b (for a WRITE), thus the 8-bit value is 1010 1100'b or AC'h.

The SDC and SDA pins are 3.3V LVCMOS signaling and include high-Z internal pull up resistors. External low impedance pull up resistors maybe required depending upon SMBus loading and speed. Note, these pins are not 5V tolerant.

### Transfer of Data via the SMBus

During normal operation the data on SDA must be stable during the time when SDC is High.

There are three unique states for the SMBus:

**START:** A High-to-Low transition on SDA while SDC is High indicates a message START condition.

**STOP:** A Low-to-High transition on SDA while SDC is High indicates a message STOP condition.

**IDLE:** If SDC and SDA are both High for a time exceeding $t_{BUF}$ from the last detected STOP condition or if they are High for a total exceeding the maximum specification for $t_{HIGH}$ then the bus will transfer to the IDLE state.

### SMBus Transactions

The device supports WRITE and READ transactions. See Table 1 for register address, type (Read/Write, Read Only), default value and function information.

### Writing a Register

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host (Master) selects the device by driving its SMBus Chip Select (CS) signal High.
2. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
3. The Device (Slave) drives the ACK bit (“0”).
4. The Host drives the 8-bit Register Address.
5. The Device drives an ACK bit (“0”).
6. The Host drive the 8-bit data byte.
7. The Device drives an ACK bit (“0”).
8. The Host drives a STOP condition.
9. The Host de-selects the device by driving its SMBus CS signal Low.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

### Reading a Register

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host (Master) selects the device by driving its SMBus Chip Select (CS) signal High.
2. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
3. The Device (Slave) drives the ACK bit (“0”).
4. The Host drives the 8-bit Register Address.
5. The Device drives an ACK bit (“0”).
6. The Host drives a START condition.
7. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
8. The Device drives an ACK bit “0”.

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9. The Device drives the 8-bit data value (register contents).
10. The Host drives a NACK bit “1”indicating end of the READ transfer.
11. The Host drives a STOP condition.
12. The Host de-selects the device by driving its SMBus CS signal Low.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

Please see Table 1 for more information.

**Table 1. SMBus Register Address**

| Name | Address | Default | Type(1) | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Status** | 0x00 | 0x00 | RO | ID Revision | | | | SD3 | SD2 | SD1 | SD0 |
| **Status** | 0x01 | 0x00 | RO | EN1 | Boost 1 | | | EN0 | Boost 0 | | |
| **Status** | 0x02 | 0x00 | RO | EN3 | Boost 3 | | | EN2 | Boost 2 | | |
| **Enable/ Boost (CH 0, 1)** | 0x03 | 0x44 | RW | EN1 Output<br>0:Enable<br>1:Disable | Boost Control for CH1<br>000 (Min Boost)<br>001<br>010<br>011<br>100 (Default)<br>101<br>110<br>111 (Max Boost) | | | EN0 Output<br>0:Enable<br>1:Disable | Boost Control for CH0<br>000 (Min Boost)<br>001<br>010<br>011<br>100 (Default)<br>101<br>110<br>111 (Max Boost) | | |
| **Enable/ Boost (CH 2, 3)** | 0x04 | 0x44 | RW | EN3 Output<br>0:Enable<br>1:Disable | Boost Control for CH3<br>000 (Min Boost)<br>001<br>010<br>011<br>100 (Default)<br>101<br>110<br>111 (Max Boost) | | | EN2 Output<br>0:Enable<br>1:Disable | Boost Control for CH2<br>000 (Min Boost)<br>001<br>010<br>011<br>100 (Default)<br>101<br>110<br>111 (Max Boost) | | |
| **Signal Detect** | 0x05 | 0x00 | RW | SD3 ON Threshold Select<br>00: 70 mV (Default)<br>01: 55 mV<br>10: 90 mV<br>11: 75 mV | | SD2 ON Threshold Select<br>00: 70 mV (Default)<br>01: 55 mV<br>10: 90 mV<br>11: 75 mV | | SD1 ON Threshold Select<br>00: 70 mV (Default)<br>01: 55 mV<br>10: 90 mV<br>11: 75 mV | | SD0 ON Threshold Select<br>00: 70 mV (Default)<br>01: 55 mV<br>10: 90 mV<br>11: 75 mV | |
| **Signal Detect** | 0x06 | 0x00 | RW | SD3 OFF Threshold Select<br>00: 40 mV (Default)<br>01: 30 mV<br>10: 55 mV<br>11: 45 mV | | SD2 OFF Threshold Select<br>00: 40 mV (Default)<br>01: 30 mV<br>10: 55 mV<br>11: 45 mV | | SD1 OFF Threshold Select<br>00: 40 mV (Default)<br>01: 30 mV<br>10: 55 mV<br>11: 45 mV | | SD0 OFF Threshold Select<br>00: 40 mV (Default)<br>01: 30 mV<br>10: 55 mV<br>11: 45 mV | |
| **SMBus Control** | 0x07 | 0x00 | RW | Reserved | | | | | | | SMBus Enable Control<br>0: Disable<br>1: Enable |
| **Output Level** | 0x08 | 0x78 | RW | Reserved | | | | Output Level:<br>00: 400 $mV_{P-P}$<br>01: 540 $mV_{P-P}$<br>10: 620 $mV_{P-P}$(Default)<br>11: 760 $mV_{P-P}$ | | Reserved | |

(1) RO = Read Only, RW = Read/Write


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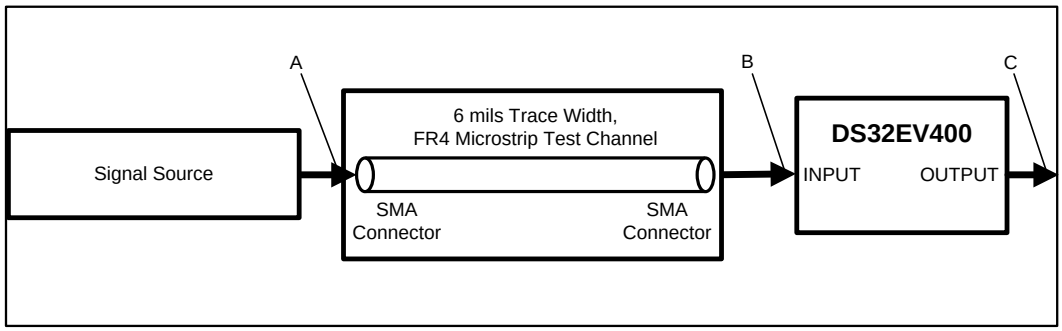



**Figure 1. Test Setup Diagram**

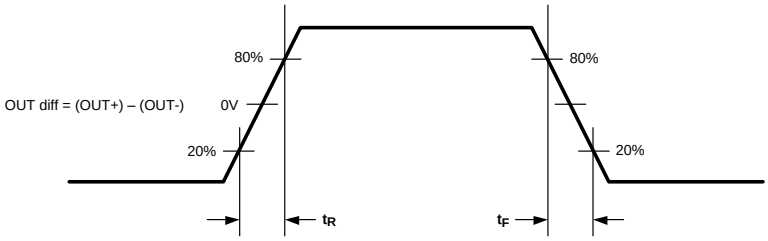



**Figure 2. CML Output Transition Times**

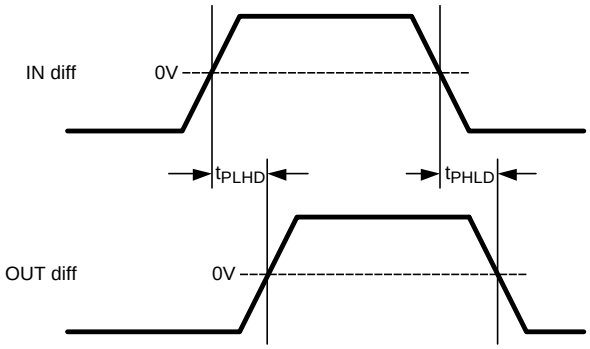



**Figure 3. Propagation Delay Timing Diagram**

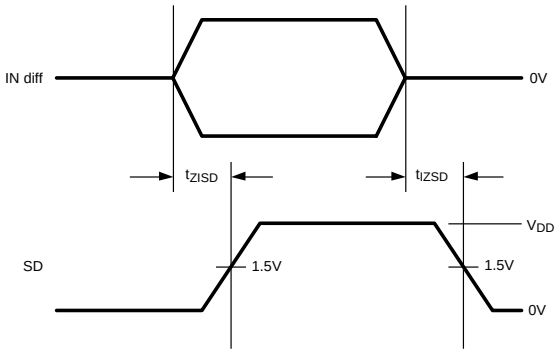



**Figure 4. Signal Detect (SD) Delay Timing Diagram**

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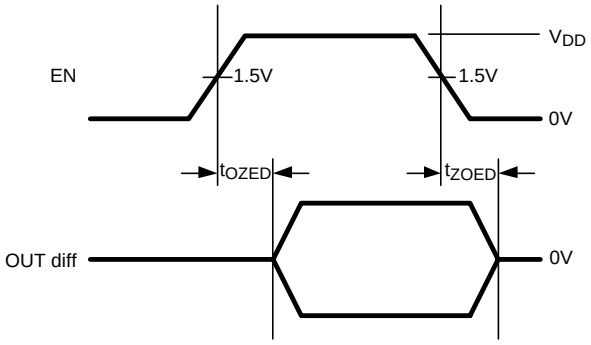



**Figure 5. Enable (EN) Delay Timing Diagram**

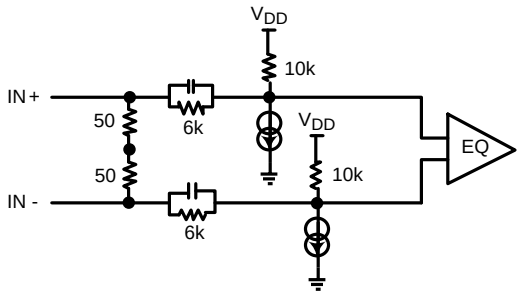



**Figure 6. Simplified Receiver Input Termination Circuit**

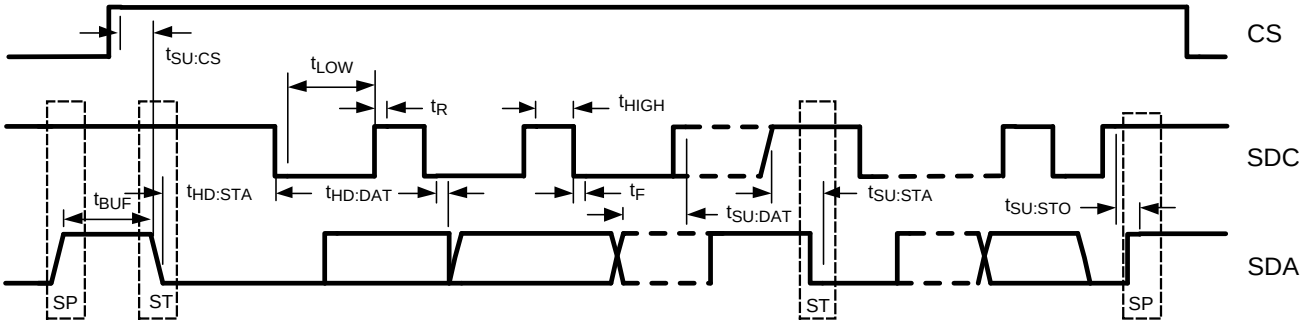



**Figure 7. SMBus Timing Parameters**


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## DS32EV400 FUNCTIONAL DESCRIPTIONS

The DS32EV400 is a programmable quad equalizer optimized for operation up to 3.2 Gbps for backplane and cable applications.

### DATA CHANNELS

The DS32EV400 provides four data channels. Each data channel consists of an equalizer stage, a limiting amplifier, a DC offset correction block, and a CML driver as shown in Figure 8.

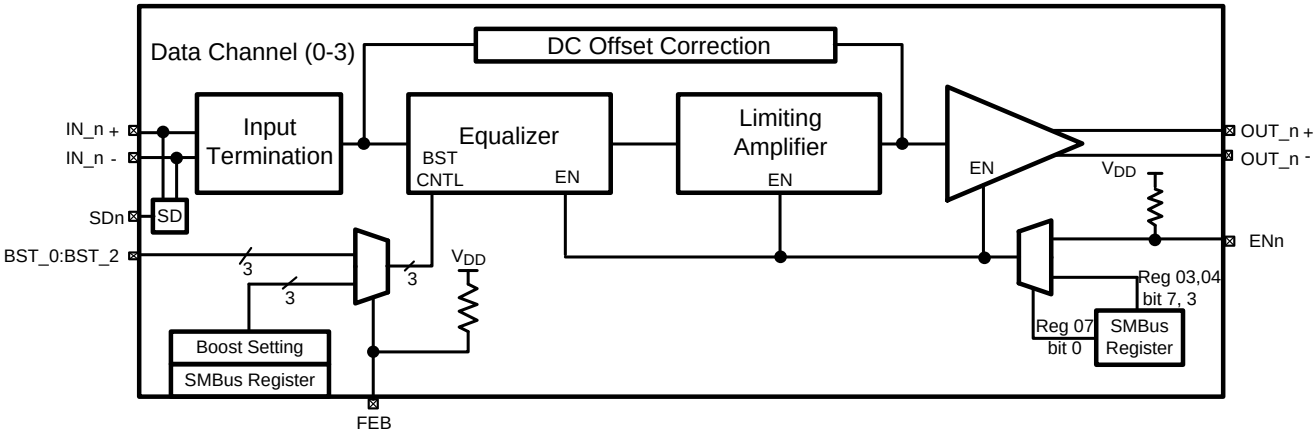



**Figure 8. Simplified Block Diagram**

### EQUALIZER BOOST CONTROL

Each data channel supports eight programmable levels of equalization boost. The state of the FEB pin determines how the boost settings are controlled. If the FEB pin is held High, then the equalizer boost setting is controlled by the Boost Set pins (BST_[2:0]) in accordance with Table 2. If this programming method is chosen, then the boost setting selected on the Boost Set pins is applied to all channels. When the FEB pin is held Low, the equalizer boost level is controlled through the SMBus. This programming method is accessed via the appropriate SMBus registers (see Table 1). Using this approach, equalizer boost settings can be programmed for each channel individually. FEB is internally pulled High (default setting); therefore if left unconnected, the boost settings are controlled by the Boost Set pins (BST_[2:0]). The eight levels of boost settings enables the DS32EV400 to address a wide range of media loss and data rates.

**Table 2. EQ Boost Control Table**

| 6 mil microstrip FR4 trace length (in) | 24 AWG Twin-AX cable length (m) | Channel Loss at 1.6 GHz (dB) | BST_N [2, 1, 0] |
|---|---|---|---|
| 0 | 0 | 0 | 0 0 0 |
| 5 | 2 | 3 | 0 0 1 |
| 10 | 3 | 6 | 0 1 0 |
| 15 | 4 | 7 | 0 1 1 |
| 20 | 5 | 8 | 1 0 0 (Default) |
| 25 | 6 | 10 | 1 0 1 |
| 30 | 7 | 12 | 1 1 0 |
| 40 | 10 | 14 | 1 1 1 |

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## DEVICE STATE AND ENABLE CONTROL

The DS32EV400 has an enable feature on each data channel which provides the ability to control device power consumption. This feature can be controlled either an Enable Pin (EN_n) with Reg 07 = 00'h (default value), or by the Enable Control Bit register which can be configured through the SMBus port (see Table 1 and Table 3 for detail register information), which require setting Reg 07 = 01'h and changing register value of Reg 03, 04. If the Enable is activated using either the external EN_n pin or SMBUS register, the corresponding data channel is placed in the ACTIVE state and all device blocks function as described. The DS32EV400 can also be placed in STANDBY mode to save power. In the STANDBY mode only the control interface including the SMBus port, as well as the signal detection circuit remain active.

**Table 3. Controlling Device State**

| Reg. 07 bit 0 | EN Pin (CMOS) | CH 0: Reg. 03 bit 3 CH 1: Reg. 03 bit 7 CH 2: Reg. 04 bit 3 CH 3: Reg. 04 bit 7 (EN Control) | Device State |
|---|---|---|---|
| 0 : Disable | 1 | X | ACTIVE |
| 0 : Disable | 0 | X | STANDBY |
| 1 : Enable | X | 0 | ACTIVE |
| 1 : Enable | X | 1 | STANDBY |

## SIGNAL DETECT

The DS32EV400 features a signal detect circuit on each data channel. The status of the signal of each channel can be determined by either reading the Signal Detect bit (SDn) in the SMBus registers (see Table 1) or by the state of each SDn pin. An output logic high indicates the presence of a signal that has exceeded the ON threshold value (called SD_ON). An output logic Low means that the input signal has fallen below the OFF threshold value (called SD_OFF). These values are programmed via the SMBus (Table 1). If not programmed via the SMBus, the thresholds take on the default values as shown in Table 4. The Signal Detect threshold values can be changed through the SMBus. All threshold values specified are DC peak-to-peak differential signals (positive signal minus negative signal) at the input of the device.

**Table 4. Signal Detect Threshold Values**

| Channel 0: Bit 1 Channel 1: Bit 3 Channel2: Bit 5 Channel 3: Bit 7 | Channel 0: Bit 0 Channel 1: Bit 2 Channel2: Bit 4 Channel 3: Bit 6 | SD_OFF Threshold Register 06 (mV) | SD_ON Threshold Register 05 (mV) |
|---|---|---|---|
| 0 | 0 | 40 (Default) | 70 (Default) |
| 0 | 1 | 30 | 55 |
| 1 | 0 | 55 | 90 |
| 1 | 1 | 45 | 75 |

## OUTPUT LEVEL CONTROL

The output amplitude of the CML drivers for each channel can be controlled via the SMBus (see Table 1). The default output level is 620 mVp-p. Table 5 presents the output level values supported:

**Table 5. Output Level Control Settings**

| All Channels: Bit 3 | All Channels: Bit 2 | Output Level Register 08 ($mV_{P-P}$) |
|---|---|---|
| 0 | 0 | 400 |
| 0 | 1 | 540 |
| 1 | 0 | 620 (Default) |
| 1 | 1 | 760 |


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### AUTOMATIC ENABLE FEATURE

It may be desirable to place unused channels in power-saving Standby mode. This can be accomplished by connecting the Signal detect (SDn) pin to the Enable (ENn) pin for each channel (See Figure 9). In order for this option to function properly, the register value for Reg. 07 should be 00'h (default value). If an input signal swing applied to a data channel is above the voltage level threshold as shown in Table 4, then the SDn output pin is asserted High. If the SDn pin is connected to the ENn pin, this will enable the equalizer, limiting amplifier, and output buffer on the data channels; thus the DS32EV400 will automatically enter the ACTIVE state. If the input signal swing falls below the SD_OFF threshold level, then the SDn output will be asserted Low, causing the channel to be placed in the STANDBY state.

**DS32EV400 APPLICATIONS INFORMATION**

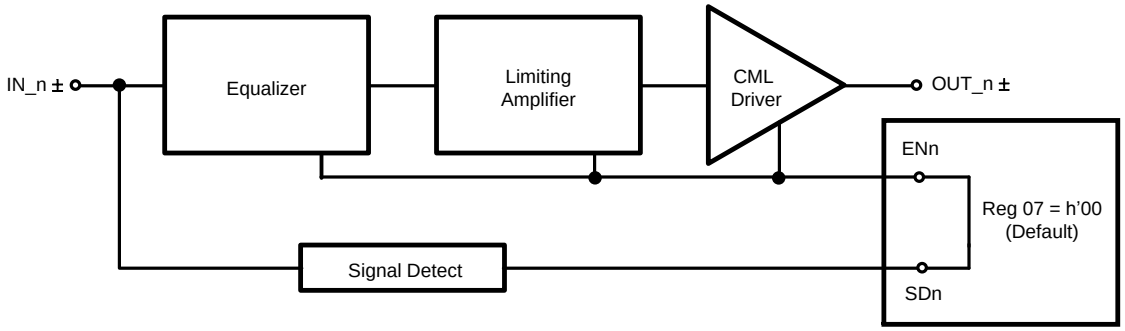



**Figure 9. Automatic Enable Configuration**

### DisplayPort™ Application

The DS32EV400 maybe used to extend the reach of the cable for DisplayPort applications. Typical DisplayPort cables are in the 6 meter range. With the DS32EV400 Equalizer, nominal cables may be doubled to 12 meters in length. The Quad devices supports 1, 2, or 4 channel applications.

The DS32EV400 is compatible with the high speed video channels of DisplayPort and can double the cable reach from six meters nominal to twelve meters. The DS32EV400 provides 20 dB of equalization at 3 Gbps and is well suited for the 2.7 Gbps DisplayPort application. Lengths up to 10 meters of 28 AWG can be supported on the input and 2 meters on the output for 12 meters total. The DisplayPort AUX channel is a low speed line and can be typically extended without the need of an equalizer. DisplayPort also provides 1.5W of power in the cable which can be used to power the DS32EV400. A single Channel version is also available (DS32EV100).

### UNUSED EQUALIZER CHANNELS

It is recommended to put all unused channels into standby mode.

### GENERAL RECOMMENDATIONS

The DS32EV400 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the LVDS Owner's Manual for more detailed information on high speed design tips to address signal integrity design issues.

### PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The CML inputs and outputs must have a controlled differential impedance of 100Ω. It is preferable to route CML lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Route the CML signals away from other signals and noise sources on the printed circuit board. See AN-1187 (SNOA401) for additional information on WQFN packages.

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## POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS32EV400 is provided with an adequate power supply. First, the supply ($V_{DD}$) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the $V_{DD}$ and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.01µF bypass capacitor should be connected to each $V_{DD}$ pin such that the capacitor is placed as close as possible to the DS32EV400. Smaller body size capacitors can help facilitate proper component placement. Additionally, three capacitors with capacitance in the range of 2.2 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic and should be placed as close as possible to the DS32EV400.

## DC COUPLING

The DS32EV400 supports both AC coupling with external ac coupling capacitor, and DC coupling to its upstream driver, or downstream receiver. With DC coupling, users must ensure the input signal common mode is within the range of the electrical specification $V_{ICMDC}$ and the device output is terminated with 50 Ω to $V_{DD}$. When power-up and power-down the device, both the DS32EV400 and the downstream receiver should be power-up and power-down together. This is to avoid the internal ESD structures at the output of the DS32EV400 at power-down from being turned on by the downstream receiver.


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## Typical Performance Eye Diagrams and Curves

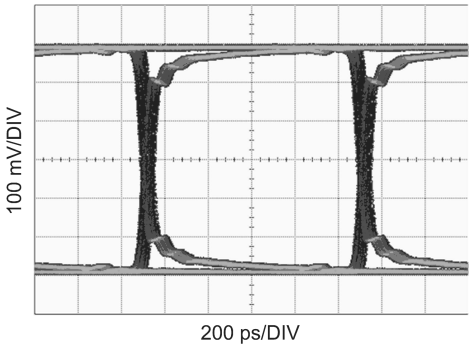



**Figure 10. Equalized Signal (40 In FR4, 1 Gbps, PRBS7, 0x07 Setting)**

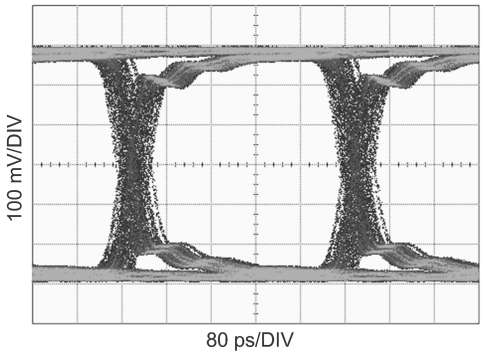



**Figure 11. Equalized Signal (40 In FR4, 2.5Gbps, PRBS7, 0x07 Setting)**

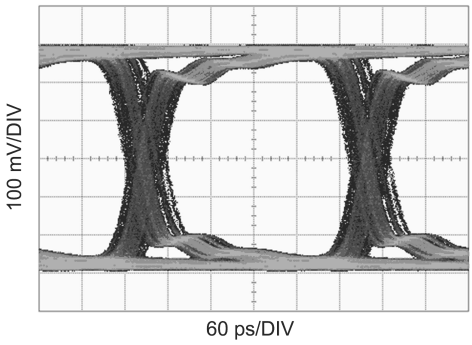



**Figure 12. Equalized Signal (40 In FR4, 3.2Gbps, PRBS7, 0x07 Setting)**

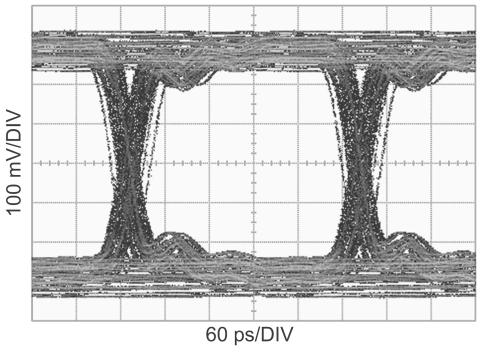



**Figure 13. Equalized Signal (10m 24 AWG Twin-AX Cable, 3.2 Gbps, PRBS7, 0x07 Setting)**

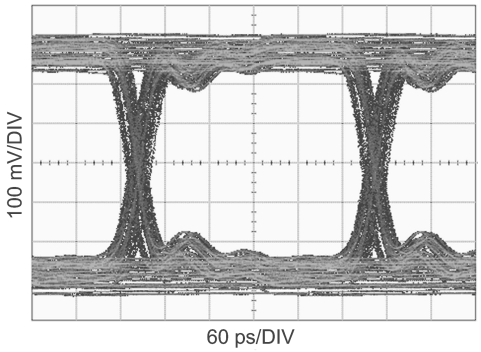



**Figure 14. Equalized Signal (32 In Tyco XAUI Backplane, 3.125 Gbps, PRBS7, 0x07 Setting)**

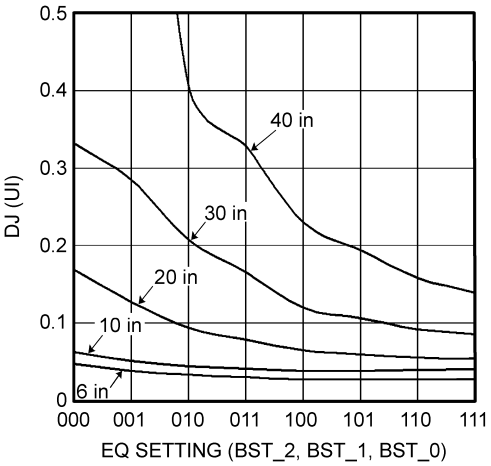



**Figure 15. DJ vs. EQ Setting (3.2 Gbps)**

## REVISION HISTORY

| Changes from Revision E (April 2013) to Revision F | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 17 |


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DS32EV400SQ/NOPB | ACTIVE | WQFN | NJU | 48 | 250 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | DS32EV400 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

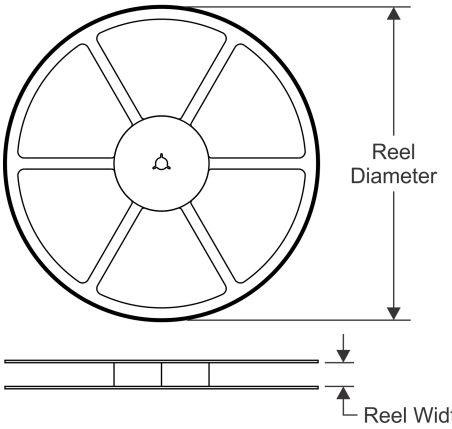
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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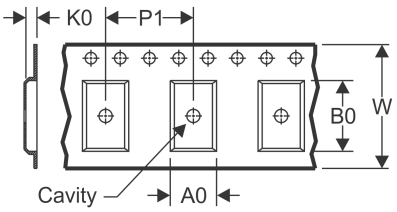
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**REEL DIMENSIONS**

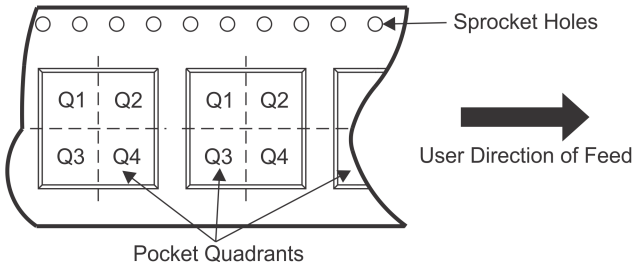



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

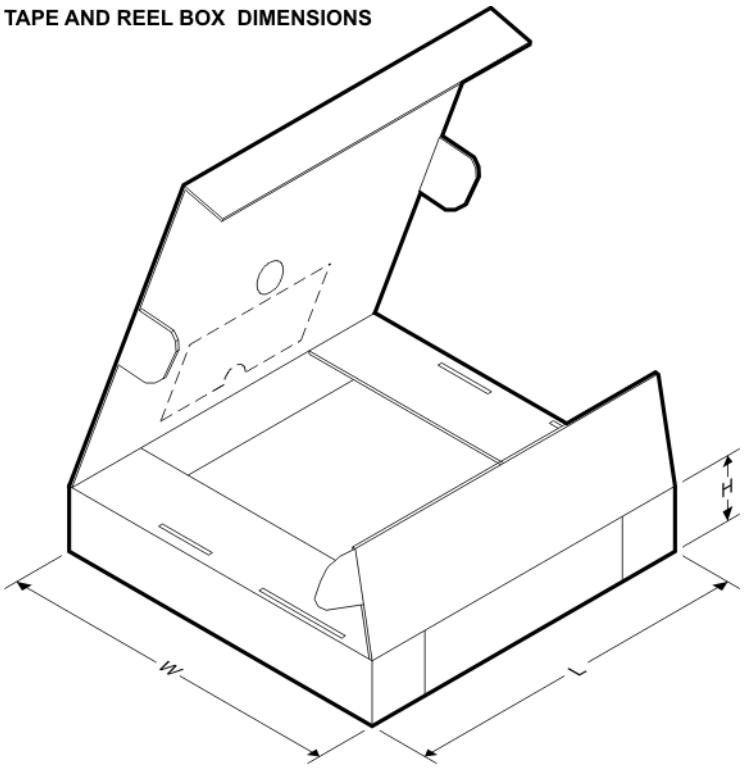
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DS32EV400SQ/NOPB | WQFN | NJU | 48 | 250 | 178.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |

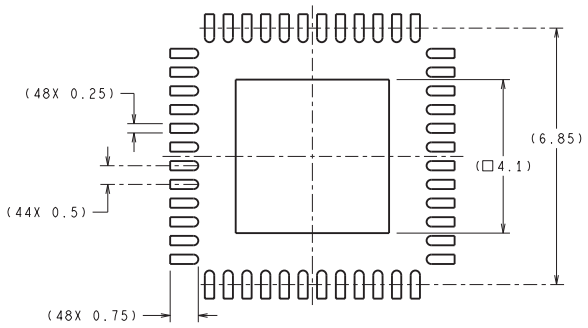
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

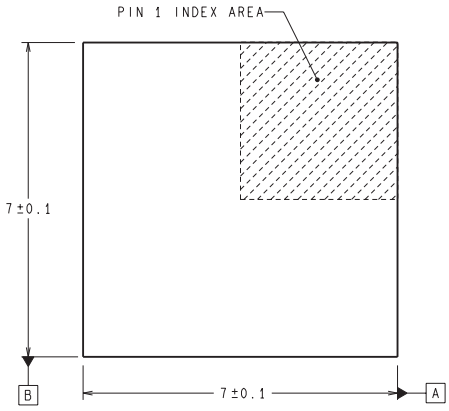
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DS32EV400SQ/NOPB | WQFN | NJU | 48 | 250 | 210.0 | 185.0 | 35.0 |

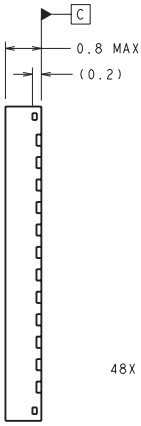
# NJU0048D

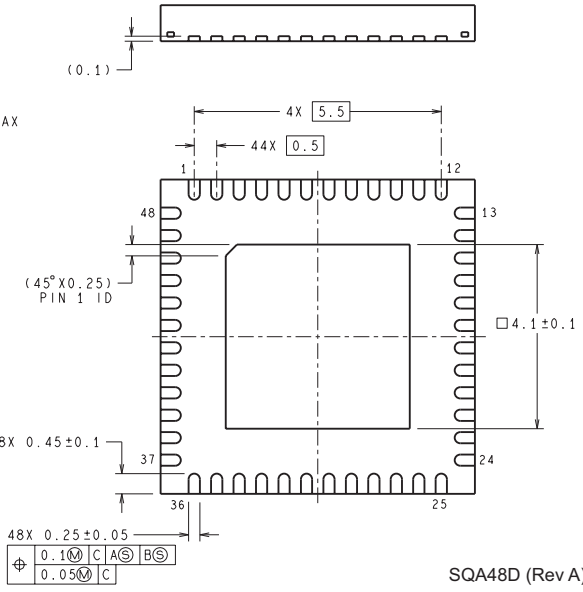



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SQA48D (Rev A)

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