FLATLINK™ TRANSMITTER

Check for Samples: SN75LVDS83C

FEATURES

- **LVDS Display Serdes Interfaces Directly to LCD Display Panels with Integrated LVDS**
- **Package: 4.5mm x 7mm BGA**
- **1.8V up to 3.3V Tolerant Data Inputs to Connect Directly to Low-Power, Low-Voltage Application and Graphic Processors**
- **Transfer Rate up to 85Mpps (Mega Pixel Per Second); Pixel Clock Frequency Range 10MHz to 85MHz**
- **Suited for Display Resolutions Ranging From HVGA up to HD With Low EMI**
- **Operates From a Single 3.3V Supply and 148mW (typical) at 75MHz**
- **28 Data Channels Plus Clock In Low-Voltage TTL to 4 Data Channels Plus Clock Out Low-Voltage Differential**
- **Consumes Less Than 1mW When Disabled**
- **Selectable Rising or Falling Clock Edge Triggered Inputs**
- **ESD: 5kV HBM**
- **Support Spread Spectrum Clocking (SSC)**

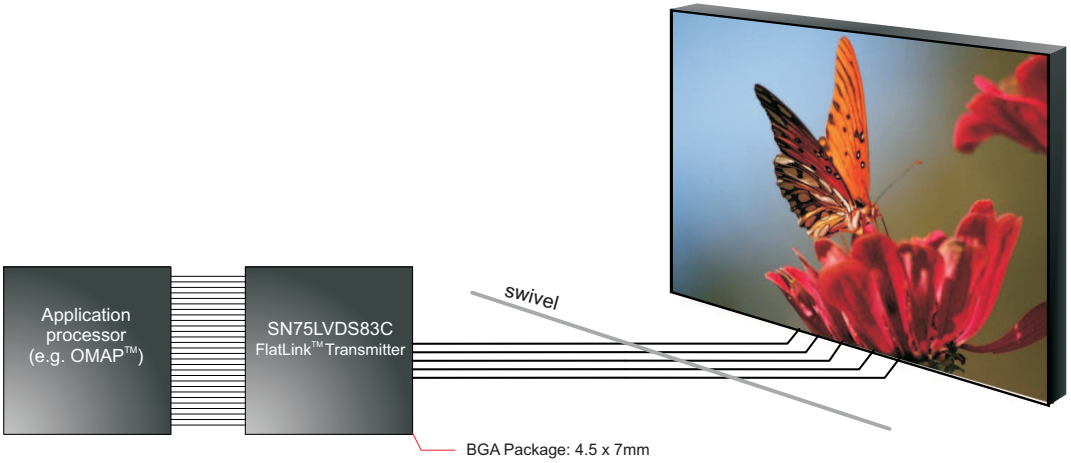
APPLICATIONS

- **LCD Display Panel Driver**
- **UMPC and Netbook PC**
- **Digital Picture Frame**

DESCRIPTION

The SN75LVDS83C FlatLink™ transmitter contains four 7-bit parallel-load serial-out shift registers, a 7X clock synthesizer, and five Low-Voltage Differential Signaling (LVDS) line drivers in a single integrated circuit. These functions allow 28 bits of single-ended LVTTL data to be synchronously transmitted over five balanced-pair conductors for receipt by a compatible receiver, such as the SN75LVDS82 and LCD panels with integrated LVDS receiver.

When transmitting, data bits D0 through D27 are each loaded into registers upon the edge of the input clock signal (CLKIN). The rising or falling edge of the clock can be selected via the clock select (CLKSEL) pin. The frequency of CLKIN is multiplied seven times, and then used to unload the data registers in 7-bit slices and serially. The four serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FlatLink is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The SN75LVDS83C requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user intervention is selecting a clock rising edge by inputting a high level to CLKSEL or a falling edge with a low-level input, and the possible use of the Shutdown/Clear (SHTDN). SHTDN is an active-low input to inhibit the clock, and shut off the LVDS output drivers for lower power consumption. A low-level on this signal clears all internal registers to a low-level.

The SN75LVDS83C is characterized for operation over ambient air temperatures of -10°C to 70°C.

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
SN75LVDS83CZQLR	LVDS83C in BGA package	56-pin ZQL LARGE Tape and Reel

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE		UNIT
		MIN	MAX	
Supply voltage range, VCC, IOVCC, LVDSVCC, PLLVCC(2)		-0.5	4	V
Voltage range at any output terminal		-0.5	VCC + 0.5	V
Voltage range at any input terminal		-0.5	IOVCC + 0.5	V
Continuous power dissipation		See the Thermal Information Table		
Storage temperature, T_s		–65	150	°C
ESD rating	Human Body Model (HBM)(3) all pins		5	kV
	Charged Device Model (CDM)(4) all pins		500	V
	Machine Model (MM)(5) all pins		150	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) All voltages are with respect to the GND terminals.
(3) In accordance with JEDEC Standard 22, Test Method A114-A.
(4) In accordance with JEDEC Standard 22, Test Method C101.
(5) In accordance with JEDEC Standard 22, Test Method A115-A.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, VCC		2.8	3.3	3.6	V
LVDS output Supply voltage, LVDSVCC		2.8	3.3	3.6	
PLL analog supply voltage, PLLVCC		2.8	3.3	3.6	
IO input reference supply voltage, IOVCC		1.62	1.8 / 2.5 / 3.3	3.6	
Power supply noise on any VCC terminal				0.1	
High-level input voltage, V_{IH}	IOVCC = 1.8V	IOVCC/2 + 0.3V			V
	IOVCC = 2.5V	IOVCC/2 + 0.4V			
	IOVCC = 3.3V	IOVCC/2 + 0.5V			
Low-level input voltage, V_{IL}	IOVCC = 1.8V			IOVCC/2 - 0.3V	V
	IOVCC = 2.5V			IOVCC/2 - 0.4V	
	IOVCC = 3.3V			IOVCC/2 - 0.5V	
Differential load impedance, Z_L		90		132	Ω
Operating free-air temperature, T_A		-10		70	C

THERMAL INFORMATION

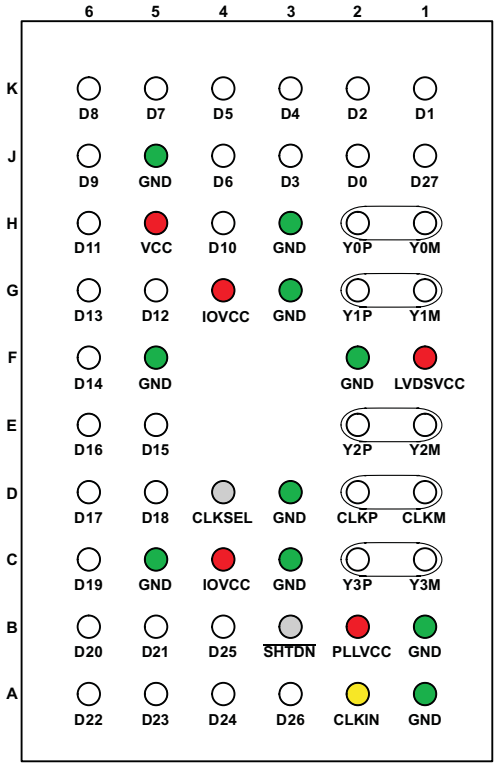
THERMAL METRIC(1)		SN75LVDS83C ZQL (56 PINS)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	67.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	25.2	°C/W
θ_{JB}	Junction-to-board thermal resistance	31.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.3	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

TIMING REQUIREMENTS

PARAMETER		MIN	MAX	UNIT
Input clock period, t_c		11.76	100	ns
Input clock modulation	with modulation frequency 30kHz		8%	
	with modulation frequency 50kHz		6%	
High-level input clock pulse width duration, t_w		0.4 t_c	0.6 t_c	ns
Input signal transition time, t_t			3	ns
Data set up time, D0 through D27 before CLKIN (See Figure 3)		2		ns
Data hold time, D0 through D27 after CLKIN		0.8		ns

ZQL PACKAGE
(TOP VIEW)



ZQL PIN LIST

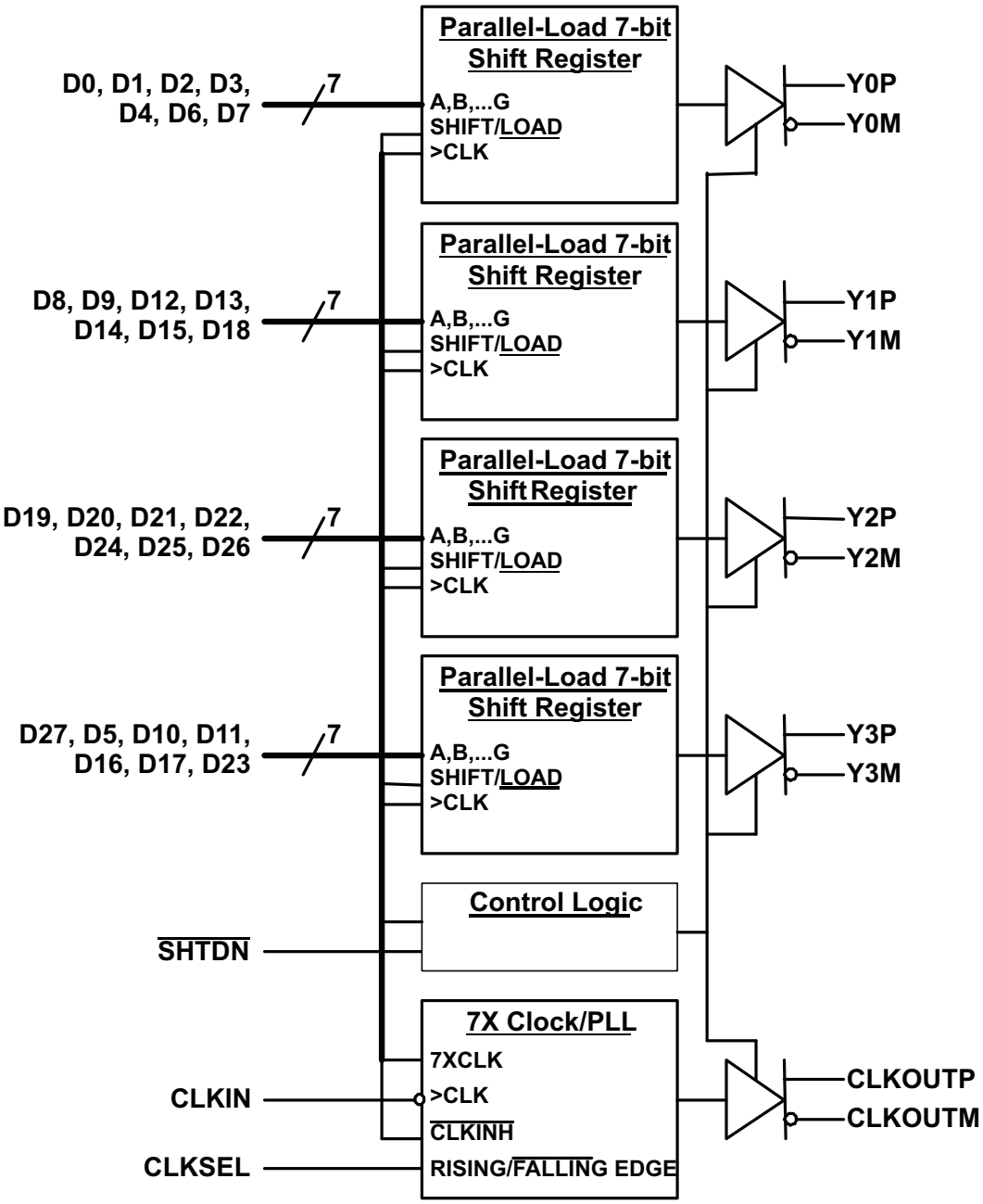
Ball #	Signal	Ball #	Signal	Ball #	Signal
A1	GND	A2	CLKIN	A3	D26
A4	D24	A5	D23	A6	D22
B1	GND	B2	PLLVCC	B3	$\overline{\text{SHTDN}}$
B4	D25	B5	D21	B6	D20
C1	Y3M	C2	Y3P	C3	GND
C4	IOVCC	C5	GND	C6	D19
D1	CLKM	D2	CLKP	D3	GND
D4	CLKSEL	D5	D18	D6	D17
E1	Y2M	E2	Y2P	E3	ball not populated
E4	ball not populated	E5	D15	E6	D16
F1	LVDSVCC	F2	GND	F3	ball not populated
F4	ball not populated	F5	GND	F6	D14
G1	Y1M	G2	Y1P	G3	GND
G4	IOVCC	G5	D12	G6	D13
H1	Y0M	H2	Y0P	H3	GND
H4	D10	H5	VCC	H6	D11
J1	D27	J2	D0	J3	D3
J4	D6	J5	GND	J6	D9
K1	D1	K2	D2	K3	D4
K4	D5	K5	D7	K6	D8

PIN FUNCTIONS

PIN	I/O	DESCRIPTION
Y0P, Y0M, Y1P, Y1M, Y2P, Y2M	LVDS Out	Differential LVDS data outputs. Outputs are high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted)
Y3P, Y3M		Differential LVDS Data outputs. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted). Note: if the application only requires 18-bit color, this output can be left open.
CLKP, CLKM		Differential LVDS pixel clock output. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted).
D0 – D27	CMOS IN with pulldn	Data inputs; supports 1.8V to 3.3V input voltage selectable by VDD supply. To connect a graphic source successfully to a display, the bit assignment of D[27:0] is critical (and not necessarily intuitive). For input bit assignment see Figure 11 to Figure 14 for details. Note: if application only requires 18-bit color, connect unused inputs D5, D10, D11, D16, D17, D23, and D27 to GND.
CLKIN		Input pixel clock; rising or falling clock polarity is selectable by Control input CLKSEL.
$\overline{\text{SHTDN}}$		Device shut down; pull low (de-assert) to shut down the device (low power, resets all registers) and high (assert) for normal operation.
CLKSEL		Selects between rising edge input clock trigger (CLKSEL = V_{IH} and falling edge input clock trigger (CLKSEL = V_{IL}).
VCC	Power Supply(1)	3.3V digital supply voltage
IOVCC		I/O supply reference voltage (1.8V up to 3.3V matching the GPU data output signal swing)
PLLVCC		3.3V PLL analog supply
LVDSVCC		3.3V LVDS output analog supply
GND		Supply ground for VCC, IOVCC, LVDSVCC, and PLLVCC.

(1) For a multilayer pcb, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

FUNCTIONAL BLOCK DIAGRAM



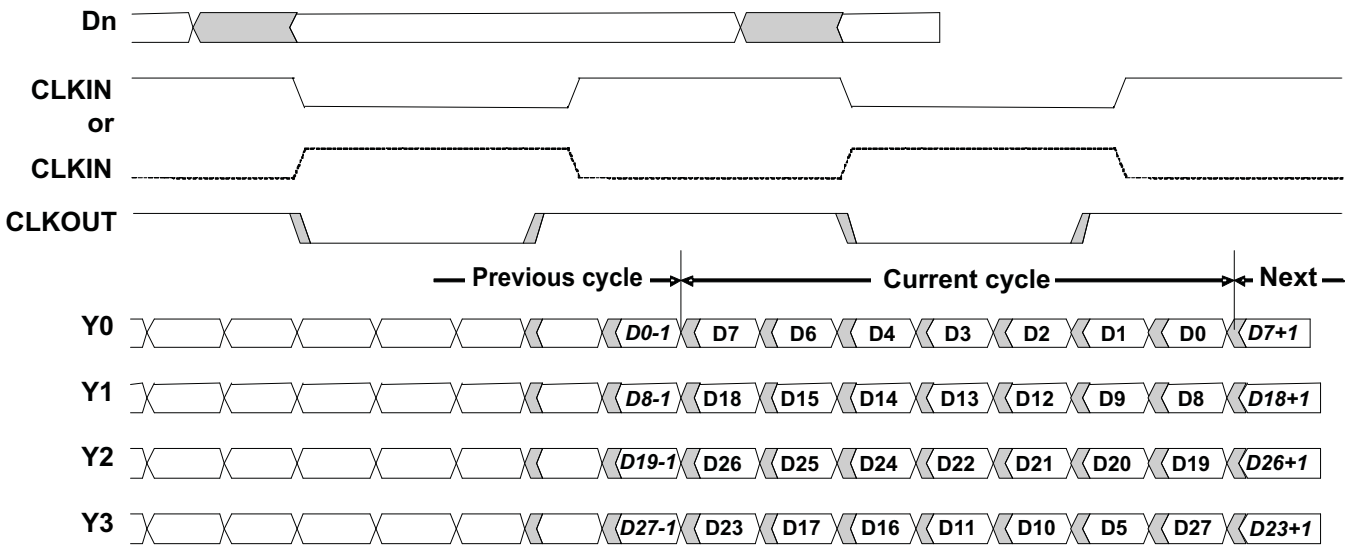


Figure 1. Typical SN75LVDS83C Load and Shift Sequences

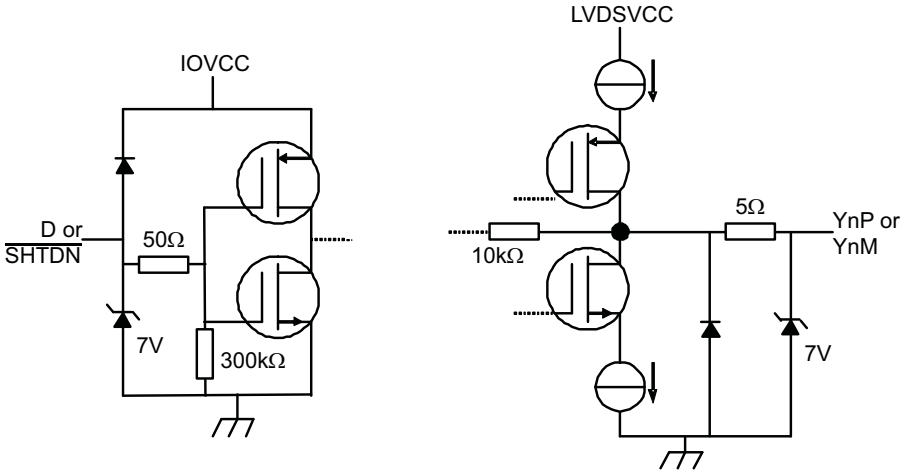


Figure 2. Equivalent Input and Output Schematic Diagrams

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_T	Input voltage threshold	R_L = 100Ω, See Figure 4		IOVCC/2		V
$\|V_{OD}\|$	Differential steady-state output voltage magnitude		250		450	mV
$\Delta\|V_{OD}\|$	Change in the steady-state differential output voltage magnitude between opposite binary states			1	35	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 4 $t_{R/F}$ (Dx, CLKin) = 1ns	1.125		1.375	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				35	mV
I_{IH}	High-level input current	V_{IH} = IOVCC			25	µA
I_{IL}	Low-level input current	V_{IL} = 0 V			±10	µA
I_{OS}	Short-circuit output current	V_{OY} = 0 V			±24	mA
		V_{OD} = 0 V			±12	mA
I_{OZ}	High-impedance state output current	V_O = 0 V to VCC			±20	µA
R_{pdn}	Input pull-down integrated resistor on all inputs (Dx, CLKSEL, $\overline{SHTDN}$, CLKIN)	IOVCC = 1.8V		200		kΩ
		IOVCC = 3.3V		100		
I_Q	Quiescent current (average)	disabled, all inputs at GND; $\overline{SHTDN}$ = V_{IL}		2	100	µA
I_{CC}	Supply current (average)	$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), grayscale pattern (Figure 5) VCC = 3.3V, f_{CLK} = 75MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		44.9		mA
		$I_{(IOVCC)}$ with IOVCC = 1.8V		0.1		
		$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), worst-case pattern (Figure 6), VCC = 3.3V, f_{CLK} = 75MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		55.1		mA
		$I_{(IOVCC)}$ with IOVCC = 1.8V		0.5		
C_I	Input capacitance			2		pF

(1) All typical values are at VCC = 3.3V, T_A = 25°C.

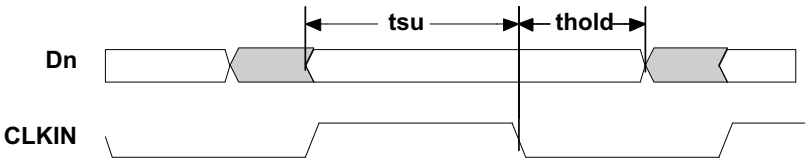
SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_0	Delay time, CLKOUT↑ after Yn valid (serial bit position 0, equal D1, D9, D20, D5)	See Figure 7, t_C = 13.3ns, |Input clock jitter| < 25ps (2)	-0.15	0	0.15	ns
t_1	Delay time, CLKOUT↑ after Yn valid (serial bit position 1, equal D0, D8, D19, D27)		$^1/_7$ t_c - 0.15		$^1/_7$ t_c + 0.15	ns
t_2	Delay time, CLKOUT↑ after Yn valid (serial bit position 2, equal D7, D18, D26. D23)		$^2/_7$ t_c - 0.15		$^2/_7$ t_c + 0.15	ns
t_3	Delay time, CLKOUT↑ after Yn valid (serial bit position 3; equal D6, D15, D25, D17)		$^3/_7$ t_c - 0.15		$^3/_7$ t_c + 0.15	ns
t_4	Delay time, CLKOUT↑ after Yn valid (serial bit position 4, equal D4, D14, D24, D16)		$^4/_7$ t_c - 0.15		$^4/_7$ t_c + 0.15	ns
t_5	Delay time, CLKOUT↑ after Yn valid (serial bit position 5, equal D3, D13, D22, D11)		$^5/_7$ t_c - 0.15		$^5/_7$ t_c + 0.15	ns
t_6	Delay time, CLKOUT↑ after Yn valid (serial bit position 6, equal D2, D12, D21, D10)		$^6/_7$ t_c - 0.15		$^6/_7$ t_c + 0.15	ns
$t_{c(o)}$	Output clock period			t_c		ns
$\Delta t_{c(o)}$	Output clock cycle-to-cycle jitter (3)	t_C = 13.3ns; clean reference clock, see Figure 8		±26		ps
		t_C = 13.3ns with 0.05UI added noise modulated at 3MHz, see Figure 8		±44		
t_w	High-level output clock pulse duration			$^4/_7$ t_c		ns
$t_{r/f}$	Differential output voltage transition time (t_r or t_f)	See Figure 4	200	250	800	ps
t_{en}	Enable time, $\overline{SHTDN}$↑ to phase lock (Yn valid)	$f_{(clk)}$ = 85MHz, See Figure 9			15	µs
t_{dis}	Disable time, $\overline{SHTDN}$↓ to off-state (CLKOUT high-impedance)	$f_{(clk)}$ = 85MHz, See Figure 10			13	ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) |Input clock jitter| is the magnitude of the change in the input clock period.
(3) The output clock cycle-to-cycle jitter is the largest recorded change in the output clock period from one cycle to the next cycle observed over 15,000 cycles.Tektronix TDSJIT3 Jitter Analysis software was used to derive the maximum and minimum jitter value.

PARAMETER MEASUREMENT INFORMATION



All input timing is defined at IOVDD / 2 on an input signal with a 10% to 90% rise or fall time of less than 3 ns. CLKSEL = 0V.

Figure 3. Set Up and Hold Time Definition

PARAMETER MEASUREMENT INFORMATION (continued)

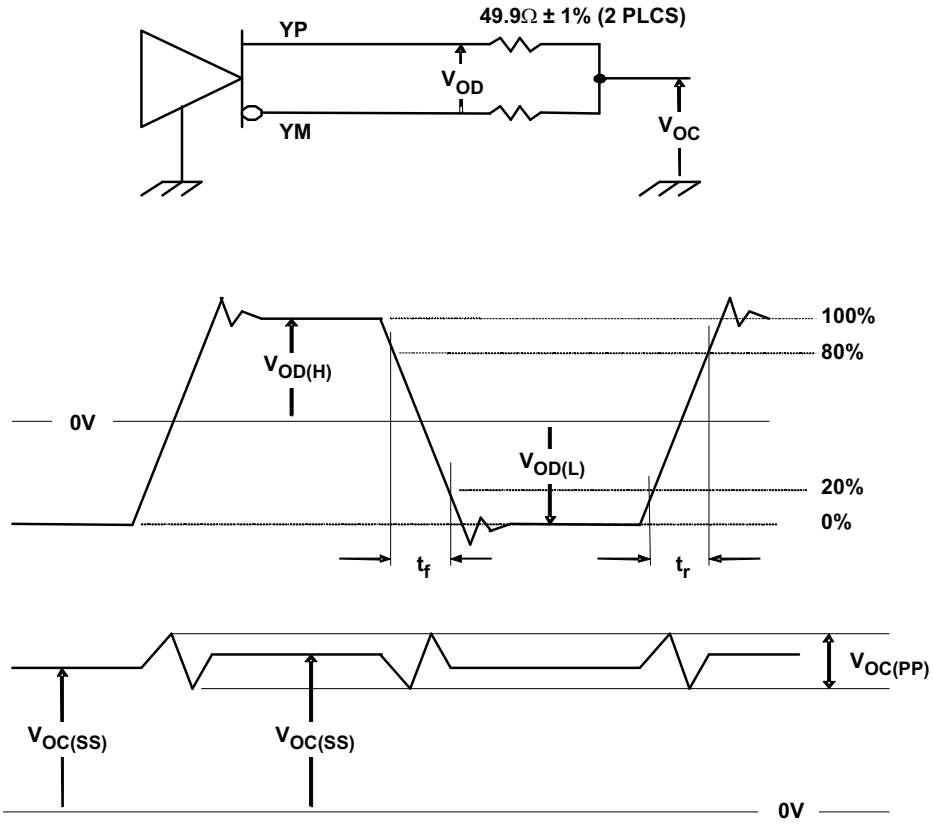
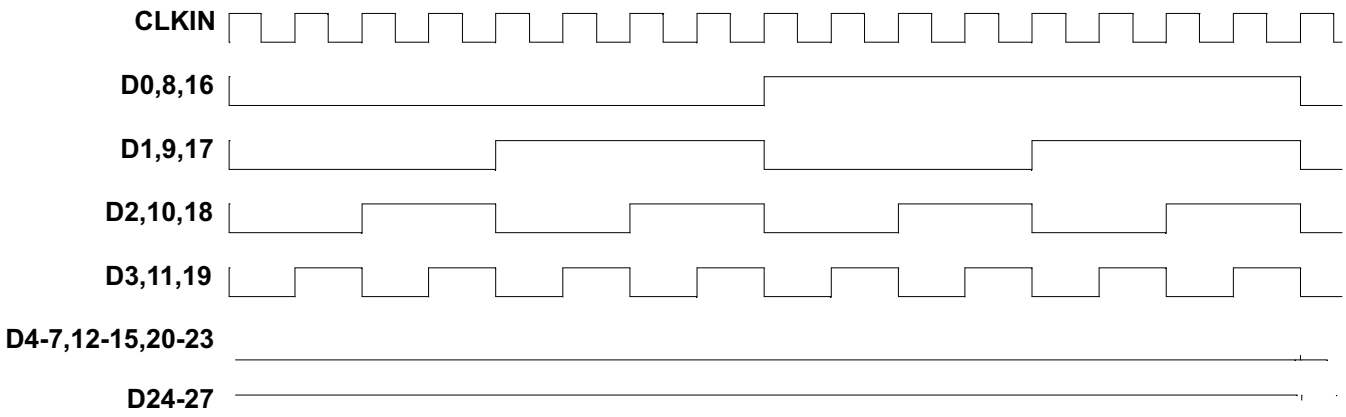


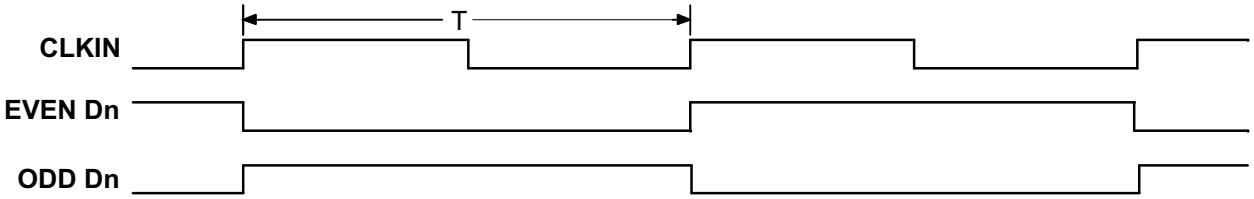
Figure 4. Test Load and Voltage Definitions for LVDS Outputs.



The 16 grayscale test pattern test device power consumption for a typical display pattern.

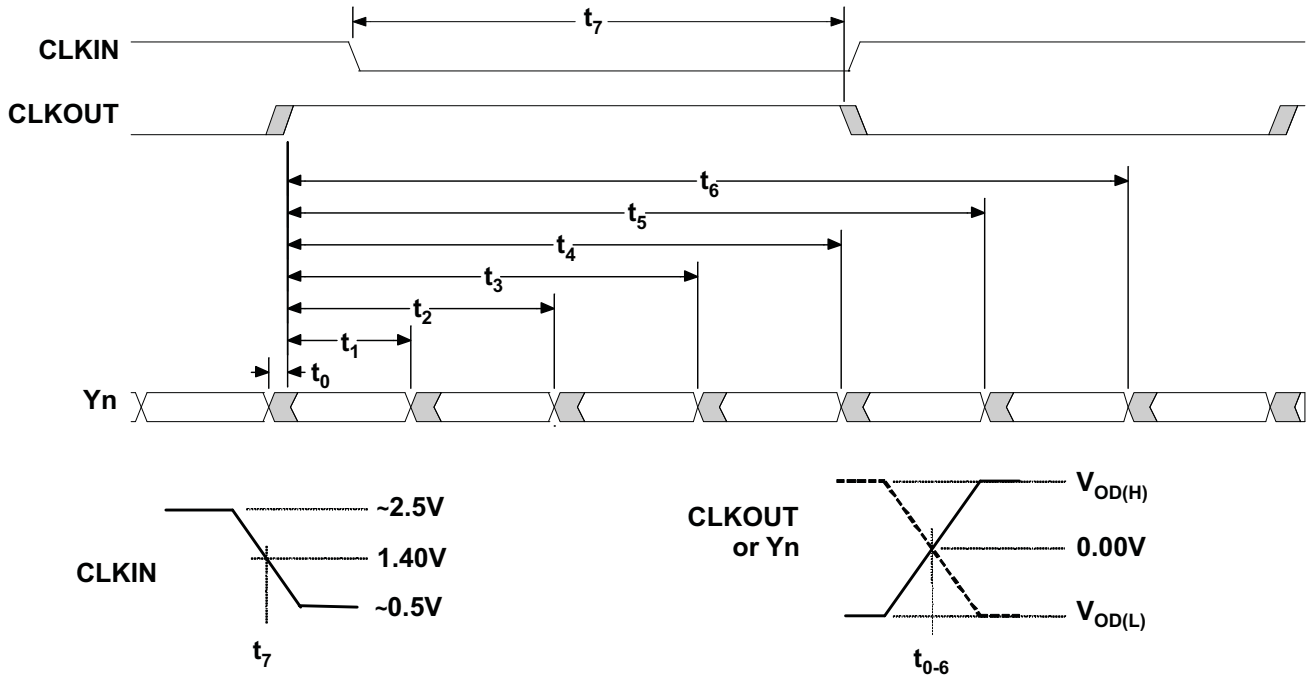
Figure 5. 16 Grayscale Test Pattern

PARAMETER MEASUREMENT INFORMATION (continued)



The worst-case test pattern produces nearly the maximum switching frequency for all of the LVDS outputs.

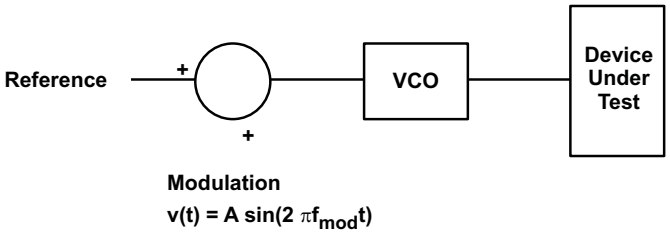
Figure 6. Worst-Case Power Test Pattern



CLKOUT is shown with CLKSEL at high-level.
CLKIN polarity depends on CLKSEL input level.

Figure 7. SN75LVDS83C Timing Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



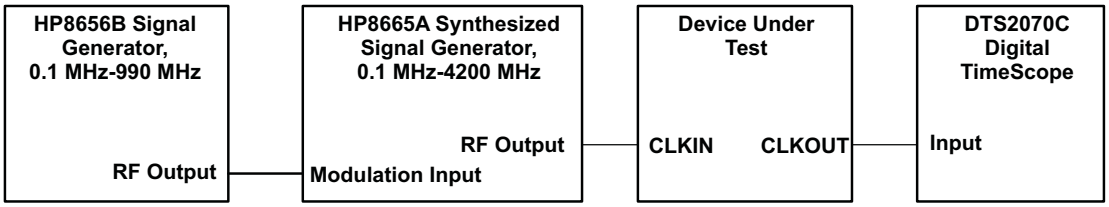


Figure 8. Output Clock Jitter Test Set Up

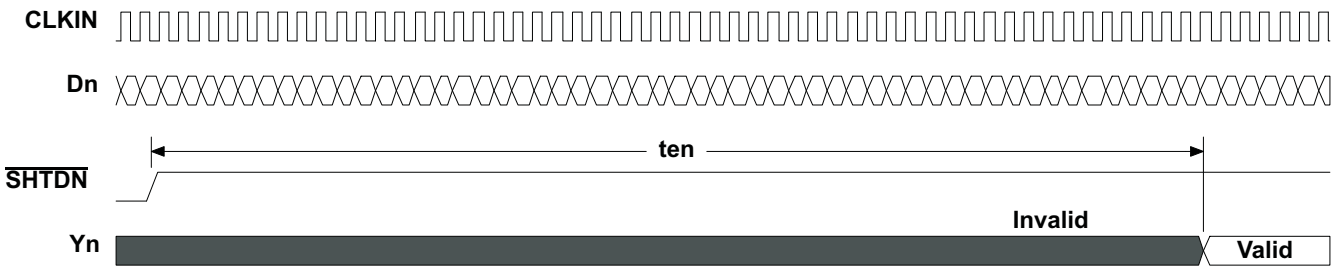


Figure 9. Enable Time Waveforms

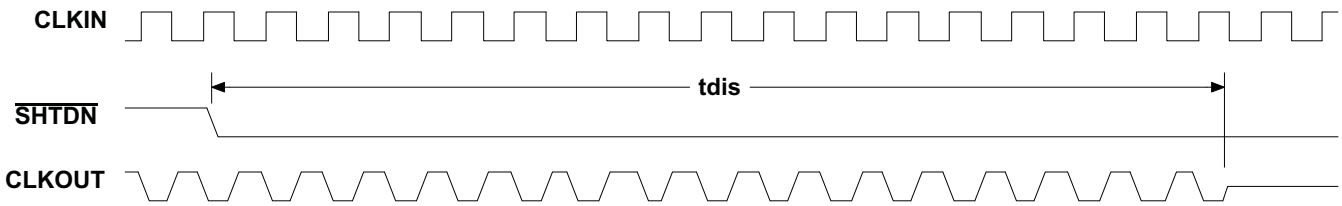


Figure 10. Disable Time Waveforms

APPLICATION INFORMATION

This section describes the power up sequence, provides information on device connectivity to various GPU and LCD display panels, and offers a pcb routing example.

Power Up Sequence

The SN75LVDS83C does not require a specific power up sequence.

It is permitted to power up IOVCC while VCC, VCCPLL, and VCCLVDS remain powered down and connected to GND. The input level of the $\overline{SHTDN}$ during this time does not matter as only the input stage is powered up while all other device blocks are still powered down.

It is also permitted to power up all 3.3V power domains while IOVCC is still powered down to GND. The device will not suffer damage. However, in this case, all the I/Os are detected as logic HIGH, regardless of their true input voltage level. Hence, connecting $\overline{SHTDN}$ to GND will still be interpreted as a logic HIGH; the LVDS output stage will turn on. The power consumption in this condition is significantly higher than standby mode, but still lower than normal mode.

The user experience can be impacted by the way a system powers up and powers down an LCD screen. The following sequence is recommended:

Power up sequence (SN75LVDS83C $\overline{SHTDN}$ input initially low):

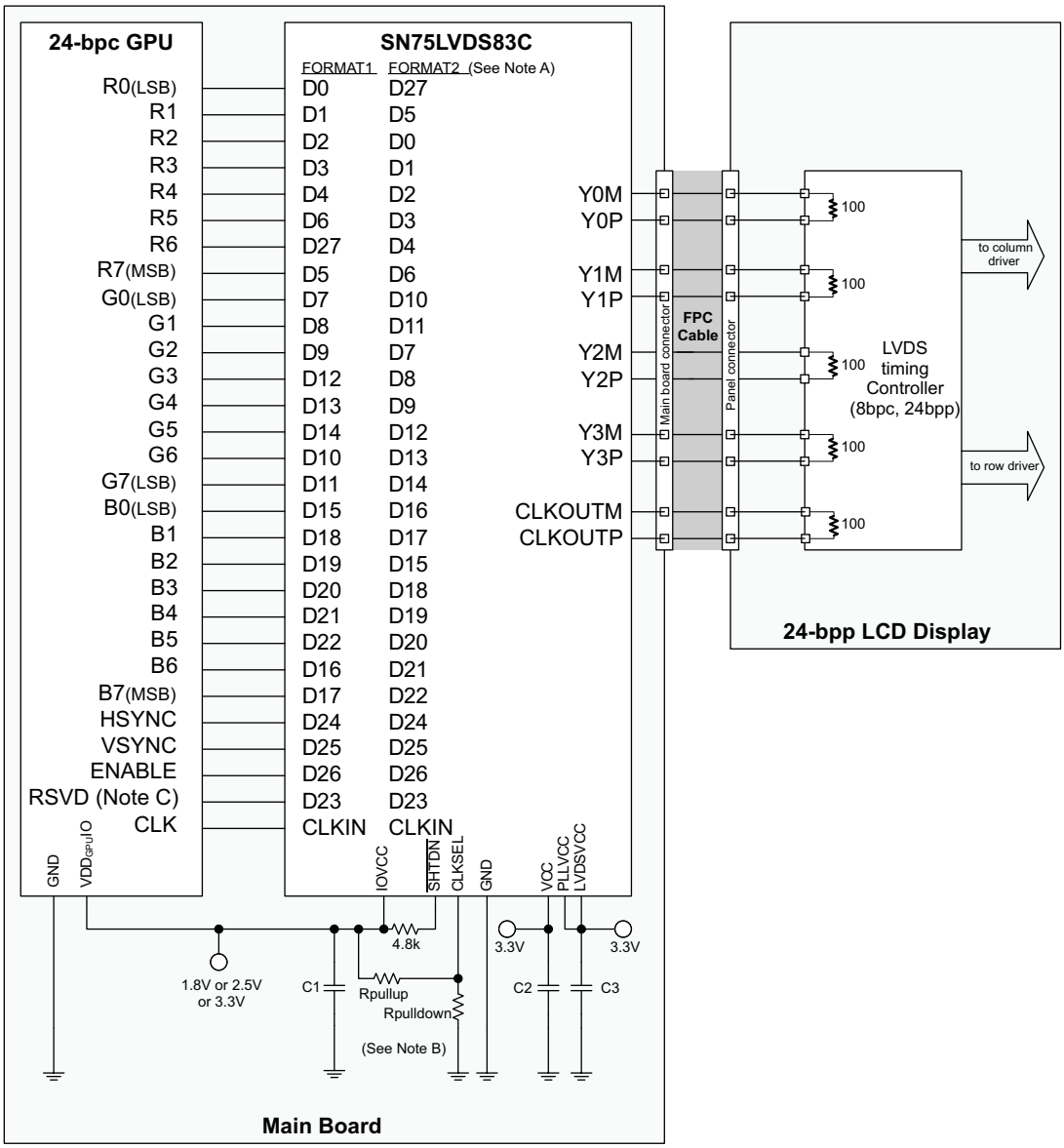
1. Ramp up LCD power (maybe 0.5ms to 10ms) but keep backlight turned off.
2. Wait for additional 0-200ms to ensure display noise won't occur.
3. Enable video source output; start sending black video data.
4. Toggle LVDS83C shutdown to $\overline{SHTDN} = V_{IH}$.
5. Send >1ms of black video data; this allows the LVDS83C to be phase locked, and the display to show black data first.
6. Start sending true image data.
7. Enable backlight.

Power Down sequence (SN75LVDS83C $\overline{SHTDN}$ input initially high):

1. Disable LCD backlight; wait for the minimum time specified in the LCD data sheet for the backlight to go low.
2. Video source output data switch from active video data to black image data (all visible pixel turn black); drive this for >2 frame times.
3. Set SN75LVDS83C input $\overline{SHTDN}$ = GND; wait for 250ns.
4. Disable the video output of the video source.
5. Remove power from the LCD panel for lowest system power.

Signal Connectivity

While there is no formal industry standardized specification for the input interface of LVDS LCD panels, the industry has aligned over the years on a certain data format (bit order). Figure 11 through Figure 14 show how each signal should be connected from the graphic source through the SN75LVDS83C input, output and LVDS LCD panel input. Detailed notes are provided with each figure.



Note A. **FORMAT**: The majority of 24-bit LCD display panels require the two most significant bits (2 MSB) of each color to be transferred over the 4th serial data output Y3. A few 24-bit LCD display panels require the two LSBs of each color to be transmitted over the Y3 output. The system designer needs to verify which format is expected by checking the LCD display data sheet.

- Format 1: use with displays expecting the 2 MSB to be transmitted over the 4th data channel Y3. This is the dominate data format for LCD panels.
- Format 2: use with displays expecting the 2 LSB to be transmitted over the 4th data channel.

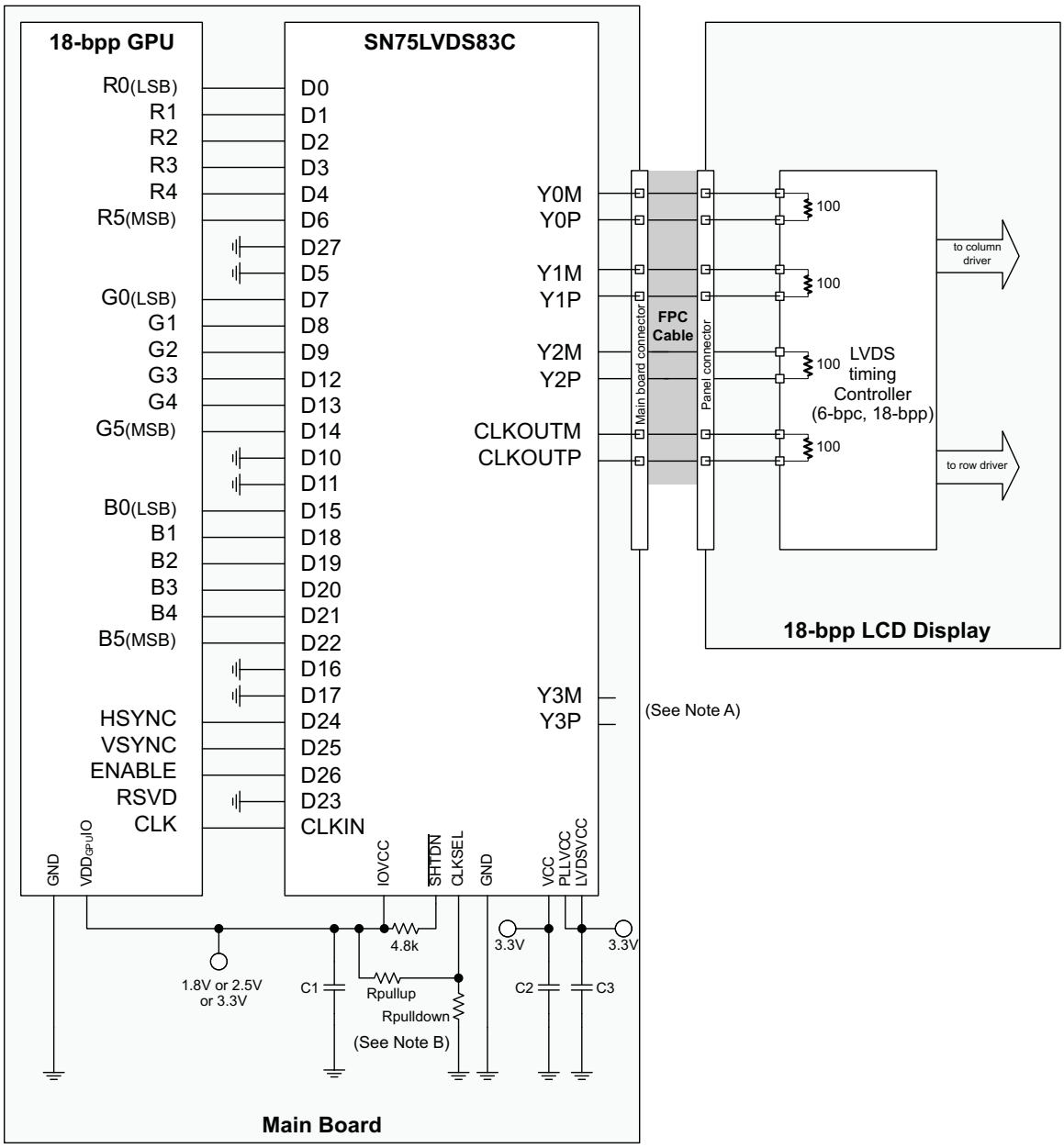
Note B. **Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

- C1: decoupling cap for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling cap for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling cap for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Note C. If RSVD is not driven to a valid logic level, then an external connection to GND is recommended.

Note D. RSVD must be driven to a valid logic level. All unused SN75LVDS83C inputs must be tied to a valid logic level.

Figure 11. 24-Bit Color Host to 24-bit LCD Panel Application

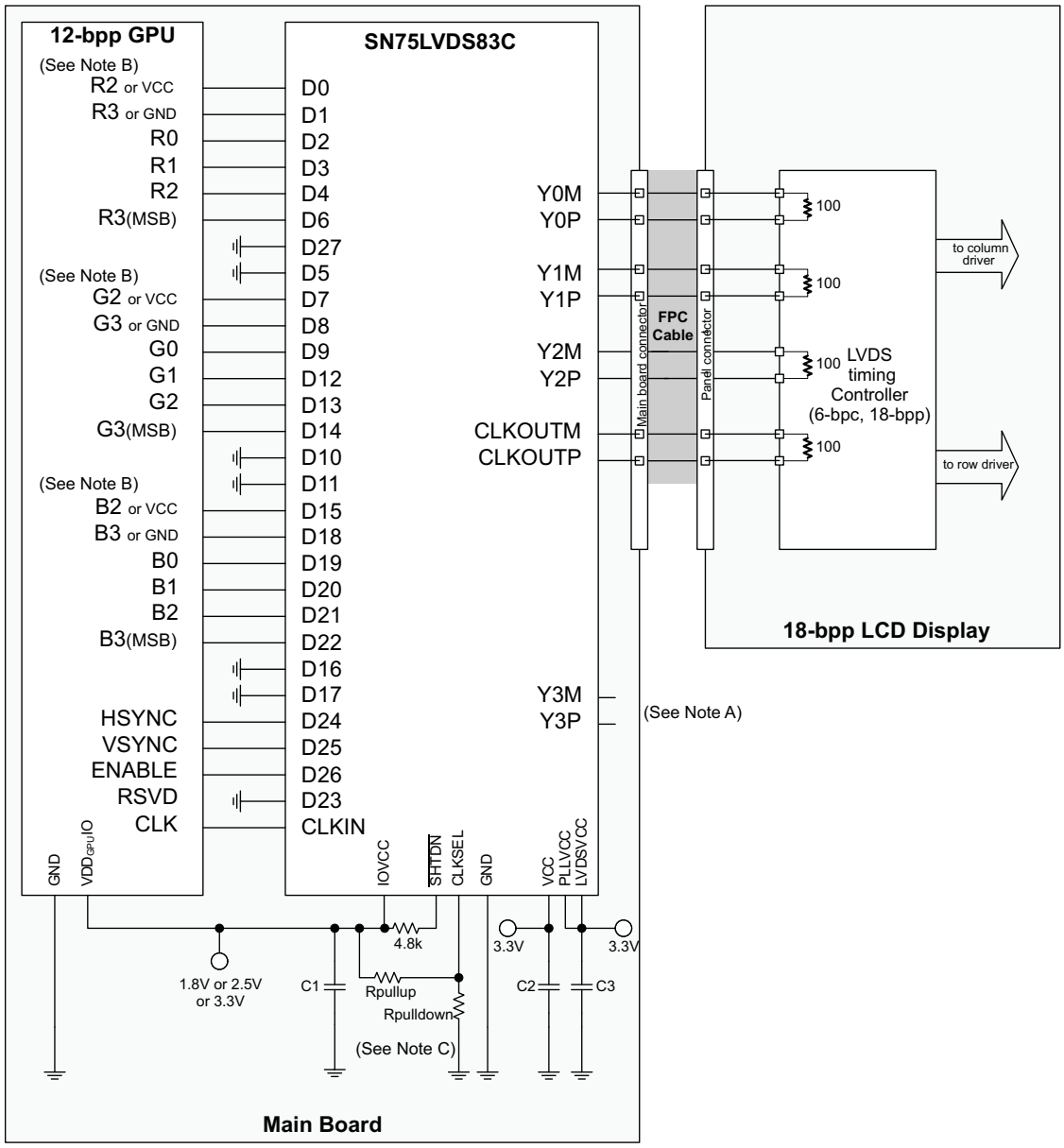


Note A. Leave output Y3 NC.

Note B.**Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

- C1: decoupling cap for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling cap for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling cap for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Figure 12. 18-Bit Color Host to 18-Bit Color LCD Panel Display Application



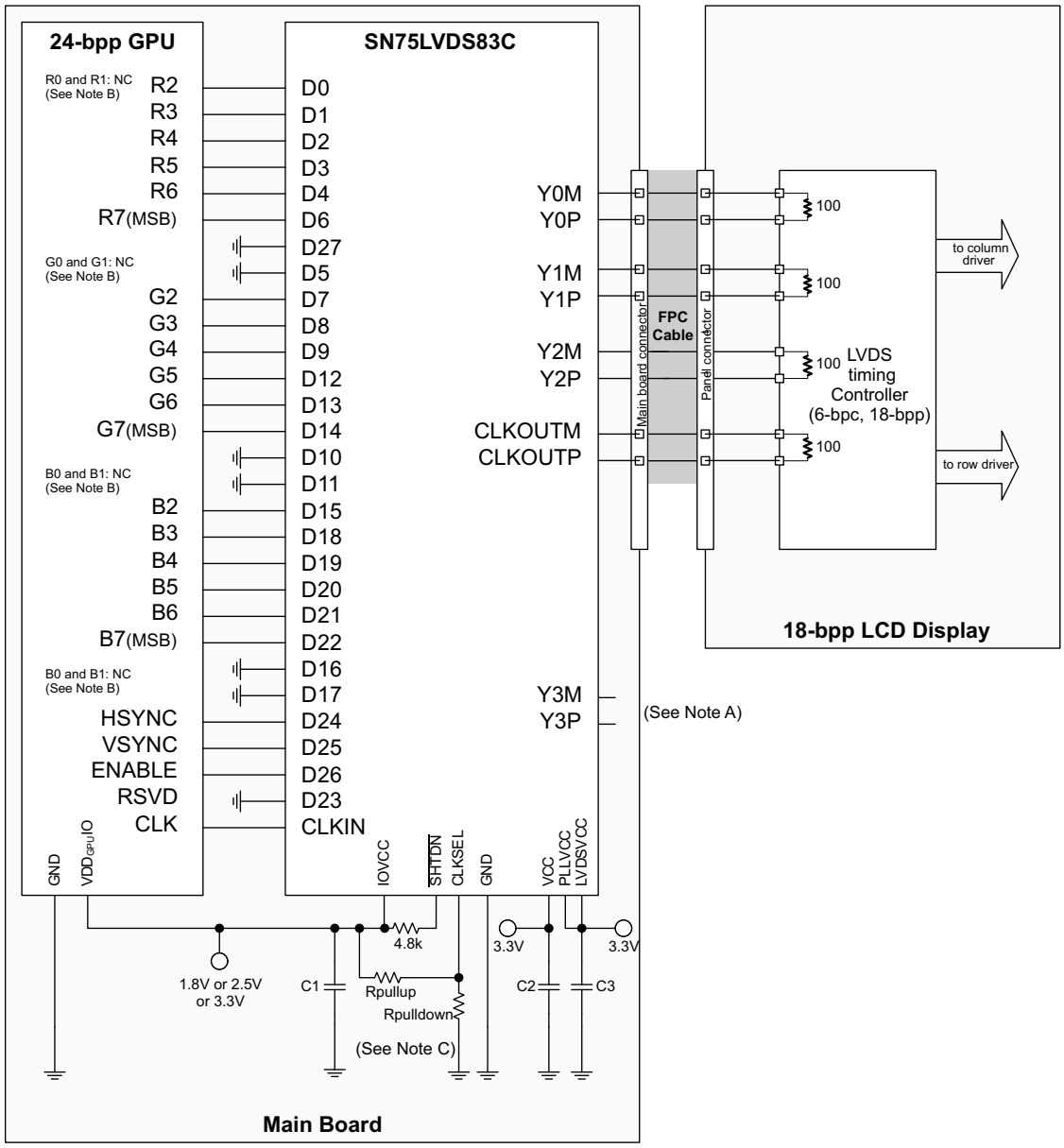
Note A. Leave output Y3 N.C.

Note B. **R3, G3, B3**: this MSB of each color also connects to the 5th bit of each color for increased dynamic range of the entire color space at the expense of none-linear step sizes between each step. For linear steps with less dynamic range, connect D1, D8, and D18 to GND.
R2, G2, B2: these outputs also connects to the LSB of each color for increased, dynamic range of the entire color space at the expense of none-linear step sizes between each step. For linear steps with less dynamic range, connect D0, D7, and D15 to VCC.

Note C.**Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

- C1: decoupling cap for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling cap for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling cap for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Figure 13. 12-Bit Color Host to 18-Bit Color LCD Panel Display Application



Note A. Leave output Y3 NC.

Note B. **R0, R1, G0, G1, B0, B1**: For improved image quality, the GPU should dither the 24-bit output pixel down to18-bit per pixel.

NoteC.**Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

- C1: decoupling cap for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling cap for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling cap for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Figure 14. 24-Bit Color Host to 18-Bit Color LCD Panel Display Application

Typical Application Schematic

Figure 15 represents the schematic drawing of the SN75LVDS83C evaluation module.

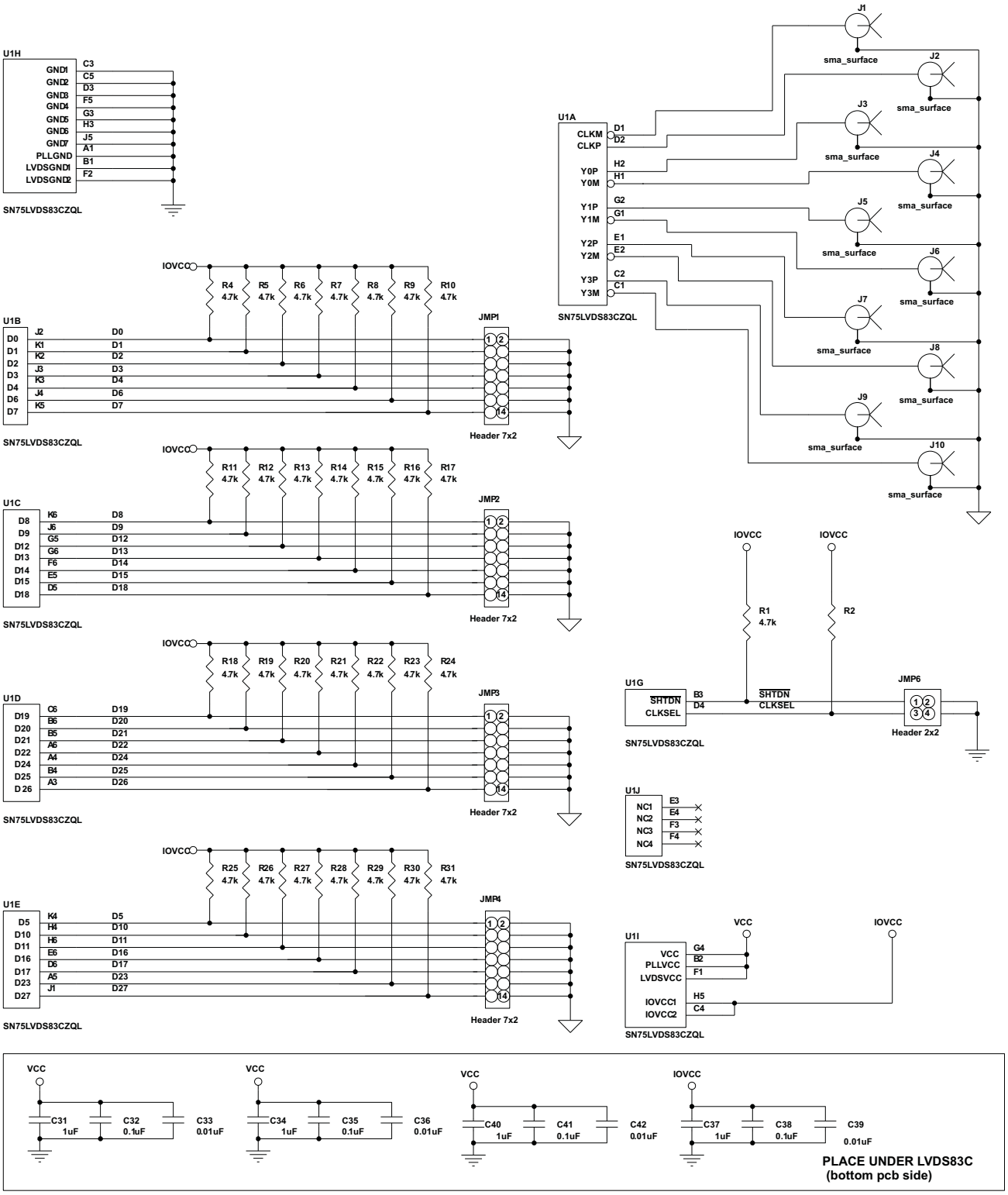


Figure 15. Schematic Example (SN75LVDS83C Evaluation Board)

PCB Routing

Figure 16 and Figure 17 show a possible breakout of the data input and output signals from the BGA package.

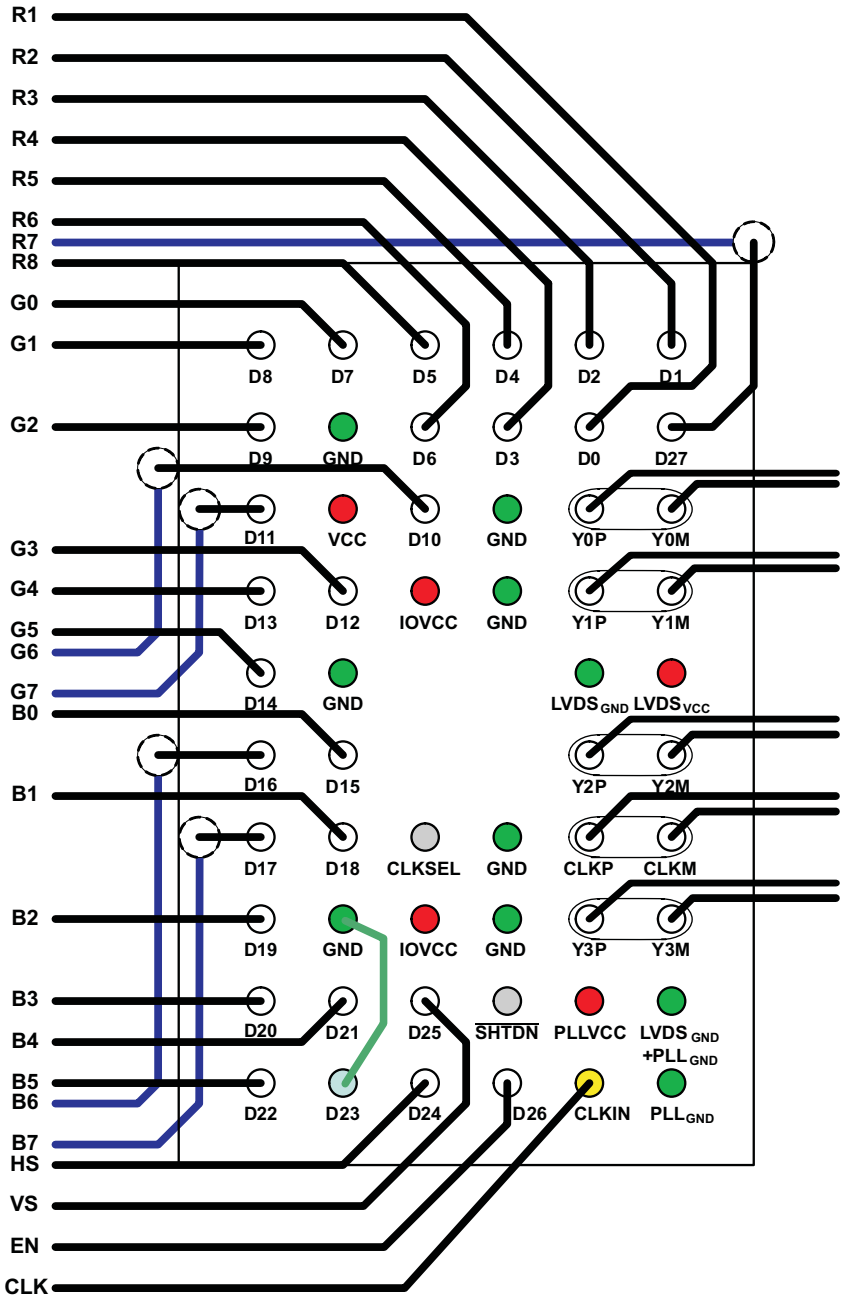


Figure 16. 24-Bit Color Routing (See Figure 11 for the Schematic)

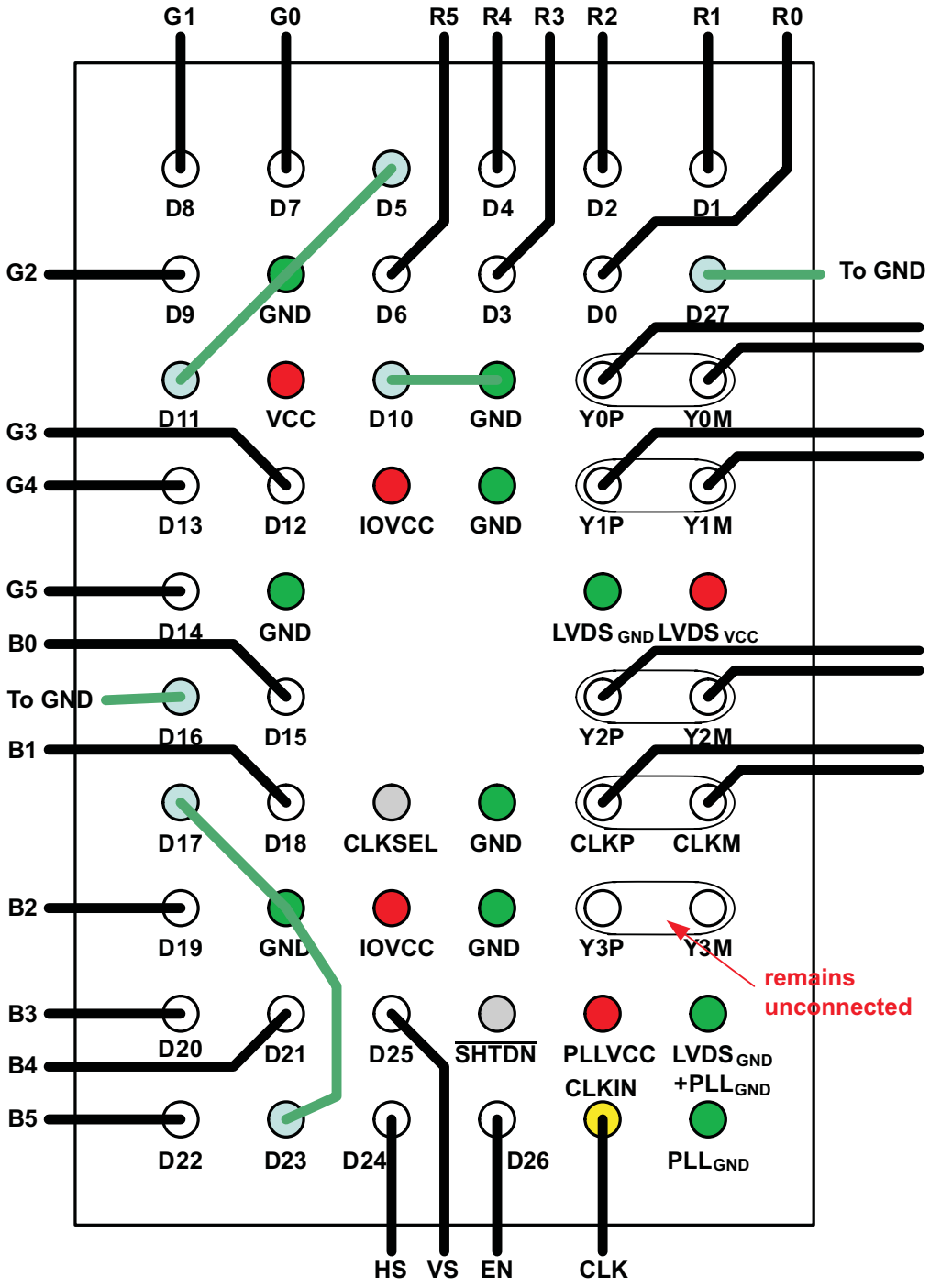


Figure 17. 18-Bit Color Routing (See Figure 12, Figure 13, and Figure 14 for the Schematic)

REVISION HISTORY

Changes from Original (May 2009) to Revision A	Page
• Multiply changes throughout the data sheet	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA02273ZQLR	LIFEBUY	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR	0 to 0	LVDS83C	
SN75LVDS83CZQLR	LIFEBUY	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR	0 to 0	LVDS83C	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

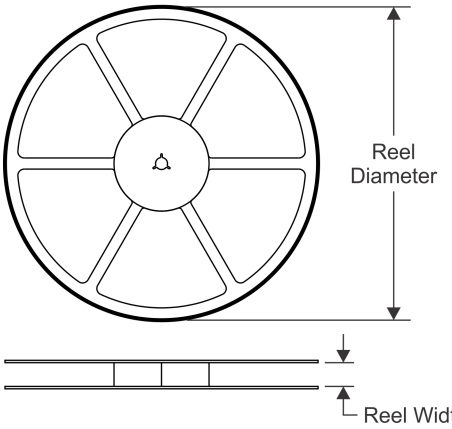
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

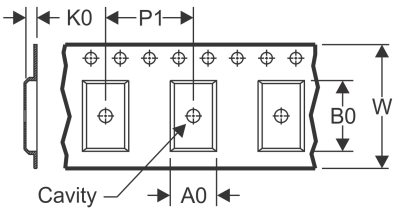
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

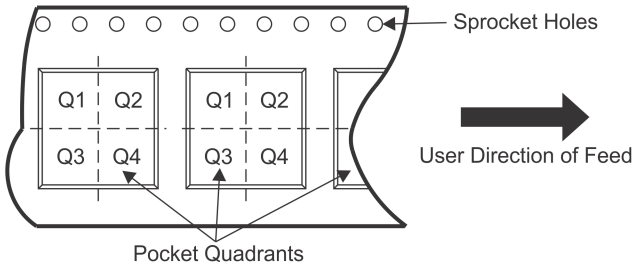


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

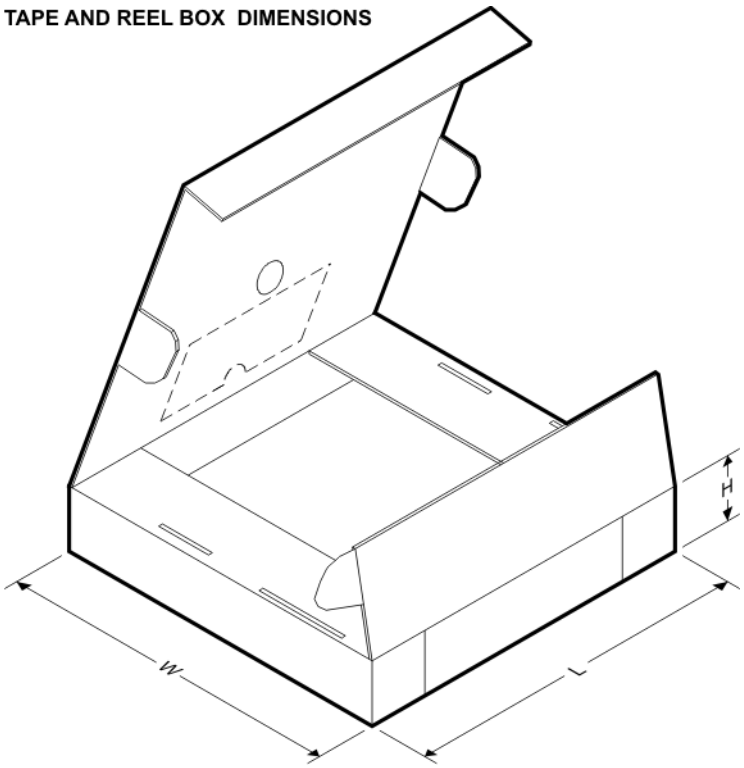
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVDS83CZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

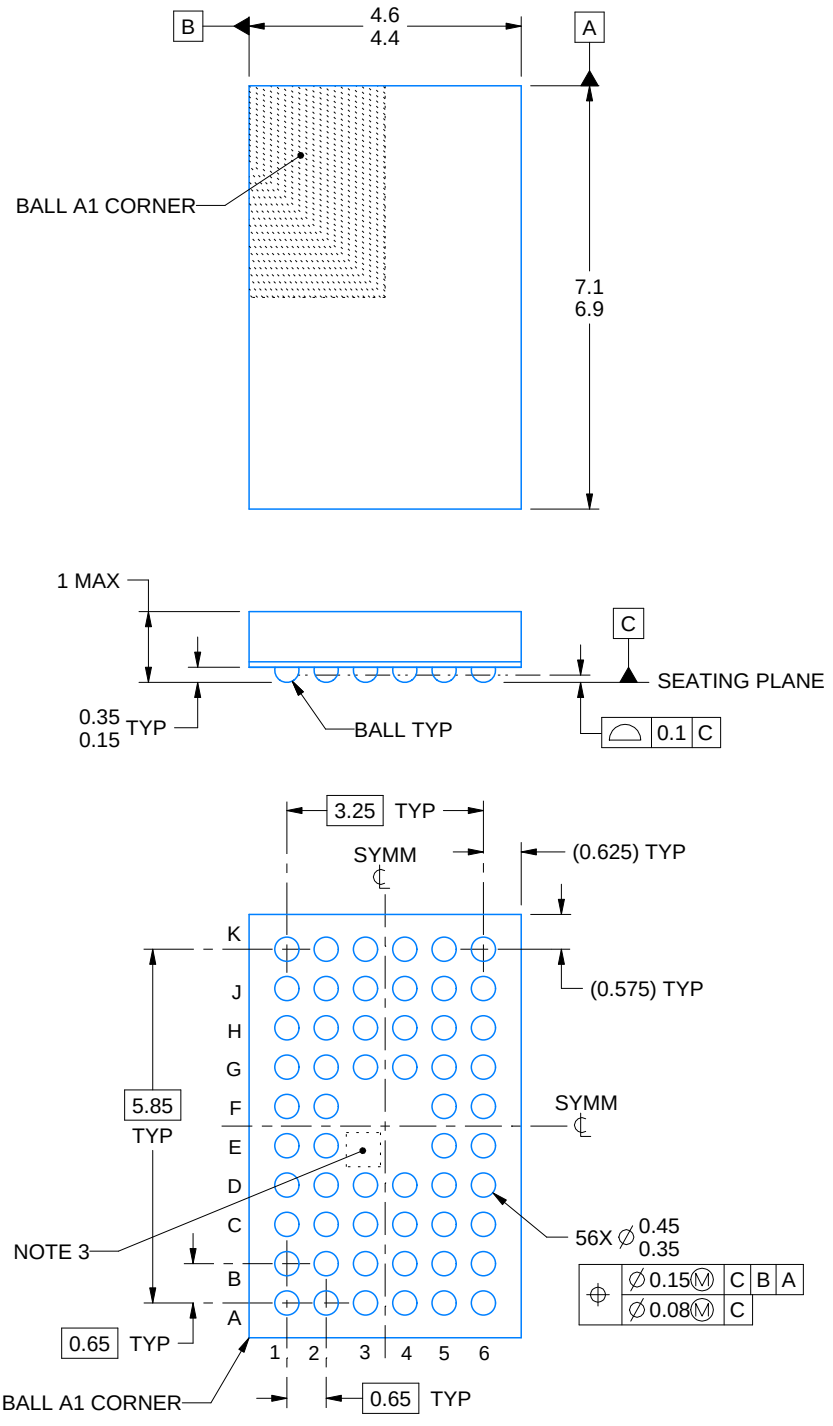
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVDS83CZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	350.0	350.0	43.0

PACKAGE OUTLINE

ZQL0056A

JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



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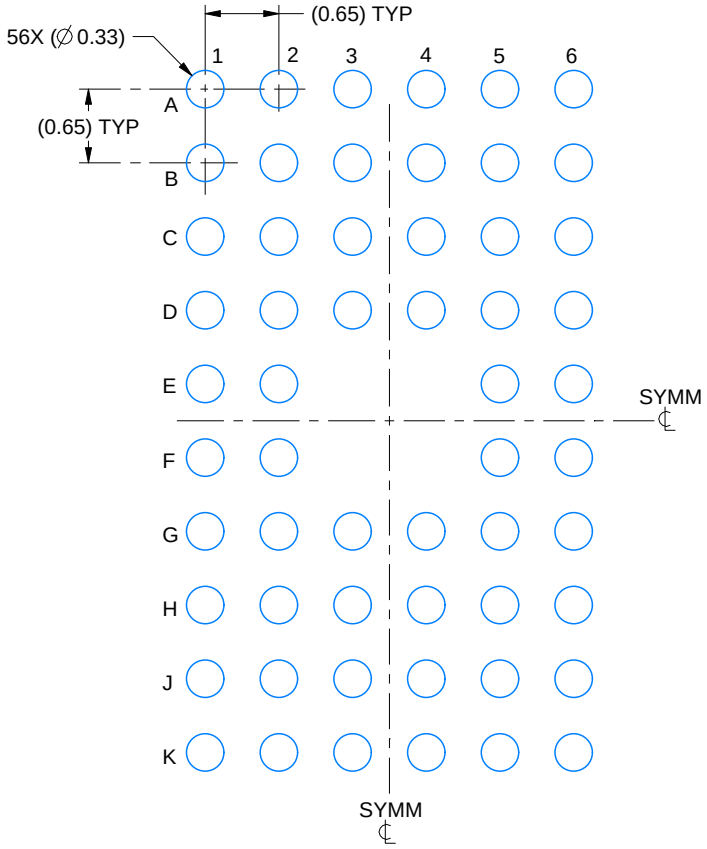
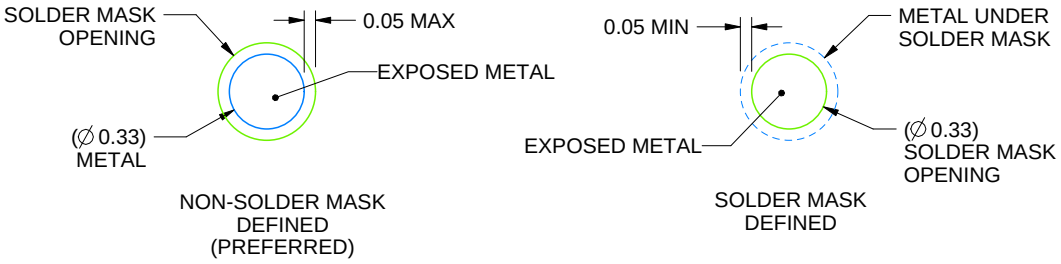
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. No metal in this area, indicates orientation.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS
NOT TO SCALE

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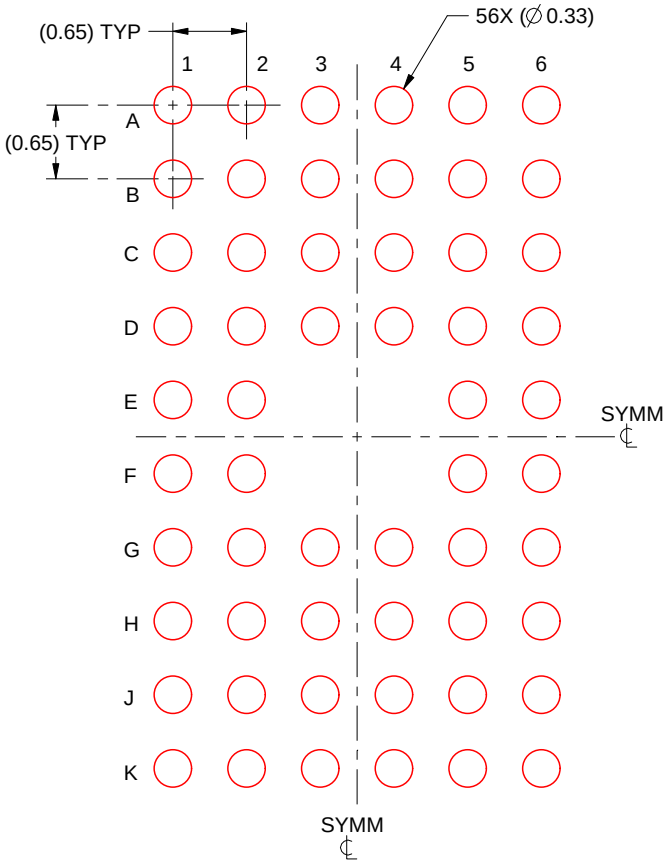
NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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