LMP7312 Precision SPI-Programmable AFE with Differential/Single-Ended Input/Output

Check for Samples: LMP7312

FEATURES

- **Typical Values, T_A = 25°C, V^+=5V, V^-=0V.**
- **Gain Bandwidth 1 MHz**
- **Input Voltage Range (G= 0.096 V/V) -15V to +15V**
- **Core Op-Amp Input Offset Voltage 100 µV (Max)**
- **Supply Current 2 mA (Max)**
- **Gain (Attenuation Mode) 0.096 V/V, 0.192 V/V0.384 V/V, 0.768 V/V**
- **Gain (Amplification Mode) 1 V/V, 2 V/V**
- **Gain Error 0.035% (Max)**
- **Core Op-Amp PSRR 90 dB (Min)**
- **CMRR 80 dB (min)**
- **Adjustable Output Common Mode 1V to 4V**
- **Temperature Range −40 to 125°C**
- **Package 14-Pin SOIC**

APPLICATIONS

- **Signal Conditioning AFE**
  - **±10V; ±5V; 0-5V; 0-10V; 0-20mA; 4-20mA**
- **Data Acquisition Systems**
- **Motor Control**
- **Instrument and Process Control**
- **Remote Sensing**
- **Programmable Automation Control**

DESCRIPTION

The LMP7312 is a digitally programmable variable gain amplifier/attenuator. Its wide input voltage range and superior precision make it a prime choice for applications requiring high accuracy such as data acquisition systems for IO modules in programmable logic control (PLC). The LMP7312 provides a differential output to maximize dynamic range and signal to noise ratio, thereby reducing the overall system error. It can also be configured to handle single ended input data converters by means of the V_{OCM} pin (see Application Section for details). The inputs of LMP7312 can be configured in attenuation mode to handle large input signals of up to +/- 15V, as well as in amplification mode to handle current loops of 0-20mA and 4-20mA.The LMP7312 is equipped with a null switch to evaluate the offset of the internal amplifier. A ensured 0.035% maximum gain error (for all gains) and a maximum gain drift of 5ppm over the extended industrial temperature range (-40° to 125°C) make the LMP7312 very attractive for high precision systems even under harsh conditions. A low input offset voltage of 100µV and low voltage noise of 3µVpp give the LMP7312 a superior performance. The LMP7312 is fully specified from -40° to 125°C and is available in SOIC-14 package.

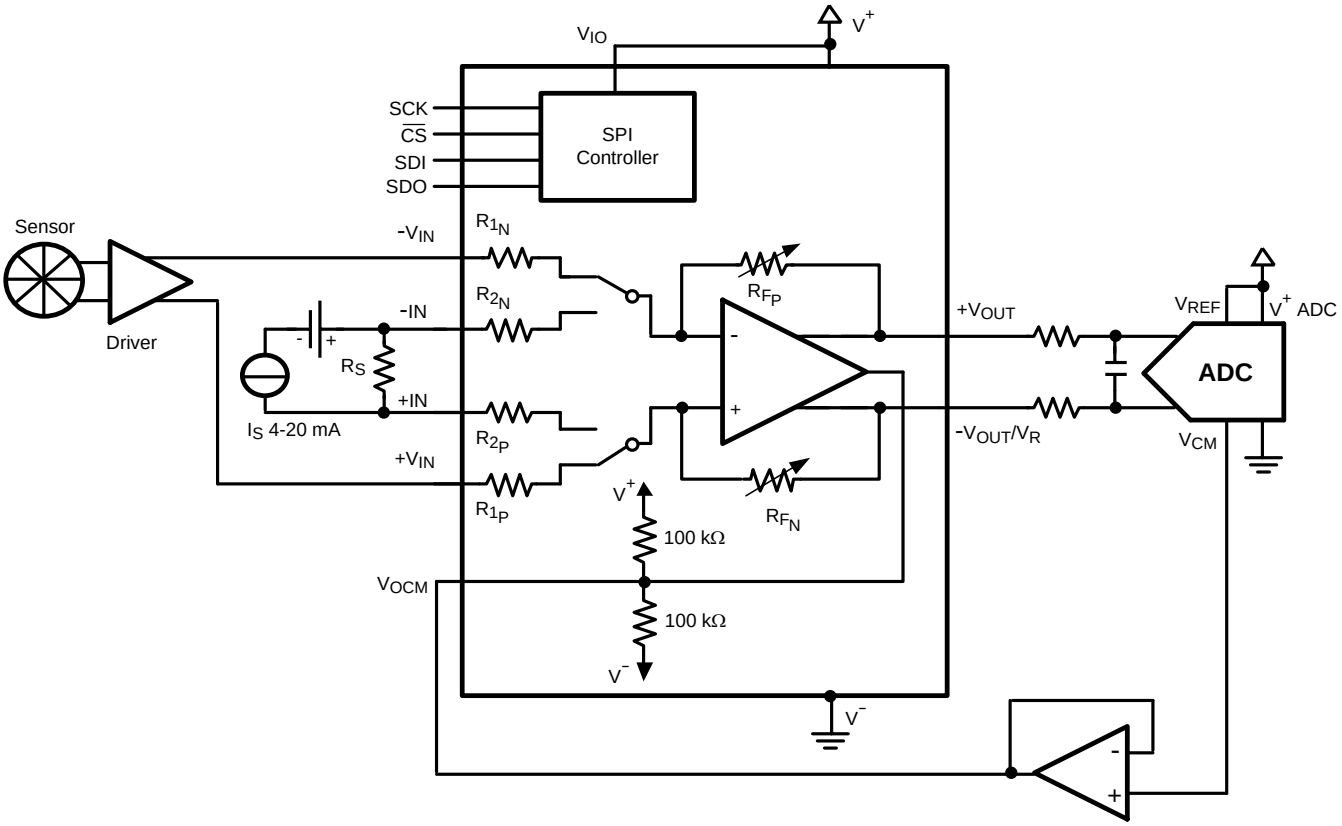
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Typical Application



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Rating (3)	
Human Body Model	2000V
Machine Body Model	150V
Charge device Model	1000V
Analog Supply Voltage ($V_S = V^+ - V^-$)	6V
Digital Supply Voltage ($V_{DIO}=V_{IO}-V^-$)	6V
Attenuation pins $-V_{IN}$, $+V_{IN}$ referred to V^-	±17.5V
Amplification pins -IN, +IN referred to V^-	±10V
Voltage at all other pins referred to V^-	6V
Storage Temperature Range	-65°C to 150°C
For soldering specification: http://www.ti.com/lit/SNOA549	
Junction Temperature	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but for which specific performance is not ensured. For ensured specifications and the test conditions, see Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22–A115–A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22–C101–C (ESD FICDM std. of JEDEC).

Operating Ratings (1)

Analog Supply Voltage ($V_S = V^+ – V^-$), V^-=0V	4.5V to 5.5V
Digital Supply Voltage ($V_{DIO} = V_{IO} – V^-$), V^-=0V	2.7V to 5.5V
Attenuation pins $-V_{IN}$, $+V_{IN}$ referred to V^-	-15V to 15V
Amplification pins -IN, +IN referred to V^-	-2.35V to 7.35V
Temperature Range (2)	−40°C to 125°C
Package Thermal Resistance (2)	
SOIC-14	145°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but for which specific performance is not ensured. For ensured specifications and the test conditions, see Electrical Characteristics.
(2) The maximum power dissipation is a function of TJ(max), θJA. The maximum allowable power dissipation at any ambient temperature is: PD(max) = (TJ(max) – TA)/ θJA. All numbers apply for packages soldered directly onto a PC Board.

5V Electrical Characteristics (1)

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = 5V, V_{IO} = 5V, V^- = 0V, G = 0.192 V/V, $V_{CM_ATT}=(+V_{IN}+(-V_{IN}))/2$, $V_{CM_AMP}=(+IN+(-IN))/2$. Differential output configuration. SE = Single Ended Output, DE = Differential Output. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Core op-amp Input Offset Voltage	Nulling Switch Mode, DE, V_{OCM} = 1V; Nulling switch Mode, SE, $-V_{OUT}/V_R$ = 1V	–100 **–250**		100 **250**	µV
		Nulling Switch Mode, DE, V_{OCM} = 4V; Nulling Switch Mode, SE, $-V_{OUT}/V_R$ = 4V	–100 **–250**		100 **250**	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are specified by testing, design, or statistical analysis.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

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5V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = 5V, V_{IO} = 5V, V^- = 0V, G = 0.192 V/V, V_{CM_ATT}=(+V_{IN}+(-V_{IN}))/2, V_{CM_AMP}=(+IN+(-IN))/2. Differential output configuration. SE = Single Ended Output, DE = Differential Output.**Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
TCV_{OS}	Core op-amp Input Offset Voltage (4)	Nulling Switch Mode, DE, V_{OCM} = 1V; Nulling Switch Mode, SE, -V_{OUT}/V_R = 1V	-3	±1.5	3	µV/°C
		Nulling Switch Mode, DE, V_{OCM} = 4V; Nulling Switch Mode, SE, -V_{OUT}/V_R = 4V	-3	±1.5	3	
Av	Gain Error	All gains, R_L = 10 kΩ, C_L = 50pF, SE / DE	–0.035 **–0.045**		0.035 **0.045**	%
	Gain Drift	SE / DE	-5	±1	5	ppm/°C
e_n	Core op-amp Voltage Noise Density	RTI, Nulling Switch Mode, f = 10 kHz		7.25		nV/√Hz
	Core op-amp Peak to Peak Voltage Noise	RTI, Nulling Switch Mode, f= 0.1Hz to 10Hz		3		μV_{PP}
I_{VA}	Analog Supply Current	+V_{IN} = −V_{IN} = V_{OCM}			**2**	mA
I_{VIO}	Digital Supply Current	Without any load connected to SDO pin			**120**	µA
R_{IN_CM}	CM Input Resistance	G= 0.192 V/V		62.08		kΩ
		G= 1 V/V		40		
R_{IN_DIFF}	Differential Input Resistance	G= 0.192 V/V		248.3		kΩ
		G= 1 V/V		160		
CMRR	DC Common Mode Rejection Ratio	G= 0.096V/V, -15V < V_{CM_ATT} < 15V, SE / DE	80 **77**			dB
		G= 0.192V/V, -11.4V < V_{CM_ATT} < 15V, SE / DE				
		G= 0.384V/V, -6V < V_{CM_ATT} < 11V, SE / DE				
		G= 0.768V/V, -3V < V_{CM_ATT} < 8V, SE / DE				
		G= 1V/V, -2.3V < V_{CM_AMP} < 7.3V, SE / DE				
		G= 2V/V, -1.15V < V_{CM_AMP} < 6.15V, SE / DE.				
PSRR	Core op-amp DC Power Supply Rejection Ratio	Nulling Switch Mode, 4.5V <V^+ <5.5V	90			dB
V_{OCM_OS}	V_{OCM} Output Offset (5)	V_{OCM} = 2.5 V	**-20**		**20**	mV
V_{OUT}	Positive Output Voltage Swing	R_L = 10 kΩ, C_L = 50 pF, +V_{IN}= 15V, -V_{IN}= -15V			V^+−0.2	V
	Negative Output Voltage Swing	R_L = 10 kΩ, C_L = 50 pF, +V_{IN}= -15V, -V_{IN}= 15V	V^-+0.2			
I_{OUT}	Short circuit current	+V_{IN}= -V_{IN} = 2.5V, +V_{OUT}, -V_{OUT}/V_R connected individually to either V^+ or V^-	10			mA
	Current limitation	Internal current limiter			55	
GBW	Bandwidth	Attenuation Mode, G = 0.096 V/V, R_L =10 kΩ, C_L = 50 pF		1.2		MHz
		Attenuation Mode, G = 0.192 V/V, R_L = 10 kΩ, C_L = 50 pF		1.0		
		Attenuation Mode, G = 0.384 V/V, R_L = 10 kΩ, C_L = 50 pF		560		kHz
		Attenuation Mode, G = 0.768 V/V, R_L = 10 kΩ, C_L = 50 pF		310		
		Amplification Mode, G = 1 V/V, R_L = 10 kΩ, C_L = 50 pF		530		kHz
		Amplification Mode, G = 2 V/V, R_L = 10 kΩ, C_L = 50 pF		280		

(4) Offset voltage temperature drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.

(5) V_{OCM_OS} is the difference between the Output Common mode voltage (+V_{OUT}+(-V_{OUT}/V_R))/2 and the Voltage on the V_{OCM} pin.

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5V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = 5V, V_{IO} = 5V, V^- = 0V, G = 0.192 V/V, V_{CM_ATT}=(+V_{IN}+(-V_{IN}))/2, V_{CM_AMP}=(+IN+(-IN))/2. Differential output configuration. SE = Single Ended Output, DE = Differential Output. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
SR	Slew Rate	R_L = 10 kΩ, C_L = 50 pF (6)		1.4		V/µsec
THD+N	Total Harmonic Distorsion + Noise	Vout = 4.096 Vpp, f = 1KHz, R_L = 10 kΩ		0.0026		%

(6) The number specified is the average of rising and falling slew rates and is measured at 90% to 10%.

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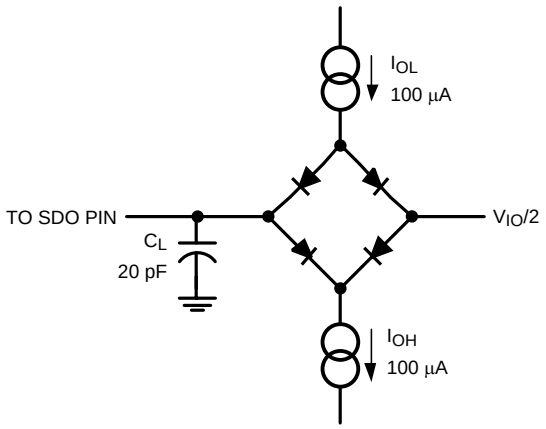
Electrical Characteristics (Serial Interface) (1)

Unless otherwise specified. All limits ensured for T_A = 25°C, V^+ = 5V, V^- = 0V, 2.7V < V_{IO} < 5.5V

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
VIL	Input Logic Low Threshold				0.8	V
VIH	Input Logic High Threshold (SDO pin)		2			V
VOL	Output logic Low Threshold (SDO pin)	I_{SDO}= 100µA			0.2	V
		I_{SDO}= 2mA			0.4	
VOH	Output logic High Threshold	I_{SDO}= 100µA	V_{IO}-0.2			V
		I_{SDO}= 2mA	V_{IO}-0.6			
t_1	High Period, SCK	(4)	100			ns
t_2	Low Period, SCK	(4)	100			ns
t_3	Set Up Time, $\overline{CS}$ to SCK	(4)	50			ns
t_4	Set Up Time, SDI to SCK	(4)	30			ns
t_5	Hold Time, SCK to SDI	(4)	10			ns
t_6	Prop. Delay, SCK to SDO	(4)			60	ns
t_7	Hold Time, SCK Transition to $\overline{CS}$ Rising Edge	(4)	50			ns
t_8	$\overline{CS}$ Inactive	(4)	100			ns
t_9	Hold Time, SCK Transition to $\overline{CS}$ Falling Edge	(4)	10			ns
t_R/t_F	Signal Rise and Fall Times	(4)	1.5		5	ns

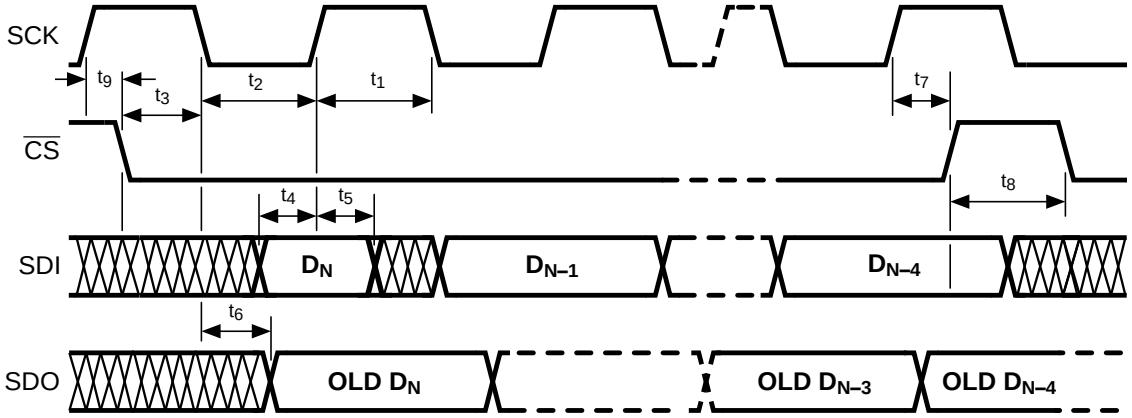
(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are specified by testing, design, or statistical analysis.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Load for these tests is shown in Test Circuit Diagram.

TEST CIRCUIT DIAGRAM



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Timing Diagram



Connection Diagram

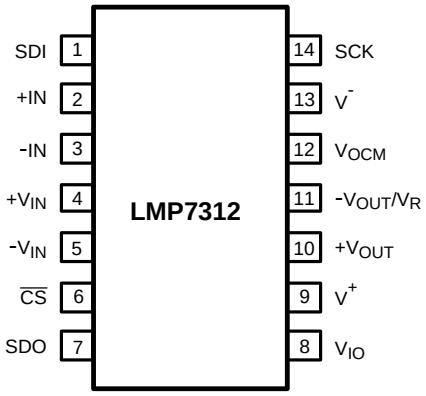


Figure 1. 14-Pin SOIC-Top View

PIN DESCRIPTIONS

Pin	Name	Description
1	SDI	SPI data IN
2	+IN	Non-inverting input of Amplification pair
3	-IN	Inverting input of Amplification pair
4	$+V_{IN}$	Non-inverting input of Attenuation pair
5	$-V_{IN}$	Inverting input of Attenuation pair
6	$\overline{CS}$	SPI chip select
7	SDO	SPI data OUT
8	V_{IO}	SPI supply voltage
9	V^+	Positive supply voltage
10	$+V_{OUT}$	Non-inverting output
11	$-V_{OUT}/V_R$	Inverting output in differential output mode, reference input in single-ended operation mode
12	V_{OCM}	Output common mode voltage in DE
13	V^-	Negative supply voltage, reference for both Analog and Digital supplies
14	SCK	SPI Clock

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Typical Performance Characteristics

Unless otherwise specified, T_A = 25°C, V^+ = 5V, V_{IO} = 5V, V^- = 0V, V_{CM_ATT}=(+V_{IN}+(-V_{IN}))/2, V_{CM_AMP}=(+IN+(-IN))/2. R_L = 10kΩ, C_L =50pF, Differential output configuration.

Offset Voltage distribution (PMOS)

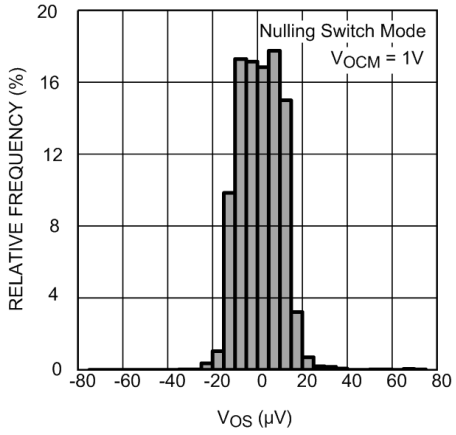


Figure 2.

Offset Voltage distribution (NMOS)

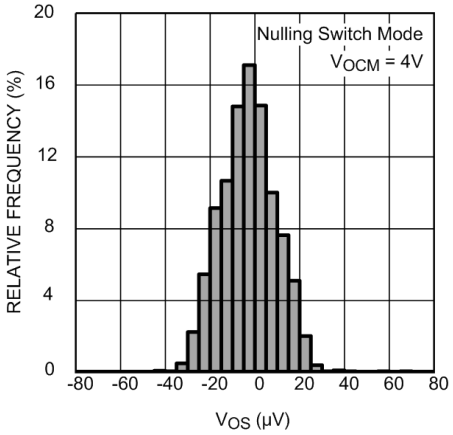


Figure 3.

TCV_{OS} distribution (PMOS)

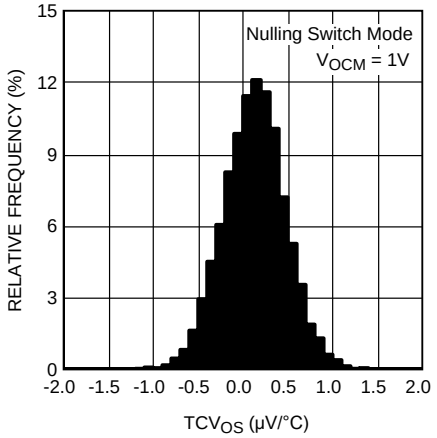


Figure 4.

TCV_{OS} distribution (NMOS)

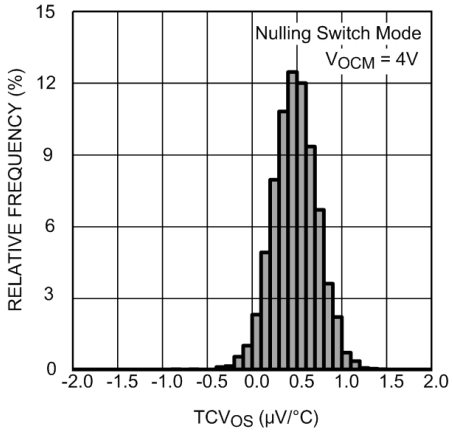


Figure 5.

Noise vs. Frequency (Core op-amp)

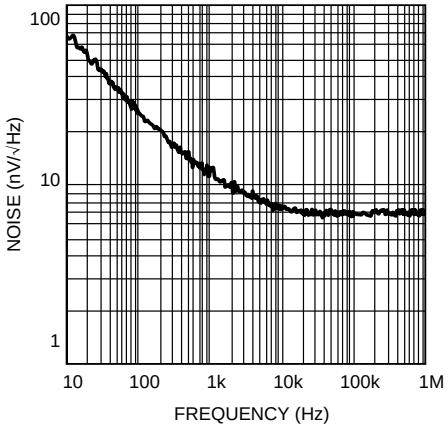


Figure 6.

0.1Hz to 10Hz Noise (Core op-amp)

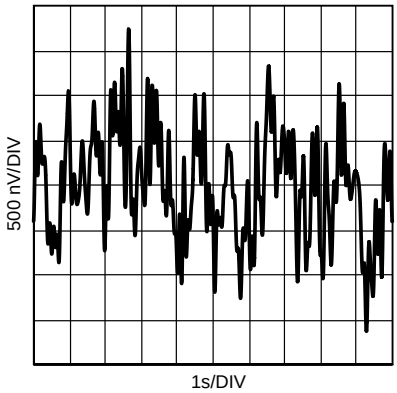


Figure 7.

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Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^+ = 5V, V_{IO} = 5V, V^- = 0V, V_{CM_ATT}=(+V_{IN}+(-V_{IN}))/2, V_{CM_AMP}=(+IN+(-IN))/2. R_L = 10kΩ, C_L =50pF, Differential output configuration.

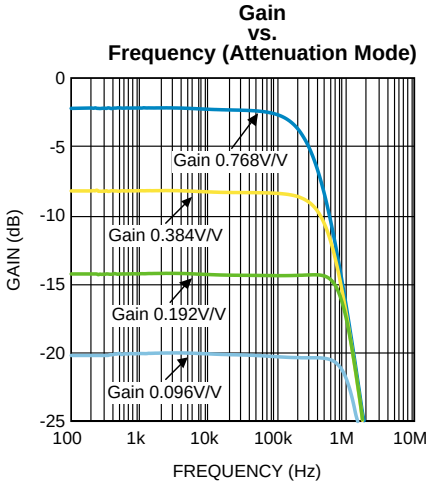


Figure 8.

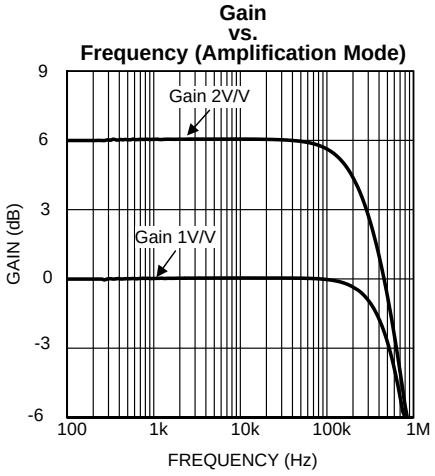


Figure 9.

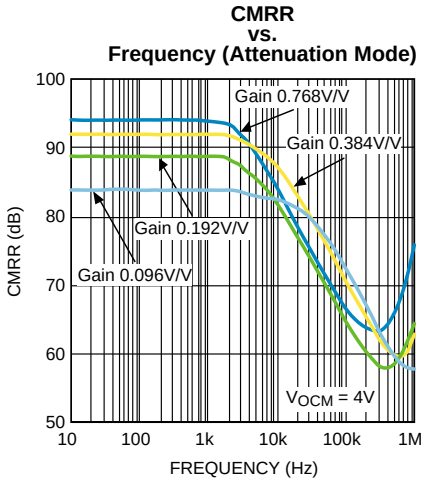


Figure 10.

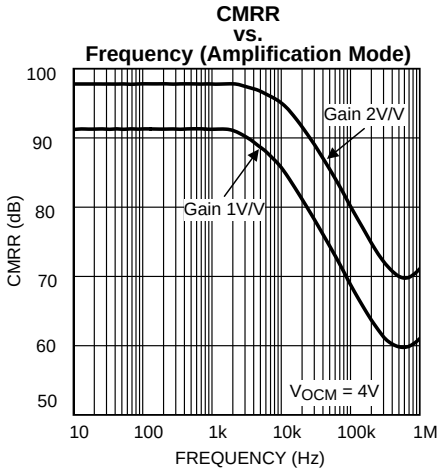


Figure 11.

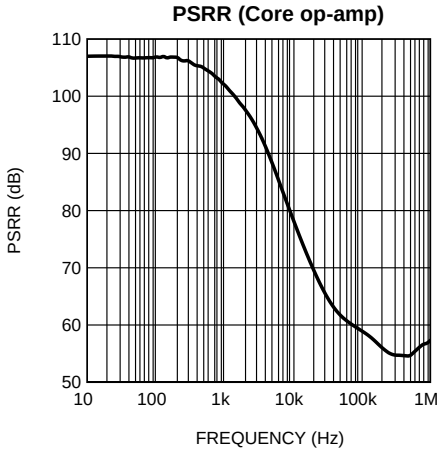


Figure 12.

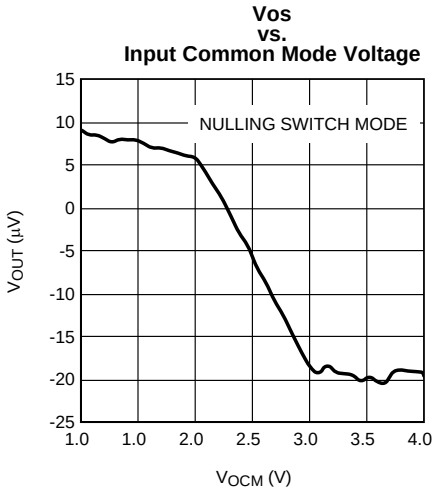


Figure 13.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^+ = 5V, V_{IO} = 5V, V^- = 0V, V_{CM_ATT}=(+V_{IN}+(-V_{IN}))/2, V_{CM_AMP}=(+IN+(-IN))/2. R_L = 10kΩ, C_L =50pF, Differential output configuration.

Small signal step (Attenuation Mode)

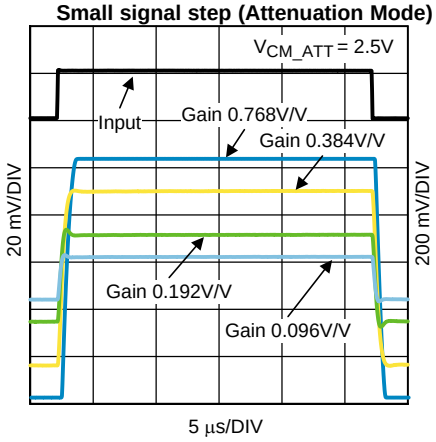


Figure 14.

Small signal step (Amplification Mode)

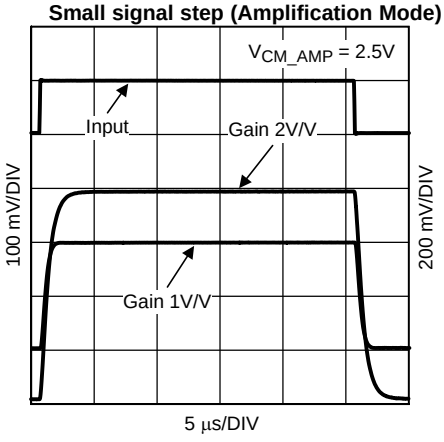


Figure 15.

Large signal step (Attenuation Mode)

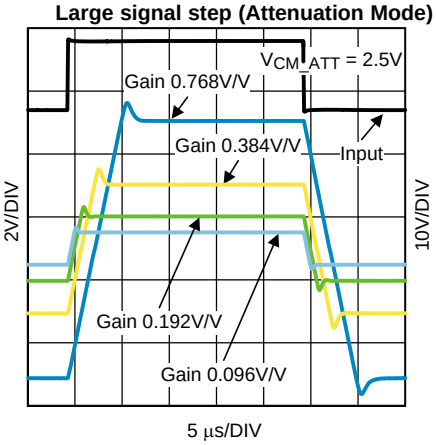


Figure 16.

Large signal step (Amplification Mode)

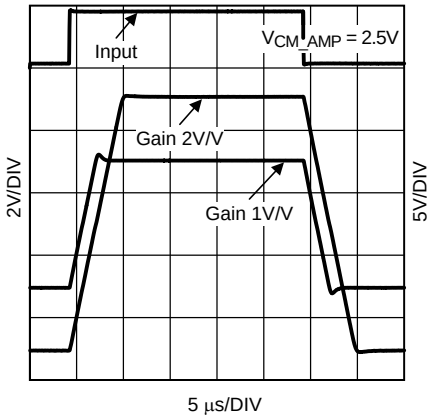


Figure 17.

Settling time – Rise (Attenuation Mode)

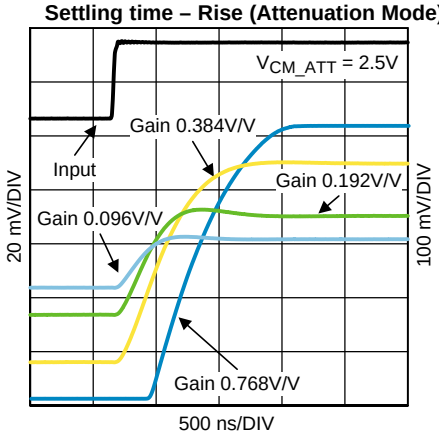


Figure 18.

Settling time – Rise (Amplification Mode)

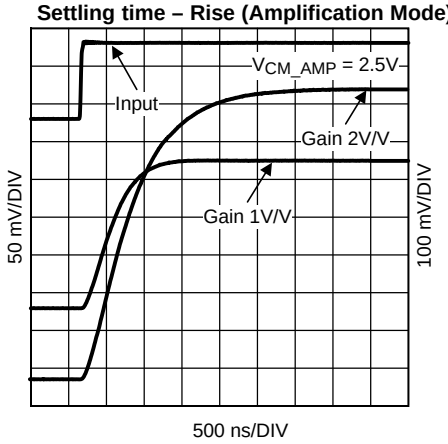


Figure 19.

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Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^+ = 5V, V_{IO} = 5V, V^- = 0V, V_{CM_ATT}=(+V_{IN}+(-V_{IN}))/2, V_{CM_AMP}=(+IN+(-IN))/2. R_L = 10kΩ, C_L =50pF, Differential output configuration.

Settling time – Fall (Attenuation Mode)

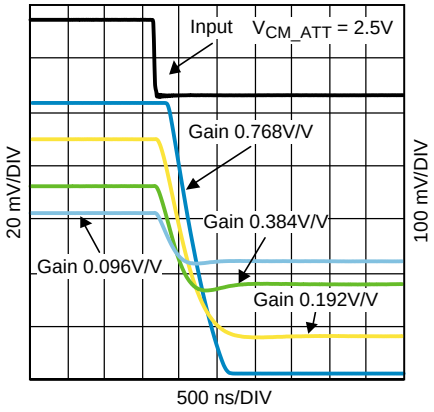


Figure 20.

Settling time – Fall (Amplification Mode)

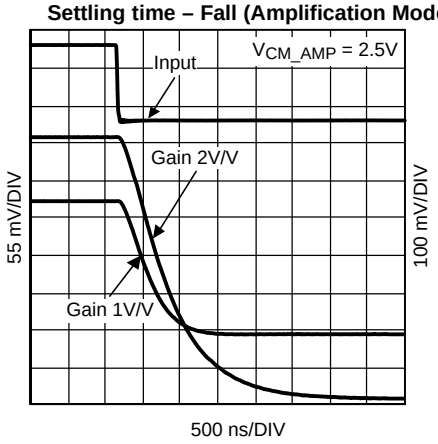


Figure 21.

Gain change (Attenuation Mode)

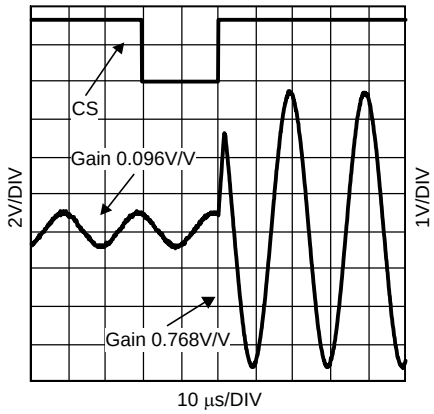


Figure 22.

Gain change (Amplification Mode)

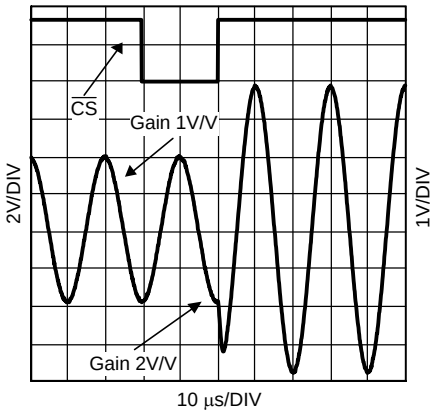


Figure 23.

THD + N (Attenuation Mode)

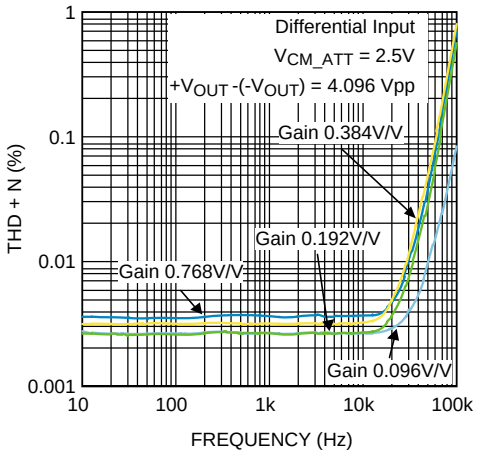


Figure 24.

THD + N (Amplification Mode)

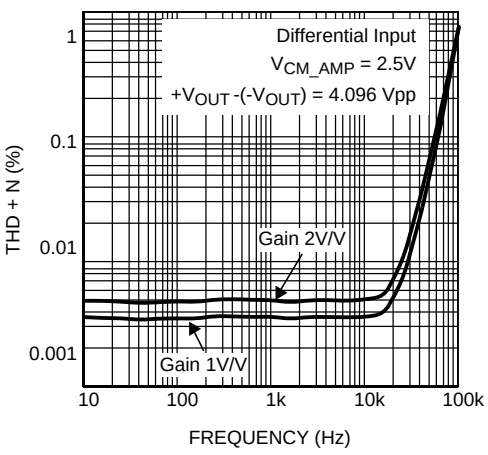


Figure 25.

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Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^+ = 5V, V_{IO} = 5V, V^- = 0V, V_{CM_ATT}=(+V_{IN}+(-V_{IN}))/2, V_{CM_AMP}=(+IN+(-IN))/2. R_L = 10kΩ, C_L =50pF, Differential output configuration.

I_{VA} vs. V_A

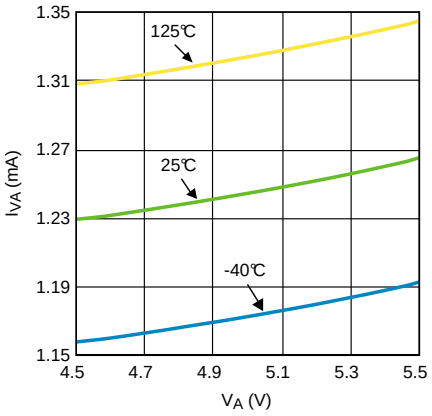


Figure 26.

I_{VIO} vs. V_{IO} Voltage

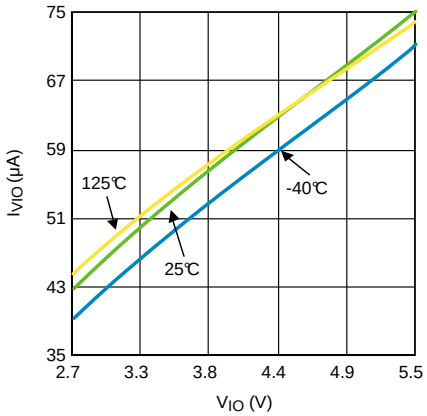


Figure 27.

Short Circuit Current +V_{OUT} vs. Temperature

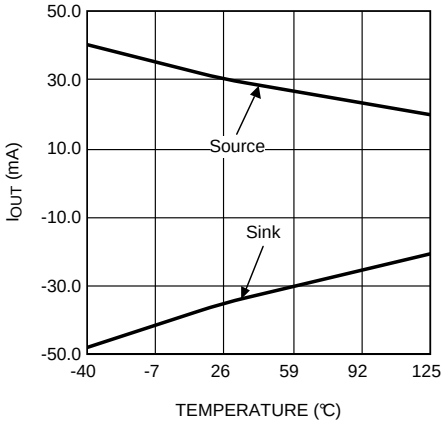


Figure 28.

Short Circuit Current -V_{OUT} vs. Temperature

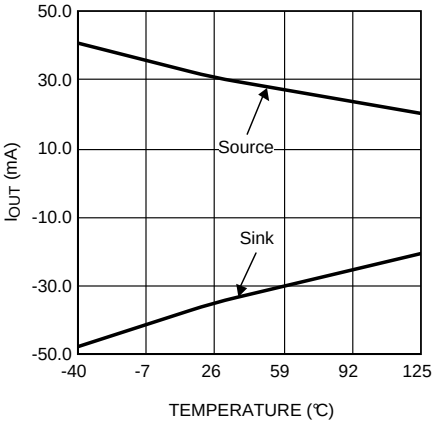


Figure 29.

Output voltage swing +V_{OUT} vs. Output current

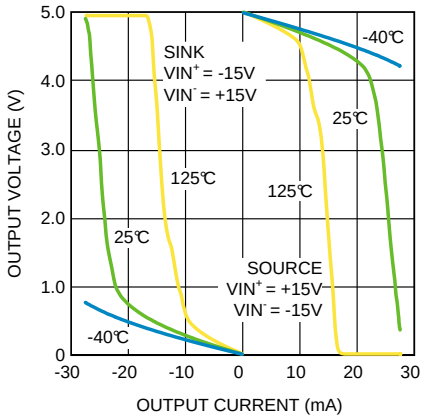


Figure 30.

Output voltage swing -V_{OUT} vs. Output current

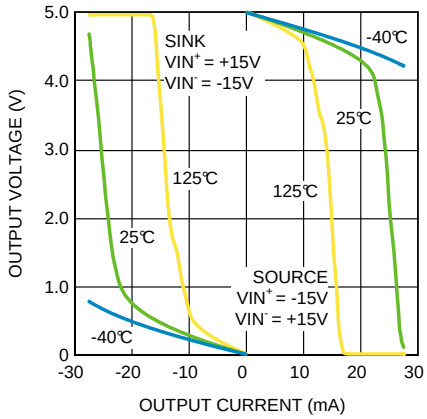


Figure 31.

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Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^+ = 5V, V_{IO} = 5V, V^- = 0V, V_{CM_ATT}=(+V_{IN}+(-V_{IN}))/2, V_{CM_AMP}=(+IN+(-IN))/2. R_L = 10kΩ, C_L =50pF, Differential output configuration.

SDO sink current vs. SDO Voltage

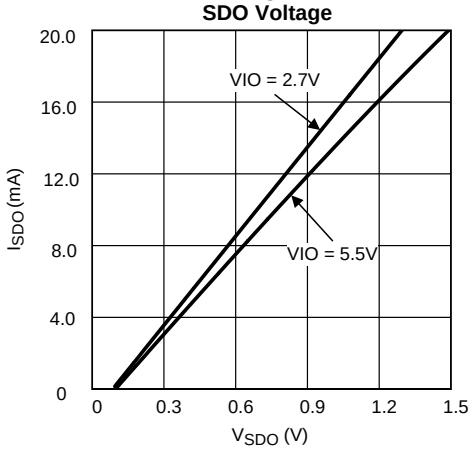


Figure 32.

SDO source current vs. SDO Voltage

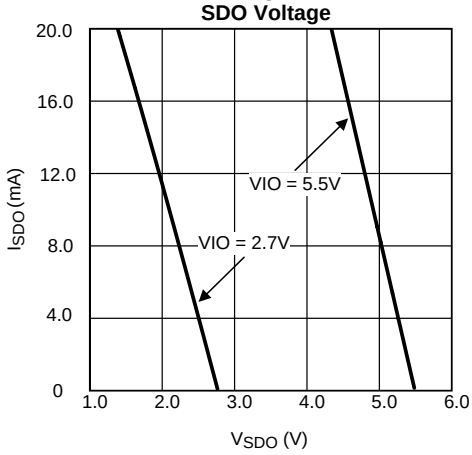


Figure 33.

APPLICATION SECTION

GENERAL DESCRIPTION

The LMP7312 is a single supply programmable gain difference amplifier with two input pairs: Attenuation pair (-V_{IN}, +V_{IN}) and Amplification pair (-IN, +IN). The output can be configured in both single-ended and differential modes with the output common mode voltage set by the user. The input selection, the gains and the mode of operation of the LMP7312 are controlled through a 4- wire SPI interface (SCK, $\overline{CS}$, SDI, SDO). These features combined make the LMP7312 a very easy interface between the analog high voltage industrial buses and the low voltage digital converters.

OUTPUT MODE CONFIGURATION

The LMP7312 is able to work in both single ended and differential output mode. The selection of the mode is made through the V_{OCM} (output common mode voltage) pin.

Differential Output

This mode of operation is enabled when the output common mode voltage pin (V_{OCM}) is connected to a voltage higher than 1V, for instance the common mode voltage supplied by an ADC, (Figure 34) or a voltage reference. If the V_{OCM} pin is floating an internal voltage divider biases it at the half supply voltage. In this configuration the output signals are set on the V_{OCM} voltage level.

Single-Ended Output

This mode of operation is enabled when the V_{OCM} pin is tied to a voltage less than 0.5 V, for example to ground. In this mode of operation the LMP7312 behaves as a difference amplifier, where the +V_{OUT} pin is the single-ended output while the –V_{OUT} /V_R is the reference voltage.

1. In the case of bipolar input signal the non inverting output will be connected to an external reference through a buffer (Figure 35).
2. In the case of unipolar input signal the non inverting output will be connected to ground (Figure 36).

In both cases the inverting output pin is configured as an input pin.

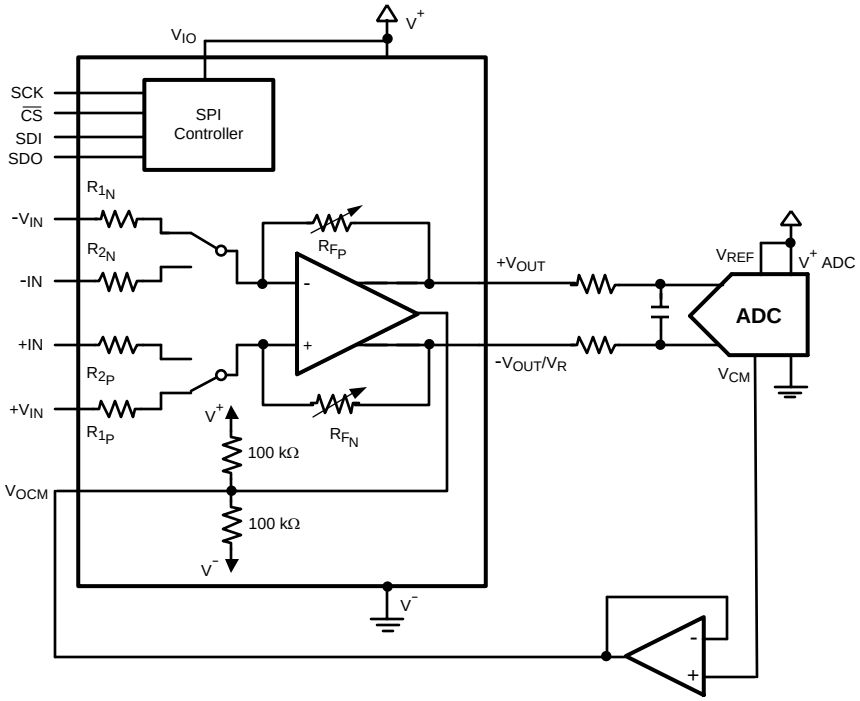


Figure 34. Differential ADC Interfacing with V_{CM} provided by the ADC

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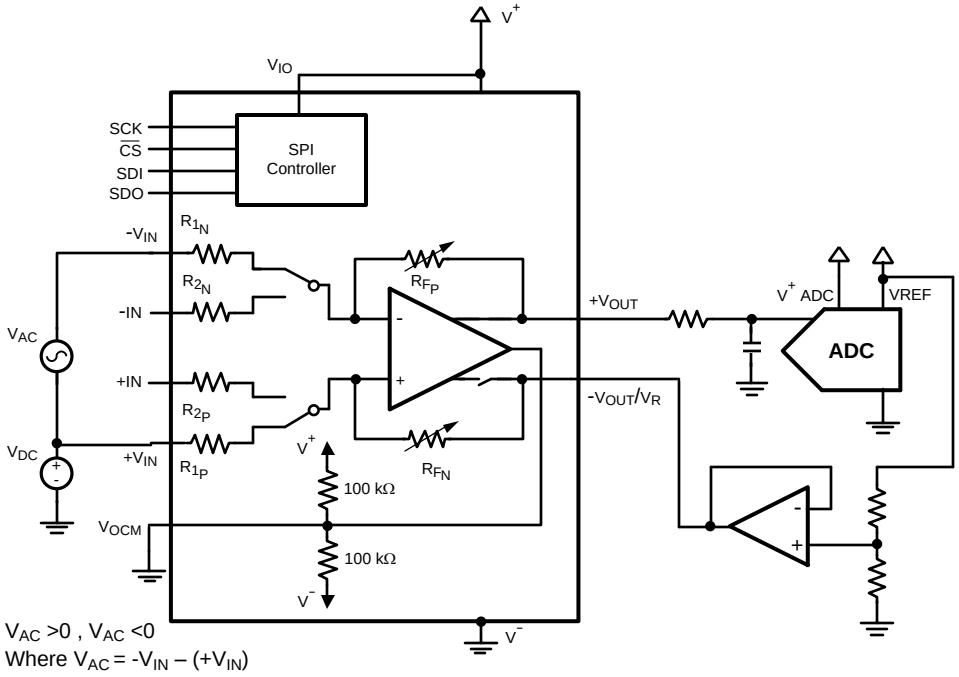


Figure 35. Bipolar Input Signal to Single-Ended ADC Interface

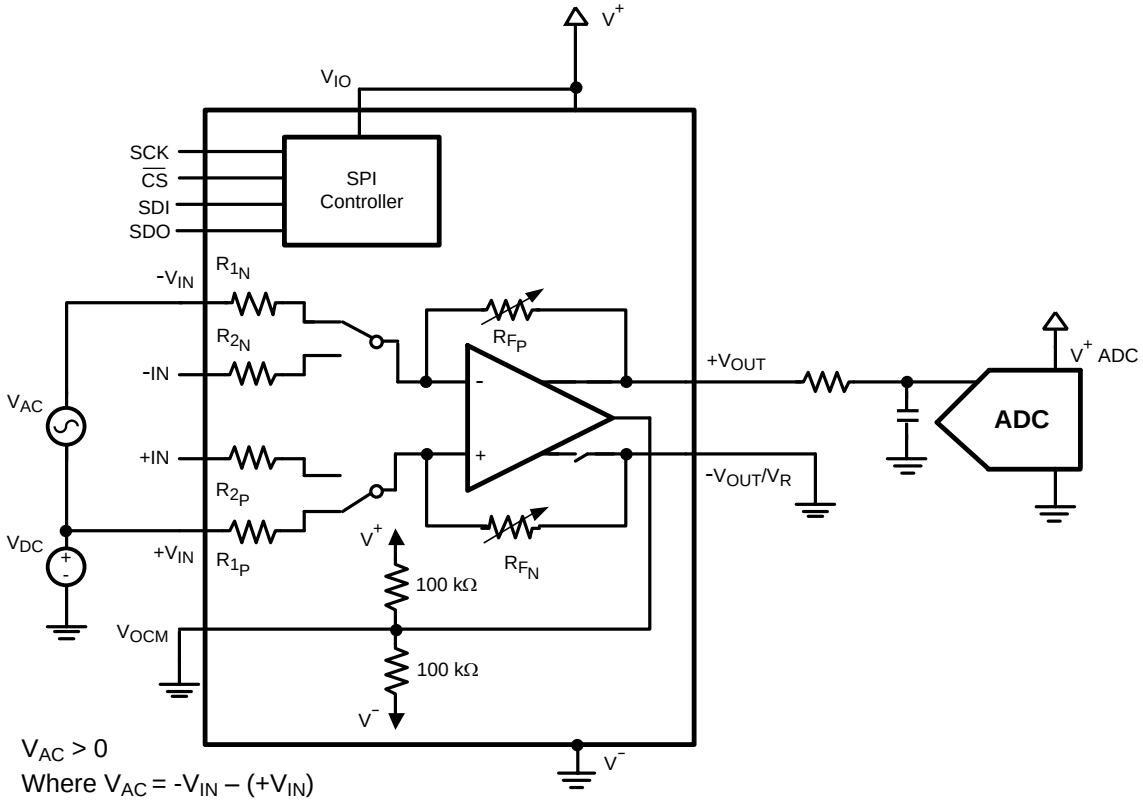


Figure 36. Unipolar Input Signal to Single-Ended ADC Interface

INPUT VOLTAGE RANGE

The LMP7312 has an internal OpAmp with rail-to-rail input voltage range capability. The requirement to stay within the V^- and V^+ rail at the OpAmp input translates in an Input Voltage Range specification as explained in this application section.

Differential Output

Considering a single positive supply (V^- = GND, $V^+ = V_S$) the Input Common mode voltage, $V_{CM_ATT} = (+V_{IN} + (-V_{IN}))/2$ for the Attenuation inputs and $V_{CM_AMP} = (+I_{IN} + (-I_{IN}))/2$ for the Amplification inputs, has to stay between the MIN and MAX values determined by these formulas:

$CM_{MAX} = V_S + 1/K_V*(V_S - V_{OCM})$

$CM_{MIN} = -1/K_V*V_{OCM}$

K_V is a function of the Gain according to the table below:

Gain	0.096 V/V	0.192 V/V	0.384 V/V	0.768 V/V	1 V/V	2 V/V
K_V	0.12	0.218	0.414	0.806	1.065	2.096

Regardless to the values derived by the formula, the voltage on each input pin must never exceed the specified Absolute Maximum Ratings.

Below are some typical values:

Table 1. Differential Input, Differential Output, V_S= 5V, V_{OCM} = 2.5V

	V_{CM_ATT}		V_{CM_AMP}	
Gain	**Min**	**Max**	**Min**	**Max**
0.096 V/V	-15 V(1)	+15 V(1)		
0.192 V/V	-11.5 V	+15 V		
0.384 V/V	-6 V	+11 V		
0.768 V/V	-3.1 V	+8.1 V		
1 V/V			-2.3 V	+7.3 V
2 V/V			-1.2 V	+6.2 V

(1) Limited by the operating ratings on input pins

In the case of a single ended input referred to ground ($-V_{IN}$ = GND, -IN = GND) the table below summarizes the voltage range allowed on the $+VI_N$ and $+I_{IN}$ inputs.

Table 2. Single Ended Input, Differential Output, V_S= 5V, V_{OCM} = 2.5V, $-V_{IN}$ = GND, $-I_{IN}$ = GND

	$+V_{IN}$		+IN	
Gain	**Min**	**Max**	**Min**	**Max**
0.096 V/V	-15 V(1)	+15 V(1)		
0.192 V/V	-15 V(1)	+15 V(1)		
0.384 V/V	-12 V(2)	+12 V(2)		
0.768 V/V	-6 V(2)	+6 V(2)		
1 V/V			-4.6 V(2)	+4.6 V(2)
2 V/V			-2.3 V(2)	+2.3 V(2)

(1) Limited by the operating ratings on input pins.
(2) Limited by the output voltage swing (0.2V to V_S-0.2V on both + V_{OUT} and $-V_{OUT}$)

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Single Ended Output

In this mode the LMP7312 behaves as a Difference Amplifier, with $-V_{OUT}/V_R$ being the reference output voltage when a zero volt differential input signal is applied. The voltages at the OpAmp inputs are determined by $+V_{IN}$ and $-V_{OUT}/V_R$ voltages. The voltage range of $+V_{IN}$ and $+I_{IN}$ inputs is as follows:

$V_{MAX} = V_S + 1/ K_V * (V_S – (-V_{OUT}/V_R))$

$V_{MIN} = -1/K_V * (-V_{OUT}/V_R)$

Regardless of the values derived by the formula, the voltage on each input pin must never exceed the specified Absolute Maximum Ratings.

Below are some typical values:

Table 3. Differential Input, Single Ended Output, V_S = 5V, V_{OCM} = GND, and $-V_{OUT}/V_R$ = 2.5V

	$+V_{IN}$		$+I_{IN}$	
Gain	**Min**	**Max**	**Min**	**Max**
0.096 V/V	-15 V(1)	+15 V(1)		
0.192 V/V	-11.5 V(1)	+15 V		
0.384 V/V	-6 V	+11 V		
0.768 V/V	-3.1 V	+8.1 V		
1 V/V			-2.3 V	+7.3 V
2 V/V			-1.2 V	+6.2 V

(1) Limited by the operating ratings on input pins

In the case of a single ended input referred to ground ($-V_{IN}$ = GND, -IN = GND) this table summarize the voltage ranges allowed on the $+V_{IN}$ and $+I_{IN}$ inputs.

Table 4. Single Ended Input, Single Ended Output, V_S = 5V, V_{OCM} = GND, $-V_{OUT}/V_R$ = 2.5V, $-V_{IN}$ = GND, $-I_{IN}$ = GND

	$+V_{IN}$		$+I_{IN}$	
Gain	**Min**	**Max**	**Min**	**Max**
0.096 V/V	-15 V(1)	+15 V(1)		
0.192 V/V	-11.5 V	+12 V(2)		
0.384 V/V	-6 V(2)	+6 V(2)		
0.768 V/V	-3 V**	+3 V(2)		
1 V/V			-2.3 V(2)	+2.3 V(2)
2 V/V			-1.1 V(2)	+1.1 V(2)

(1) Limited by the operating ratings on input pins.
(2) Limited by the output voltage swing (0.2V to V_S-0.2V on $+V_{OUT}$)

SERIAL INTERFACE CONTROL OPERATION

The serial interface control of the LMP7312 can be supplied with a voltage between 2.7V and 5.5V through the V_{IO} pin for compatibility with different logic families present in the market.

The LMP7312 Attenuation, Amplification, Null switch and HiZ modes are controlled by a register. Data to be written into the control register is first loaded into the LMP7312 via the serial interface. The serial interface employs a 5-bit shift register. Data is loaded through the serial data input, SDI. Data passing through the shift register is obtained through the serial data output, SDO. The serial clock, SCK controls the serial loading process. All five data bits are required to correctly program the device. The falling edge of $\overline{CS}$ enables the shift register to receive data. The SCK signal must be high during the falling edge of $\overline{CS}$. Each data bit is clocked into the shift register on the rising edge of SCK. Data is transferred from the shift register to the holding register on the rising edge of $\overline{CS}$. Operation is shown in the Timing Diagram.

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SPI Registers

MSB				LSB
Gain_1	Gain_0	EN_CL	Null_SW	Hi_Z

Gain_0, Gain_1 bit:*Gain Values*

Different gains are available in Attenuation Mode or Amplification Mode according to the following Gain Table.

Gain_1	Gain_0	EN_CL	Gain Value (V/V)
0	0	0	**0.096**
0	1	0	**0.192**
1	0	0	**0.384**
1	1	0	**0.768**
1	0	1	**1**
1	1	1	**2**

EN_CL bit:*Enable Amplification Mode*

This register selects which input pair is processed.

EN_CL	Mode	Description
0	Attenuation Mode	$\pm V_{IN}$ inputs are processed through the 104.16k input resistors
1	Amplification Mode	±IN inputs are processed through the 40k input resistors

NULL_SW bit: *Input Offset Nulling Switch Mode*

This register selects a mode in which the amplifier is not processing any input but it is configured in unity gain to allow system level amplifier offset calibration. The Nulling Switch mode is available in both single ended and fully differential output mode. The LMP7312 in Nulling Switch and fully differential mode has he following configuration.

NULL_SW	Mode	Description
0	Normal Operation Mode	$\pm V_{IN}$ and ±IN inputs are processed depending on EN_CL register setting.
1	Nulling Switch Mode	Enables to evaluate the offset of the internal amplifier for system level calibration

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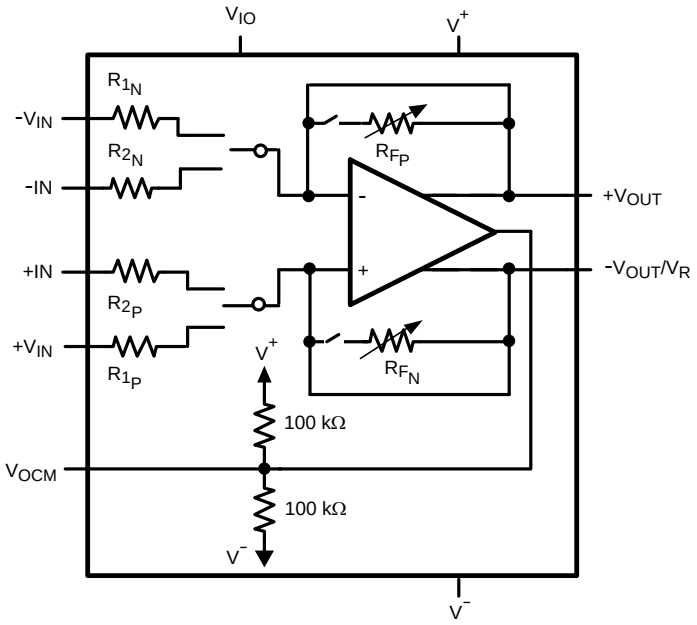


Figure 37. LMP7312 in Nulling Switch Mode

In this condition at the Output pins is possible to measure the input voltage offset of the op-amp:

Output Mode	**$+V_{OUT}$**	**$-V_{OUT}/V_R$**
Differential	$V_{CM_out}+V_{OS}/2$	$V_{CM_out}-V_{OS}/2$
Single-Ended	V_R+V_{OS}	V_R

Hi_Z bit:*High Impedance*

In this mode both outputs $+V_{OUT}$ and $-V_{OUT}/V_R$ of the LMP7312 are in tri-state Figure 38.

HI_Z	Mode	Description
0	Normal Operation Mode	The LMP7312 is configured according to value of the other 4 bits of the register.
1	High Impedance Mode	The LMP7312 output is in high impedance

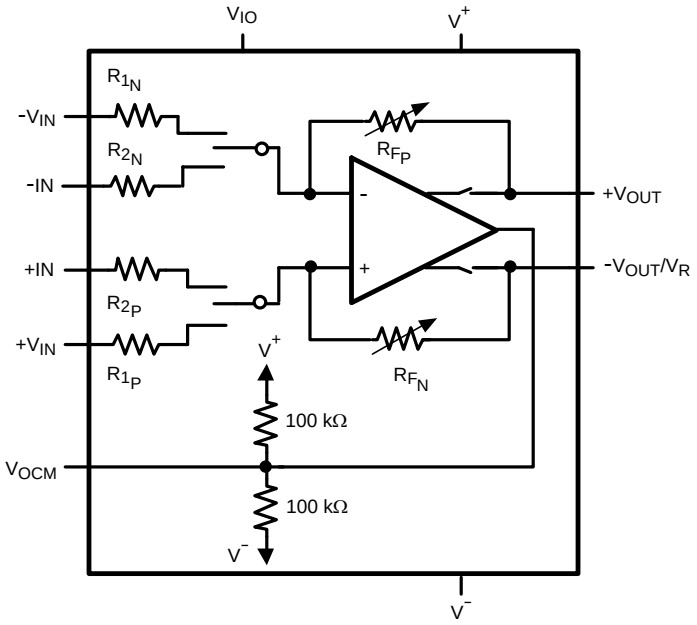


Figure 38. LMP7312 in High Impedance Mode

In each case the SPI registers require 5 bits. The table below is a summary of all allowed configurations.

MSB				LSB		
Gain_1	**Gain_0**	**EN_CL**	**Null_SW**	**Hi_Z**	**Gain Value (V/V)**	**Mode of Operation**
0	0	0	0	0	0.096	Attenuation Mode
0	1	0	0	0	0.192	Attenuation Mode
1	0	0	0	0	0.384	Attenuation Mode
1	1	0	0	0	0.768	Attenuation Mode
1	0	1	0	0	1	Amplification Mode
1	1	1	0	0	2	Amplification Mode
x	x	x	x	1	–	High Impedance Output
x	x	x	1	0	1	Null Switch Mode

Daisy Chain

The LMP7312 supports daisy chaining of the serial data stream between multiple chips. To use this feature serial data is clocked into the first chip SDI pin, and the next chip SDI pin is connected to the SDO pin of the first chip. Both chips may share a chip select signal, or the second chip can be enabled separately. When the chip select pin goes low on both chips and 5 bits have been clocked into the first chip the next 5 clock cycle begins moving new configuration data into the second chip. With a full 10 clock cycles both chips have valid data and the chip select pin of both chips should be brought high to prevent the data from overshooting.

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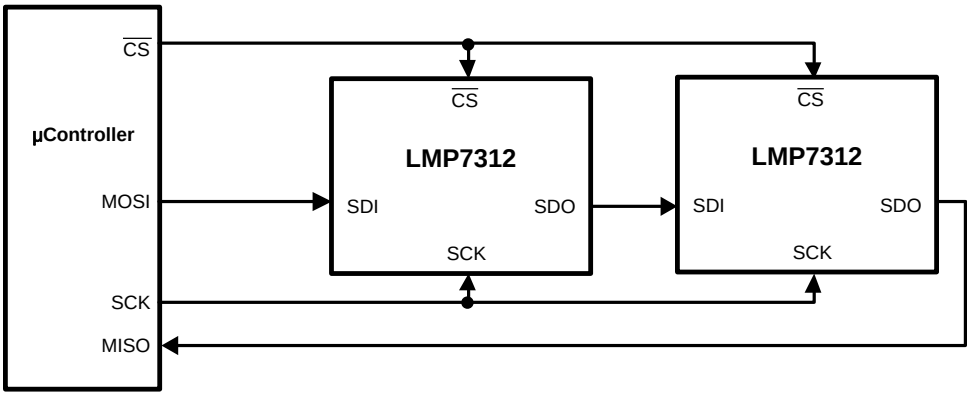


Figure 39. Daisy Chain

Shared 4-wire SPI with ADC

The LMP7312 is a good choice when interfacing to differential analog to digital converters ADC141S626 and ADC161S626 of PowerWise® Family. Its SPI interface has been designed to enable sharing CSB with the ADC. LMP7312 register access happens only when CSB is asserted low while SCK is high. However, the ADC starts conversion under any of the following conditions:

1. CSB goes low while SCK is high
2. CSB goes low while SCK is low
3. CSB and SCK both going low

Therefore, if a system uses timing condition #2 above, LMP7312 and ADC1x1S626 can share CSB and SCK as shown in Figure 40. The only side-effect would be that writing to LMP7312 triggers an ADC conversion, but then the result can be ignored. At other times, the LMP7312 is not affected by the CSB assertions used to initiate normal ADC conversions.

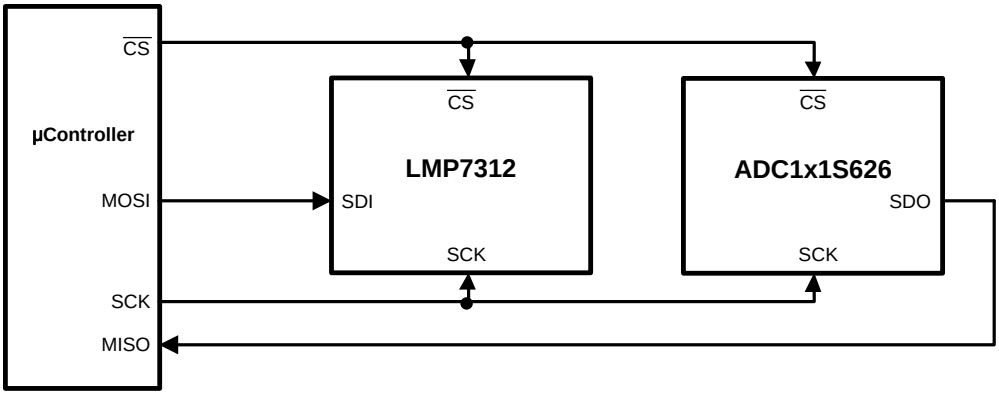


Figure 40. 4-wire SPI with ADC interface

LMP7312 IN 4-20mA CURRENT LOOP APPLICATION

The 4-20mA current loop shown in Figure 41 is a common method of transmitting sensor information in many industrial process-monitoring applications. Transmitting sensor information via a current loop is particularly useful when the information has to be sent to a remote location over long distances (1000 feet, or more). The loop's operation is straightforward: a sensor's output voltage is first converted to a proportional current, with 4mA normally representing the sensor's zero-level output, and 20mA representing the sensor's full-scale output. Then, a receiver at the remote end converts the 4-20mA current back into a voltage which in turn can be further processed by a computer or display module. A typical 4-20mA current-loop circuit is made up of four individual elements: a sensor/transducer; a voltage-to-current converter (commonly referred to as a transmitter and/or signal conditioner); a loop power supply; and a receiver/monitor. In loop powered applications, all four elements

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are connected in a closed, series circuit, loop configuration (Figure 41). Sensors provide an output voltage whose value represents the physical parameter being measured. The transmitter amplifies and conditions the sensor's output, and then converts this voltage to a proportional 4-20mA dc-current that circulates within the closed series-loop. The loop power-supply generally provides all operating power to the transmitter and receiver, and any other loop components that require a well-regulated dc voltage. In loop-powered applications, the power supply's internal elements also furnish a path for closing the series loop. The receiver/monitor, normally a subsection of a panel meter or data acquisition system, converts the 4-20mA current back into a voltage which can be further processed and/or displayed. The high DC performance of the LMP7312 makes this difference amplifier an ideal choice for use in current loop AFE receiver. The LMP7312 has a low input offset voltage and low input offset voltage drift when configured in amplification mode. In the circuit shown in Figure 41 the LMP7312 is in amplification mode with a gain of 2V/V and differential output in order to well match the input stage of the ADC141S626 (SAR ADC with differential input). The shunt resistor is 100ohm in order to have a max voltage drop of 2V when 20mA flows in the loop. The first order filter between the LMP7312 and the ADC141S626 reduces the noise bandwidth and allows handling input signal up to 2kHz. That frequency has been calculated taking in account the roll off of the filter and ensuring a gain error less than 1LSB of the ADC141S626. In order to utilize the maximum number of bits of the ADC141S626 in this configuration, a 4.1V reference voltage is used. With this system, the current of the 4-20mA loop is accurately gained to the full scale of the ADC and then digitized for further processing.

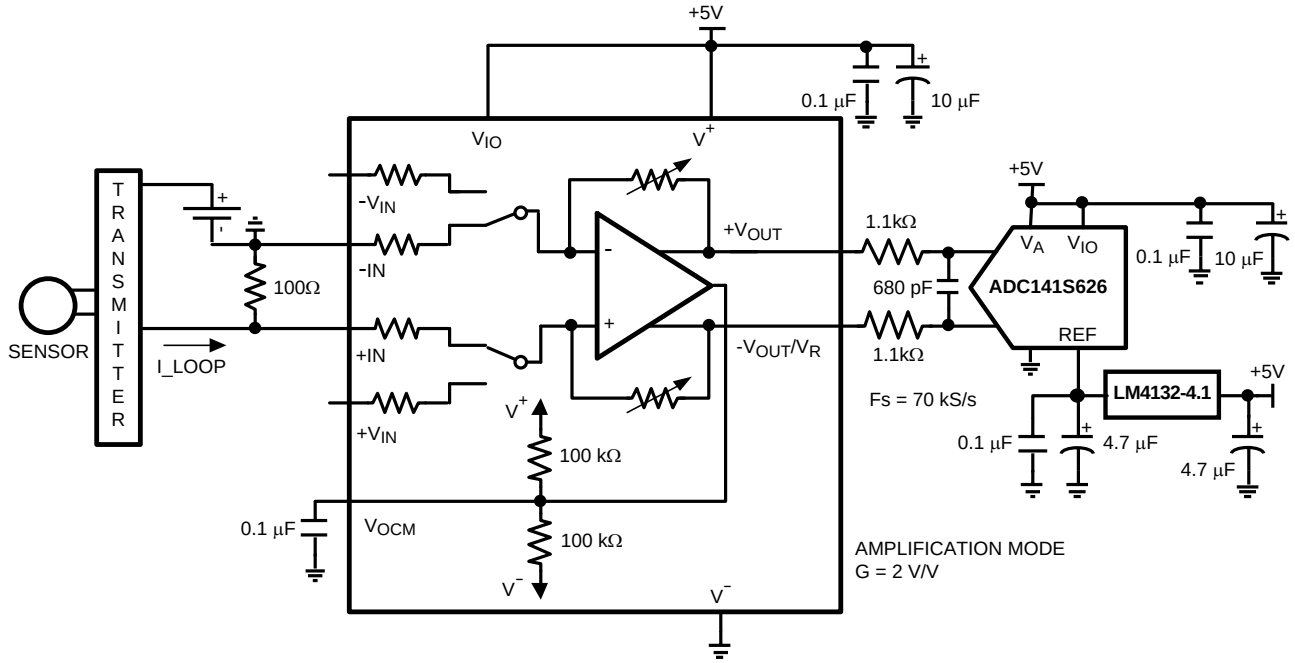


Figure 41. LMP7312 in 4-20mA Current Loop application

LAYOUT CONSIDERATIONS

Power supply bypassing

In order to preserve the gain accuracy of the LMP7312, power supply stability requires particular attention. The LMP7312 ensures minimum PSRR of 90dB (or 31.62 µV/V). However, the dynamic range, the gain accuracy and the inherent low-noise of the amplifier can be compromised by introducing and amplifying power supply noise. To decouple the LMP7312 from supply line AC noise, a 0.1 µF ceramic capacitor should be located on the supply line, close to the LMP7312. Adding a 10 µF tantalum capacitor in parallel with the 0.1 µF ceramic capacitor will reduce the noise introduced to the LMP7312 even further by providing an AC path to ground for most frequency ranges.

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APPENDIX

Offset Voltage and Offset Voltage Drift calculation

Listed in the table below are the calculated values for Offset Voltage and Offset Voltage Drift based on the max specifications of these parameters for the core op-amp (for all gain configurations).

Parameter	Unit	Value					
Gain	V/V	**0.096**	**0.192**	**0.384**	**0.768**	**1**	**2**
Total Offset Input Referred (MAX)	µV	±1141	±620	±360	±230	±200	±150
Total Offset Output Referred (MAX)	µV	±109	±119	±138	±176	±200	±300
TCV_{OS} Input Referred @ 25°C (MAX)	µV/°C	±32.3	±18.6	±10.8	±6.9	±6	±4.5
TCV_{OS} Output Referred @ 25°C (MAX)	µV/°C	±3.3	±3.6	±4.1	±5.3	±6	±9

Noise calculation

Listed in the table below are the calculated values for Voltage Noise based on the spectral density of the core op-amp at 10kHz (for all gain configurations).

Parameter	Unit	Value					
Gain	V/V	**0.096**	**0.192**	**0.384**	**0.768**	**1**	**2**
Total Noise Referred to Input	nV/√Hz	211	150	112	89	53	46
Total Noise Referred to Output	nV/√Hz	20	29	43	68	53	92

Input resistance calculation

The common mode input resistance is the resistance seen from node “A” when ΔV1 = ΔV2 = 0 and a common mode voltage ΔVCM is applied to both inputs of the LMP7312. The differential input resistance is the resistance seen from the nodes “B” and “C” when ΔVCM=0 and a differential voltage ΔV1 = ΔV2 = V/2 is applied to the inputs of the LMP7312.

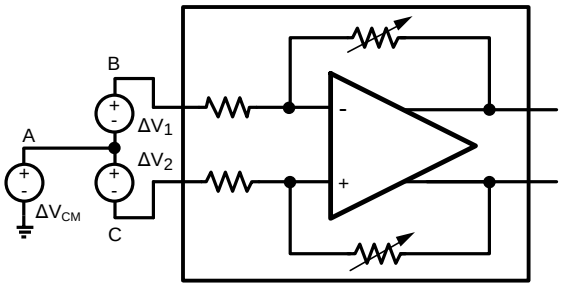


Figure 42. Circuit for Input Resistance calculation

Mode of Operation		Unit	Gains			
Attenuation Mode			**0.096**	**0.192**	**0.384**	**0.768**
	Common Mode Resistance	kΩ	57.08	62.08	72.08	92.08
	Differential Resistance	kΩ	228.30	248.30	288.30	368.30
Amplification Mode			**1**		**2**	
	Common Mode Resistance	kΩ	40.0		60.0	
	Differential Resistance	kΩ	160.0		240.0	

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REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	23

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP7312MA/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMP7312 MA	Samples
LMP7312MAX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMP7312 MA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

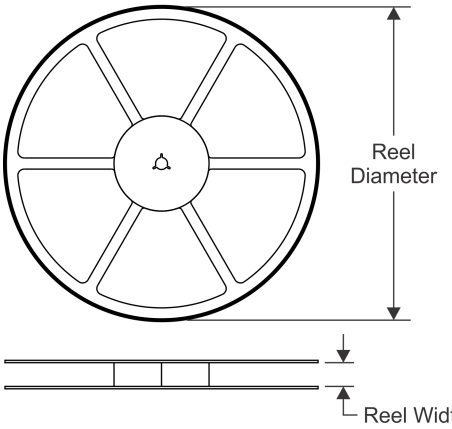
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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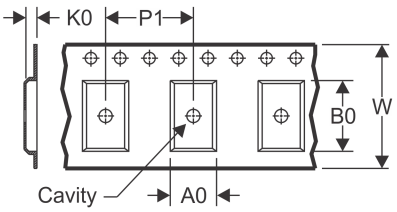
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

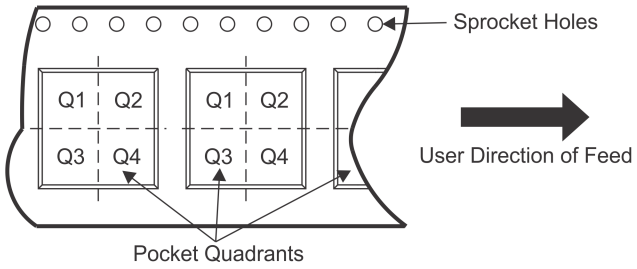


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

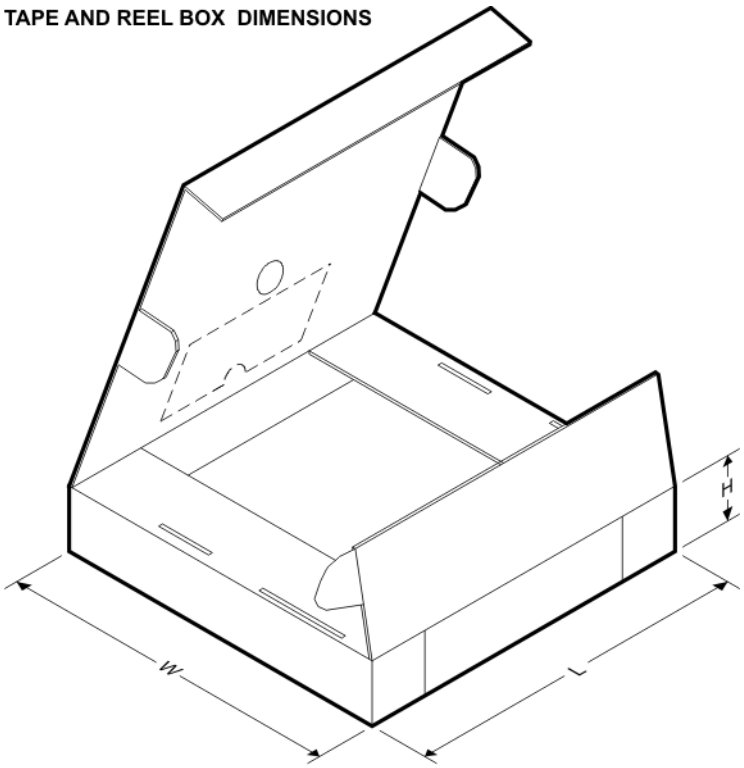
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP7312MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

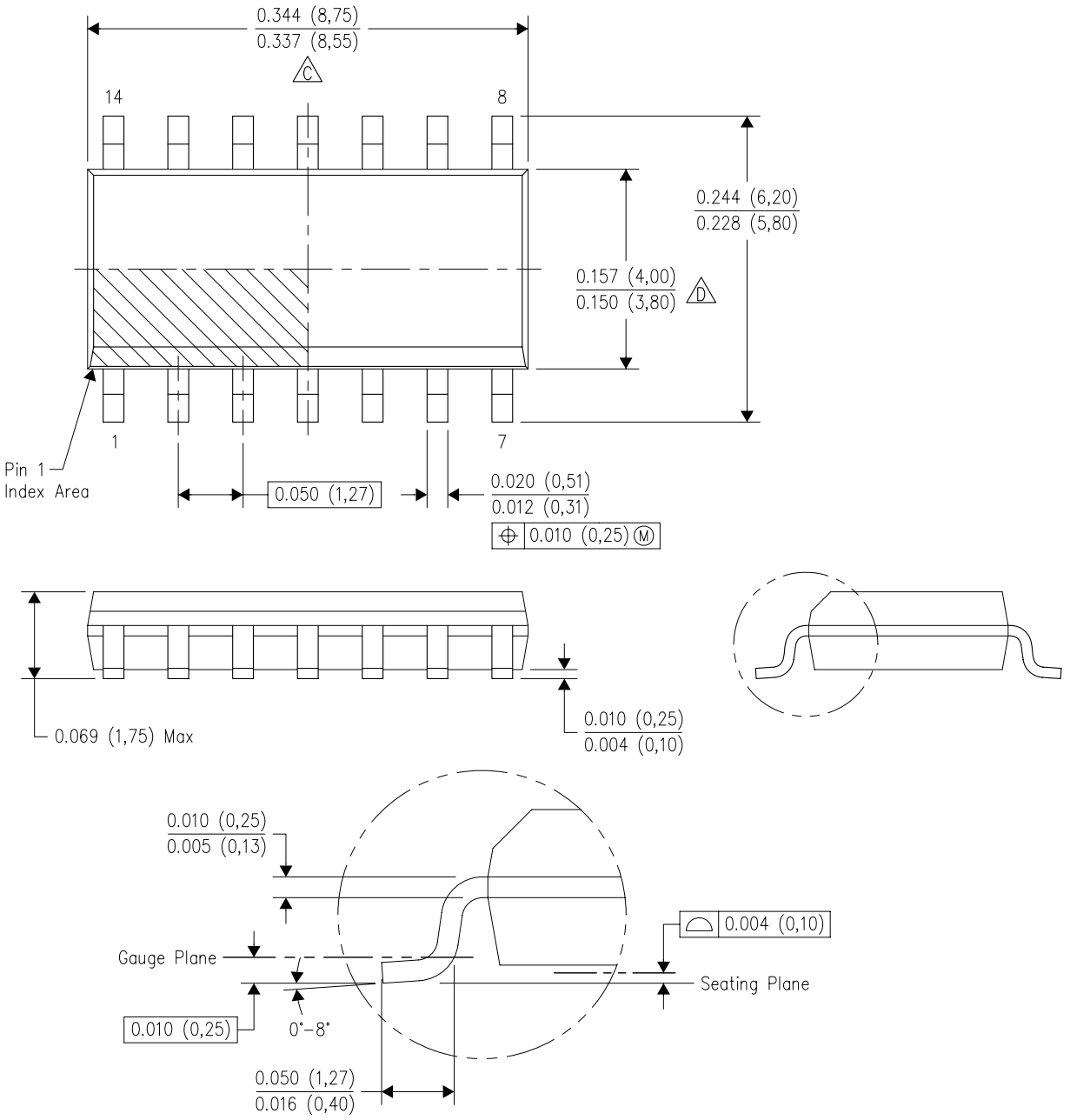
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP7312MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

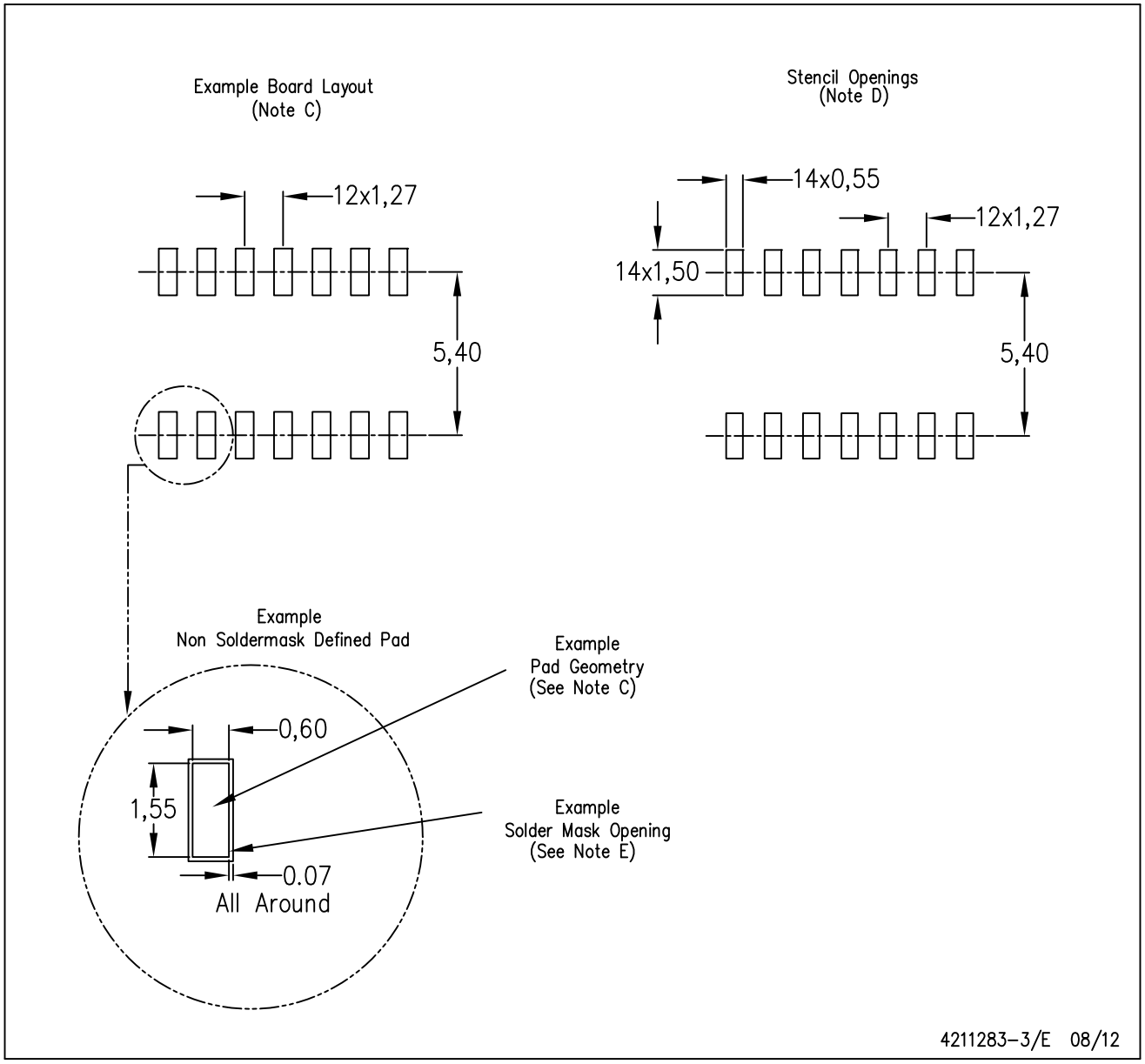
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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