



megaAVR[®] 0-series

megaAVR[®] 0-series Silicon Errata and Data Sheet Clarifications

General Notes

The megaAVR[®] 0-series devices you have received conform functionally to the current Device Data Sheets that are available online at <https://www.microchip.com/8-bit/microchip-avr-mcus>, except for the anomalies described in this document.

The errata described in this document may be addressed in future revisions of the silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Note: If you are unable to extract the silicon revision, contact your local Microchip sales office for assistance.

Table of Contents

General Notes.....	1
1. Errata Summary.....	3
2. Silicon Errata.....	4
2.1. Errata Details.....	4
2.2. PORTMUX.....	4
2.3. ADC.....	4
2.4. CCL.....	6
2.5. RTC.....	6
2.6. TCB.....	6
2.7. USART.....	7
2.8. CPUINT.....	8
3. Data Sheet Clarifications.....	10
4. Revision History.....	11
4.1. Document Rev.C - 08/2019.....	11
4.2. Document Rev.B - 07/2019.....	11
4.3. Document Rev.A - 02/2018.....	11
The Microchip Website.....	12
Product Change Notification Service.....	12
Customer Support.....	12
Microchip Devices Code Protection Feature.....	12
Legal Notice.....	12
Trademarks.....	13
Quality Management System.....	13
Worldwide Sales and Service.....	14

1. Errata Summary

Legend

- A, B,..** Erratum is valid for silicon revisions A, B,... of the device in that column.
- Erratum is not applicable for any silicon revision of this device.

Errata Overview

Peripheral	Short Description	Valid for Silicon Revision							
		48 Pins		40 Pins	32 Pins		28 Pins		
		ATmega4809, ATmega3209	ATmega1609, ATmega809	ATmega4809	ATmega4808, ATmega3208	ATmega1608, ATmega808	ATmega4808, ATmega3208	ATmega1608, ATmega808	
PORTMUX	2.2.1 SPI SS Pin is Connected to Pin Even if SPI is Configured to Have No Port Connection	A, B	A	A, B	A, B	A	A, B	A	
ADC	2.3.1 One Extra Measurement Performed After Disabling ADC Free Running Mode	A, B	A	A, B	A, B	A	A, B	A	
	2.3.2 Pending Event Stuck When Disabling the ADC	A, B	-	A, B	A, B	-	A, B	-	
	2.3.3 ADC - Functionality Cannot be Ensured With ADCCLK Above 1.5 MHz for All Conditions	A, B	A	A, B	A, B	A	A, B	A	
CCL	2.4.1 D-Latch is Not Functional	A, B	-	A, B	A, B	-	A, B	-	
RTC	2.5.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler	A, B	-	A, B	A, B	-	A, B	-	
TCB	2.6.1 TCA Restart Command Does Not Force a Restart of TCB	A, B	A	A, B	A, B	A	A, B	A	
	2.6.2 Minimum Event Duration Must Exceed Selected Clock Period	A, B	A	A, B	A, B	A	A, B	A	
USART	2.7.1 TXD Pin Override Not Released When Disabling the Transmitter	A, B	A	A, B	A, B	A	A, B	A	
CPUINT	2.8.1 Interrupt Level 1 Does Not Work	A, B		A, B					

2. Silicon Errata

2.1 Errata Details

- Erratum is not applicable.
- X** Erratum is applicable.
- * This silicon revision was never released to production.

2.2 PORTMUX

2.2.1 SPI \overline{SS} Pin is Connected to Pin Even if SPI is Configured to Have No Port Connection

The SPIn \overline{SS} pin is connected even if NONE is selected in the SPIn field in PORTMUX.TWISPIROUTE. If SPIn is operating in Master mode and the \overline{SS} pin goes low, or input is disabled, the SPIn will exit Master mode.

Work around

Write the SSD bit in SPIn.CTRLB to '1' to ignore the \overline{SS} signal.

Affected Silicon Revisions

Device		Rev. A	Rev. B				
48 pins	ATmega3209/4809	*	X				
	ATmega809/1609	X					
40 pins	ATmega4809	*	X				
32 pins	ATmega3208/4808	*	X				
	ATmega808/1608	X					
28 pins	ATmega3208/4808	*	X				
	ATmega808/1608	X					

2.3 ADC

2.3.1 One Extra Measurement Performed After Disabling ADC Free Running Mode

The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN.

Work around

Write ADCn.CTRLA.ENABLE to '0' to stop the free running mode immediately.

Affected Silicon Revisions

Device		Rev. A	Rev. B				
48 pins	ATmega3209/4809	*	X				
	ATmega809/1609	X					
40 pins	ATmega4809	*	X				

.....continued

Device		Rev. A	Rev. B					
32 pins	ATmega3208/4808	*	X					
	ATmega808/1608	X						
28 pins	ATmega3208/4808	*	X					
	ATmega808/1608	X						

2.3.2 Pending Event Stuck When Disabling the ADC

If the ADC is disabled during an event-triggered conversion, the event will not be cleared.

Work around

Clear ADC.EVCTRL.STARTEI and wait for conversion to complete before disabling the ADC.

Affected Silicon Revisions

Device		Rev. A	Rev. B					
48 pins	ATmega3209/4809	*	X					
	ATmega809/1609	-						
40 pins	ATmega4809	*	X					
32 pins	ATmega3208/4808	*	X					
	ATmega808/1608	-						
28 pins	ATmega3208/4808	*	X					
	ATmega808/1608	-						

2.3.3 ADC - Functionality Cannot be Ensured With ADCCLK Above 1.5 MHz for All Conditions

The ADC functionality cannot be ensured if ADCCLK > 1.5 MHz with ADCn.CALIB.DUTYCYC set to 1. The ADC functionality cannot be ensured if ADCCLK > 1.5 MHz and VDD < 2.7V.

Work around

If ADC is operated with ADCCLK > 1.5 MHz and VDD > 2.7V, ADCn.CALIB.DUTYCYC must be set to zero (50% duty cycle). Do not use ADC at ADCCLK > 1.5 MHz and VDD < 2.7V

Affected Silicon Revisions

Device		Rev. A	Rev. B					
48 pins	ATmega3209/4809	*	X					
	ATmega809/1609	X						
40 pins	ATmega4809	*	X					
32 pins	ATmega3208/4808	*	X					
	ATmega808/1608	X						
28 pins	ATmega3208/4808	*	X					
	ATmega808/1608	X						

2.4 CCL

2.4.1 D-Latch is Not Functional

The CCL D-latch is not functional.

Work around

None.

Affected Silicon Revisions

Device		Rev. A	Rev. B				
48 pins	ATmega3209/4809	*	X				
	ATmega809/1609	-					
40 pins	ATmega4809	*	X				
32 pins	ATmega3208/4808	*	X				
	ATmega808/1608	-					
28 pins	ATmega3208/4808	*	X				
	ATmega808/1608	-					

2.5 RTC

2.5.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler

Any write to the RTC.CTRLA register resets the RTC and PIT prescaler.

Work around

None.

Affected Silicon Revisions

Device		Rev. A	Rev. B				
48 pins	ATmega3209/4809	*	X				
	ATmega809/1609	-					
40 pins	ATmega4809	*	X				
32 pins	ATmega3208/4808	*	X				
	ATmega808/1608	-					
28 pins	ATmega3208/4808	*	X				
	ATmega808/1608	-					

2.6 TCB

2.6.1 TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force a restart of the TCB when TCB is running in SYNCUPD mode. TCB is only restarted after a TCA OVF.

Work around

None.

Affected Silicon Revisions

Device		Rev. A	Rev. B					
48 pins	ATmega3209/4809	*	X					
	ATmega809/1609	X						
40 pins	ATmega4809	*	X					
32 pins	ATmega3208/4808	*	X					
	ATmega808/1608	X						
28 pins	ATmega3208/4808	*	X					
	ATmega808/1608	X						

2.6.2 Minimum Event Duration Must Exceed Selected Clock Period

Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA).

This applies to the TCB modes (CNTMODE in TCBn.CTRLB) *Time-out check* and *Input Capture Frequency and Pulse-Width Measurement* mode.

Work around

Ensure that the high/low period of the input events is equal to or longer than the period of the selected clock source (CLKSEL in TCBn.CTRLA).

Affected Silicon Revisions

Device		Rev. A	Rev. B					
48 pins	ATmega3209/4809	*	X					
	ATmega809/1609	X						
40 pins	ATmega4809	*	X					
32 pins	ATmega3208/4808	*	X					
	ATmega808/1608	X						
28 pins	ATmega3208/4808	*	X					
	ATmega808/1608	X						

2.7 USART

2.7.1 TXD Pin Override Not Released When Disabling the Transmitter

Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA).

The USART will not release the TXD pin override if:

1. The USART transmitter is disabled by writing the TXEN bit in USART.CTRLB to '0' while the USART receiver is disabled (RXEN in USART.CTRLB is '0').
2. Both the USART transmitter and receiver are disabled at the same time by writing the TXEN and RXEN bits in USART.CTRLB to '0'.

Work around

There are two possible workarounds:

- Make sure the receiver is enabled (RXEN in USART.CTRLB is '1') while disabling the transmitter (writing TXEN in USART.CTRLB to '0').
- Write to any register in the USART after disabling the transmitter. This will start the USART for long enough to release the pin override of TXD pin.

Affected Silicon Revisions

Device		Rev. A	Rev. B				
48 pins	ATmega3209/4809	*	X				
	ATmega809/1609	X					
40 pins	ATmega4809	*	X				
32 pins	ATmega3208/4808	*	X				
	ATmega808/1608	X					
28 pins	ATmega3208/4808	*	X				
	ATmega808/1608	X					

2.8 CPUINT

2.8.1 Interrupt Level 1 Does Not Work

Interrupt Level 1 may fail to execute correctly, by executing the Reset vector rather than the intended interrupt vector. This only applies to the following products and is limited to date codes older than 1914 (week 14 of 2019).

- ATMEGA4809-AF
- ATMEGA4809-AFR
- ATMEGA4809-AU
- ATMEGA4809-AUR
- ATMEGA4809-MF
- ATMEGA4809-MFR
- ATMEGA4809-MU
- ATMEGA4809-MUR
- ATMEGA4809-PF

Work around

Use interrupt Level 0 instead of interrupt Level 1.

Affected Silicon Revisions

Device		Rev. A	Rev. B				
48 pins	ATmega3209/4809	*	X				
	ATmega809/1609	-					
40 pins	ATmega4809	*	X				
32 pins	ATmega3208/4808	*	-				
	ATmega808/1608	-					

.....continued

Device		Rev. A	Rev. B					
28 pins	ATmega3208/4808	*	-					
	ATmega808/1608	-						

3. Data Sheet Clarifications

None.

4. Revision History

4.1 Document Rev.C - 08/2019

- New Errata:
 - CPUINT: [2.8.1 Interrupt Level 1 Does Not Work](#)

4.2 Document Rev.B - 07/2019

- Document
 - Adding variants with 16 KB and 8 KB Flash
 - Adding 40-pin variant of ATmega4809
 - Changing document title
 - Adding section [3. Data Sheet Clarifications](#)
- New Errata:
 - PORTMUX: [2.2.1 SPI SS Pin is Connected to Pin Even if SPI is Configured to Have No Port Connection](#)
 - TCB: [2.6.2 Minimum Event Duration Must Exceed Selected Clock Period](#)
 - USART: [2.7.1 TXD Pin Override Not Released When Disabling the Transmitter](#)
- Erratum for TCA removed: Issuing a restart will clear the direction bit - the data sheet is describing this correctly.

4.3 Document Rev.A - 02/2018

Initial version.

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